8bit 500MSPS Single VIDEO DAC (ECL input)

Description

The CXA1236Q is an ultra high-speed D/A converter that multiplexes two 8-bit input data.

This IC realizes a maximum conversion speed of 500MSPS and is suitable for signal processings which require high speed and high resolution D/A conversions such as high quality displays, high definition video systems and others.

44 pin QFP (Ceramic)

Features

- Ultra high-speed
  : 500MSPS, multiplexed input
- High resolution: 8bit
- Low power consumption
  : 1W (for $V_{EE} = -4.5V$)
- Video control input
  : Sync, Blank, Ref. White, Bright
- ECL 100K and 10K compatible input
- Can drive 25Ω, 37.5Ω, 50Ω, and 75Ω loads
- Differential current output
- RS-343A compatible output
- −5.5 to −4.2V range single power supply operation

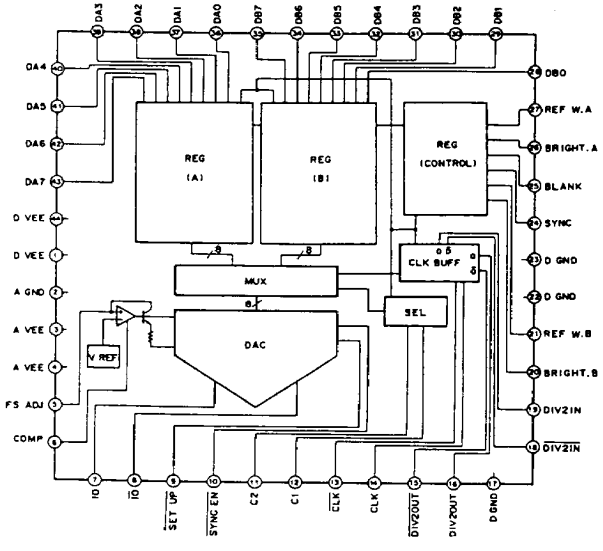
Functions

8bit 500MSPS Single VIDEO D/A Converter

Structure

Bipolar silicon monolithic IC

Block Diagram and Pin Configuration (Top View)



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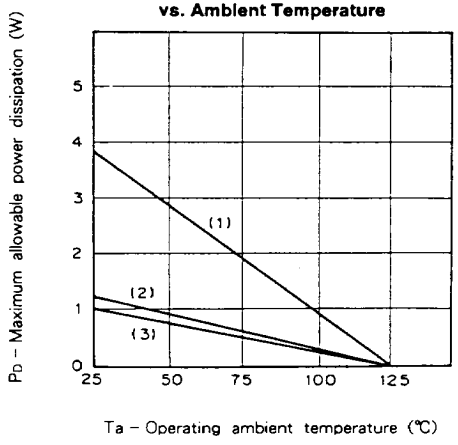
Absolute Maximum Ratings (Ta = 25°C)

• Supply voltage	AV_{EE}, DV_{EE}	− 7 to + 0.5	V
• Input voltage (digital)	V_I	DV_{EE} to + 0.5	V
(FS ADJ pin)	V_{REF}	AV_{EE} to + 0.5	V
• Input current (FS ADJ pin)	I_{REF}	2.0	mA
• Output voltage	V_O	− 2.0 to + 2.0	V
• Output current	I_O	50	mA
• Storage temperature	Tstg	− 65 to + 150	°C
• Allowable power dissipation	P_D	1.3	W

Operating Conditions

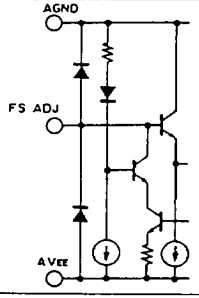
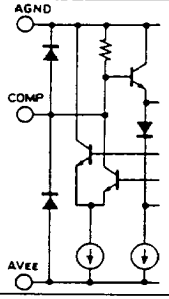
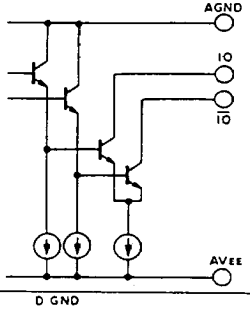
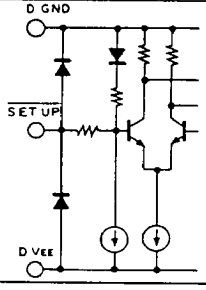
• Supply voltage	AV_{EE}, DV_{EE}	− 5.5 to − 4.2	V
	$AV_{EE} - DV_{EE}$	− 0.05 to + 0.05	V
• Digital input voltage	V_{IH}	− 1.05 to − 0.7	V
	V_{IL}	− 1.9 to − 1.49	V
• Reference current	I_{REF}	0.5 to 1.7	mA
• Load resistance	R_L	25 to 75	Ω
• Output voltage	V_O (FS.)	0.8 to 1.2	V
• CLK pulse width MUX (1) mode	t_{PW1}	0.9 (Min.)	ns
	t_{PW0}	0.9 (Min.)	ns
MUX (2) mode	t_{PW1}	1.8 (Min.)	ns
SELECT mode	t_{PW0}	1.8 (Min.)	ns
• Operating temperature	Tc	− 55 to 70	°C

Maximum allowable Power Dissipation vs. Ambient Temperature



(1) Ta = Tc
(When infinitely large heat sink is used.)
(2) For PCB mounting
(PCB area equivalent to 20 × 10 × 1.6mm and copper foil area covering 30 % of one side.)
(3) Before mounting

Pin Description and I/O Pin Equivalent Circuits

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
1, 44	DV_{EE}	− 4.5V (typ.)		Digital power supply
2	AGND	GND		Analog GND
3, 4	AV_{EE}	− 4.5V (typ.)		Analog power supply
5	FS ADJ	− 1.24V (typ.)		Controls full scale voltage of analog output. Output current can be varied by adjusting the value of the external resistor connected to this pin.
6	COMP			Compensation pin for internal amplifier. Connect capacitor between COMP and AV_{EE}.
7	IO	0 ~ − 1071mV (typ.)		Analog output pin. Function as differential current output.
8	$\overline{IO}$			
9	$\overline{SET\ UP}$	ECL		Control input for SET UP. When "1" is input, output becomes BLANK 1 level ; when this pin is fed with "0" or left open, output becomes BLANK 2 level. (Refer to Table 1.)

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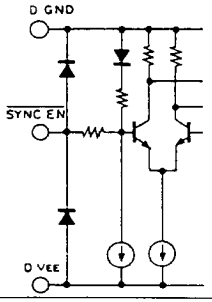
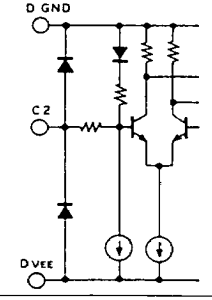
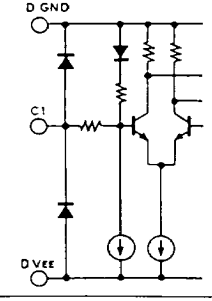
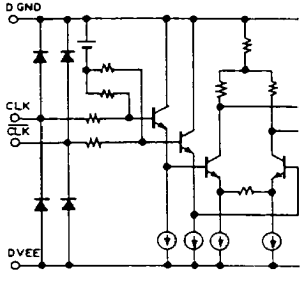
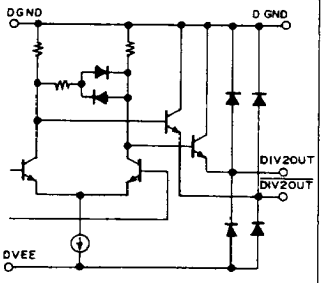
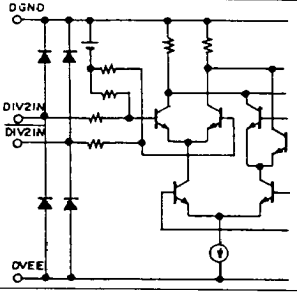
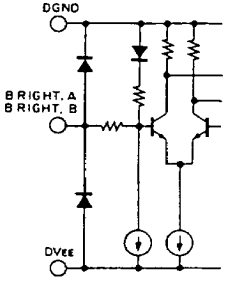
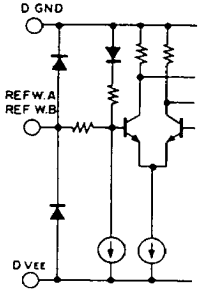
Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
10	$\overline{\text{SYNC EN}}$	ECL		Enable input for Sync output. When "0" is input or left open, output for Sync level is obtained.
11	C2	ECL		Control input for operating mode. For multiplex mode, CLK input frequency can be selected. For data select mode, either input data A or B can be selected. (Refer to Table 2.)
12	C1	ECL		Control input for operating mode. Input of "0" selects multiplex mode and input of "1" selects data select mode. (Refer to Table 2.)
13	$\overline{\text{CLK}}$	ECL		Clock input pin.
14	CLK			

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
15	$\overline{\text{DIV2OUT}}$	ECL		Outputs 1/2 clock frequency signal. Only when both C1 and C2 inputs are "0", a 1/2 clock frequency signal synchronized with DIV2IN is output. Otherwise, a signal at the clock frequency is output. (Refer to Timing Diagrams.)
16	DIV2OUT			
17, 22, 23	DGND	GND		Digital GND.
18	$\overline{\text{DIV2IN}}$	ECL		In multiplex mode, this converter is able to be synchronized by inputting 1/2 clock as a system clock into these pins. (Refer to Fig. 6. (1)).
19	DIV2IN			
20	BRIGHT. B	ECL		BRIGHT control input for DATA A and DATA B. When "1" is input, D/A output is shifted up by 10 %. (Refer to Table 1.)
26	BRIGHT. A			
21	REF W. B	ECL		Ref. White control input for DATA A and DATA B. When "1" is input, output is set to WHITE Level. (Refer to Table 1.)
27	REF W. A			

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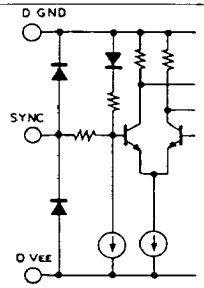
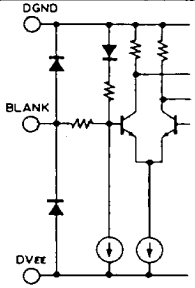
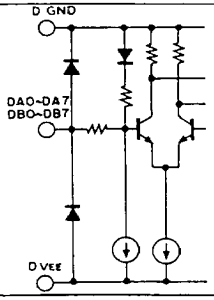
Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
24	SYNC	ECL		Input control for Sync. Active only when the SYNC EN input is "0". When "1" is input, D/A output is shifted to Sync level regardless of other inputs.
25	BLANK	ECL		Control input for BLANK. When "1" is input, D/A output is shifted to either BLANK 1 or BLANK 2 level.
28~35	DB0~DB7	ECL		Digital input pin. DA0 (LSB) to DA7 (MSB) are for DATA A ; DB0 (LSB) to DB7 (MSB) are for DATA B.
36~43	DA0~DA7			

Electrical Characteristics (AV_{EE} = DV_{EE} = − 4.5V, Ta = 25°C)

Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Resolution	n		8	8	8	bit
Linearity error	E_L	V_{FS} = 1071mV			± 1/2	LSB
Differential linearity error	E_D				± 1/2	LSB
Digital input current	I_{IH}	V_{IN} = − 0.7V			100	μA
	I_{IL}	V_{IN} = − 1.9V	− 100			μA
Input capacitance	C_{IN}			5		pF
Digital output voltage	V_{OH}	R_T = 50Ω to − 2V	− 1.05			V
	V_{OL}				− 1.49	V
FS ADJ pin voltage	$V_{ADJ.}$		− 1.14	− 1.24	− 1.34	V
Max. output current	Io		48			mA
Compliance voltage	V_{OC}		− 1.2		1.5	V
Output offset current	I_{OF}			7	50	μA
Output resistance	Ro			50		kΩ
Output capacitance	Co			8		pF
Absolute gain error	E_G	V_{FS} = − 1071mV	− 10		+ 10	% of F.S.
Gain error temperature coefficient	T_{CG}			0.05		% of F.S./°C
Currect consumption	I_{EE}	R_L = 25Ω	− 300	− 235	− 170	mA
Max. conversion rate	Fs		500			MSPS
MUX (1) mode						
DIV2IN setup time	ts_2		0.3			ns
DIV2IN hold time	th_2		1.1			ns
DIV2OUT output delay	tdck	R_T = 50Ω to − 2V	1.2		1.6	ns
DATA setup time	ts		0.4			ns
DATA hold time	th		1.4			ns
Analog output delay	td		2.4		4.1	ns
Pipeline delay			3	3	3	clocks
MUX (2), SELECT mode						
DIV2OUT output delay	tdck	R_T = 50Ω to − 2V	1.1		1.4	ns
DATA setup time	ts		0.6			ns
DATA hold time	th		1.2			ns
C2 setup time	tsc		0.3			ns
C2 hold time	thc		0.9			ns
Analog output delay	td	R_L = 25Ω	2.3		3.9	ns
Pipeline delay			1.5	1.5	1.5	clocks

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Item	Symbol	Condition	Min.	Typ.	Max.	Unit
Analog output						
Rise time	tr	R_L = 25Ω		0.4	0.6	ns
Fall time	tf			0.4	0.6	ns
Settling time	t_{SET}			1.5		ns
Glitch energy	GE			5		pVs

Description of Operation (Refer to Block Diagram and Pin Configuration)

Normal multiplex mode (MUX (1) mode) is defined as a state when C1 and C2 are set to "0". When the system clock (CLK/2) is input to DIV2IN, the output signal is in phase with the system clock at the 1/2 CLK frequency. When C1 is set to "0" and C2 to "1", the clock with duty cycle of exactly 50% must be input.
DATA A (DA0 to DA7), DATA B (DB0 to DB7) and all control signal (C2, BRIGHT.A, REF W.A, BRIGHT.B, REF W.B, BLANK, and SYNC) data are latched in internal registers on the rising edge of the internal clock, which has the same frequency as the DIV2OUT.
Internally, the DB, BRIGHT.B, and REF W.B are delayed by 1/2 period of the DIV2OUT output. After the upper 4 bits of DA and DB are decoded into thermometer code, they are multiplexed within MUX block together with the lower 4 bit data and control signals, and then fed to DAC block.
When C1 is "1", DA, BRIGHT.A, and REF W.A can be selected by inputting "0" at C2. In the same way, DB, BRIGHT.B, and REF W.B. can be selected by inputting "1" at C2.
In the DAC block, the input DATA are converted into current. The DAC creates analog output current composing of the following portions :

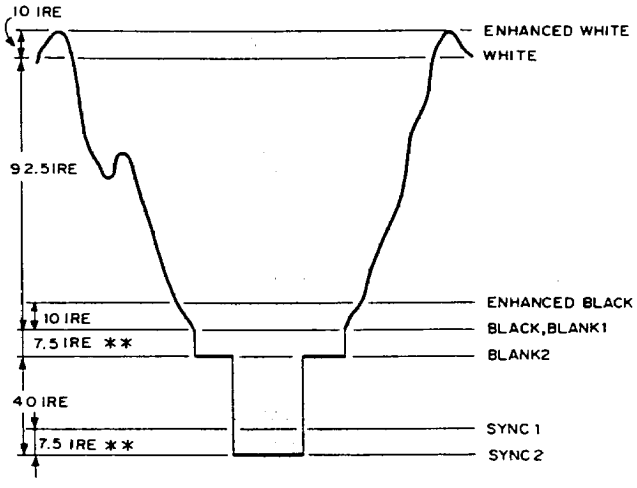
- Weighted lower 4bit current
- Thermometer-coded upper 4bit current
- Function output currents

The output comes out delayed by 1.5 clocks of DIV2OUT after the rising edge of the CLK.
The analog current can be change into a voltage when a load resistor is connected to the output pin.
This IC contains an internal band-gap voltage source which allows adjustment of the output voltage full scale by varying the resistance value Rset externally connected between FS ADJ and AGND. The following formula describes this relationship.

$$R_{set} = \frac{V_{ADJ.}}{\frac{661mV}{R_L} \times \frac{16}{255}} \ [\Omega]$$

$V_{ADJ.\ (TYP.)} = -1.24V$

$\overline{IO}$ (mA) *	V ($\overline{IO}$) (mV)
0	0
− 2.84	− 71
− 26.44	− 661
− 29.28	− 732
− 31.42	− 785.5
− 40.7	− 1017.5
− 42.84	− 1071



* In case of doubly-terminated 50 Ω load

** 7.5 IRE difference·····Available when $\overline{SETUP}$ pin is floating or "0" level, not available when SETUP pin is "1" level.

Fig. 1. Composite Video Output

Description	$\overline{IO}$ (mA)	$\overline{SETUP}$	$\overline{SYNC\ EN}$	BRIGHT	SYNC	BLANK	REF W	Input DATA
Enhanced White	0	×	×	1	0	0	0	11111111
	0	×	×	1	0	0	1	XXXXXXXX
White	− 2.84	×	×	0	0	0	1	XXXXXXXX
	− 2.84	×	×	0	0	0	0	11111111
Enhanced DATA	DATA	×	×	1	0	0	0	DATA
DATA	DATA − 2.84	×	×	0	0	0	0	DATA
Enhanced BLACK	− 26.44	×	×	1	0	0	0	00000000
BLACK, BLANK1	− 29.28	×	×	0	0	0	0	00000000
	− 29.28	1	×	×	0	1	×	XXXXXXXX
	− 29.28	1	1	×	1	×	×	XXXXXXXX
BLANK2	− 31.42	0	×	×	0	1	×	XXXXXXXX
	− 31.42	0	1	×	1	×	×	XXXXXXXX
SYNC1	− 40.7	1	0	×	1	×	×	XXXXXXXX
SYNC2	− 42.84	0	0	×	1	×	×	XXXXXXXX

Table 1. I/O Correspondence Chart

C1	C2	MODE		CLK IN (MHz)	DATA IN (Mbps)	OUT (Mbps)
0	0	MUX	(1)	500	250	500
0	1		(2)	250*	250	500
1	0	A		250	250	250
1	1	B		250	250	250

* The CLK duty cycle must be set to 50%.
A : DA0 to DA7 is selected.
B : DB0 to DB7 is selected.

Table 2. Output Mode Chart

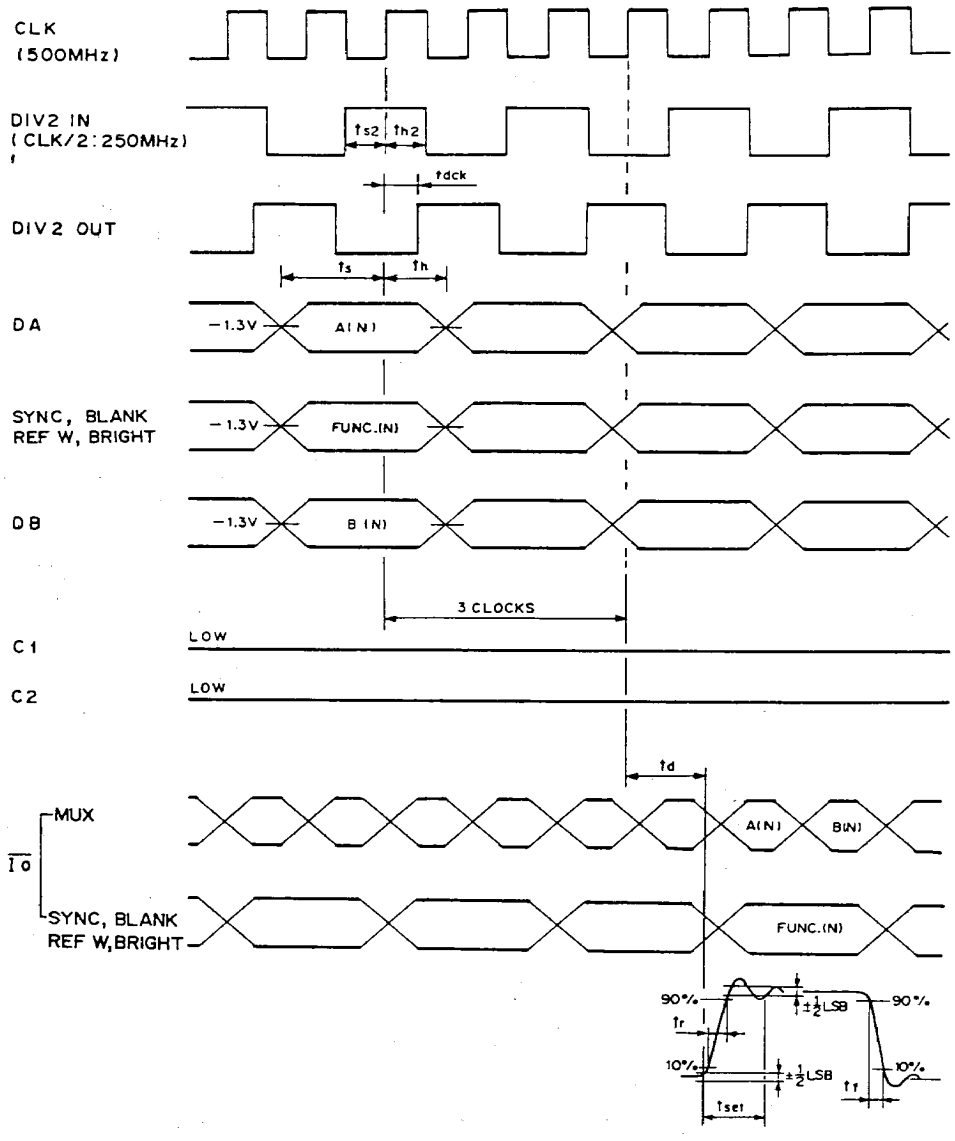


Fig. 2. Timing Diagram – MUX (1) MODE

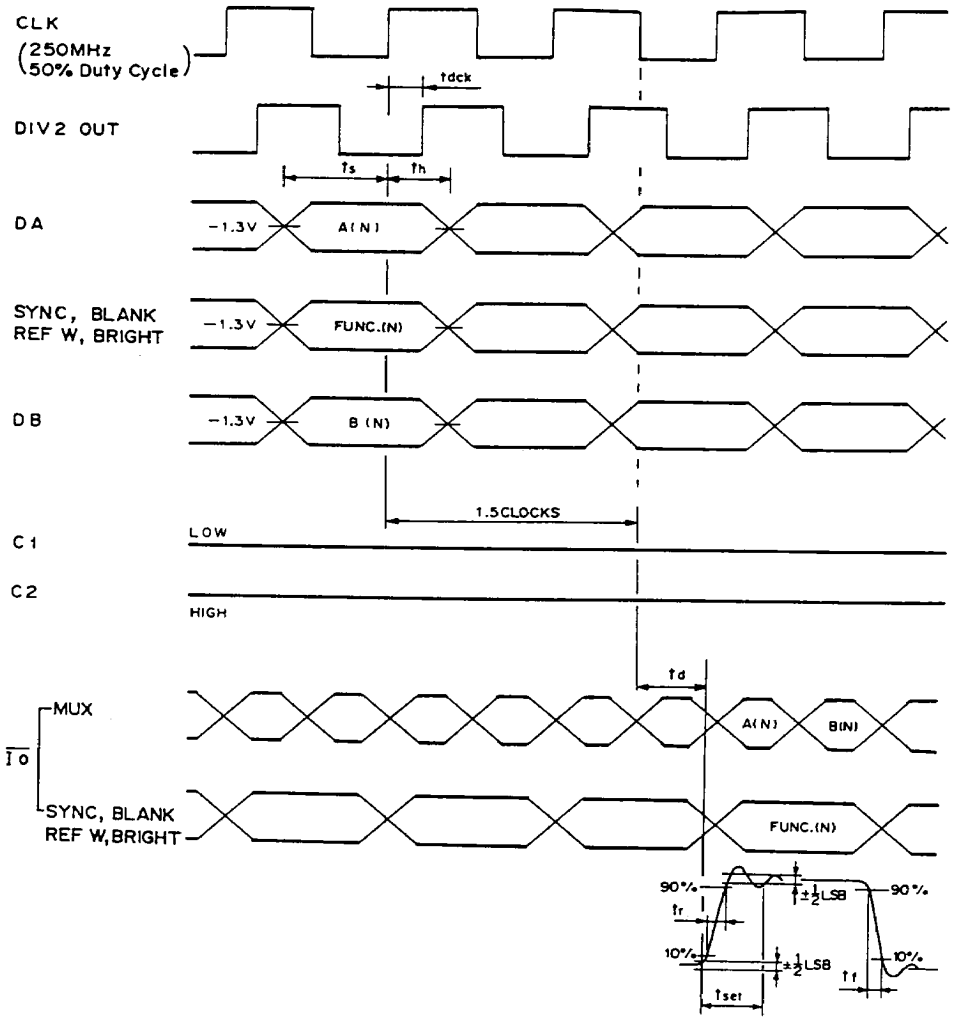


Fig. 3. Timing Diagram – MUX (2) MODE

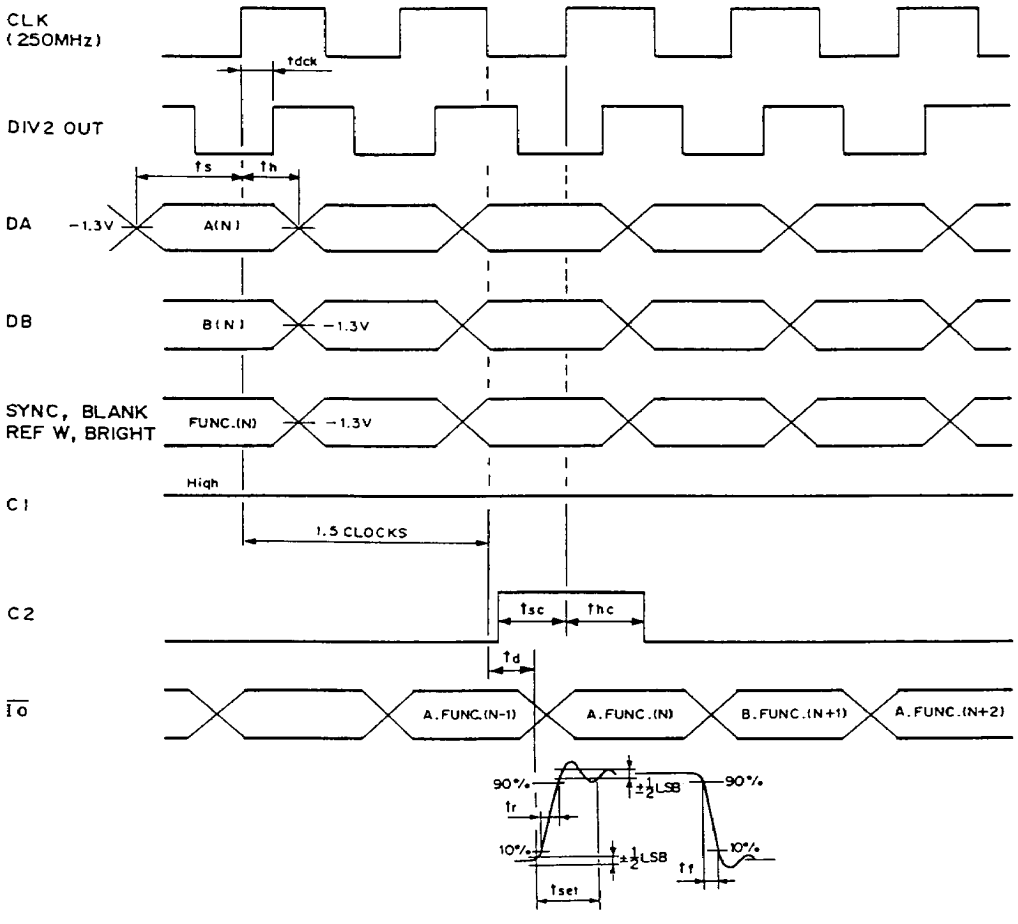
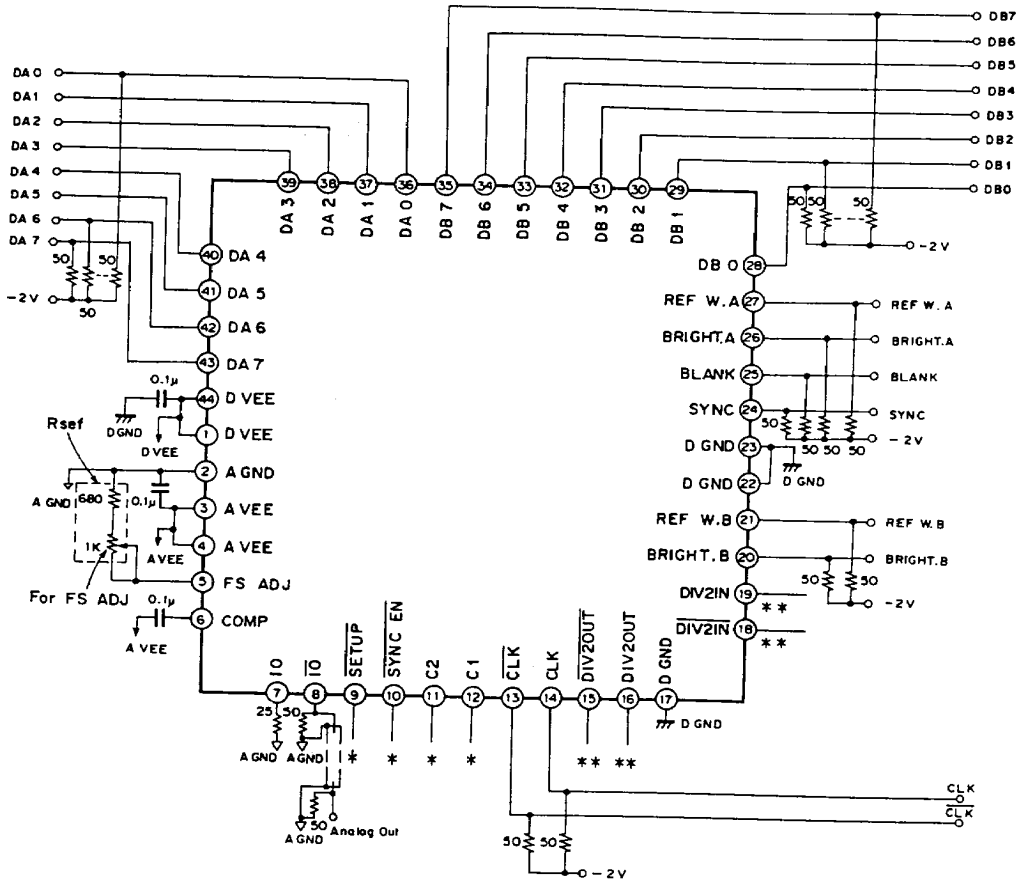


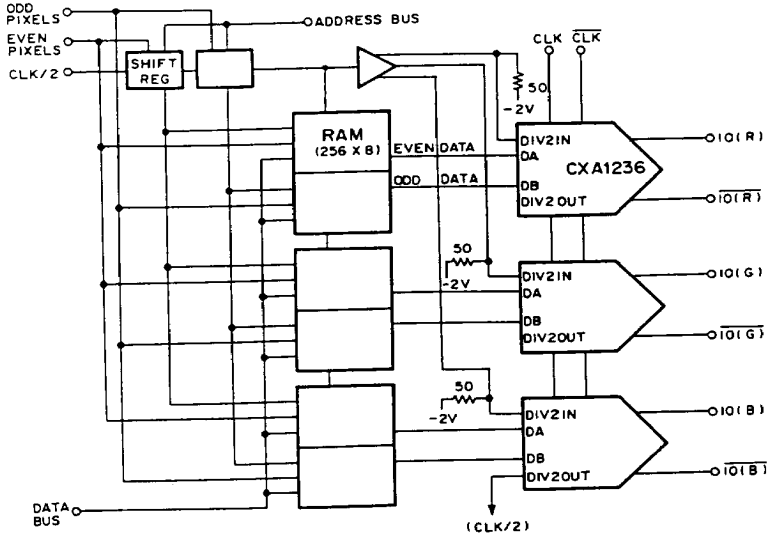
Fig. 4. Timing Diagram – SELECT MODE



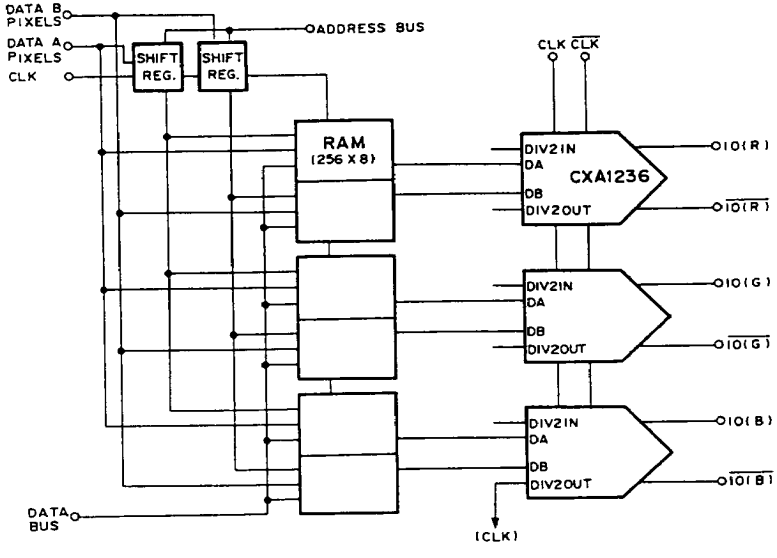
* Refer to Pin Description

** Refer to Pin Description and Application Circuit

Fig. 5. Typical Usage Circuit Configuration



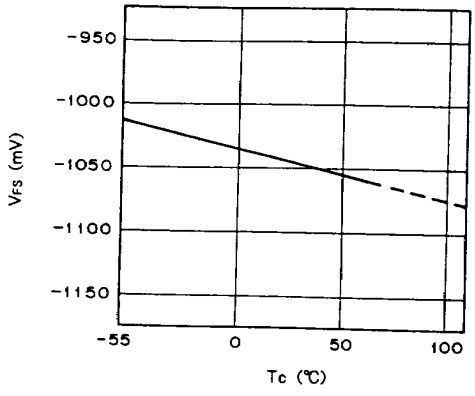
(1) MUX MODE



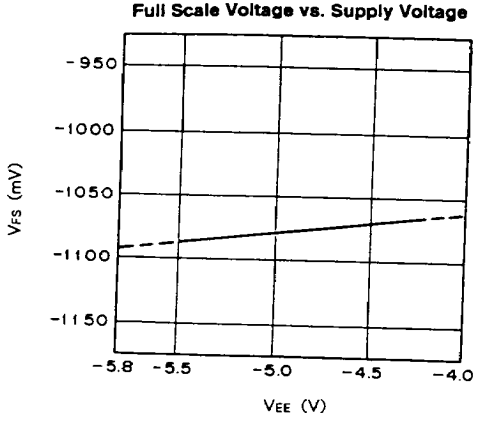
(2) SELECT MODE

Fig. 6. Application Circuit Examples

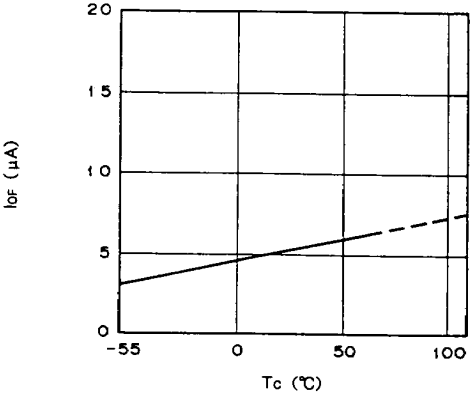
Full Scale Voltage vs. Case Temperature



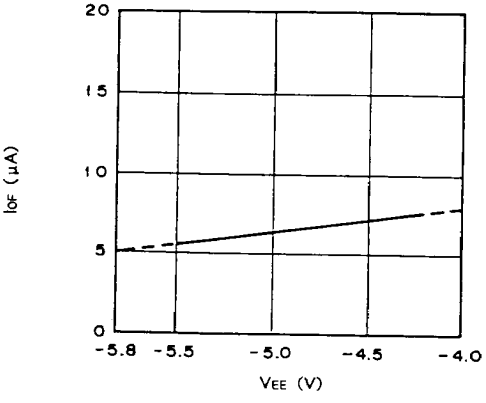
Full Scale Voltage vs. Supply Voltage



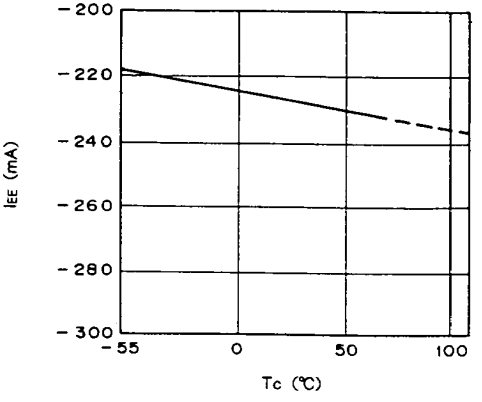
Output Offset Current vs. Case Temperature



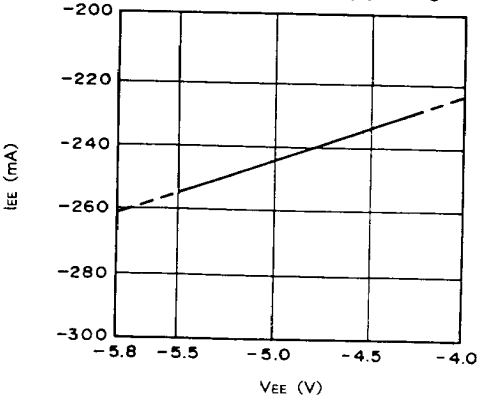
Output Offset Current vs. Supply Voltage



Supply Current vs. Case Temperature



Supply Current vs. Supply Voltage



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Notes on Usage

(1) Wiring for Digital Input
- All of the digital inputs are single-ended ECL compatible inputs. For high-speed operation, the wiring characteristic impedance and terminal resistance should be about 50Ω and the resistors should be connected to V_{TT} (−2V) which is close to the input pins.

(2) Noise Reduction Measures
- Try to provide grounding widely on the whole board to prevent parasitic inductances and resistances.
- Keep AGND and DGND separated as much as possible. Keep AV_{EE} and DV_{EE} separated as much as possible also. For making connections of AGND and DGND or AV_{EE} and DV_{EE}, using the board connectors is recommended.
- Connect a bypass capacitor of 1 µF and 0.01 µF between the AGND, DGND and the AV_{EE}, DV_{EE} respectively as close as possible to the IC pins. Also, connect a bypass capacitor between the DGND and the VTT (−2V) closely to the terminal resistors. The most suitable capacitor is a 0.01 µF ceramic chip type.
- For the external Rset resistor connected to the FS ADJ pin, the wiring should be as short as possible.

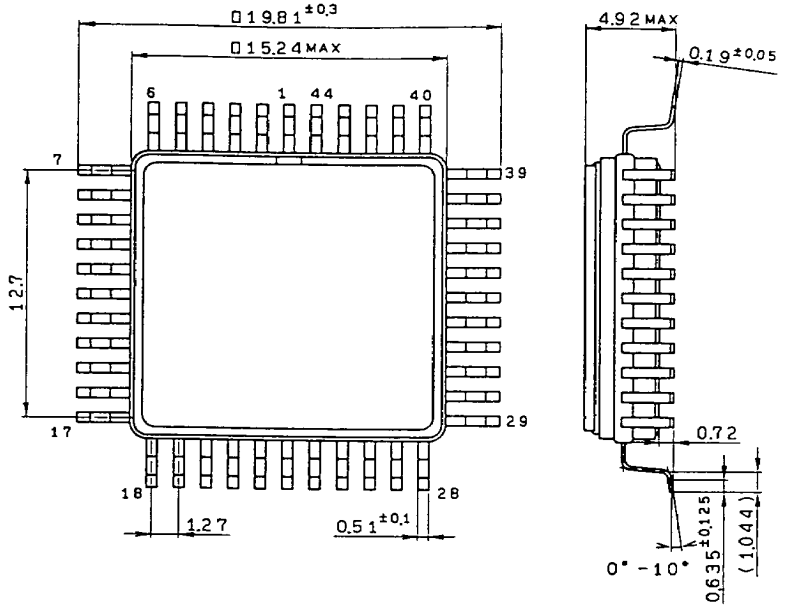
(3) Preventing Output Oscillation
Insert a 0.1 µF capacitor between the COMP and AVEE pins with the shortest distance possible.

(4) Procedures for Analog Output
The D/A converter is designed to directly drive a 50Ω or 75Ω line.
For line matching, both ends of the line must be terminated at 50Ω (or 75Ω) as shown in the application circuit.

(5) When C1 is "0" and C2 is "1", a 50% CLK must be input for the duty cycle. When the CLK duty cycle is off, the ratio of the analog output width for DA and DB is directly affected.

Package Outline Unit : mm

44pin QFP (Ceramic)



SONY NAME	QFP-44C-L01
EIAJ NAME	XQFP044-G-0000-A
JEDEC CODE	MO-084-AB*

* (Similar)

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