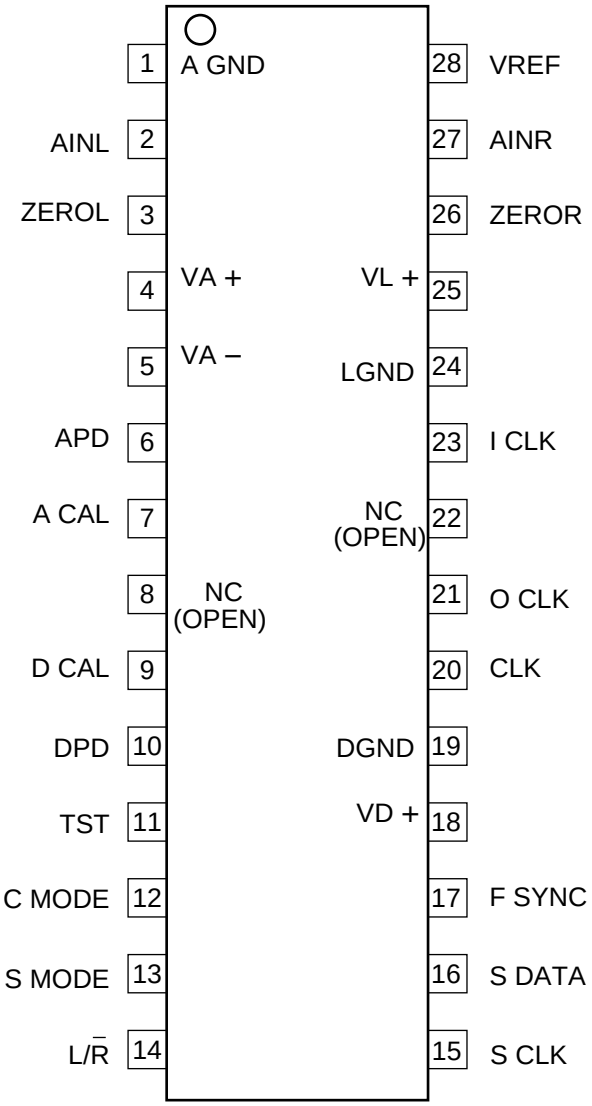
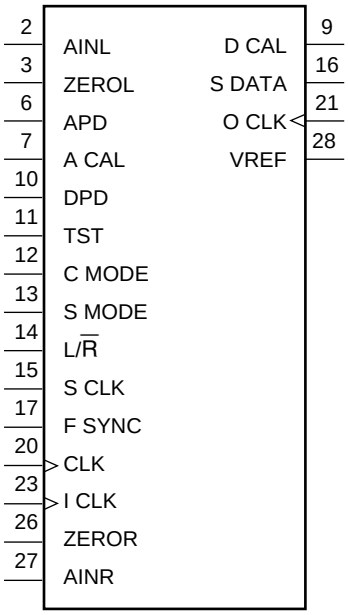
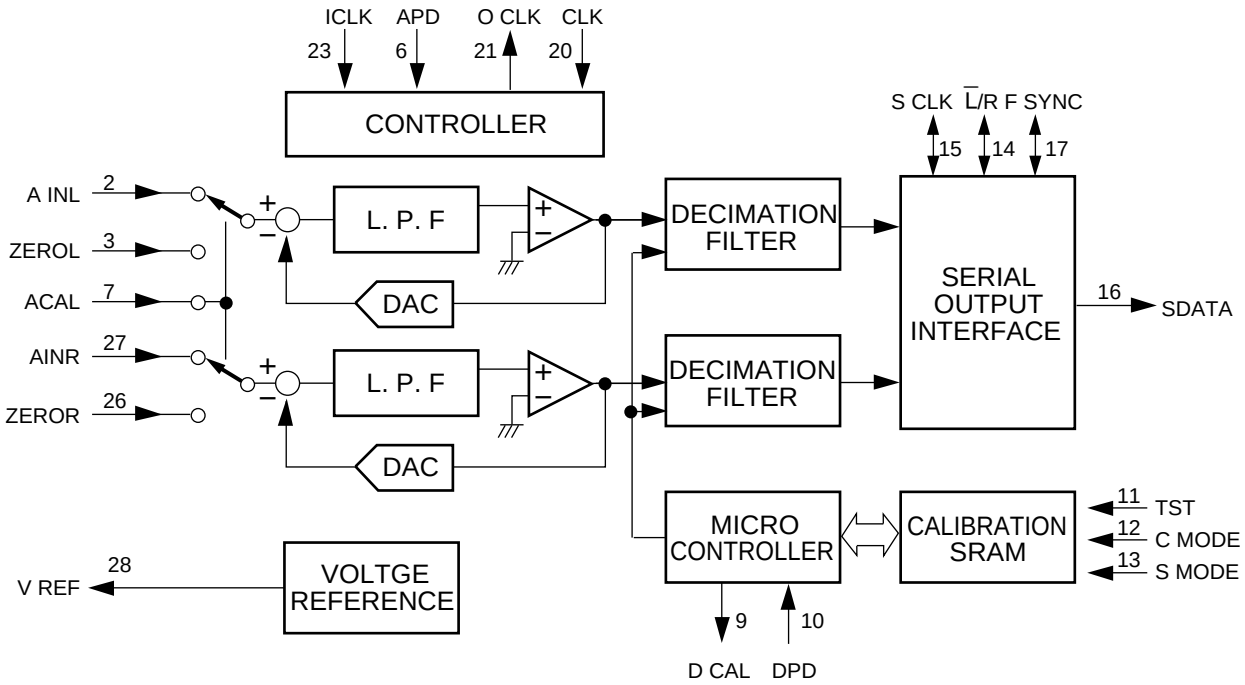
C-MOS OVER-SAMPLING STEREO A/D CONVERTER

—TOP VIEW—





A GND ; ANALOG GROUND
D GND ; DIGITAL GROUND
L GND ; LOGIC GROUND
VA + ; V_{CC} FOR ANALOG
VA – ; V_{EE} FOR ANALOG
VD + ; V_{CC} FOR DIGITAL
VL + ; V_{CC} FOR LOGIC



INPUT

ACAL	;	ANALOG CALIBRATION NORMALLY, CONNECT TO DCAL PIN.
AINL	;	L CHANNEL ANALOG INPUT
AINR	;	R CHANNEL ANALOG INPUT
APD	,	ANALOG POWER DOWN (H = POWER DOWN MODE) NORMALLY, CONNECT TO DPD PIN.
CLK	;	MASTER CLOCK
CMODE	;	MASTER CLOCK SELECTION L : CLK = 256fs H : CLK = 384fs
DPD	;	DIGITAL POWER DOWN (H = POWER DOWN MODE)
ICLK	;	128fs CLOCK INPUT (CONNECT TO OCLK PIN.)
L/$\overline{R}$	;	INPUT CHANNEL SELECTION DATA CHANNEL OUTPUT FROM SDATA PIN IS SELECTED. (H = L CHANNEL DATA, L = R CHANNEL DATA)
SCLK	;	SERIAL DATA OUTPUT CLOCK
SMODE	;	INTERFACE SELECTION L : CONTROLED MODE H : CONTROL MODE
TST	;	TEST (CONNECT TO DGND)
ZEROL	;	L CHANNEL ZERO LEVEL INPUT
ZEROR	;	R CHANNEL ZERO LEVEL INPUT

OUTPUT

DCAL	;	DIGITAL CALIBRATION
OCLK	;	128fs CLOCK OUTPUT
SDATA	;	SERIAL DATA OUTPUT DATA IS OUTPUT IN ORDER FROM MSB IN 2ND COMPLEMENT.
VREF	;	REFERENCE VOLTAGE SUPPLY OF –3.68V