A Modular Embedded DRAM Core Concept in 0.24 μm Technology

Konrad Schönemann

SIEMENS AG
Semiconductor Group
Balanstr. 73
D - 81617 München, Germany
konrad.schoenemann@hl.siemens.de

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Abstract

The development of embedded DRAMs is an important step ahead due to the processor-memory performance gap and the need for new memory architectures with high data bandwidths.

In this paper, the motivation for the development of embedded DRAMs is shown, followed by an introduction to advantages, disadvantages, applications and market shares of embedded systems. The main part of the paper is a description of the SIEMENS Modular Embedded DRAM Core Concept, that allows a customer a large number of degrees of freedom in customizing his special embedded DRAM application.

1. Introduction

In the evolution of integrated circuits the technologies for processing logic devices and dynamic memory devices have diverged because of the different requirements for these circuits.

Logic devices need very fast transistors because of the complexity of the logic structures, e.g. in processors. This can be achieved by extremely thin gate oxides. But these oxides cannot be used in a DRAM technology because they lead to high leakage currents and thus to short retention times. This means that DRAMs have to use thicker gate oxides than logic devices and so the short switching times of a logic transistor can not be met in a DRAM cell transistor.

Because of the irregular organisation of logic circuits a logic technology needs a higher number of metalization layers than a DRAM technology using the regular structures of memories.

Embedded systems, consisting of logic and embedded DRAM, can be developed from two directions:

- By using a logic technology the logic part of the chip benefits from the fast transistors, but because of the high saturation current the memory cannot be realized with a 1T cell. This means a relatively high area penalty. In this case an embedded system may not compete against a classical printed circuit board (PCB) solution in terms of silicon area, if a large amount of memory is required. On the other hand a very compact logic design is possible because of the high number of metalization levels.

- A DRAM technology allows the creation of embedded DRAMs with very low leakage currents, but the speed of logic transistors cannot be achieved in this case. On the other hand a DRAM technology allows the design of embedded systems with up to 128 Mbits of DRAM and more. This is impossible with a logic technology because it would lead to tremendously large chip areas.
  The disadvantages against logic technologies can be partly compensated by the introduction of one or two additional metalization layers, which allow the design of very compact logic structures. The speed of the transistors can be increased by decreasing the gate oxide thickness or the channel length relative to a commodity DRAM process.

SIEMENS has an advanced 0.24 μm DRAM trench technology and has the experience of processing high quality DRAMs in high volumes. Because our focus is on the market of embedded systems with a DRAM capacity of several Mbits, the usage of a DRAM technology best fits our customers‘ requirements.

When used in embedded DRAMs, the trench capacitor is superior to the normal stacked capacitor, be-

cause the planar trench cell array induces no step at the transition to the periphery whereas a stack cell array results in this step, which causes a critical thinning of the metal lines and reduces the resolution for the lithography.

Additionally the trench cell is less susceptible to noise and other disturbance than the stacked cell, because the trench cell lies deeply buried in the substrate.

2. Motivation for Embedded DRAM

In the last years an increasing gap was observed between processor and DRAM speed: the performance of processors increased by 60% per year in contrast to only a 10% improvement of the performance of commodity DRAMs. Several cache structures where introduced to partially compensate this performance gap at the expense of increased latency, which in turn limited the performance of many applications.

The integration of a logic circuit and a sufficient amount of dynamic memory on the same substrate offers the possibility of lowering this performance gap because of the following advantages [1]:

+ The on-chip memory interface of an embedded DRAM allows the replacement of large off-chip drivers (OCD) by small on-chip drivers. This results in decreased capacitive loads, power consumption and heat loss.

+ Because the interface between memory and logic needs no OCDs and pads, a higher clock frequency can be applied to the memory.
  The wire length of the interface in embedded system can be optimized for every application. This results in lower propagation delays and in an enhancement of noise immunity.

+ In a commodity DRAM every data bit in a data word needs its own pin. Because of area aspects there is a pin limitation that directly results in a limitation of the word width. Embedded DRAMs do not need a pin for each databit, so much higher word widths are possible. In the SIEMENS embedded DRAM concept a word width of up to 512 bits per memory macro is supported.

+ If a customer needs a special memory size for his application he has to rely on the memories available on the DRAM market. By using an embedded DRAM he can get memory organisations and memory sizes that are not available as commodity DRAMs.

+ The integration of several devices on the same substrate allows a cost reduction for packaging, because only one package and a fewer total number of interface pins are needed. By using embedded systems on a PCB the lower chipcount results in a saving of board space.

In spite of all these advantages there are still some challenges and disadvantages that should be mentioned:

- The integration of logic and DRAM can‘t be mastered without an adjustment of the technology as already descriped in the introduction. For this eDRAM technology new libraries must be developed and characterized, macros have to be ported and sometimes the design flow has to be adapted.

- Although the embedded memory has a decreased power consumption, the power consumption of the whole chip may increase. This can have an effect on the DRAM retention time by increasing the junction temperature of the devices.

- Because not every data bit is accessible by an external pin the known test concepts for commodity DRAMs cannot be applied to embedded DRAM. Therefore a special eDRAM test concept has to be developed.

- If a customer has decided to use an embedded system he cannot later expand the on-chip memory size.

The market for embedded DRAM is growing very fast and is estimated to rise from $ 100 - 200 m in 1997 to $ 4 - 8 bn in 2001. The following four market segments are currently the largest applications of eDRAM:

• The market for 3D graphics accelerator chips for laptops and other portable devices. In this segment the advantages of high performance and low power dissipation are the key features.

• The market for hard disk drive controllers. This segment does not benefit as much from the high data bandwidth as the graphics market but exploits the low system costs.

• The market for printer controllers. It has similiar requirements as the hard disk drive market.

• The market for network switching. This is the high end market for embedded DRAM: very large

memories with up to 128 Mbits and bus widths with 512 bits are needed for the operation in networks.

3. State of the art

Since the volume manufacturing of embedded DRAM is new, only a few companies have introduced embedded DRAM concepts. As shown above, the main market for eDRAM is in product categories with very short development times and life cycles, where customized memory cores are needed. Because the development of a new dynamic memory or even a cut-down from an existing design can last nearly as long as the life cycle of the dedicated product, no company can afford to start with the development after the customer request.

Therefore most companies offering embedded DRAM concepts provide a certain number of tailored DRAM cores with different, but fixed parameters like memory size, page length, word width and redundancy capability. A customer in need of an embedded DRAM for a special application must choose between the available cores and take the one that best fits his needs.

4. The SIEMENS Modular Embedded DRAM Core Concept

SIEMENS decided to choose a completely different approach and developed a modular embedded DRAM core concept in its 0.24 µm DRAM trench technology.

The concept lets our customers realize tailored solutions in a very short time, with the uncompromising quality of standard DRAMs. This can be achieved, because the eDRAM core concept has a large number of degrees of freedom the customer can choose from.

4.1 Modularity and flexibility

The modular embedded DRAM core concept is based on the idea of a toolbox. In this toolbox all parts are available that are needed to form a customer specific embedded DRAM core.

The main part is a 1 Mbit memory block containing all cells, wordlines and bitlines, that are needed for a memory array, and additionally the whole row path with row decoder, wordline drivers and word redundancy steering circuits for this memory block. Based on this building block the creation of memories with up to 128 Mbit are supported with a memory granularity of 1 Mbit.

The other parts in the toolbox are all building blocks that are needed in the interface to perform DRAM functionality: column decoder, secondary sense amplifier, data multiplexer, column redundancy fuses, data I/O, address input, test interface and power supply module.

The construction of a memory core depends on the application and the customer‘s requirements. First of all he must know the general operating conditions of the embedded DRAM: the size of the memory, the page length, the data word width, the latency mode, the clock frequency and the memory organisation.

The core concept supports a multi bank operation mode with up to four independent banks in one memory module, where a memory module is a concatenated stack of memory blocks with a shared interface. In this memory module up to 16 1Mbit building blocks can be stacked above each other. Because of power consumption aspects, the maximum number of memory blocks, that can be activated in parallel, is 8. As a 1Mbit memory block has a pagelength of 2 kbits, the maximum page length, that can be achieved by parallel activation, is 16 kbit. More than 8 blocks can be activated in parallel at the expense of an extra power supply module.

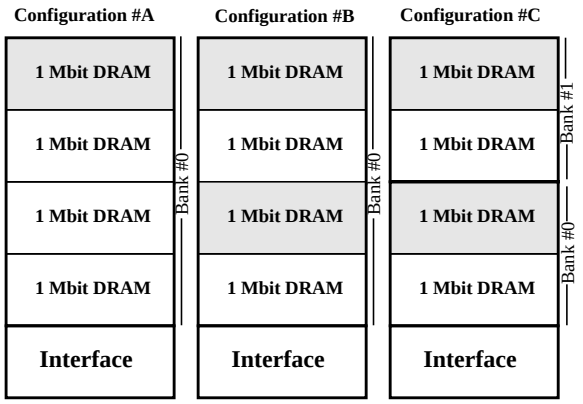

Figure 1: Examples of Embedded DRAM cores

Figure 1 shows three different memory configurations. Each of them has a memory size of 4 Mbit. Configuration #A consists of one bank, where only one memory block can be activated at a time. An activated memory block appears greyed-out in the figure. This activation results in a page length of 2 kbit.

Configuration #B consists of one bank, but in this bank two memory blocks are activated in parallel. In this example a page length of 4 kbits is available at the expense of a higher activation current.

Configuration #C consists of two banks. In every bank only one memory block can be activated at a time. Basically this results in a page length of 2 kbit. But by activating bank #0 and then bank #1 a page length of 4

kbit is possible. The customer can decide by addressing whether he wants to operate the DRAM core in a high power mode or in a low power mode.

The word width delivered by the interface is 64 bit. By activating up to 8 memory modules in parallel a maximum data word width of 512 bit is possible.

If a customer needs a small memory with a high data word width he can expand the word width of one memory module to 128 bit by using two 64 bit interfaces in parallel in only one memory module as shown in figure 2.

This does not mean that for the wide 128 bit interface the double area of a 64 bit interface is needed, because some circuits, notably the column decoder and the test interface, are needed only once for both 64 bit interfaces.

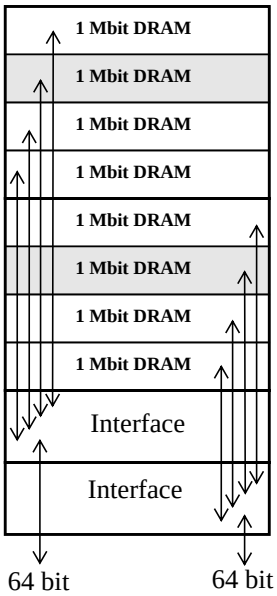

Figure 2: Embedded DRAM with 128 bit interface

The core concept offers the programmable latency stages of latency 1, 2 and 3. In latency mode 3 the embedded DRAM can be clocked with up to 166 MHz, depending on the memory size.

A memory module with an interface of 64 bit wordwidth achieves data rates of up to 10.6 Gbit/s in page mode. By combining four of the memory modules shown in figure 2 with a total data word width of 512 bit, a maximum data rate of 84.8 Gbit/s in page mode can be achieved.

Because of the set of finished building blocks it only takes a few days to compose the layout of the eDRAM macro and to create all other views, that are requested by the customer.

4.2 Redundancy

The redundancy performance needed in an eDRAM core depends on the application and the memory size. For instance, graphics applications may have less stringent error requirements and so may use a less powerful redundancy than is needed for the program memory in high-end applications.

The redundancy concept of the embedded DRAM core concept offers row- and column redundancy, that can be configured in wide ranges to be adapted to the application. In this way the area penalty of the redundancy can be tailored to the customer‘s requirements.

Every 1 Mbit building block has a fixed number of redundant word line clusters. Depending on the wanted redundancy capability, the size of the spare word line cluster can be chosen from three different versions.

The redundant clusters can repair defective word lines both in the same memory block and in other memory blocks. The capability of this interblock word redundancy depends on the memory size and the activation scheme of the core and can be increased at the expense of some additional space in the area of the local sense amplifiers.

The column redundancy is based on a new flexible approach, that was developed for modular DRAM applications. It allows one to expand the redundancy performance to the customer‘s needs and uses the available redundant cells in a more efficient way than the conventional concepts. Because of patent evaluation reasons further information cannot yet be presented.

4.3 Test concept

SIEMENS offers an embedded DRAM quality that meets the high quality standards of commodity DRAMs. To provide this, SIEMENS has developed a special embedded DRAM test concept, based on the on-chip integration of a test controller, which can be programmed by an external automated test equipment (ATE), and which is able to apply all test patterns to the memory. Because not every data I/O is accessible by its own external pin, the read data can be compressed and afterwards be evaluated by the ATE. Figure 3 shows a diagram of the embedded DRAM test concept [2]. The customer can choose between two supported test modes.

- The direct access provides the same functionality as commodity DRAMs and can be used for bit fail map generation, yield analysis and redundancy calculation. Therefore multiplexers and registers are implemented to use the available number of external pins.

- The Test Controller also provides a built-in-logic to support algorithmic test pattern generation (ATPG) and expected value comparison. This test mode is needed for package tests on a normal logic ATE without memory test option. Additionally the built-in-logic also provides a built-in power-on self test and burn-in capabilities.

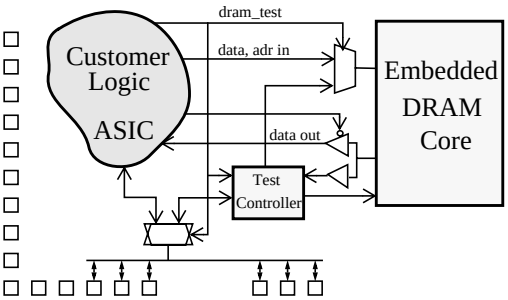

Figure 3: The Embedded DRAM Test Concept with Test Controller

The Test Controller always presents the same hardware to the ATE regardless of the internal core configuration and allows the reuse of ATE test software with only small modifications. For wafer test, a memory tester or a logic tester with memory test option is required, whereas for package test any logic tester can be taken.

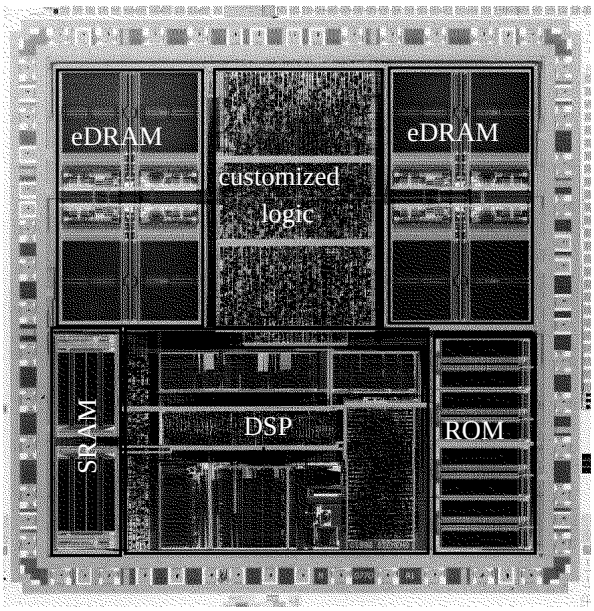

Figure 4: Die photo of an embedded chip for voice applications

4.4 Applications

SIEMENS has nearly 10 years of experience in developing embedded DRAMs, starting with a PIP (picture in picture) device for TV applications in 1989. This was the first embedded DRAM application and was produced in a 1 Mbit technology.

In figure 4 the chip photo of an embedded device is shown, that was dedicated to speech recognition applications. This chip was designed in 1997 in a 0.35µm DRAM technology and included 1 Mbit DRAM, a DSP core, ROM and SRAM.

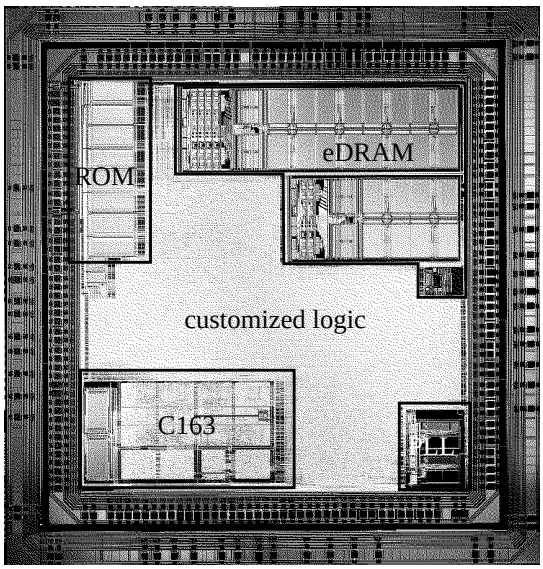

Figure 5: Die photo of an integrated hard-disk-drive controller with 1.5 Mbit eDRAM

Figure 5 and figure 6 show die photos of two integrated hard-disk-drive controllers. These devices are produced in a 0.35 µm technology and include 1.5 Mbit respectively 1.875 Mbit of embedded DRAM in addition to all other components, that are required for the controller operation [3],[4].

5. Conclusion

In this paper a modular embedded DRAM core concept in a 0.24 µm DRAM technology has been introduced. The modularity and the flexibility of this approach allow the design of customized embedded DRAM cores in a very short time.

The core concept performs the creation of embedded DRAMs with a memory size of up to 128 Mbit and supports a large number of memory organisations and

memory activation schemes.

An innovative redundancy concept permits the adaption of the redundancy capability to the application and so keeps the area penalty low.

To arrive at an equivalent quality as known from commodity DRAMs, a special test concept based on the on-chip integration of a test controller was developed and implemented.

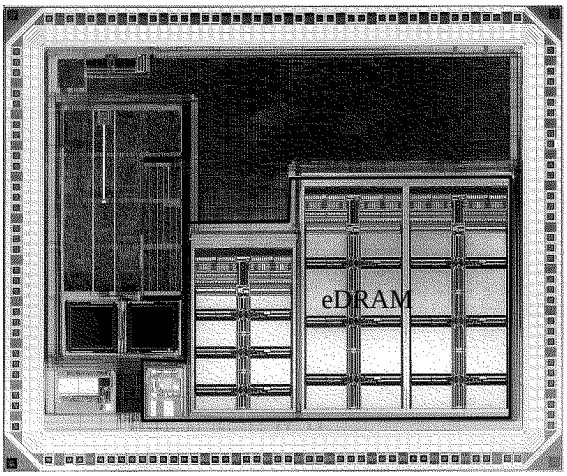

Figure 6: Die photo of an integrated hard-disk-drive controller with 1.875 Mbit eDRAM

The comparison of pros and cons of embedded DRAMs, the inspection of the embedded DRAM market and the introduction of some applications for embedded DRAMs show the wide range of use and the market potential for this modular embedded DRAM core concept.

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