DATA SHEET

CGY2010G; CGY2011G
GSM 4 W power amplifiers

Objective specification
Supersedes data of 1995 Oct 25
File under Integrated Circuits, IC17

1996 Jul 08

Philips Semiconductors

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FEATURES

- Power Amplifier (PA) overall efficiency 45%
- 35.5 dB gain
- 0 dBm input power
- Gain control range >55 dB
- Integrated power sensor driver
- Low output noise floor of PA < –129 dBm/Hz in GSM RX band
- Wide operating temperature range –20 to +85 °C
- LQFP 48 pin package
- Compatible with power ramping controller PCA5075
- Compatible with GSM RF transceiver SA1620.

APPLICATIONS

- 880 to 915 MHz hand-held transceivers for E-GSM applications
- 900 MHz TDMA systems.

GENERAL DESCRIPTION

The CGY2010G and CGY2011G are GSM class 4 GaAs Monolithic Microwave Integrated Circuits (MMICs) power amplifiers specifically designed to operate at 4.8 V battery supply. These ICs also include a power sensor driver so that no directional coupler is required in the power control loop.

Both ICs have the same performance but are issued from different wafer fabs.

The PAs require only a 30 dB harmonic low-pass filter to comply with the GSM transmit spurious specification. They can be switched off and their power controlled by monitoring the actual drain voltage applied to the amplifier stages.

QUICK REFERENCE DATA

SYMBOL	PARAMETER (1)	MIN.	TYP.	MAX.	UNIT
V_{DD}	positive supply voltage	–	4.2	–	V
I_{DD}	positive peak supply current	–	1.8	–	A
$P_{out(max)}$	maximum output power	–	35.5	–	dBm
T_{amb}	operating ambient temperature	–20	–	+85	°C

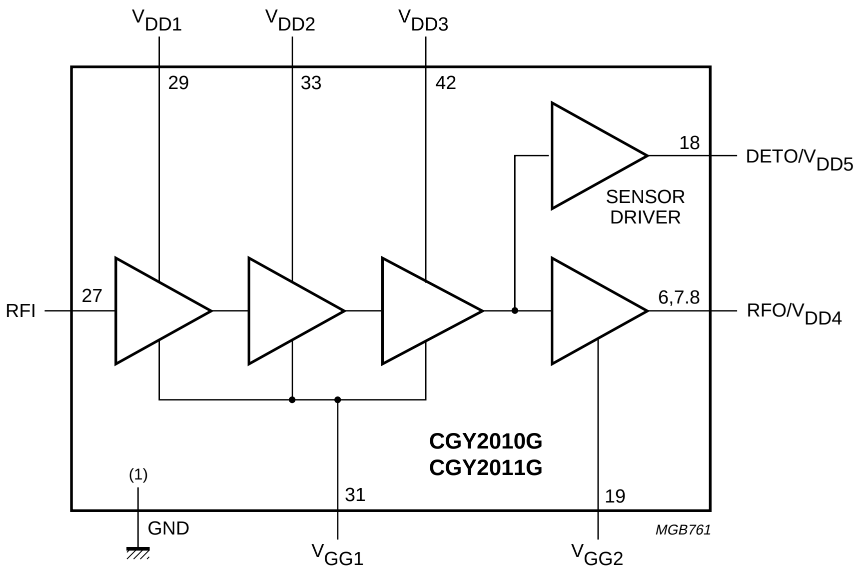
Note

1. For conditions, see Chapters “AC characteristics” and “DC characteristics”.

ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
CGY2010G	LQFP48	plastic low profile quad flat package; 48 leads; body 7 × 7 × 1.4 mm	SOT313-2
CGY2011G			

BLOCK DIAGRAM



(1) Ground pins 1 to 5, 9 to 17, 20 to 26, 28, 30, 32, 34 to 41 and 43 to 48.

Fig.1 Block diagram.

PINNING

SYMBOL	PIN	DESCRIPTION
GND	1 to 5	ground
RFO/V_{DD4}	6 to 8	power amplifier output and fourth stage supply voltage
GND	9 to 17	ground
DETO/V_{DD5}	18	power sensor output and supply voltage
V_{GG2}	19	fourth stage negative gate supply voltage
GND	20 to 26	ground
RFI	27	power amplifier input
GND	28	ground
V_{DD1}	29	first stage supply voltage
GND	30	ground
V_{GG1}	31	first three stages negative gate supply voltage
GND	32	ground
V_{DD2}	33	second stage supply voltage
GND	34 to 41	ground
V_{DD3}	42	third stage supply voltage
GND	43 to 48	ground

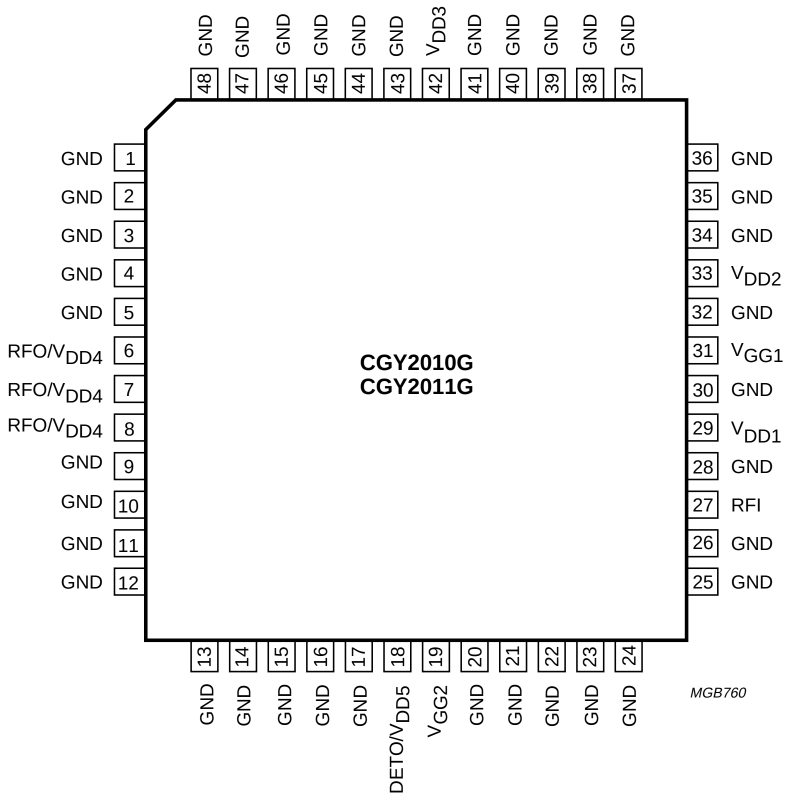


Fig.2 Pin configuration.

FUNCTIONAL DESCRIPTION

Operating conditions

The CGY2010G and CGY2011G are designed to meet the European Telecommunications Standards Institute (ETSI) GSM documents, the *“ETS 300 577 specification”*, which are defined as follows:

- t_{on} = 542.8 μs
- T = 4.3 ms
- Duty cycle = 1/8

The devices are specifically designed for pulse operation allowing the use of a LQFP48 plastic package.

Power amplifier

The power amplifier consists of four cascaded gain stages with an open-drain configuration. Each drain has to be loaded externally by an adequate reactive circuit which also has to be a DC path to the supply.

The amplifier bias is set by means of a negative voltage applied at pins V_{GG1} and V_{GG2}. This negative voltage must be present before the supply voltage is applied to the drains to avoid current overstress for the amplifier.

Power sensor driver

The power sensor driver is a buffer amplifier that delivers a signal to the DETO output pin which is proportional to the amplifier power. This signal can be detected by external diodes for power control purpose. As the sensor signal is taken from the input of the last stage of the PA, it is isolated from disturbances at the output by the reverse isolation of the PA output stage.

Impedance mismatch at the PA output therefore, does not significantly influence the signal delivered by the power sensor as this normally occurs when power sense is made using a directional coupler. Consequently the cost and space of using a directional coupler are saved.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134); general operating conditions applied.

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	positive supply voltage	–	7	V
V_{GG}	negative supply voltage	–	–10	V
$T_{j(max)}$	maximum operating junction temperature	–	150	°C
T_{stg}	IC storage temperature	–	150	°C
P_{tot}	total power dissipation	–	1.5	W

THERMAL CHARACTERISTICS

General operating conditions applied.

SYMBOL	PARAMETER	VALUE	UNIT
$R_{th\ j\text{-}c}$	thermal resistance from junction to case; note 1	32	K/W

Note

1. This thermal resistance is measured under GSM pulse conditions.

DC CHARACTERISTICS

V_{DD} = 4.5 V; T_{amb} = 25 °C; general operating conditions applied; peak current values during burst; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Pins RFO/V_{DD4}, V_{DD3}, V_{DD2}, V_{DD1} and DETO/V_{DD5}						
V_{DD}	positive supply voltage		0	4.2	5.5	V
I_{DD}	positive peak supply current		–	1.8	2.2	A
Pins V_{GG1} and V_{GG2}						
V_{GG1}	negative supply voltage	note 1	–	–2	–	V
V_{GG2}	negative supply voltage	note 1	–	–2	–	V
$I_{GG1} + I_{GG2}$	negative peak supply current		–	2.5	5	mA

Note

1. The negative bias V_{GG1} and V_{GG2} must be applied 10 µs before the power amplifier is switched on, and must remain applied until the power amplifier has been switched off.

AC CHARACTERISTICS

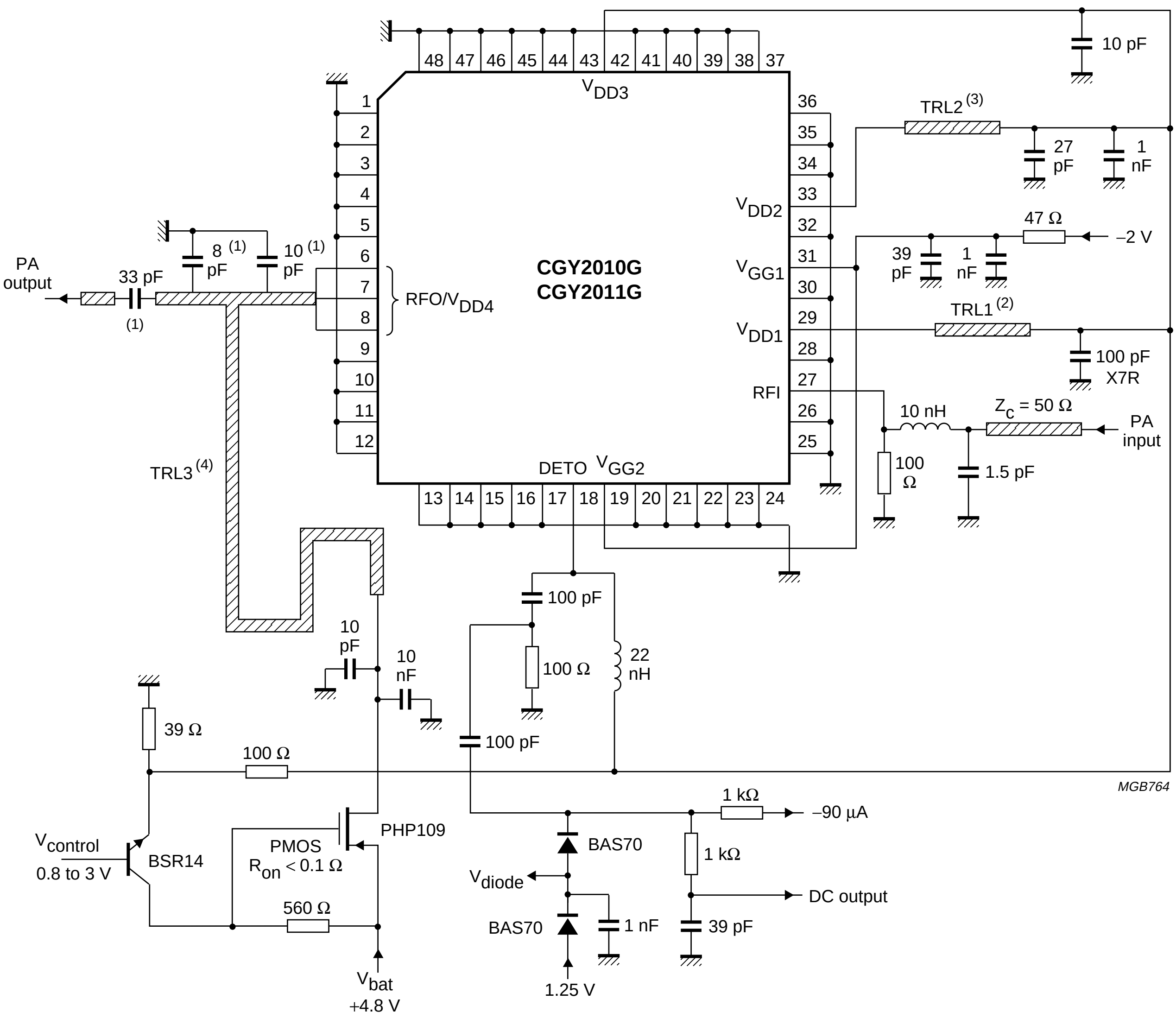
V_{DD} = 4.5 V; T_{amb} = 25 °C; general operating conditions applied; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Power amplifier						
P_{in}	input power		–1.5	–	+1.5	dBm
S_{11}	input return loss	note 1; 50 Ω source	–	–	–6	dB
f_{RF}	RF frequency range		880	–	915	MHz
$P_{out(max)}$	maximum output power	T_{amb} = 25 °C; V_{DD} = 4.5 V	34.5	35.5	–	dBm
		T_{amb} = –20 to +85 °C; V_{DD} = 4.2 V	32.5	–	–	dBm
η	efficiency	V_{DD} = 4.2 V	–	45	–	%
$P_{out(min)}$	minimum output power	V_{DD} < 0.1 V	–	–	–20	dBm
N_{RX}	output noise in RX band	f_{RF} = 925 MHz at $P_{out(max)}$	–	–	–117	dBm/Hz
		f_{RF} = 935 MHz at $P_{out(max)}$	–	–	–129	dBm/Hz
		f_{RF} = 960 MHz at $P_{out(max)}$	–	–	–129	dBm/Hz
H2	2nd harmonic level		–	–33	–30	dBc
H3	3rd harmonic level		–	–40	–37	dBc
Stab	stability	note 2	–	–	–70	dBc
Power sensor driver						
$P_{out(DET)}$	sensor driver output power	R_L = 100 Ω; relative to PA output power into 50 Ω load	–	–23	–	dBc
$\Delta P_{out(DET)}$	driver output power variation	load VSWR < 6 : 1 at PA output	–	–	2	dB

Notes

1. Including the 100 Ω resistor connected in parallel at the power amplifier input on the evaluation board.
2. The device is adjusted to provide nominal value of load power into a 50 Ω load. The device is switched off and a 6 : 1 load replaces the 50 Ω load. The device is switched on and the phase of the 6 : 1 load is varied 360 electrical degrees during a 60 second period.

APPLICATION INFORMATION

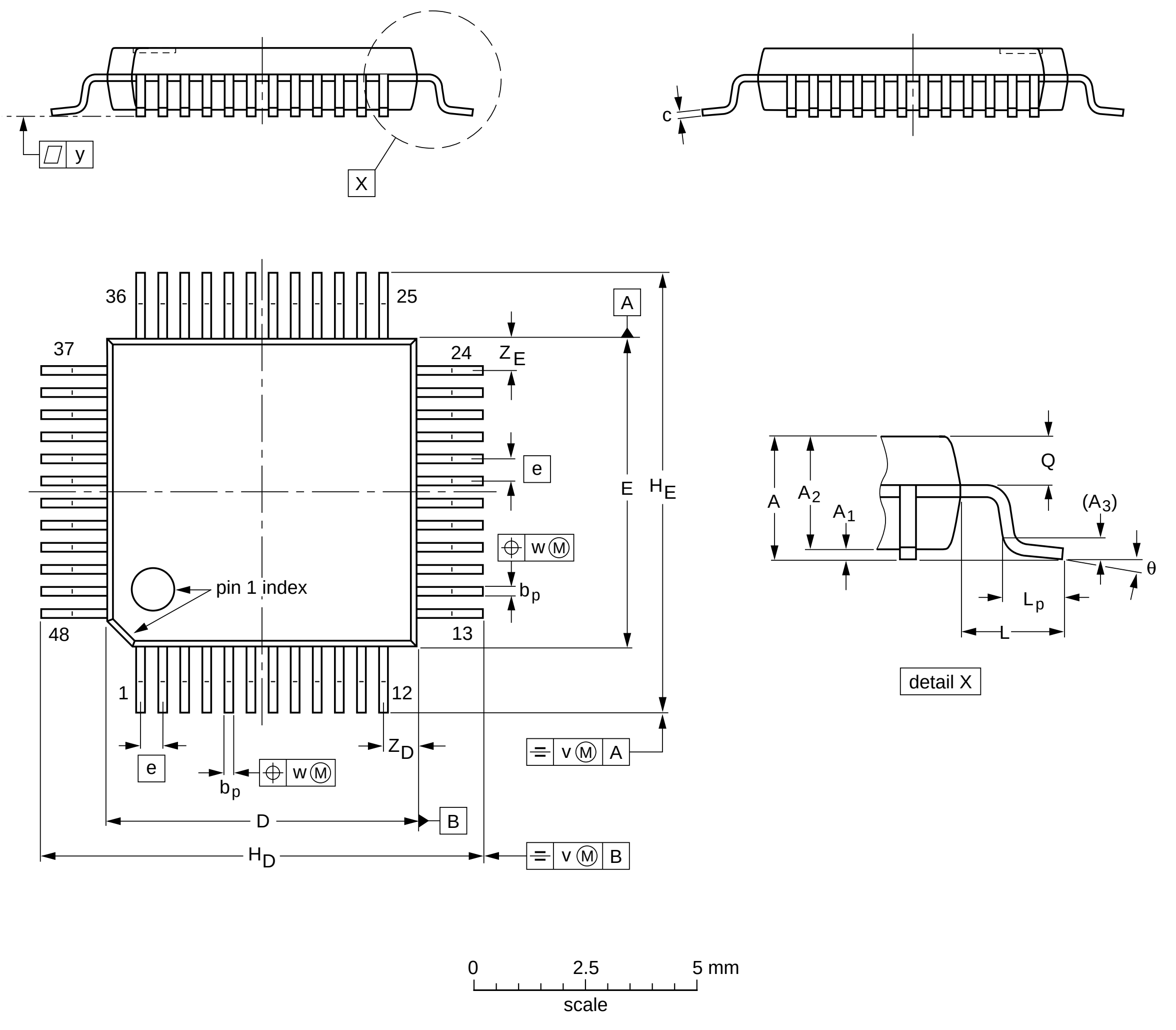


(1) These capacitors are type: SMD0402; rest of the capacitors: SMD0603.
(2) TRL1: width: 0.3 mm; length: 16 mm.
(3) TRL2: width: 0.3 mm; length: 6.3 mm.
(4) TRL3: width: 0.3 mm; length: 20 mm.

Fig.3 Evaluation board schematic (FR4, 0.8 mm).

PACKAGE OUTLINE

LQFP48: plastic low profile quad flat package; 48 leads; body 7 x 7 x 1.4 mm **SOT313-2**



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_D	H_E	L	L_p	Q	v	w	y	Z_D(1)	Z_E(1)	θ
mm	1.60	0.20 0.05	1.45 1.35	0.25	0.27 0.17	0.18 0.12	7.1 6.9	7.1 6.9	0.5	9.15 8.85	9.15 8.85	1.0	0.75 0.45	0.69 0.59	0.2	0.12	0.1	0.95 0.55	0.95 0.55	7^o 0^o

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT313-2						~~93-06-15~~ 94-12-19

SOLDERING

Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *“IC Package Databook”* (order code 9398 652 90011).

Reflow soldering

Reflow soldering techniques are suitable for all LQFP packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

Wave soldering

Wave soldering is **not** recommended for LQFP packages. This is because of the likelihood of solder bridging due to closely-spaced leads and the possibility of incomplete solder penetration in multi-lead devices.

If wave soldering cannot be avoided, the following conditions must be observed:

- **A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.**
- **The footprint must be at an angle of 45° to the board direction and must incorporate solder thieves downstream and at the side corners.**

Even with these conditions, do not consider wave soldering LQFP packages LQFP48 (SOT313-2), LQFP64 (SOT314-2) or LQFP80 (SOT315-1).

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

Repairing soldered joints

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Short-form specification	The data in this specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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