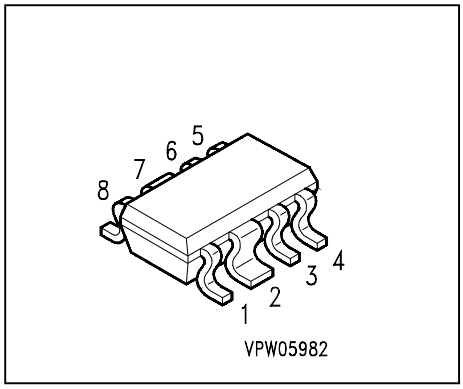
GaAs MMIC

Preliminary Data

- Broadband Power Amplifier [800..3500 Mhz]
- DECT,PHS,PCS,GSM,AMPS,WLAN,WLL
- Single Voltage Supply
- Operating voltage range: 2.0to 6 V
- Pout = 25.5dBm at Vd=2.4V
- Pout = 27.0dBm at Vd=3.0V
- Pout = 30.0dBm at Vd=5.0V
- Overall power added efficiency up to 50 %
- Easy external matching



ESD: **E**lectro**s**tatic **d**ischarge sensitive device,
observe handling precautions!

Type	Marking	Ordering code (taped)	Package
CGY 196	t.b.d.	t.b.d.	SCT598

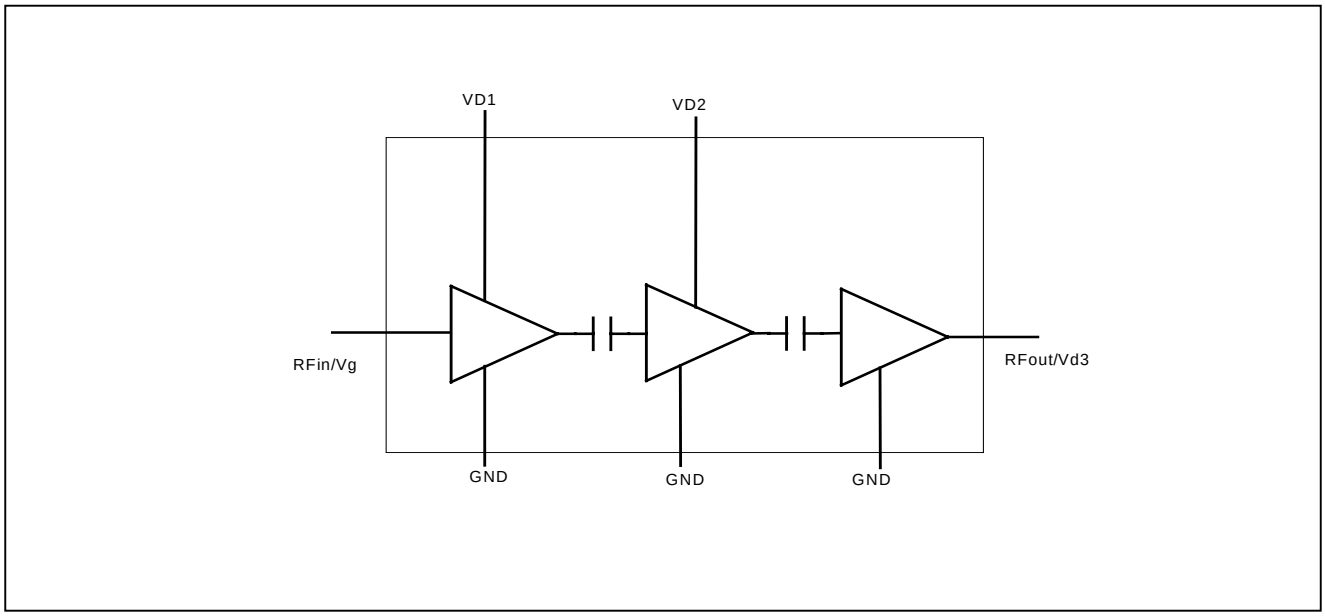
Maximum ratings

Characteristics	Symbol	max. Value	Unit
Positive supply voltage	V_D	6	V
Supply current	I_D	1.0	A
Maximum input power	*Pinmax*	20	dBm
Channel temperature	T_{Ch}	150	°C
Storage temperature	T_{stg}	-55...+150	°C
Total power dissipation *(Ts ≤ 81 °C)* *Ts: Temperature at soldering point*	P_{tot}	1.0	W
Pulse peak power	P_{Pulse}	2.0	W

Thermal Resistance

Characteristics	Symbol	max. Value	Unit
Channel-soldering point	R_{thChS}	70	K/W

Functional Block Diagram



Pin #	Name	Configuration
1	**RFin/Vg**	RF input power + Gate voltage [0V internal]
2	**GND**	RF and DC ground
3	**VD2**	Pos. drain voltage of the 2nd stage
4	**n.c.**	not connected
5	**n.c.**	not connected
6	**RFout/VD3**	RF output power / Pos. drain voltage of the 3rd stage
7	**GND**	RF and DC ground
8	**VD1**	Pos. drain voltage of the 1st stage

DC characteristics

Characteristics		Symbol	Conditions	min	typ	max	Unit
Drain current	stage 1	*IDSS1*	VD1=3V		45		mA
	stage 2	*IDSS2*	VD2=3V		65		mA
	stage 3	*IDSS2*	VD2=3V		340		mA
Transconductance	stage 1	*gfs1*	VD=3V, ID=50mA		110		mS
	stage 2	*gfs2*	VD=3V, ID=300mA		650		mS
	stage 3	*gfs3*	VD=3V, ID=300mA		650		mS

Determination of Permissible Total Power Dissipation for Continuous and Pulse Operation

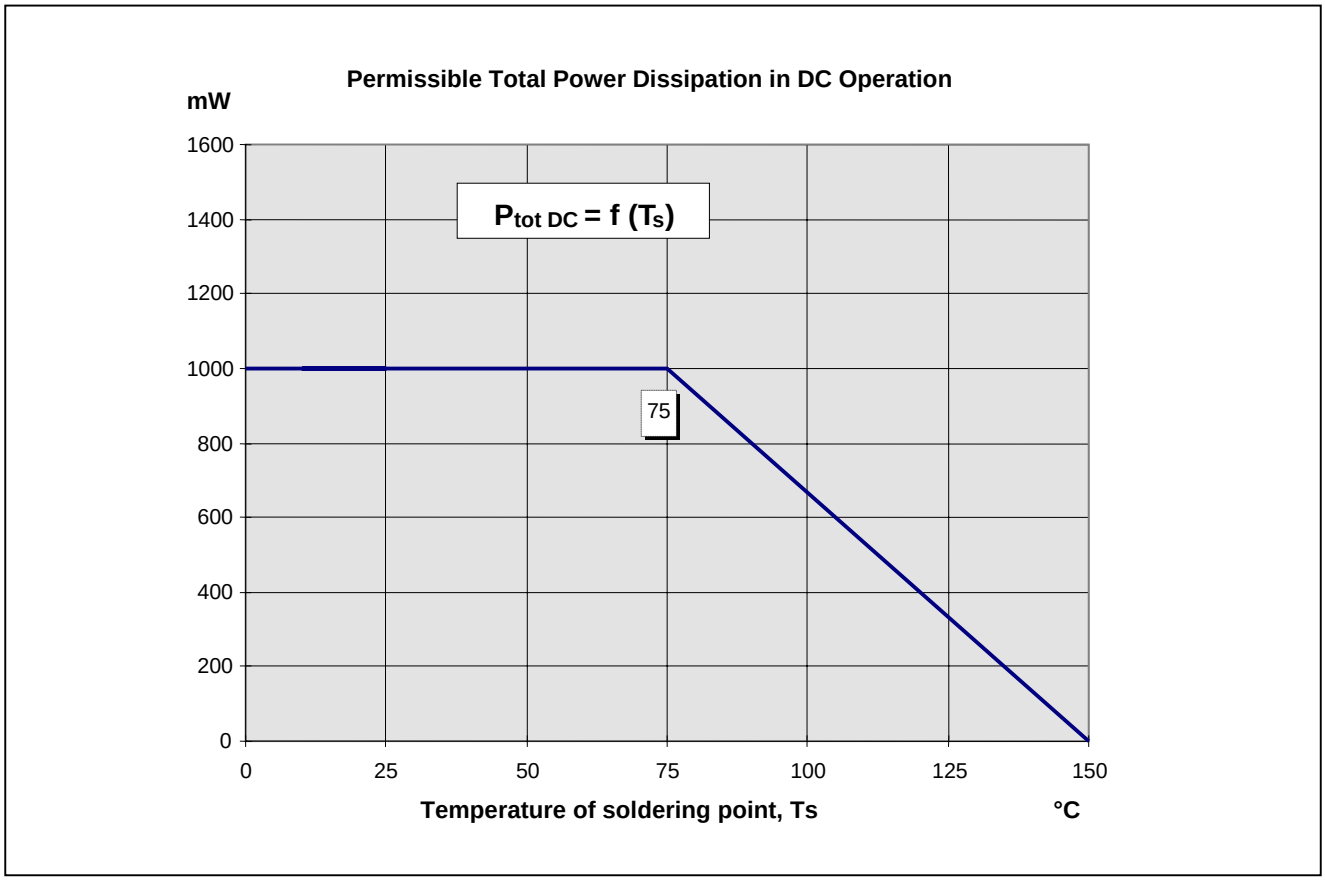
The dissipated power is the power which remains in the chip and heats the device. It does not contain RF signals which are coupled out consistently.

a) Continuous Wave / DC Operation

For the determination of the permissible total power dissipation $\mathbf{P_{tot\text{-}DC}}$ from the diagram below it is necessary to obtain the temperature of the soldering point T_S first. There are two cases:

- When R_{thSA} (soldering point to ambient) is not known: Measure T_S with a temperature sensor at the leads were the heat is transferred from the device to the board (normally at the widest source or ground lead for GaAs). Use a small sensor of low heat transport, for example a thermoelement (< 1mm) with thin wires or a temperature indicating paper while the device is operating.

- When R_{thSA} is already known: $T_S = P_{diss} \times R_{thSA} + T_A$



b) Pulsed Operation

For the calculation of the permissible pulse load $P_{tot\text{-}max}$ the following formula is applicable:

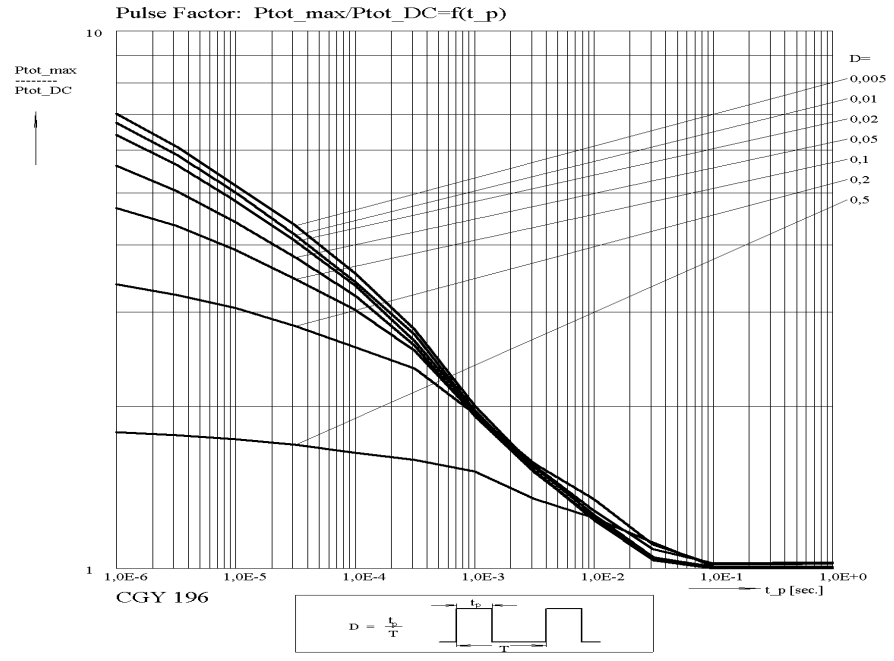
$$P_{tot\text{-}max} = P_{tot\text{-}DC} \times \text{Pulse factor}$$
$$= P_{tot\text{-}DC} \times (P_{tot\text{-}max} / P_{tot\text{-}DC})$$

Use the values for $P_{tot\text{-}DC}$ as derived from the above diagram and for the

$$\text{pulse factor} = P_{tot\text{-}max} / P_{tot\text{-}DC}$$

from the following diagram to get a specific value.

Pulse factor:



$P_{tot\text{-}max}$ should not exceed the absolute maximum rating for the dissipated power
P_{Pulse} = " Pulse peak power " = 2 W

c) Reliability Considerations

This procedure yields the upper limit for the power dissipation for continuous wave (cw) and pulse applications which corresponds to the maximum allowed channel temperature. For best reliability keep the channel temperature low. The following formula allows to track the individual contributions which determine the channel temperature.

T_{ch} =	(P_{diss} x	R_{thChS}) +	T_S
Channel temperature (= junction temperature)	Power dissipated in the chip. It does not contain decoupled RF-power	Rth of device from channel to soldering point	Temperature of soldering point, measured or calculated

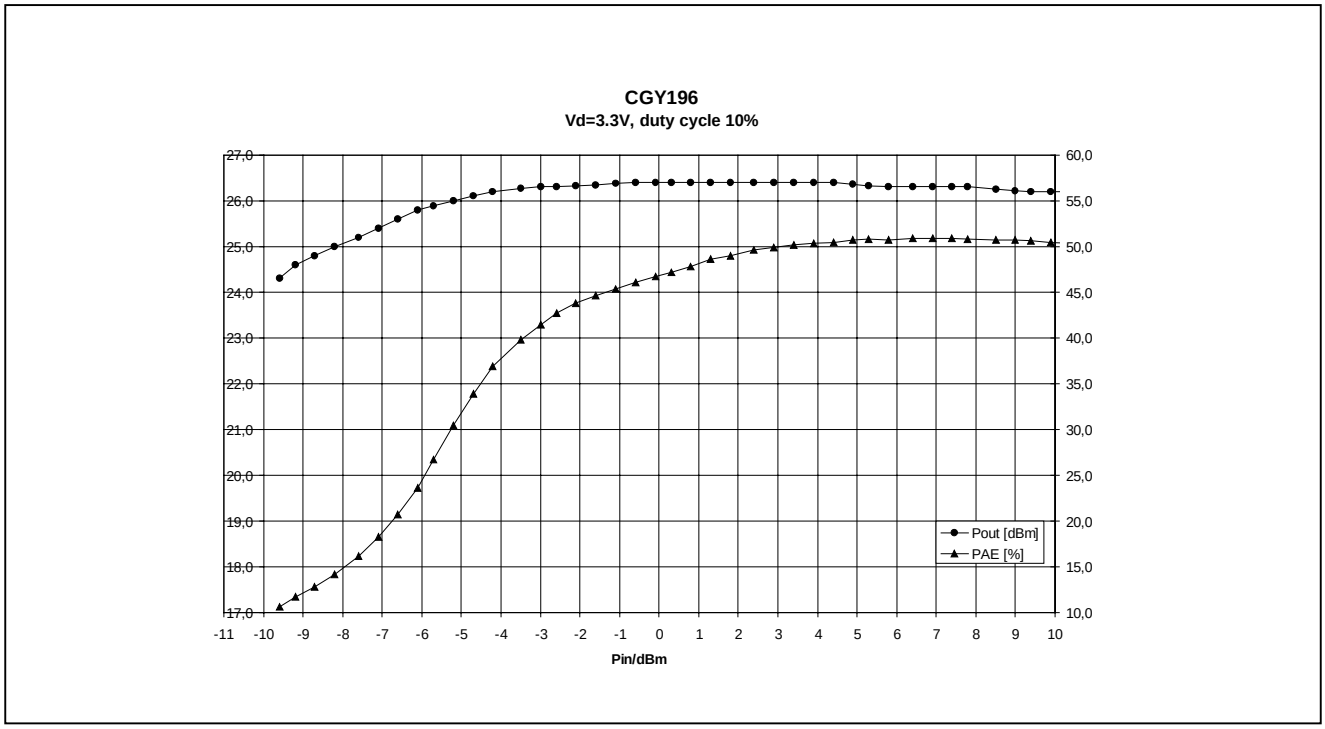
Electrical characteristics [3.0V DECT-Application: PCB-Layout see page 9]
(T_A = 25°C , f=1.89 GHz, Z_S=Z_L=50 Ohm, unless otherwise specified)

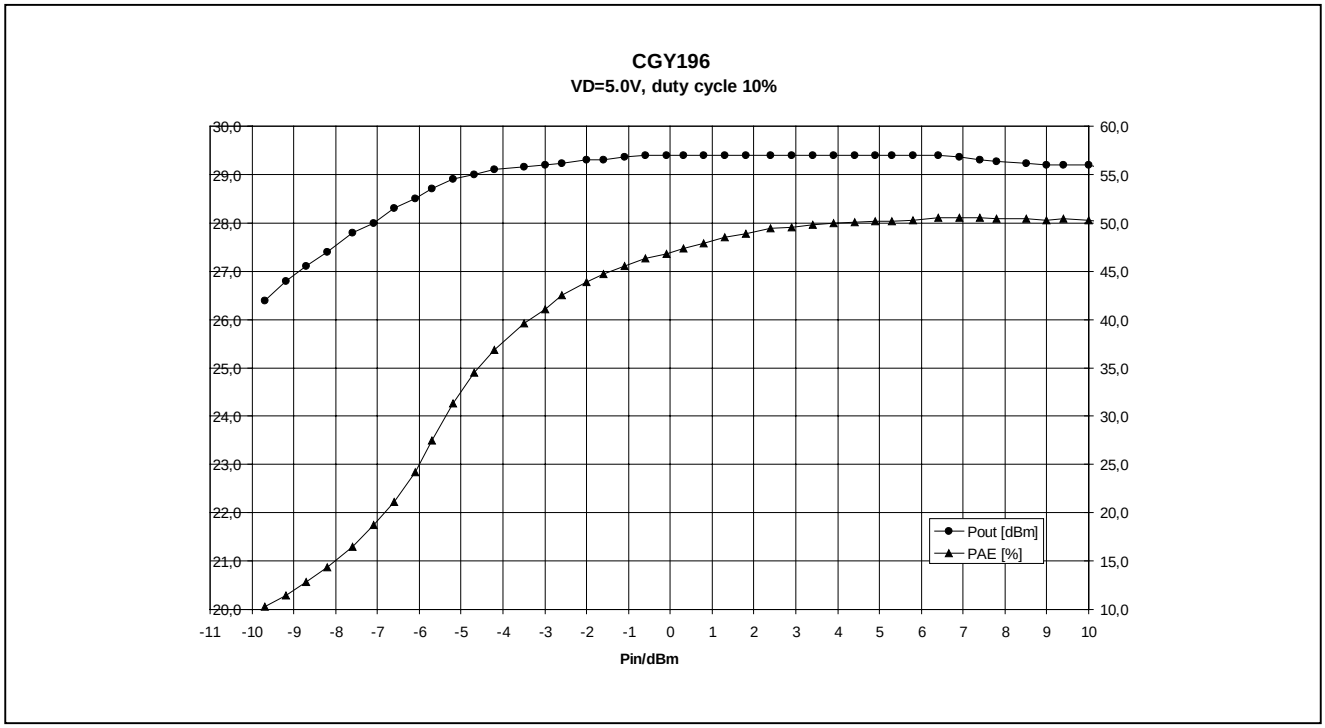
Characteristics	Symbol	min	typ	max	Unit
Supply current *VD=3.0V; Pin = +0 dBm*	I_{DD}	-	300	-	mA
Supply current *VD=3.0V; Pin = -10 dBm*	I_{DD}	-	450	-	mA
Gain *VD=3.0V; P_{in} = -10 dBm*	*G*		32		dB
Output Power *VD=3.0V; P_{in} = 0 dBm*	P_o		26.0		dBm
Overall Power added Efficiency *VD=3.0V; P_{in} = +0 dBm*	*PAE*		45	-	%
Overall Power added Efficiency *VD=3.0V; P_{in} = 3 dBm*	*PAE*		50	-	%
Supply current *VD=4.8V; Pin = -10 dBm*	I_{DD}	-	450	-	mA
Supply current *VD=4.8V; Pin = 0 dBm*	I_{DD}	-	370	-	mA
Gain *VD=4.8V; P_{in} = -10 dBm*	*G*	-	32	-	dB
Output Power *VD=4.8V; P_{in} = 0 dBm*	P_o		29		dBm
Overall Power added Efficiency *VD=4.8V; P_{in} = 0 dBm*	*PAE*		45	-	%
Overall Power added Efficiency *VD=4.8V; P_{in} = 5 dBm*	*PAE*		50	-	%
Off Isolation *VD=0V; P_{in} = 0 dBm*	*-S21*		40		dB
Load mismatch *Pin=0dBm , VD≤3.6V , Z_S=50 Ohm, Load VSWR = 20:1 for all phase,*	-	No module damage for 10 sec.			-
Load mismatch *Pin=3dBm , VD≤5.0V , Z_S=50 Ohm, Load VSWR = 20:1 for all phase,*	-	No module damage for 10 sec.			-
Stability *Pin=0dBm, VD=3.6V, Z_S=50 Ohm, Load VSWR = 3:1 for all phase*	-	All spurious output more than 70 dB below desired signal level			-
Stability *Pin=3dBm , VD=5.0V , Z_S=50 Ohm, Load VSWR = 3:1 for all phase,*	-	All spurious output more than 70 dB below desired signal level			-

Output power and power added efficiency

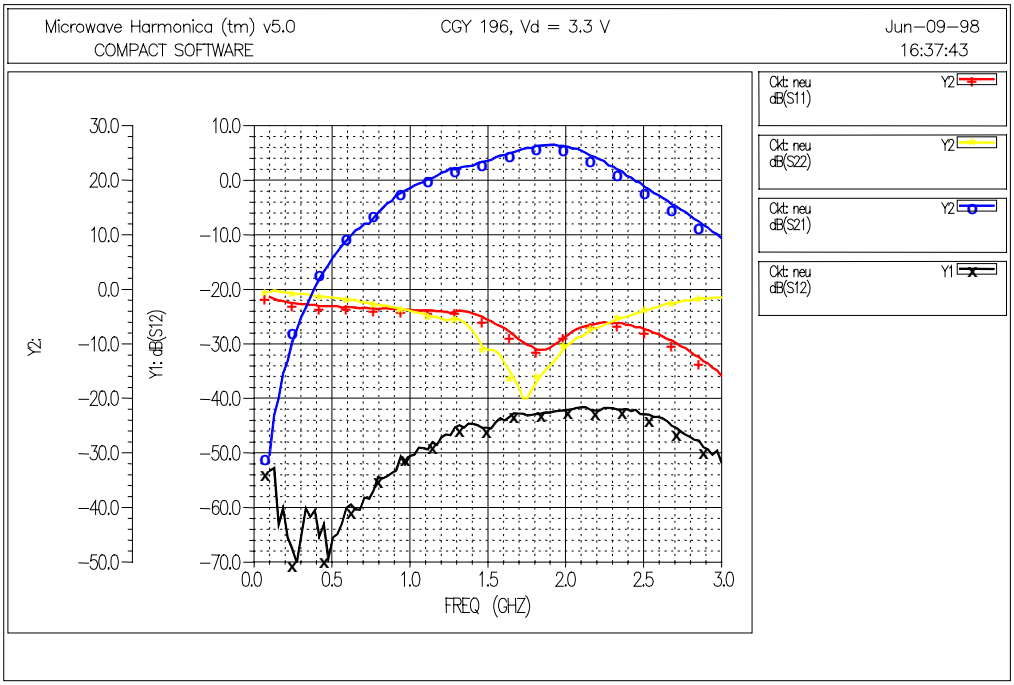
pulsed mode: T=417µs, duty cycle 12.5%

Electrical characteristics [3.0V DECT-Application: PCB-Layout see page 9]

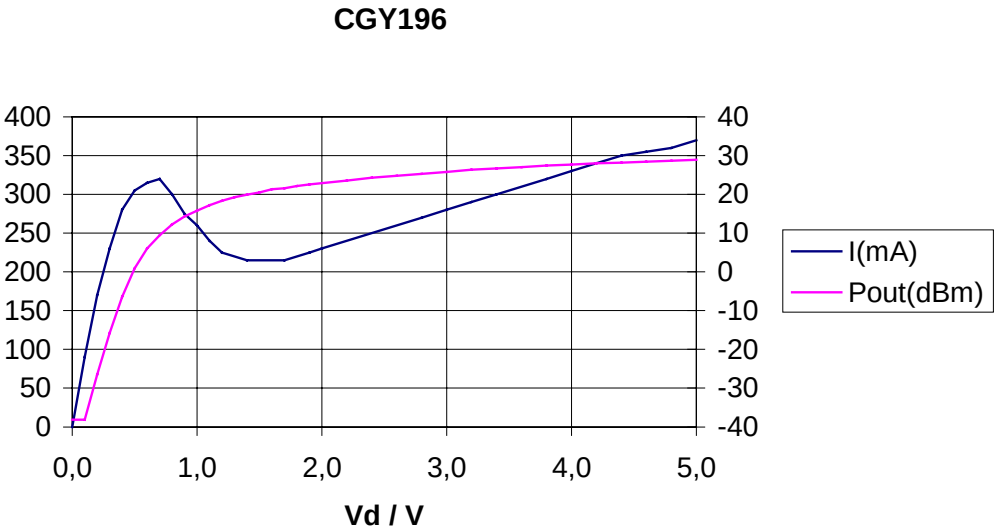




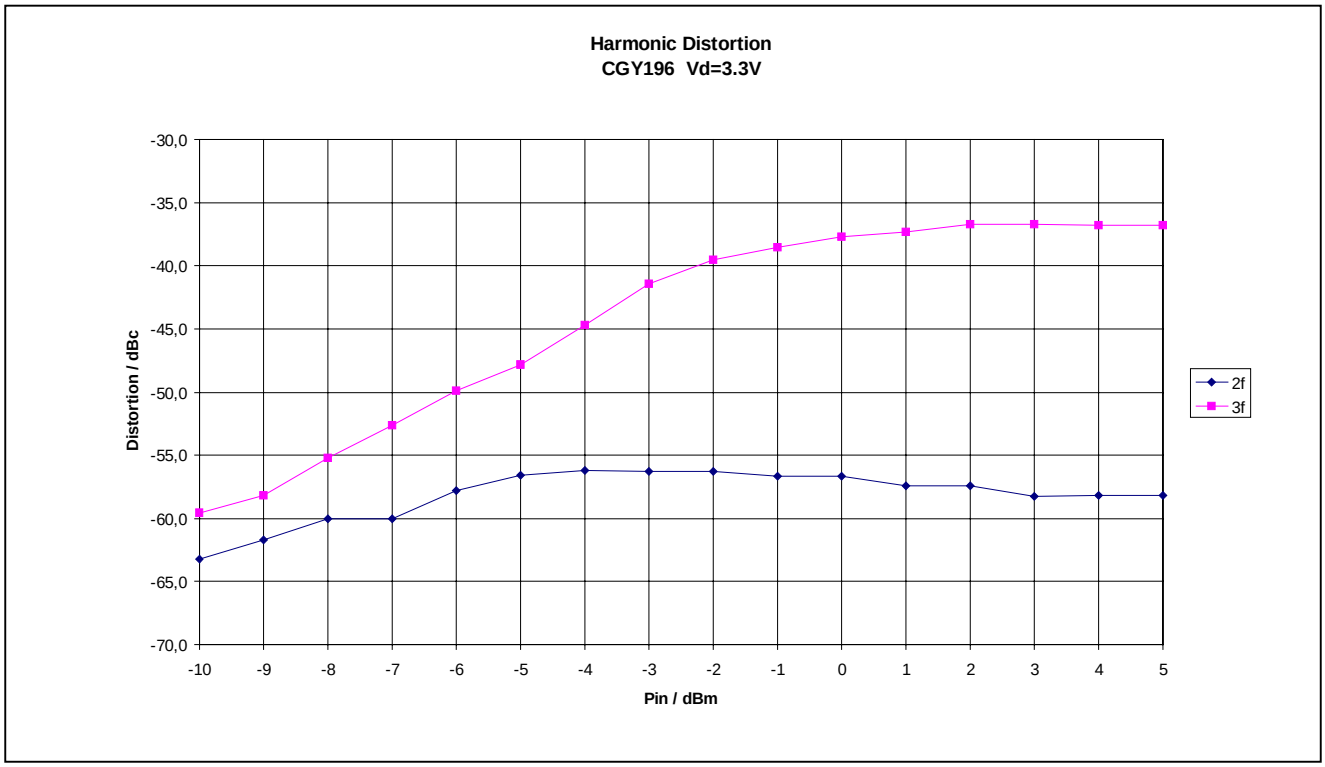
Electrical characteristics [3.0V DECT-Application: PCB-Layout see page 9]
S-Parameter [pulsed mode: T=417µs, duty cycle 12.5%, Pin=0dBm,Vd=3.3V]

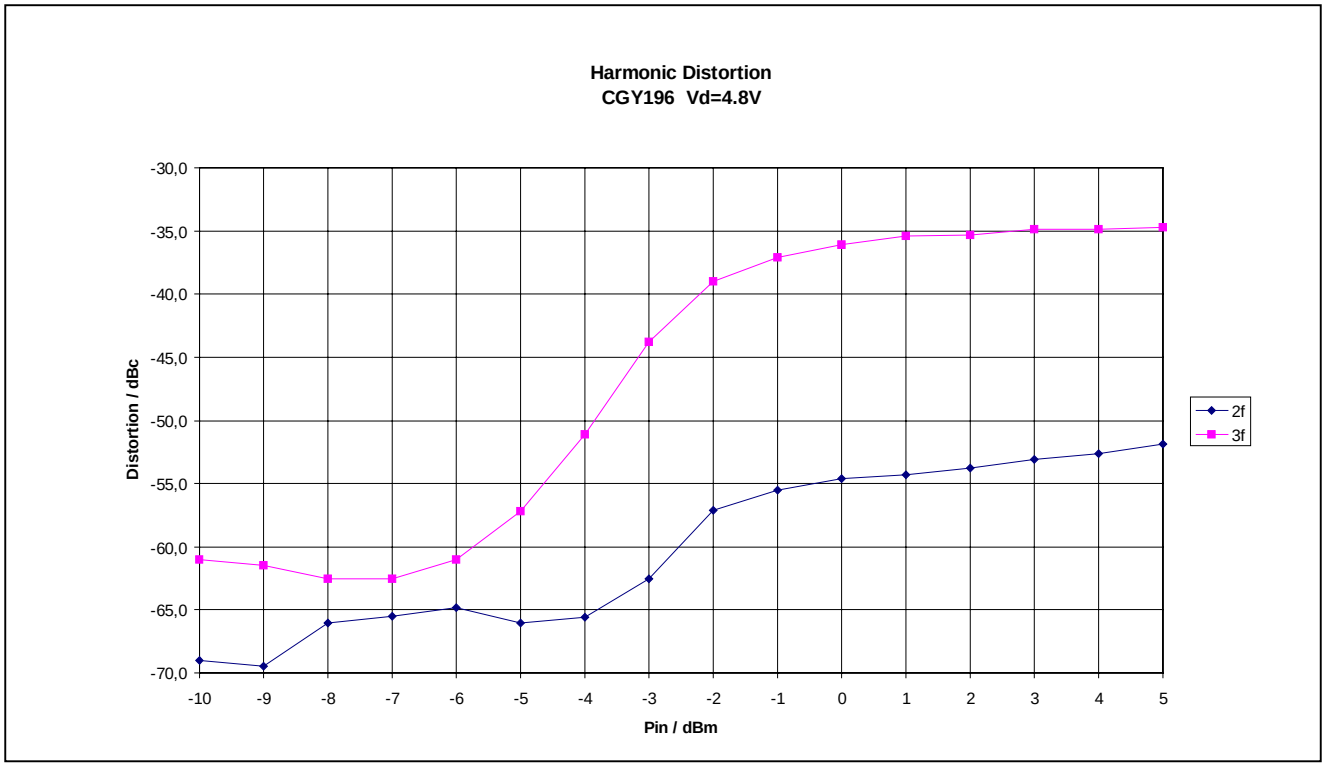


Pout,Id = f (Vd) | Pin=0dBm [pulsed mode: T=417µs, duty cycle 12.5%]

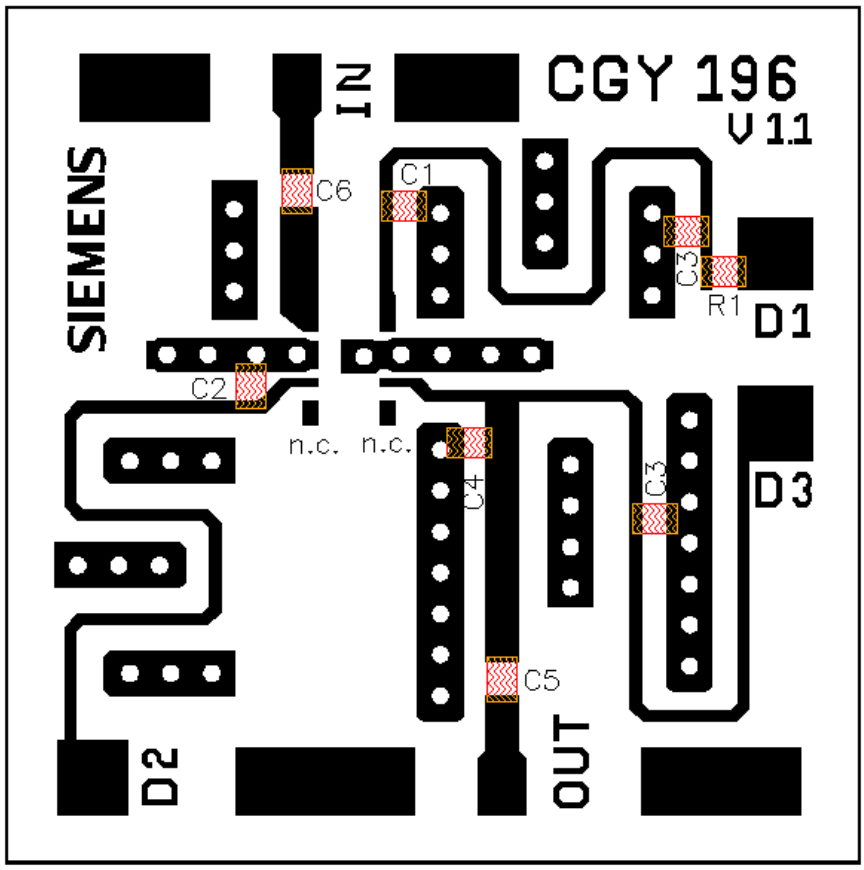


Electrical characteristics [3.0V DECT-Application: PCB-Layout see page 9]





Test Board Layout [3.0V DECT-Application f=1.89GHz]

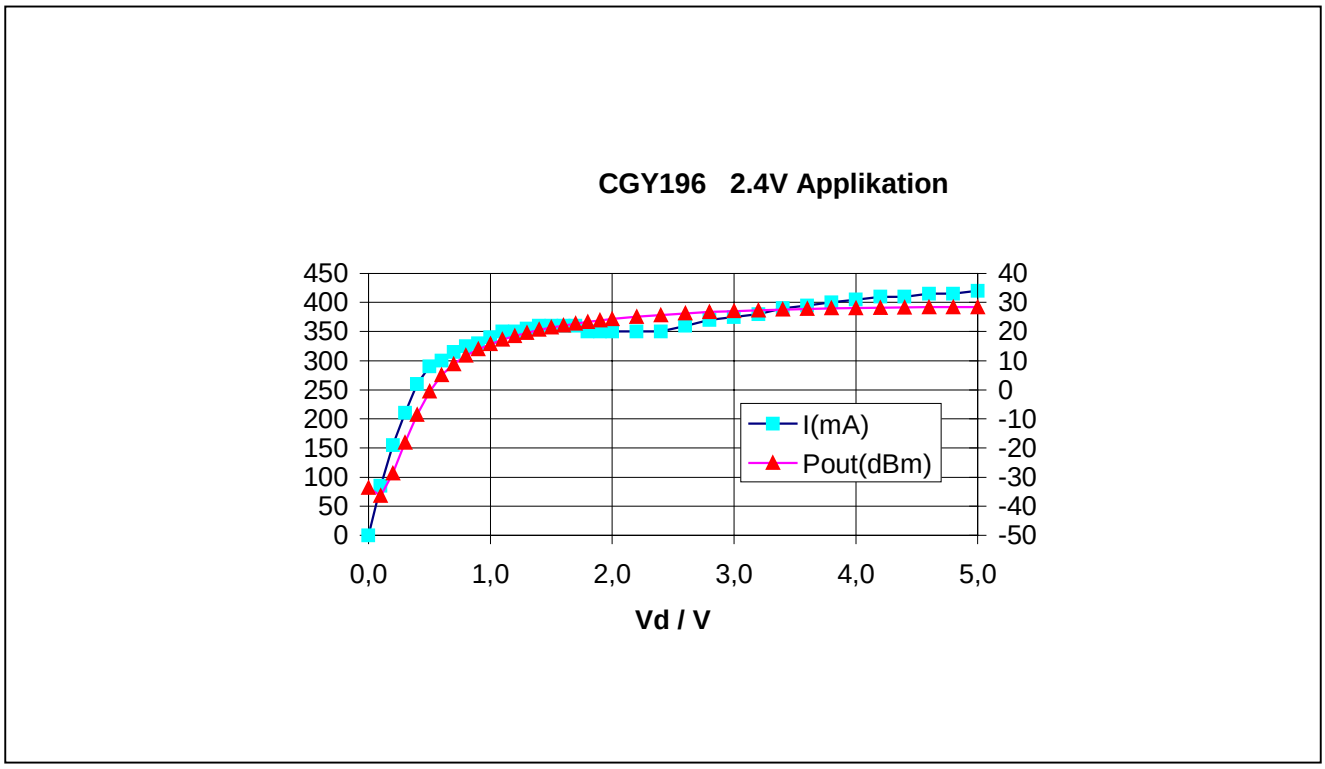


C1 = C2 = C3 = 100nF
C4 = 3.3 pF
C5 = C6 = 680 pF
R1 = 2.7 Ohm

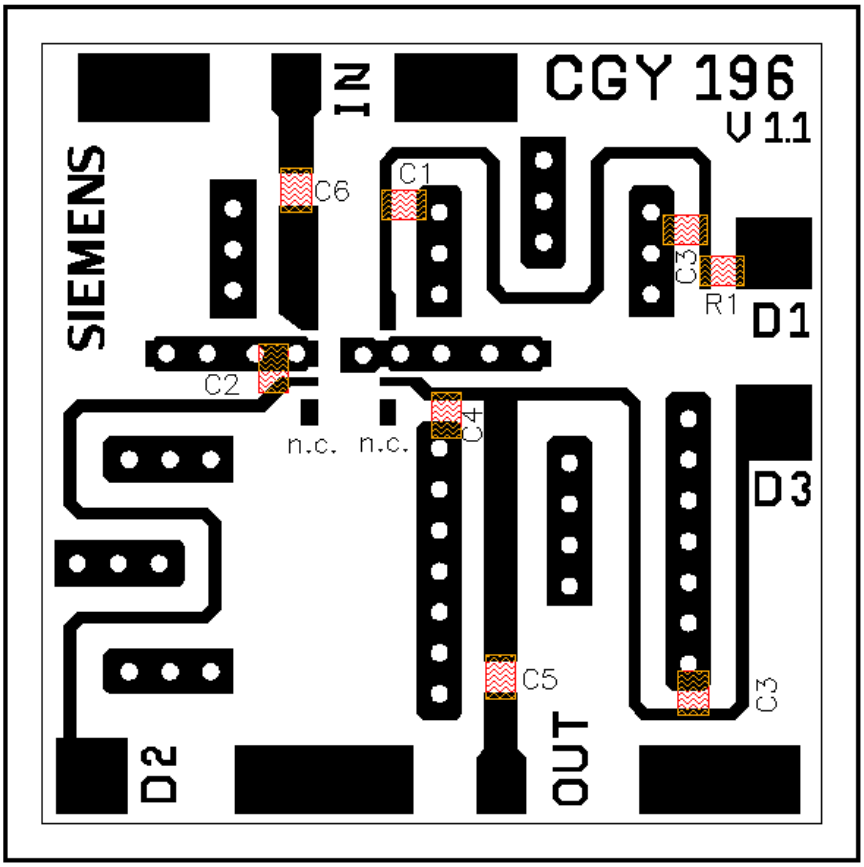
Electrical characteristics [2.4V DECT-Application: PCB-Layout see page 12]
(T_A = 25°C , f=1.89 GHz, Z_S=Z_L=50 Ohm, unless otherwise specified)

Characteristics	Symbol	min	typ	max	Unit
Supply current *VD=2.4V; Pin = +0 dBm*	I_{DD}	-	360	-	mA
Supply current *VD=2.4V; Pin = -10 dBm*	I_{DD}	-	450	-	mA
Output Power *VD=2.4V; P_{in} = 0 dBm*	P_O		25.7		dBm
Overall Power added Efficiency *VD=2.4V; P_{in} = +0 dBm*	*PAE*		44	-	%
Supply current *VD=2.2V; Pin = +0 dBm*	I_{DD}	-	350	-	mA
Supply current *VD=2.2V; Pin = -10 dBm*	I_{DD}	-	450	-	mA
Output Power *VD=2.2V; P_{in} = 0 dBm*	P_O		25.1		dBm
Overall Power added Efficiency *VD=2.2V; P_{in} = +0 dBm*	*PAE*		42	-	%
Supply current *VD=3.0V; Pin = +0 dBm*	I_{DD}	-	370	-	mA
Supply current *VD=3.0V; Pin = -10 dBm*	I_{DD}	-	450	-	mA
Output Power *VD=3.0V; P_{in} = 0 dBm*	P_O		27.0		dBm
Overall Power added Efficiency *VD=3.0V; P_{in} = +0 dBm*	*PAE*		44	-	%
Off Isolation *VD=0V; P_{in} = 0 dBm*	*-S21*		34		dB
Load mismatch *Pin=0dBm , VD≤3.6V , Z_S=50 Ohm, Load VSWR = 20:1 for all phase,*	-	No module damage for 10 sec.			-
Load mismatch *Pin=3dBm , VD≤5.0V , Z_S=50 Ohm, Load VSWR = 20:1 for all phase,*	-	No module damage for 10 sec.			-
Stability *Pin=0dBm, VD=3.6V, Z_S=50 Ohm, Load VSWR = 3:1 for all phase*	-	All spurious output more than 70 dB below desired signal level			-
Stability *Pin=3dBm , VD=5.0V , Z_S=50 Ohm, Load VSWR = 3:1 for all phase,*	-	All spurious output more than 70 dB below desired signal level			-

Pout,Id = f (Vd) | Pin=0dBm [pulsed mode: T=417µs, duty cycle 12.5%]



Test Board Layout [2.4V DECT-Application f=1.89GHz]



C1 = C2 = C3 = 100nF
C4 = 3.3 pF
C5 = C6 = 680 pF
R1 = 2.7 Ohm

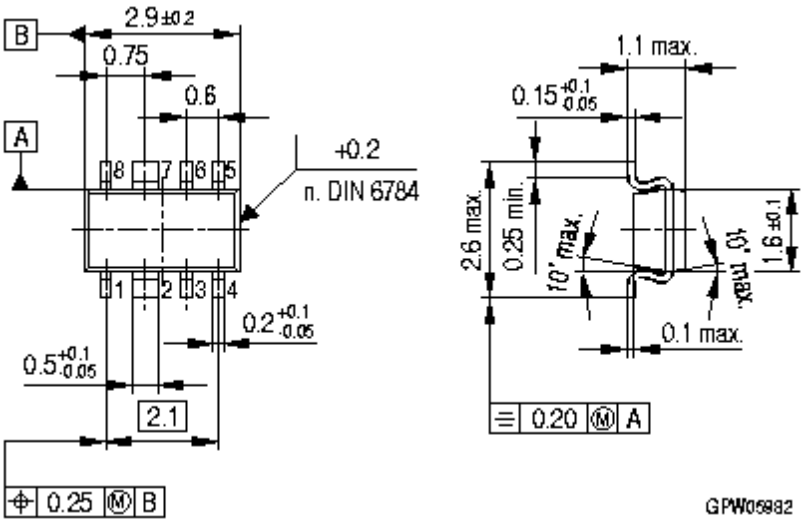
SIEMENS	High Frequency Semiconductors		
Type	*Package*	*File*	*Date*
CGY196 GaAs MMIC	SCT598	D:\Projekte\AKTUELL\EH_DB\lieferung_pdf\Lieferung\word\cgy19	26.02.1998

Key-word

Notes on Processing

Preliminary soldering recommendation

• **Foot Print**	drawing C63060-A2123-A001-01-0027	
• **Soldering**	wave soldering: unsuitable reflow soldering: suitable (IR or VPR)	
soldering profile:		
ramp-up preheating	temperature gradient: time at 100 - 150 °C:	max. + 2 K/sec min. 90 sec.
ramp-up peak exposure to molten solder typ. solder temperature peak temperature ramp-down	temperature gradient above 183°C typ. 215-245°C max. peak 260°C temperature gradient:	max. + 6 K/sec max. 150 sec max. 30 sec. max. 10 sec. min. - 6°C/sec
	(see also soldering standard profile of databook 'package information')	
comments	slow ramp-up, long preheating phase and low max. temperature recommended	
• **Solder paste thickness**	150 - 200 µm	
• **Control of soldering** (voids)	- visual inspection - cross sectioning - measurement of case temperature / thermal resistance case to ambient	
• **Jedec A-112A**	level 1	storage floor life at 30°C/90% unlimited
• **IPC-9501 (IPC-4202)**	level 111	storage floor life at 30°C/60% unlimited IR/Convection; max. 245°C; < 6K/sec.



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