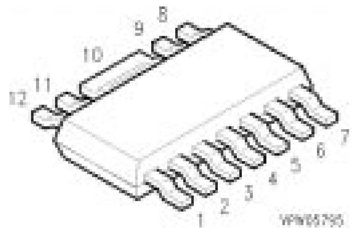
Preliminary Datasheet

* Power amplifier for PCN/PCS applications
* Fully integrated 2 stage amplifier
* Operating voltage range: 2.7 to 6 V
* Overall power added efficiency 35 %
* Input matched to 50 Ω, simple output match



ESD: **E**lectro**s**tatic **d**ischarge sensitive device, observe handling precautions!

Type	Marking	Ordering code (8-mm taped)	Package 1)
CGY 181	**CGY 181**	**Q68000-A8883**	**MW 12**

Maximum ratings

Characteristics	Symbol	max. Value	Unit
Positive supply voltage	V_D	9	V
Negative supply voltage [2])	V_G	-8	V
Supply current	I_D	2	A
Channel temperature	T_{Ch}	150	°C
Storage temperature	T_{stg}	-55...+150	°C
RF input power	P_{in}	25	dBm
Total power dissipation *(Ts ≤ 81 °C)* *Ts: Temperature at soldering point*	P_{tot}	5	W

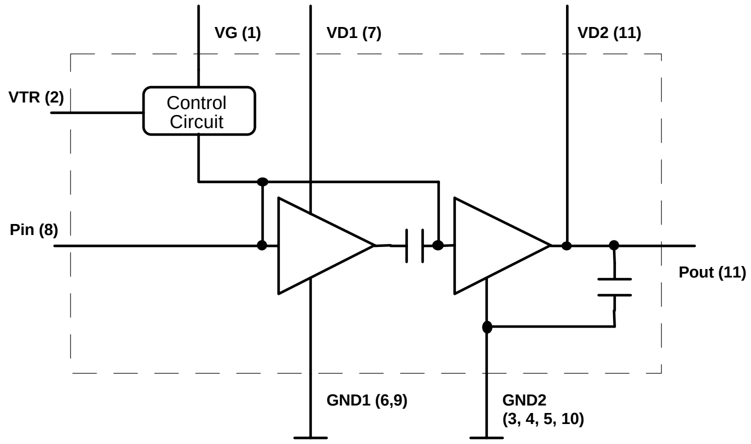
Thermal Resistance

Channel-soldering point	R_{thChS}	≤14	K/W

1) Plastic body identical to SOT 223, dimensions see chapter Package Outlines

2) V_G = -8V only in combination with V_{TR} = 0V; V_G = -6V while $V_{TR} \neq$ 0V

Functional block diagramm:



Short description of CGY181 operation:

A negative voltage between -4V to -6V (stabilization not necessary) has to be connected to the VG-pin, a positive supply voltage has to be applied to the VD-pins.
The VTR-pin has to switched to 0V (GND) during transmit operation. The MMIC CGY181 is self-biased, the operating current is adjusted by the internal control circuit.
In receive mode the VTR-pin is not connected (shut off mode).

Pin #		Configuration
1	**VG**	Negative voltage at control circuit (-4V...-8V)
2	**VTR**	Control voltage for transmit mode (0V) or receive mode (open)
3,4,5,10	**GND 2**	RF and DC ground of the 2nd stage
6,9	**GND 1**	RF and DC ground of the 1st stage
7	**VD1**	Positive drain voltage of the 1st stage
8	**RFin**	RF input power
11	**VD2,RFout**	Positive drain voltage of the 2nd stage, RF output power
12	**-**	not connected

DC characteristics

Characteristics	Symbol	Conditions	min	typ	max	Unit
Drain current stage 1	*IDSS1*	VD=3V, VG=0V, VTR n.c.	0.6	0.9	1.2	A
stage 2	*IDSS2*		2.4	3.5	4.8	A
Drain current with active current control	*ID*	VD=3V, VG=-4V, VTR=0V		1.0		A
Transconductance	*gfs1*	VD=3V, ID=350mA	0.28	0.32	-	S
(stage 1 and 2)	*gfs2*	VD=3V, ID=700mA	1.1	1.3	-	S
Pinch off voltage	*Vp*	VD=3V, ID<500µA (all stages)	-3.8	-2.8	-1.8	V

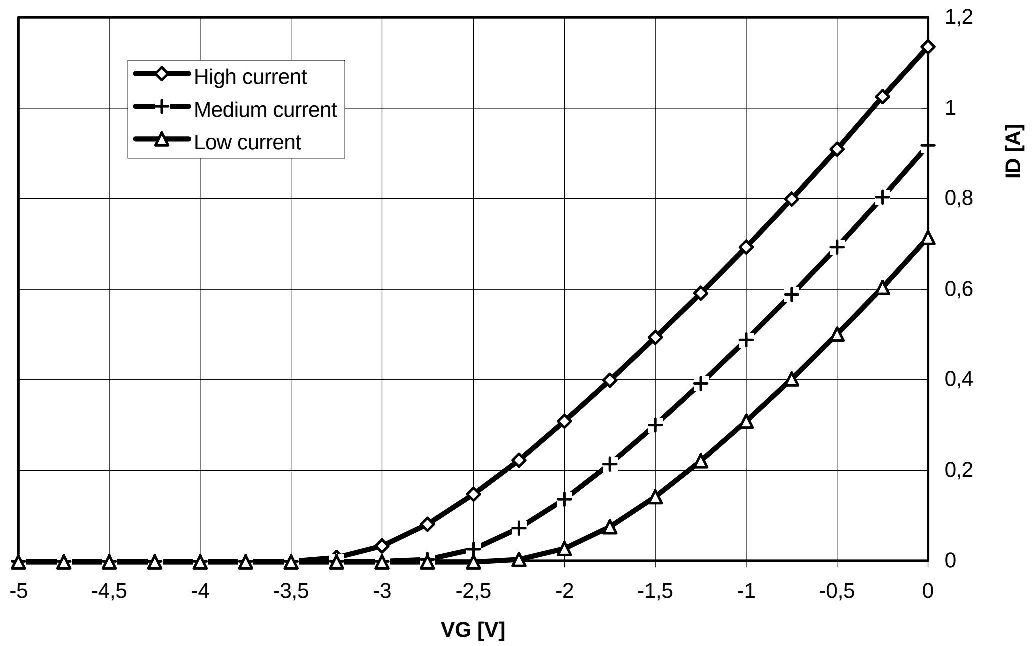
Electrical characteristics

(T_A = 25°C , f=1.75 GHz, Z_S=Z_L=50 Ohm, VD=3.6V, VG =-4V, VTR pin connected to ground, unless otherwise specified)

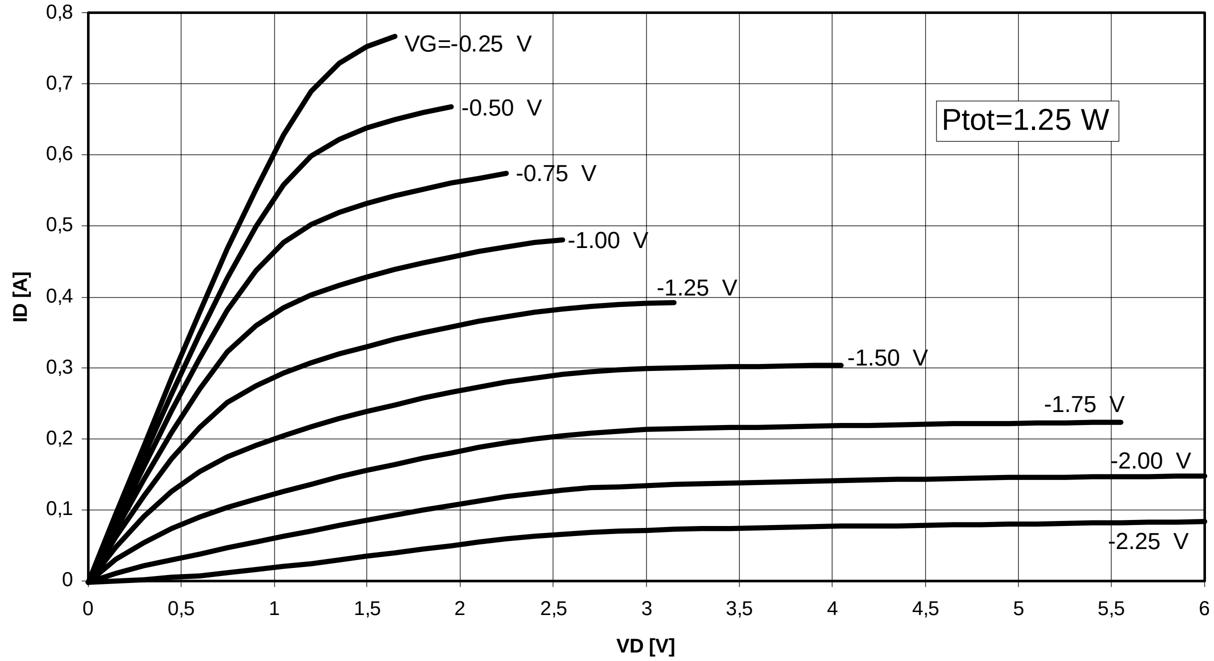
Characteristics	**Symbol**	**min**	**typ**	**max**	**Unit**
Supply current Pin= 0 dBm	I_{DD}	-	1.2	-	A
Negative supply current *(normal operation)*	I_G	-	2	3	mA
Shut-off current *VTR n.c.*	I_D	-	400	-	µA
Negative supply current *(shut off mode, VTR pin n.c.)*	I_G	-	10	-	µA
Small signal gain P_{in} = -5dBm	*G*	-	20.5	-	dB
Power Gain V_D=3.6V, Pin = 16 dBm	*G*	14.5	15.5	-	dB
Power Gain V_D=5V, Pin = 16 dBm	*G*	17.5	18.5	-	dB
Output Power V_D=3.6V, Pin = 16 dBm	P_0	30.5	31.5	-	dBm
Output Power V_D=5V , Pin = 16 dBm	P_0	33.5	34.5	-	dBm
Overall Power Added Efficiency V_D=3.6V, P_{in} = 16 dBm	η	-	37	-	%
Overall Power Added Efficiency V_D=5V, P_{in} = 16 dBm	η	-	35	-	%
Harmonics (P_{in} =16dBm) $2f_0$ V_D=3.6V (P_{out}=31.85dBm) $3f_0$		- -	-44.8 -70	- -	dBc
Harmonics (P_{in} =16dBm) $2f_0$ V_D=5V (P_{out}=31.85dBm) $3f_0$			-45.1 -75		dBc
Input VSWR V_D=3.6V			1.9:1		
Third order intercept point f_1=1.7500GHz; f_2=1.7502GHz; V_D = 3.6V	IP_3		41		dBm
Third order intercept point f_1=1.7500GHz; f_2=1.7502GHz; V_D = 5V	IP_3		44		dBm

All RF-measurements were done in a pulsed mode with a duty cycle of 10% (t_{on}=0.33ms)!

DC-ID(VG) characteristics - typical values of stage 1, VD=3V

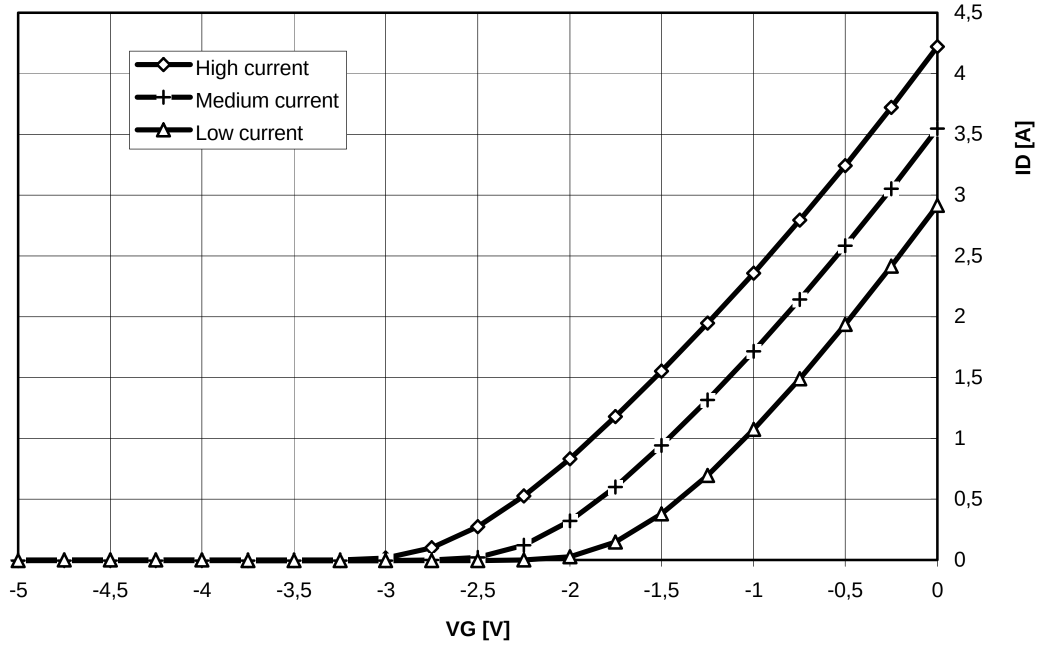


DC-Output characteristics - typical values of stage 1

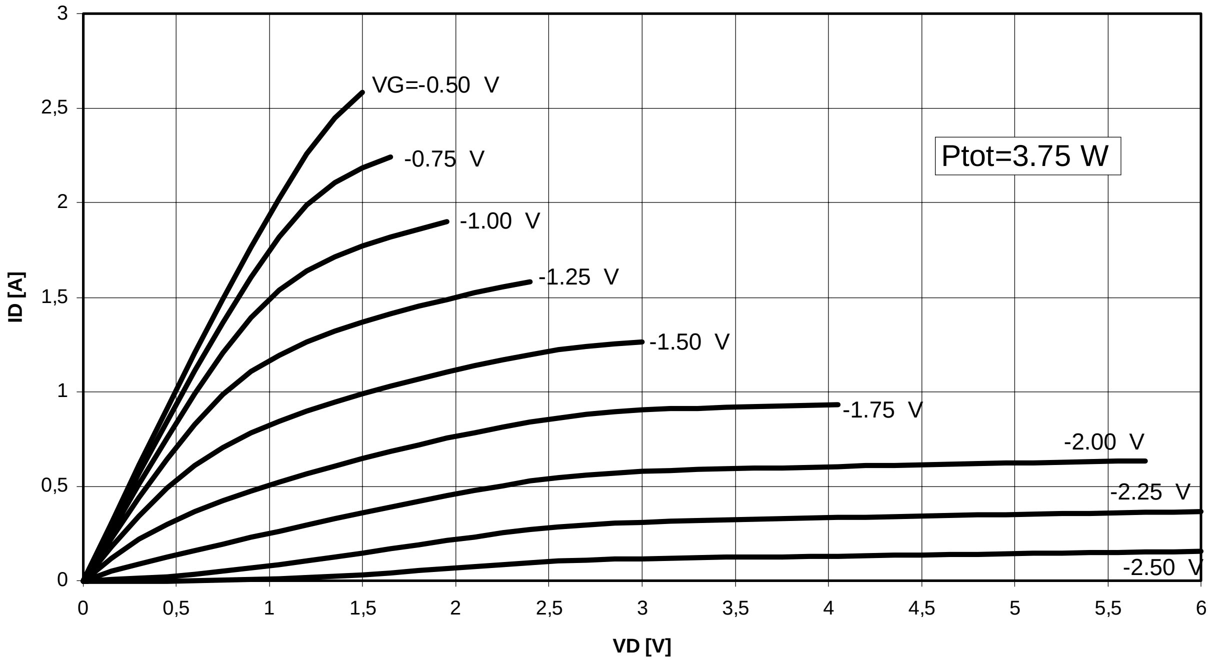


Pin 2 (V_{TR}) has to be open during measuring DC-characteristics!

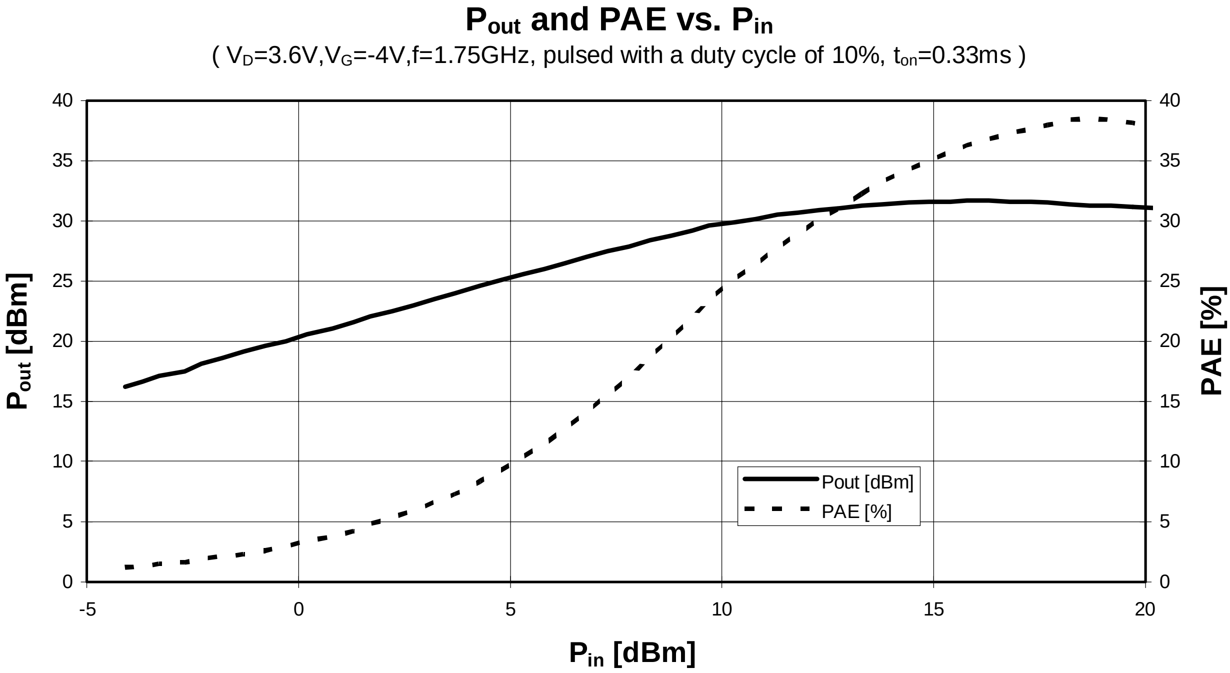
DC-ID(VG) characteristics - typical values of stage 2, VD=3V

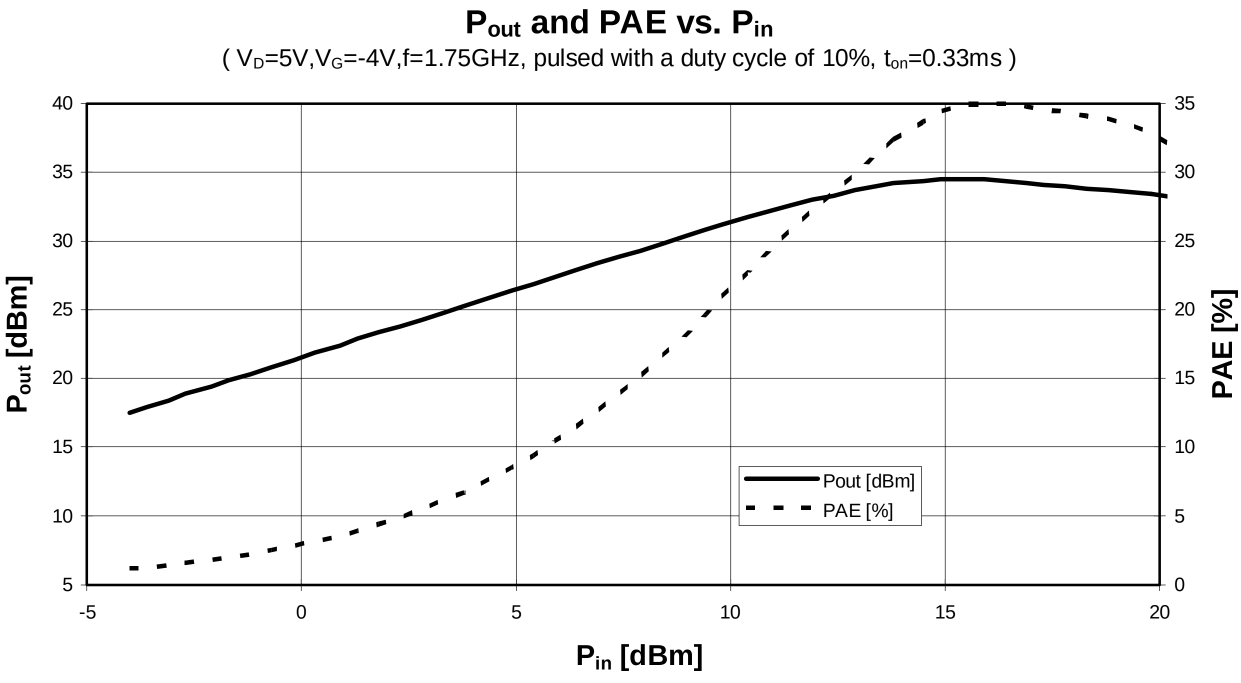


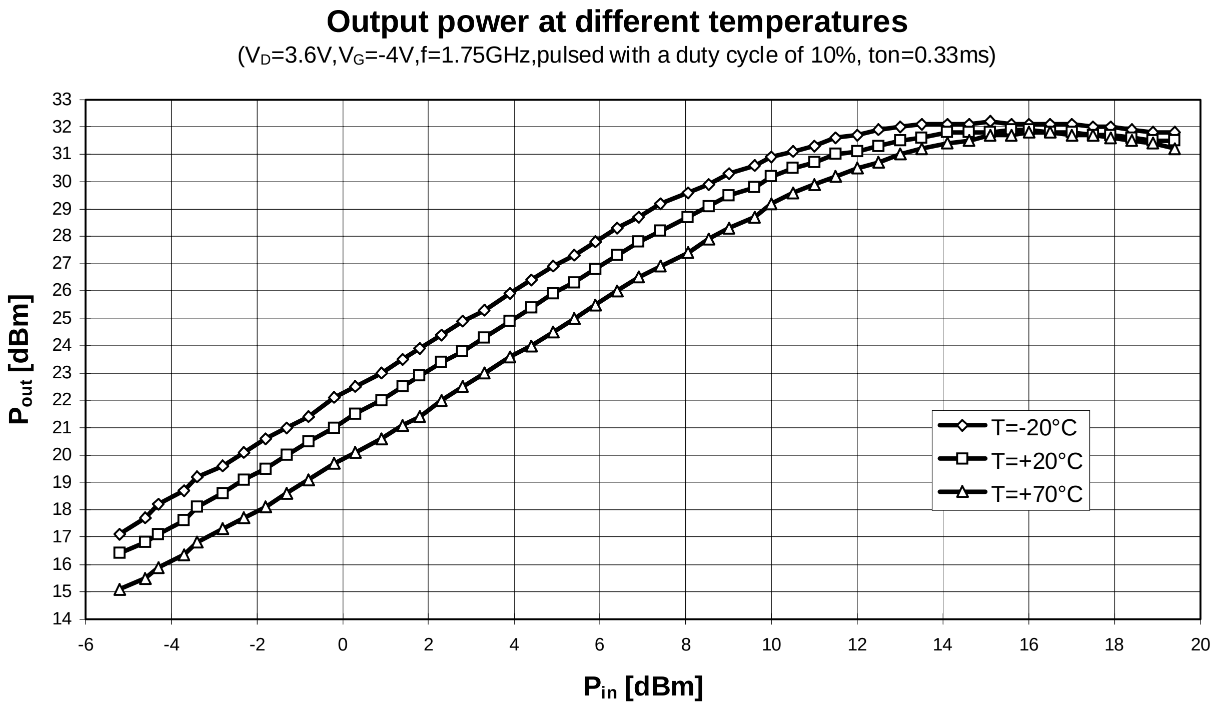
DC-Output characteristics - typical values of stage 2



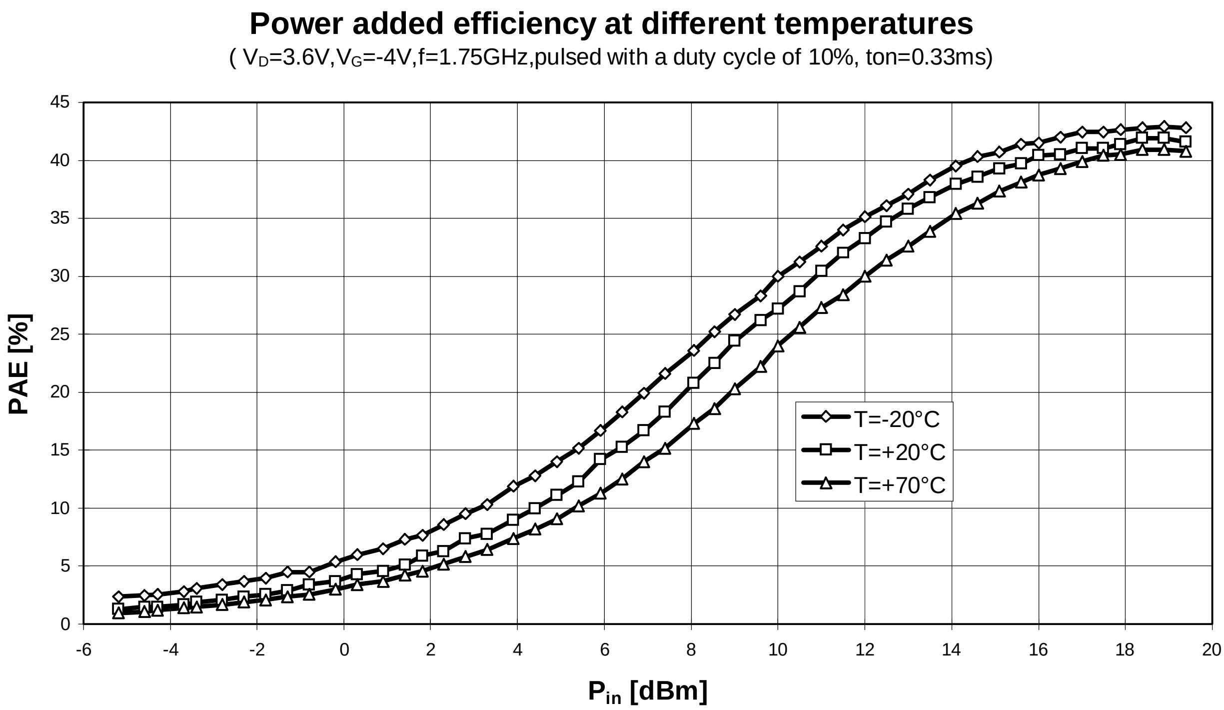
Pin 2 (V_{TR}) has to be open during measuring DC-characteristics!


Pout and PAE vs. Pin
(VD=3.6V,VG=-4V,f=1.75GHz, pulsed with a duty cycle of 10%, ton=0.33ms)
Pout [dBm]
PAE [%]
Pin [dBm]
Pout [dBm]
PAE [%]
40
35
30
25
20
15
10
5
0
-5
0
5
10
15
20


Pout and PAE vs. Pin
(VD=5V,VG=-4V,f=1.75GHz, pulsed with a duty cycle of 10%, ton=0.33ms)
Pout [dBm]
PAE [%]
Pin [dBm]
Pout [dBm]
PAE [%]
40
35
30
25
20
15
10
5
0
-5
0
5
10
15
20



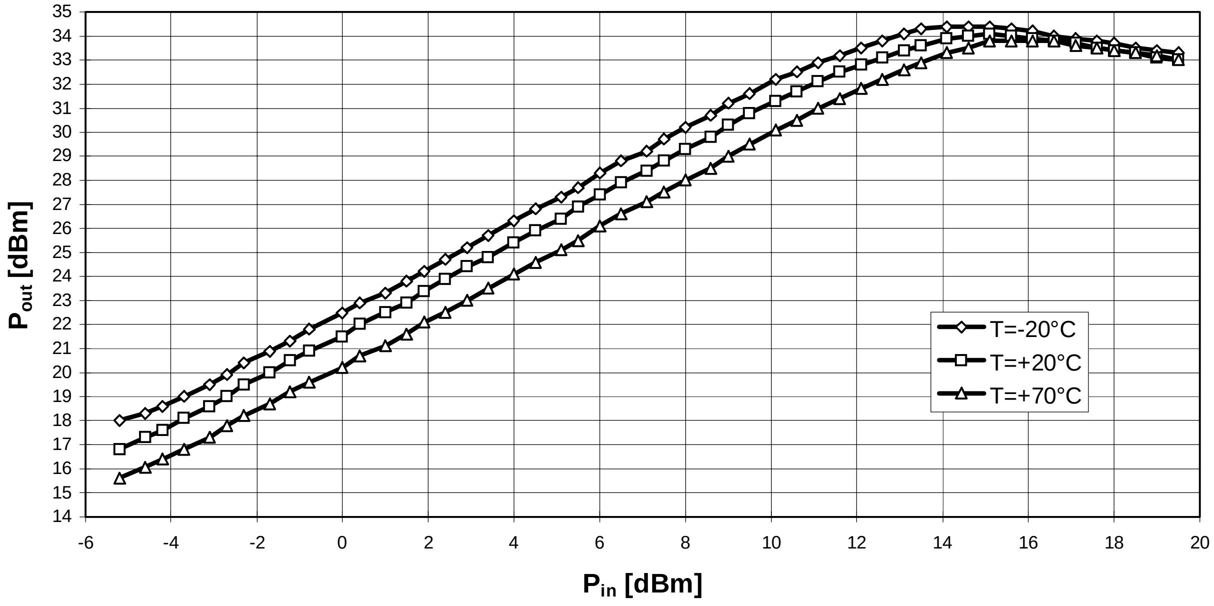
Output power at different temperatures
(V_D=3.6V,V_G=-4V,f=1.75GHz,pulsed with a duty cycle of 10%, ton=0.33ms)
P_{out} [dBm]
P_{in} [dBm]
T=-20°C
T=+20°C
T=+70°C



Power added efficiency at different temperatures
(V_D=3.6V,V_G=-4V,f=1.75GHz,pulsed with a duty cycle of 10%, ton=0.33ms)
PAE [%]
P_{in} [dBm]
T=-20°C
T=+20°C
T=+70°C

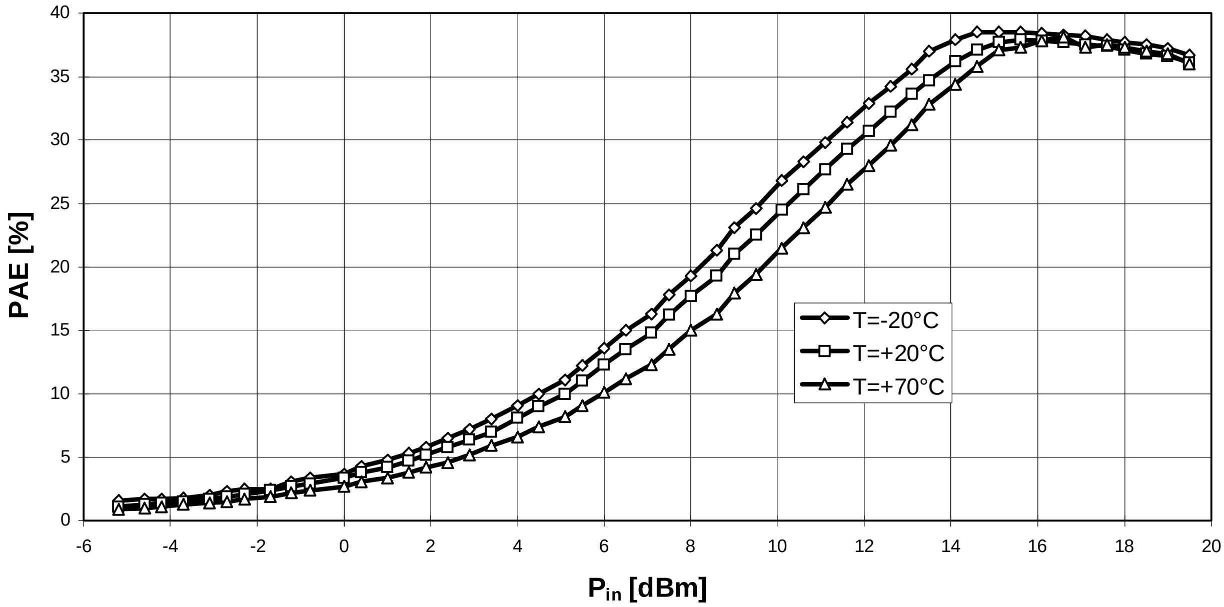
Output power at different temperatures

(V_D=5V,V_G=-4V,f=1.75GHz,pulsed with a duty cycle of 10%, ton=0.33ms)



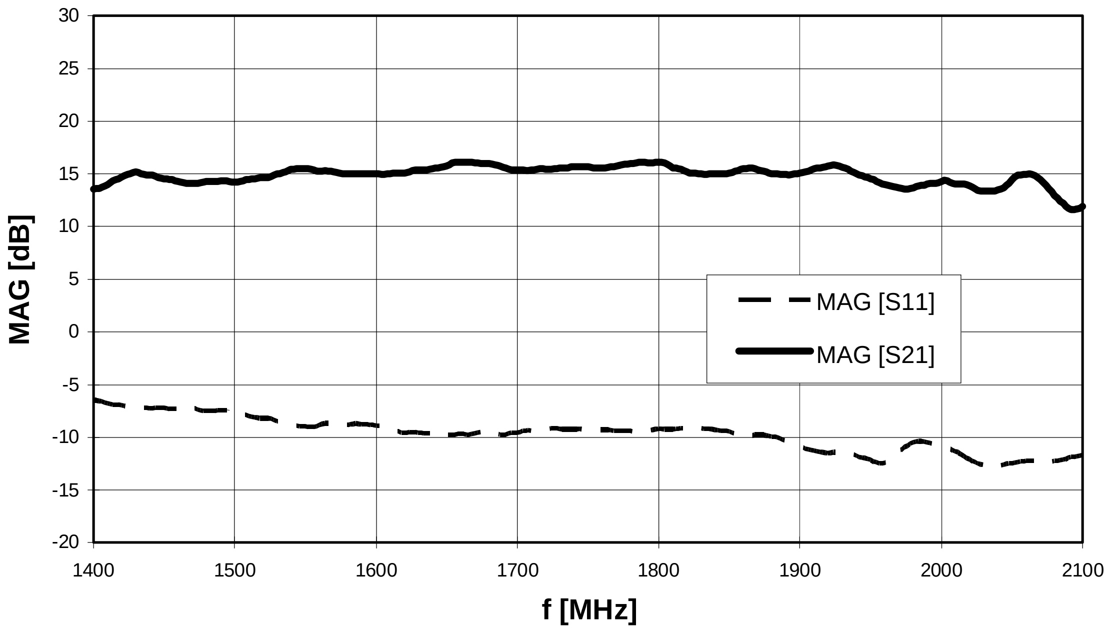
Power added efficiency at different temperatures

(V_D=5V,V_G=-4V,f=1.75GHz,pulsed with a duty cycle of 10%, ton=0.33ms)



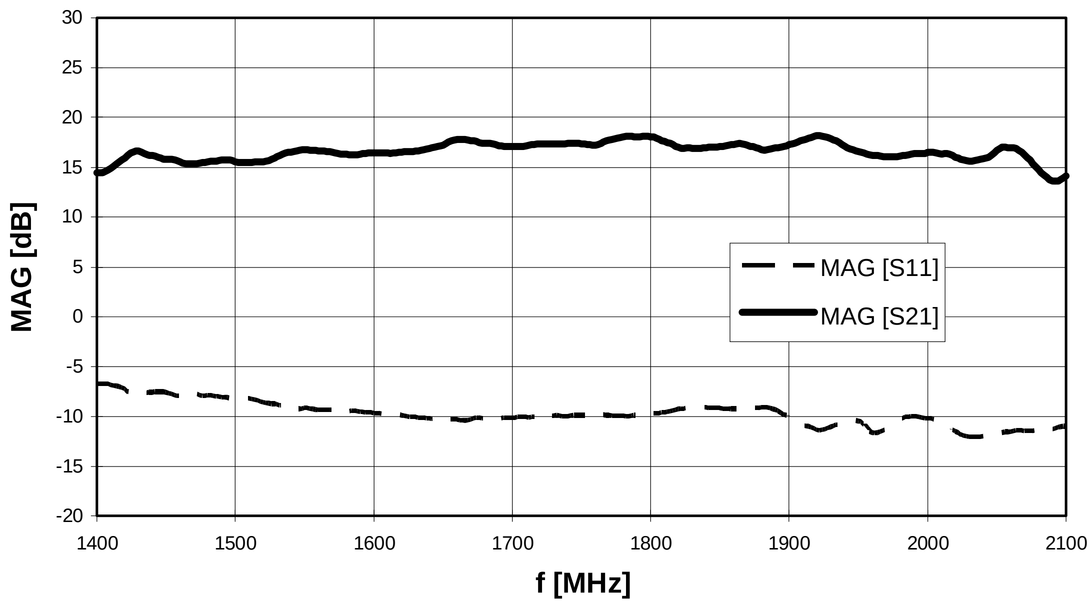
Measured S-parameter at V_D=3.6V and Pin=16dBm

(V_G=-4V, VTR connected to ground, pulsed with a duty cycle of 10%, ton=0.33ms)



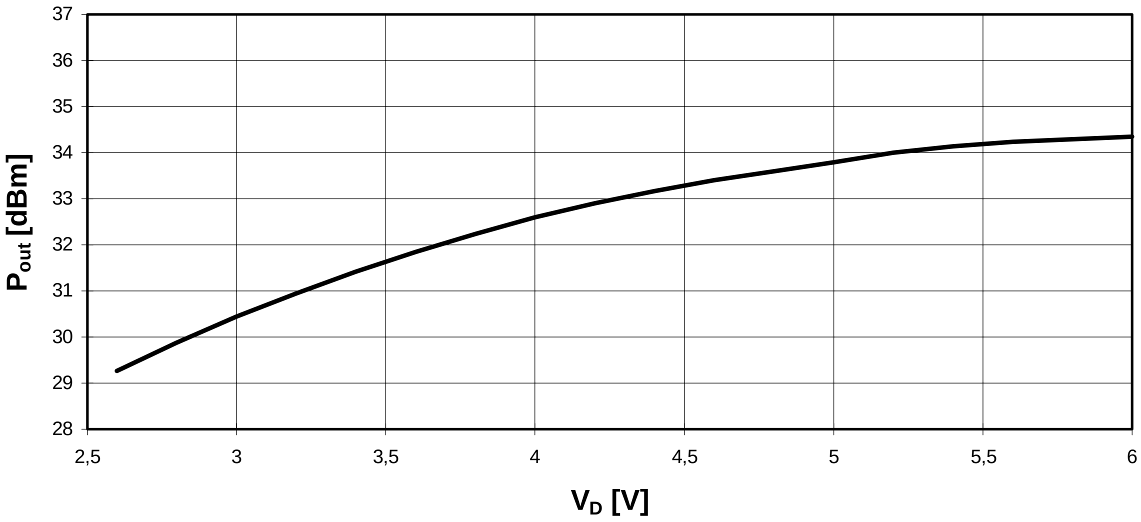
Measured S-parameter at V_D=5V and Pin=16dBm

(V_G=-4V, VTR connected to ground, pulsed with a duty cycle of 10%, ton=0.33ms)



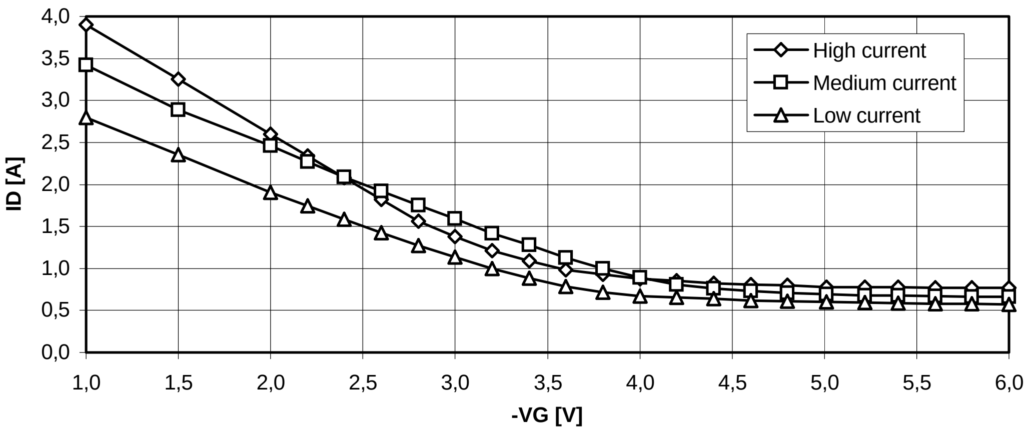
P_{out} vs. V_D

(V_G=-4V,f=1.75GHz, P_{in}=16dBm,pulsed with a duty cycle of 10%, ton=0.33ms)



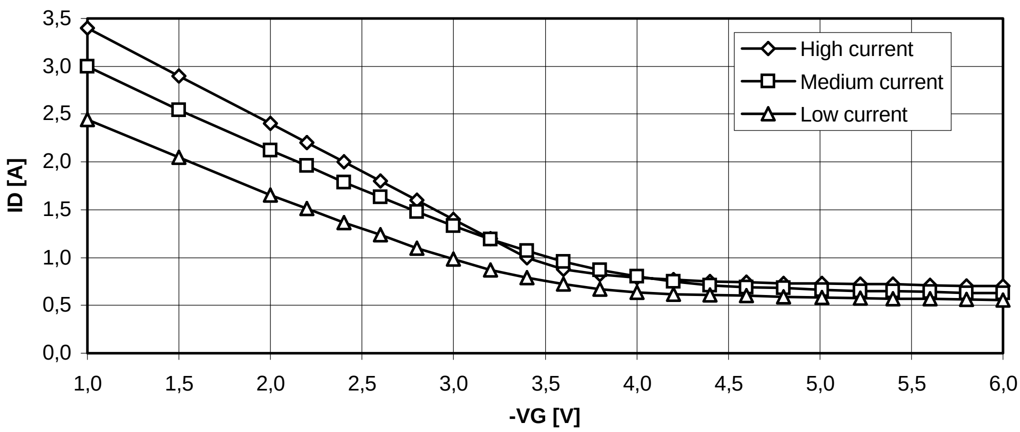
Performance of internal bias control circuit @VD=3V

(VTR=0V, pulsed with a duty cycle of 10%, ton=0.33ms)

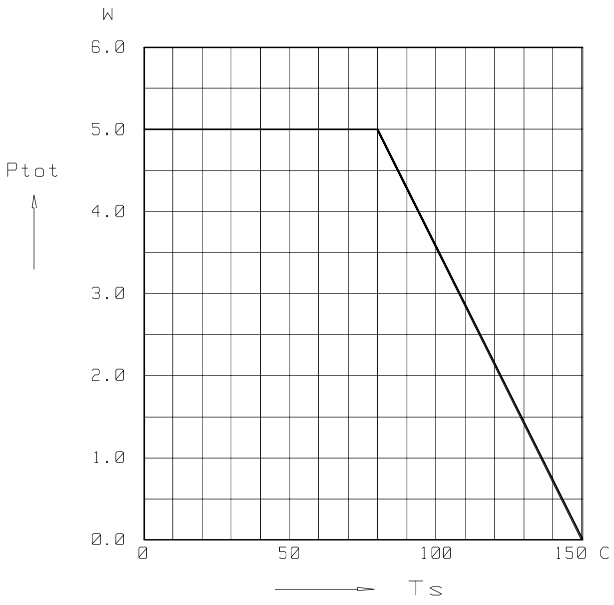


Performance of internal bias control circuit @VD=5V

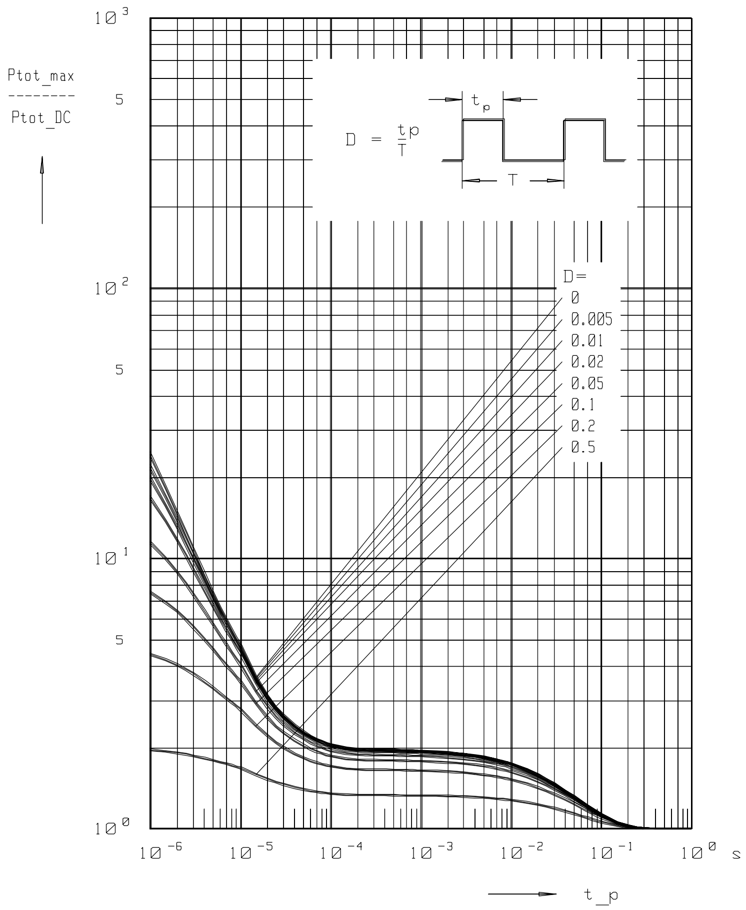
(VTR=0V, pulsed with a duty cycle of 10%, ton=0.33ms)



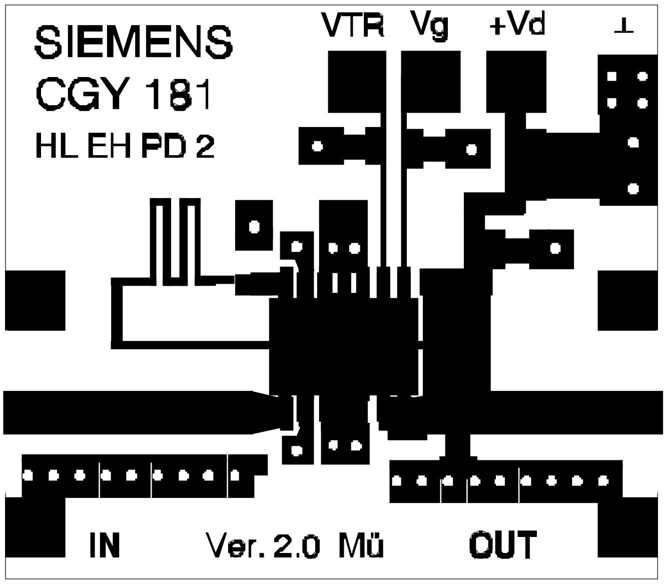
Total Power Dissipation Ptot=f(T_S)



Permissible pulse load P_{tot_max}/P_{tot_DC} = f(t_p)



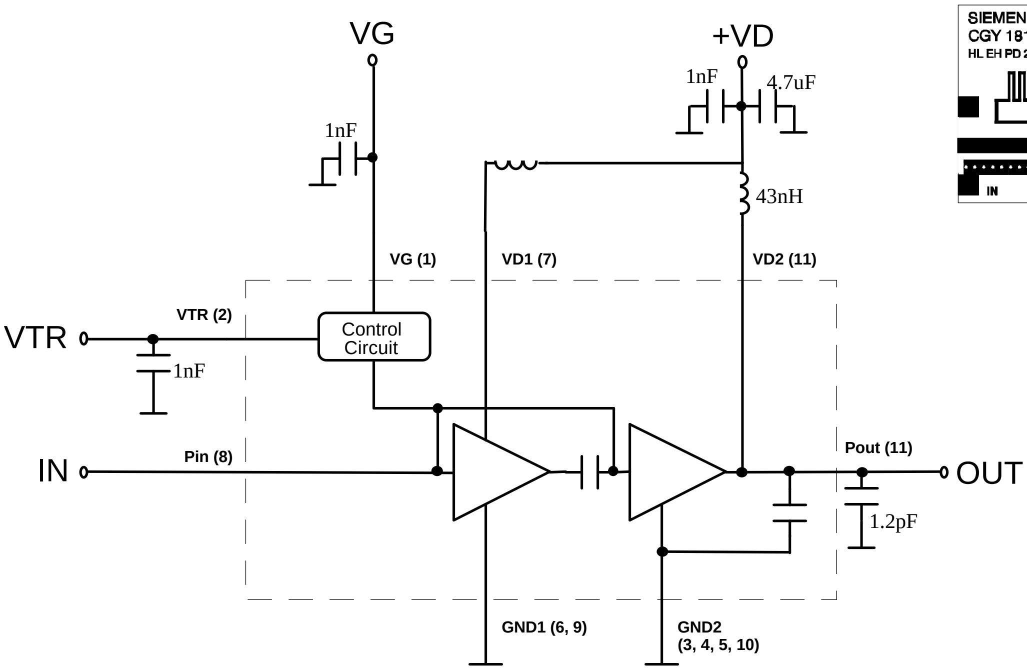
CGY181 application board:



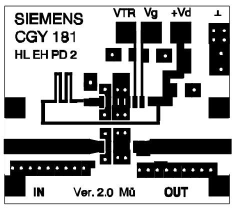
Part Type	Description:
CGY181	**Siemens GaAs-MMIC**
1nF	Capacitor SMD 0805
1nF	Capacitor SMD 0805
1nF	Capacitor SMD 0805
1p2	Capacitor SMD 0805
4µ7	Capacitor SMD Tantal
43nH	Coilcraft SMD Spring Inductor B10T (distributed by Ginsbury Electronic GmbH Am Moosfeld 85, D-81829 München Tel.: 089/45170-223)

Layout size is 30mm x 26mm.

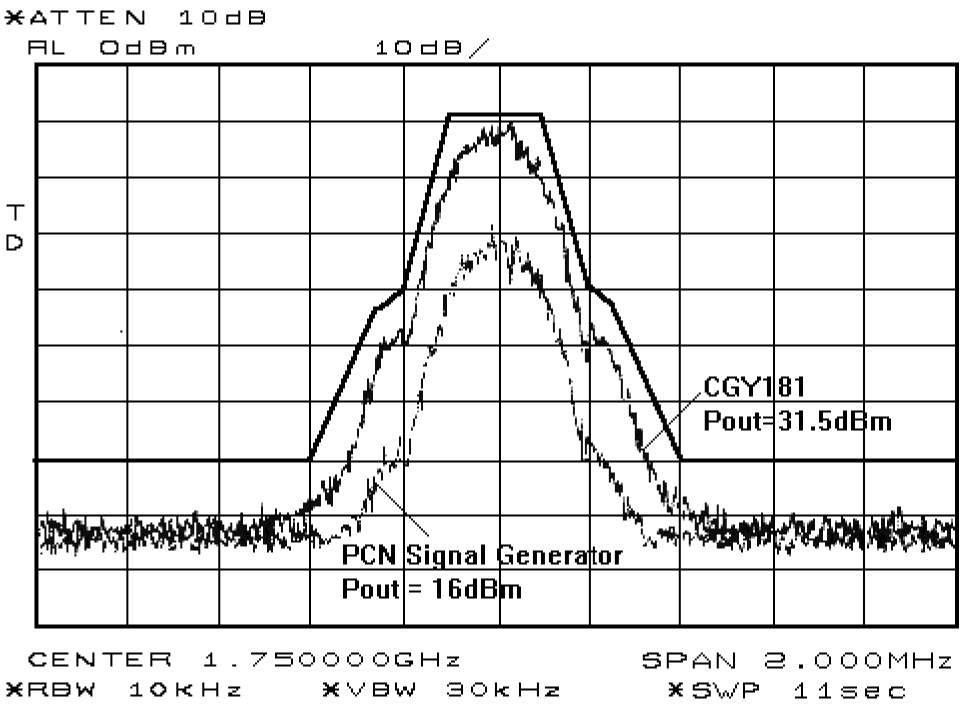
Principal circuit:



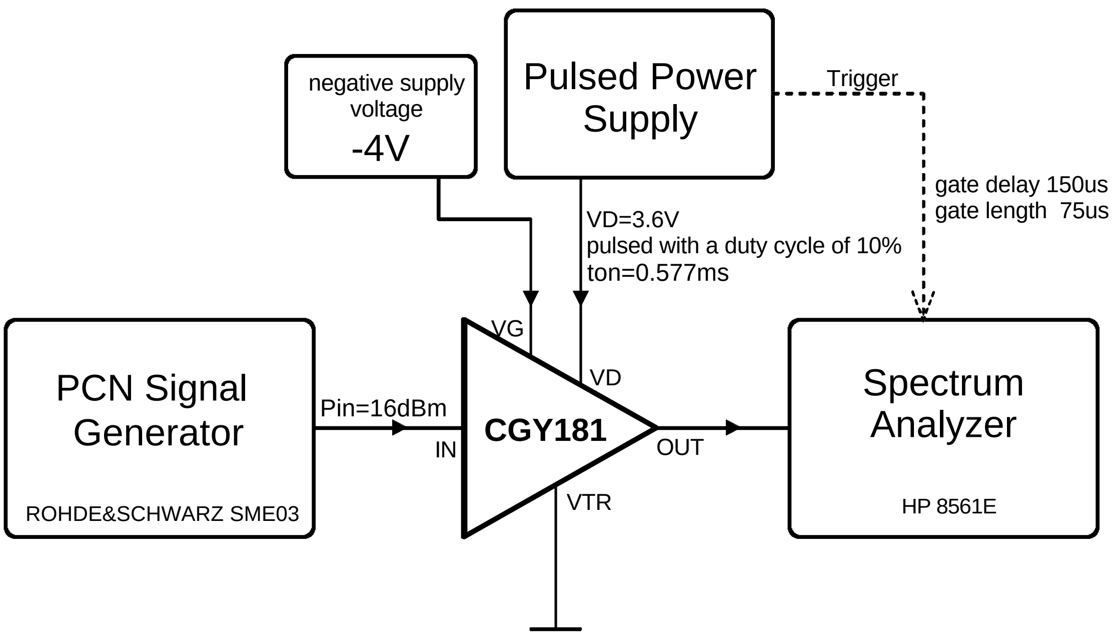
Original Size:



Emissions due to GMSK modulation:



Measurement was done with the following equipment:



APPLICATION - HINTS

1. CW - capability of the CGY181

Proving the possibility of CW - operations there must be known the total power dissipation of the device. This value can be found as a function of temperature in the datasheet (page 12). The CGY181 has a maximum total power dissipation of P_{tot} = 5 W.
As an example we take the operating point with a drain voltage V_D = 3.6 V and a typical drain current of I_D=1.2A. So the maximum DC - power can be calculated to:

$$P_{DC} = V_D \cdot I_D = 4.32W.$$

This value is smaller than 5W and CW - operation is possible.

By decoupling RF power out of the CGY181 the power dissipation of the device can be further reduced. Assuming a power added efficiency PAE of 35 % the total power dissipation P_{tot} can be calculated using the following formula:

$$P_{tot} = P_{DC}(1 - PAE) = 4.32W(1 - 0.35) = 2.808W$$

2. Operation without using the internal current control

If you don' t want to use the internal current control, it is recommended to connect the negative gate voltage at pin 2 (V_{TR}) instead of pin 1 (V_G). In that case V_G is not connected.

3. Biasing and use considerations

Biasing should be timed in such a way the that gate voltage (V_G) is always applied before the drain voltages (V_D), and when returning to the standby mode, the drain voltages have be removed before the gate voltage.