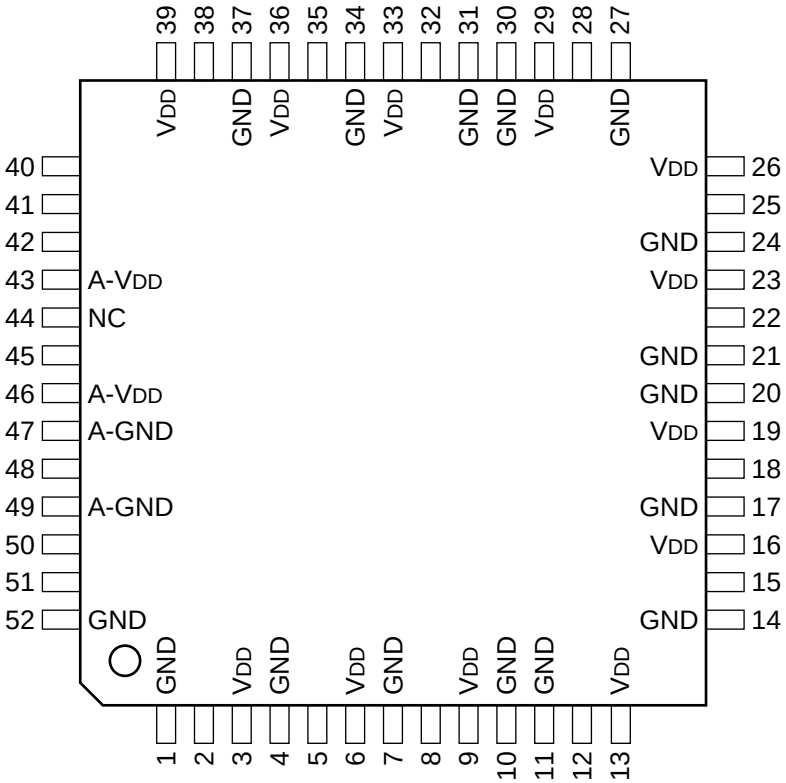
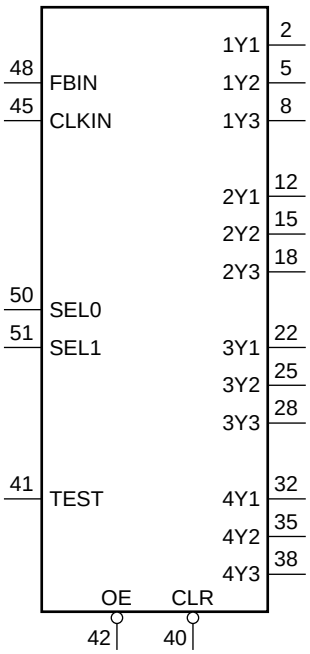
C-MOS PHASE-LOCK-LOOP CLOCK DRIVER

—TOP VIEW—





PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL	PIN NO.	I/O	SIGNAL
1	—	GND	14	—	GND	27	—	GND	40	I	$\overline{CLR}$
2	O	1Y1	15	O	2Y2	28	O	3Y3	41	I	TEST
3	—	VDD	16	—	VDD	29	—	VDD	42	I	$\overline{OE}$
4	—	GND	17	—	GND	30	—	GND	43	—	A-VDD
5	O	1Y2	18	O	2Y3	31	—	GND	44	—	NC
6	—	VDD	19	—	VDD	32	O	4Y1	45	I	CLKIN
7	—	GND	20	—	GND	33	—	VDD	46	—	A-VDD
8	O	1Y3	21	—	GND	34	—	GND	47	—	A-GND
9	—	VDD	22	O	3Y1	35	O	4Y2	48	I	FBIN
10	—	GND	23	—	VDD	36	—	VDD	49	—	A-GND
11	—	GND	24	—	GND	37	—	GND	50	I	SEL0
12	O	2Y1	25	O	3Y2	38	O	4Y3	51	I	SEL1
13	—	VDD	26	—	VDD	39	—	VDD	52	—	GND

INPUT		**OUTPUT**	
CLKIN	: CLOCK	1Y1 - 1Y3	: OUTPUT PORTS
$\overline{\text{CLR}}$	: CLEAR	2Y1 - 2Y3	: OUTPUT PORTS
FBIN	: FEEDBACK	3Y1 - 3Y3	: OUTPUT PORTS
$\overline{\text{OE}}$	: OUTPUT ENABLE	4Y1 - 4Y3	: OUTPUT PORTS
SEL0, SEL1	: OUTPUT SELECT		
TEST	: TEST