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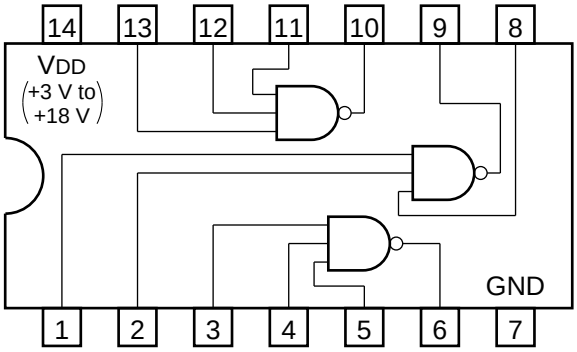
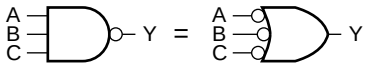
CD4023AE/BE
IL00

C-MOS 3-INPUT NAND GATE

— TOP VIEW —





$Y = \overline{A \bullet B \bullet C} = \overline{A} + \overline{B} + \overline{C}$

A	B	C	Y
X	X	0	1
X	0	X	1
0	X	X	1
1	1	1	0

0 ; LOW LEVEL
1 ; HIGH LEVEL
X ; DON'T CARE