

## Advance Information

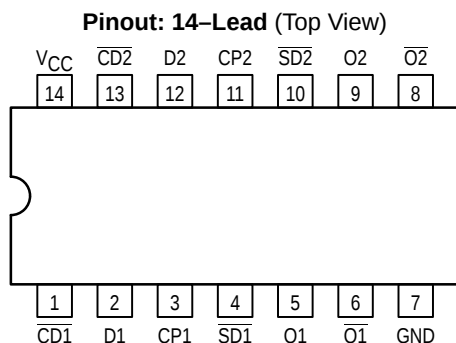
# Low-Voltage Quiet CMOS

# Dual D-Type Flip-Flop

The MC74LVQ74 is a high performance, dual D-type flip-flop with asynchronous clear and set inputs and complementary ( $O$ ,  $\bar{O}$ ) outputs. It operates from a 2.7 to 3.6V supply. High impedance TTL compatible inputs significantly reduce current loading to input drivers while TTL compatible outputs offer improved switching noise performance.

The MC74LVQ74 consists of 2 edge-triggered flip-flops with individual D-type inputs. The flip-flop will store the state of individual D inputs, that meet the setup and hold time requirements, on the LOW-to-HIGH Clock (CP) transition.

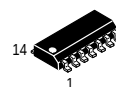
- Designed for 2.7 to 3.6V  $V_{CC}$  Operation – Ideal for Low Power/Low Noise Applications
- Guaranteed Simultaneous Switching Noise Level and Dynamic Threshold Performance
- Guaranteed Skew Specifications
- Guaranteed Incident Wave Switching into 75 $\Omega$
- Low Static Supply Current (10 $\mu$ A) Substantially Reduces System Power Requirements
- Latchup Performance Exceeds 500mA
- ESD Performance: Human Body Model >2000V



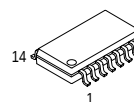
# MC74LVQ74

# LVQ

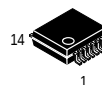
**LOW-VOLTAGE CMOS  
DUAL D-TYPE FLIP-FLOP**



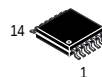
**D SUFFIX**  
PLASTIC SOIC  
CASE 751A-03



**M SUFFIX**  
PLASTIC SOIC EIAJ  
CASE 965-01



**SD SUFFIX**  
PLASTIC SSOP  
CASE 940A-03



**DT SUFFIX**  
PLASTIC TSSOP  
CASE 948G-01

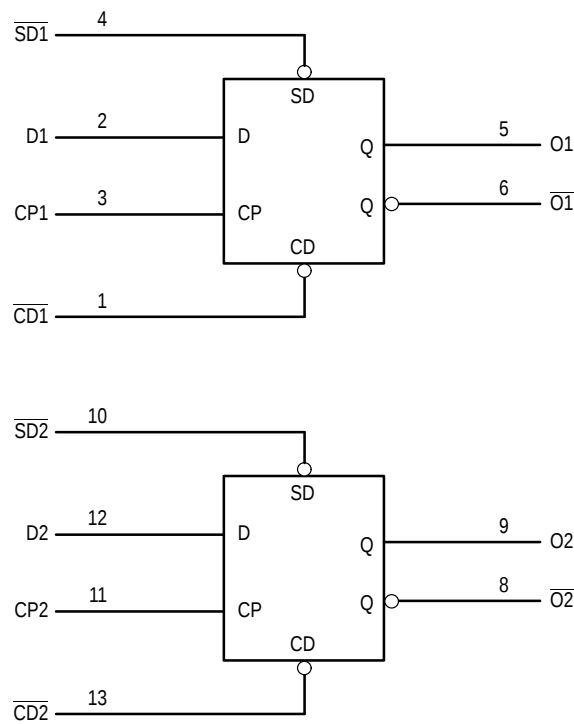
### PIN NAMES

| Pins                                | Function            |
|-------------------------------------|---------------------|
| CP1, CP2                            | Clock Pulse Inputs  |
| D1, D2                              | Data Inputs         |
| $\overline{CD1}$ , $\overline{CD2}$ | Direct Clear Inputs |
| $\overline{SD1}$ , $\overline{SD2}$ | Direct Set Inputs   |
| $O1$ , $O1$                         | Outputs             |

This document contains information on a new product. Specifications and information herein are subject to change without notice.



LOGIC DIAGRAM



| INPUTS |     |     |    | OUTPUTS |    | OPERATING MODE                                         |
|--------|-----|-----|----|---------|----|--------------------------------------------------------|
| SDn    | CDn | CPn | Dn | On      | On |                                                        |
| L      | H   | X   | X  | H       | L  | Asynchronous Set<br>Asynchronous Clear<br>Undetermined |
| H      | L   | X   | X  | L       | H  |                                                        |
| L      | L   | X   | X  | H       | H  |                                                        |
| H      | H   | ↑   | h  | H       | L  | Load and Read Register                                 |
| H      | H   | ↑   | l  | L       | H  |                                                        |
| H      | H   | ⊕   | X  | NC      | NC | Hold                                                   |

H = High Voltage Level; h = High Voltage Level One Setup Time Prior to the Low-to-High Clock Transition; L = Low Voltage Level; l = Low Voltage Level One Setup Time Prior to the Low-to-High Clock Transition; NC = No Change; X = High or Low Voltage Level or Transitions are Acceptable; ↑ = Low-to-High Transition; ⊕ = Not a Low-to-High Transition; For I<sub>CC</sub> Reasons DO NOT FLOAT Inputs

**ABSOLUTE MAXIMUM RATINGS\***

| Symbol    | Parameter                     | Value                              | Condition                   | Unit |
|-----------|-------------------------------|------------------------------------|-----------------------------|------|
| $V_{CC}$  | DC Supply Voltage             | -0.5 to +7.0                       |                             | V    |
| $V_I$     | DC Input Voltage              | $-0.5 \leq V_I \leq V_{CC} + 0.5V$ |                             | V    |
| $V_O$     | DC Output Voltage             | $-0.5 \leq V_O \leq V_{CC} + 0.5$  | Output in HIGH or LOW State | V    |
| $I_{IK}$  | DC Input Diode Current        | -20                                | $V_I = -0.5V$               | mA   |
|           |                               | +20                                | $V_I = V_{CC} + 0.5V$       | mA   |
| $I_{OK}$  | DC Output Diode Current       | -20                                | $V_O = -0.5V$               | mA   |
|           |                               | +20                                | $V_I = V_{CC} + 0.5V$       | mA   |
| $I_O$     | DC Output Source/Sink Current | $\pm 50$                           |                             | mA   |
| $I_{CC}$  | DC Supply Current             | $\pm 200$                          |                             | mA   |
| $I_{GND}$ | DC Ground Current             | $\pm 200$                          |                             | mA   |
| $T_{STG}$ | Storage Temperature Range     | -65 to +150                        |                             | °C   |

\* Absolute maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute-maximum-rated conditions is not implied.

**RECOMMENDED OPERATING CONDITIONS**

| Symbol              | Parameter                                                                       | Min | Typ | Max      | Unit  |
|---------------------|---------------------------------------------------------------------------------|-----|-----|----------|-------|
| $V_{CC}$            | Supply Voltage                                                                  | 2.0 | 3.3 | 3.6      | V     |
| $V_I$               | Input Voltage                                                                   | 0   |     | $V_{CC}$ | V     |
| $V_O$               | Output Voltage                                                                  | 0   |     | $V_{CC}$ | V     |
| $T_A$               | Operating Free-Air Temperature                                                  | -40 |     | +85      | °C    |
| $\Delta V/\Delta t$ | Input Transition Rise or Fall Rate, $V_{IN}$ from 0.8V to 2.0V, $V_{CC} = 3.0V$ | 0   |     | 125      | mV/ns |

**DC ELECTRICAL CHARACTERISTICS**

| Symbol    | Characteristic                          | Condition                                                         | $T_A = -40^\circ\text{C to } +85^\circ\text{C}$ |           | Unit    |
|-----------|-----------------------------------------|-------------------------------------------------------------------|-------------------------------------------------|-----------|---------|
|           |                                         |                                                                   | Min                                             | Max       |         |
| $V_{IH}$  | HIGH Level Input Voltage (Note 1)       | $2.7V \leq V_{CC} \leq 3.6V$ ,<br>$V_O = 0.1V$ or $V_{CC} - 0.1V$ | 2.0                                             |           | V       |
| $V_{IL}$  | LOW Level Input Voltage (Note 1)        | $2.7V \leq V_{CC} \leq 3.6V$ ,<br>$V_O = 0.1V$ or $V_{CC} - 0.1V$ |                                                 | 0.8       | V       |
| $V_{OH}$  | HIGH Level Output Voltage               | $2.7V \leq V_{CC} \leq 3.6V$ ; $I_{OH} = -50\mu A$                | $V_{CC} - 0.1$                                  |           | V       |
|           |                                         | $V_{CC} = 2.7V$ ; $I_{OH} = -12mA$                                | 2.2                                             |           |         |
|           |                                         | $V_{CC} = 3.0V$ ; $I_{OH} = -12mA$                                | 2.48                                            |           |         |
| $V_{OL}$  | LOW Level Output Voltage                | $2.7V \leq V_{CC} \leq 3.6V$ ; $I_{OL} = 50\mu A$                 |                                                 | 0.1       | V       |
|           |                                         | $2.7V \leq V_{CC} \leq 3.6V$ ; $I_{OL} = 12mA$                    |                                                 | 0.4       |         |
| $I_I$     | Input Leakage Current                   | $2.7V \leq V_{CC} \leq 3.6V$ ; $V_I = V_{CC}$ , GND               |                                                 | $\pm 1.0$ | $\mu A$ |
| $I_{OLD}$ | Minimum Dynamic Output Current (Note 2) | $V_{CC} = 3.6V$ ; $V_{OLD} = 0.8V$ Max                            |                                                 | 36        | mA      |
| $I_{OHD}$ |                                         | $V_{CC} = 3.6V$ ; $V_{OHD} = 2.0V$ Min                            |                                                 | -25       | mA      |
| $I_{CC}$  | Quiescent Supply Current                | $2.7V \leq V_{CC} \leq 3.6V$ ; $V_I = V_{CC}$ , GND               |                                                 | 10        | $\mu A$ |

1. These values of  $V_I$  are used to test DC electrical characteristics only. Functional test should use  $V_{IH} \geq 2.4V$ ,  $V_{IL} \leq 0.5V$ .
2. Incident wave switching on transmission lines with impedances as low as  $75\Omega$  for commercial temperature range is guaranteed. Maximum test duration is 2ms, one output loaded at a time.

**DYNAMIC SWITCHING CHARACTERISTICS** ( $V_{CC} = 3.3V$ )

| Symbol    | Characteristic                            | Condition                                              | $T_A = +25^\circ C$ |      |      | Unit |
|-----------|-------------------------------------------|--------------------------------------------------------|---------------------|------|------|------|
|           |                                           |                                                        | Min                 | Typ  | Max  |      |
| $V_{OLP}$ | Dynamic LOW Peak Voltage (Note 1)         | $C_L = 50pF$ , $V_{IH} = 3.3V$ , $V_{IL} = 0V$         |                     | 0.6  | 1.0  | V    |
| $V_{OLV}$ | Dynamic LOW Valley Voltage (Note 1)       | $C_L = 50pF$ , $V_{IH} = 3.3V$ , $V_{IL} = 0V$         |                     | -0.5 | -1.0 | V    |
| $V_{IHD}$ | High Level Dynamic Input Voltage (Note 2) | Input–Under–Test Switching 0V to Threshold, $f=1MHz$   |                     | 1.5  | 2.0  | V    |
| $V_{ILD}$ | Low Level Dynamic Input Voltage (Note 2)  | Input–Under–Test Switching 3.3V to Threshold, $f=1MHz$ |                     | 1.5  | 0.8  | V    |

- Number of outputs defined as “n”. Measured with “n–1” outputs switching from HIGH–to–LOW. The remaining output is measured in the LOW state.
- Number of data inputs is defined as “n” switching, “n–1” inputs switching 0V to 3.3V.

**AC CHARACTERISTICS** ( $t_R = t_F = 2.5ns$ ;  $C_L = 50pF$ ;  $R_L = 500\Omega$ )

| Symbol            | Parameter                                                                          | Limits                         |      |      |                        |      |      |                                 |      |                        | Unit |
|-------------------|------------------------------------------------------------------------------------|--------------------------------|------|------|------------------------|------|------|---------------------------------|------|------------------------|------|
|                   |                                                                                    | T <sub>A</sub> = +25°C         |      |      |                        |      |      | T <sub>A</sub> = −40°C to +85°C |      |                        |      |
|                   |                                                                                    | V <sub>CC</sub> = 3.0V to 3.6V |      |      | V <sub>CC</sub> = 2.7V |      |      | V <sub>CC</sub> = 3.0V to 3.6V  |      | V <sub>CC</sub> = 2.7V |      |
|                   |                                                                                    | Min                            | Typ  | Max  | Min                    | Typ  | Max  | Min                             | Max  | Max                    |      |
| f <sub>max</sub>  | Maximum Clock Frequency                                                            | 100                            | 125  |      | 50                     | 100  |      | 95                              |      |                        | MHz  |
| t <sub>PLH</sub>  | Propagation Delay                                                                  | 4.5                            | 8.0  | 13.5 | 4.5                    | 9.5  | 18.0 | 4.0                             | 16.0 | 20.0                   | ns   |
| t <sub>PHL</sub>  | CP <sub>n</sub> to On or $\overline{\text{On}}$                                    | 3.5                            | 8.0  | 14.0 | 3.5                    | 9.5  | 19.0 | 3.5                             | 14.5 | 20.0                   |      |
| t <sub>PLH</sub>  | Propagation Delay                                                                  | 3.5                            | 8.0  | 12.0 | 4.0                    | 9.5  | 15.0 | 3.5                             | 13.0 | 18.0                   | ns   |
| t <sub>PHL</sub>  | $\overline{\text{SDn}}$ or $\overline{\text{CDn}}$ to On or $\overline{\text{On}}$ | 4.0                            | 10.5 | 12.0 | 4.0                    | 12.5 | 16.0 | 3.5                             | 13.5 | 18.0                   |      |
| t <sub>OSHL</sub> | Output-to-Output Skew                                                              |                                | 1.0  | 1.5  |                        | 1.0  | 1.5  |                                 | 1.5  | 1.5                    | ns   |
| t <sub>OSLH</sub> | (Note 1)                                                                           |                                | 1.0  | 1.5  |                        | 1.0  | 1.5  |                                 | 1.5  | 1.5                    |      |

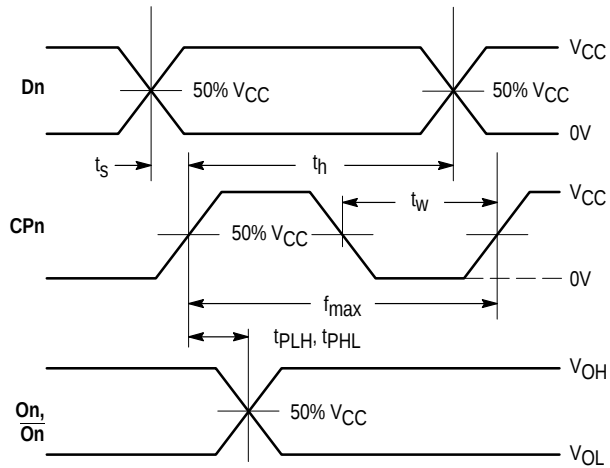
- Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH–to–LOW ( $t_{OSHL}$ ) or LOW–to–HIGH ( $t_{OSLH}$ ); parameter guaranteed by design.

**AC OPERATING REQUIREMENTS** ( $t_R = t_F = 2.5ns$ ;  $C_L = 50pF$ ;  $R_L = 500\Omega$ )

| Symbol           | Parameter                                                 | Limits                         |                        |                                 |                        | Unit |
|------------------|-----------------------------------------------------------|--------------------------------|------------------------|---------------------------------|------------------------|------|
|                  |                                                           | T <sub>A</sub> = +25°C         |                        | T <sub>A</sub> = −40°C to +85°C |                        |      |
|                  |                                                           | V <sub>CC</sub> = 3.0V to 3.6V | V <sub>CC</sub> = 2.7V | V <sub>CC</sub> = 3.0V to 3.6V  | V <sub>CC</sub> = 2.7V |      |
|                  |                                                           | Min                            | Min                    | Min                             | Min                    |      |
| t <sub>S</sub>   | Setup Time, HIGH or LOW Dn to CPn                         | 4.0                            | 5.0                    | 4.5                             | 6.5                    | ns   |
| t <sub>H</sub>   | Hold Time, HIGH or LOW Dn to CPn                          | 0.5                            | 0.5                    | 0.5                             | 0.5                    | ns   |
| t <sub>W</sub>   | $\overline{SDn}$ or $\overline{CDn}$ Pulse Width, LOW     | 5.5                            | 7.0                    | 7.0                             | 10.0                   | ns   |
| t <sub>W</sub>   | CPn Pulse Width HIGH or LOW                               | 5.5                            | 7.0                    | 7.0                             | 10.0                   | ns   |
| t <sub>rec</sub> | Recovery Time $\overline{SDn}$ or $\overline{CDn}$ to CPn | 0.0                            | 0.0                    | 0.0                             | 0.0                    | ns   |

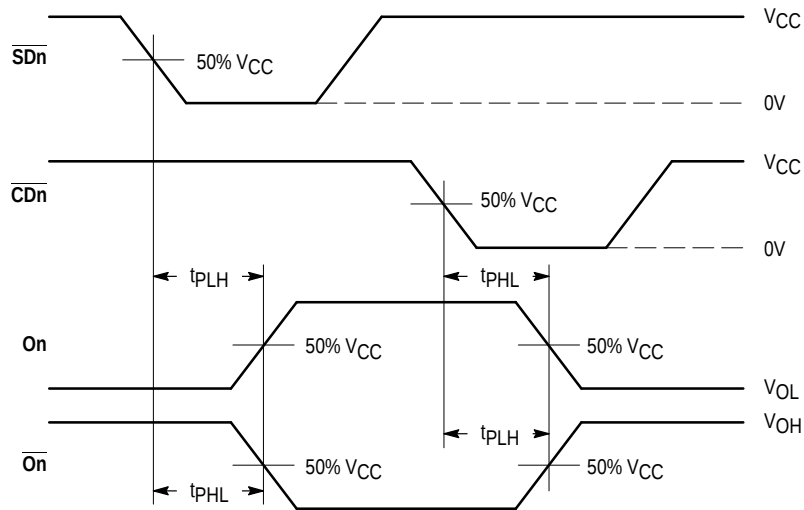
**CAPACITIVE CHARACTERISTICS**

| Symbol   | Parameter                     | Condition                                       | Typical | Unit |
|----------|-------------------------------|-------------------------------------------------|---------|------|
| $C_{PD}$ | Power Dissipation Capacitance | 10MHz, $V_{CC} = 3.3V$ , $V_I = 0V$ or $V_{CC}$ | 25      | pF   |
| $C_{IN}$ | Input Capacitance             | $V_{CC} = \text{Open}$ , $V_I = 0V$ or $V_{CC}$ | 4.5     | pF   |



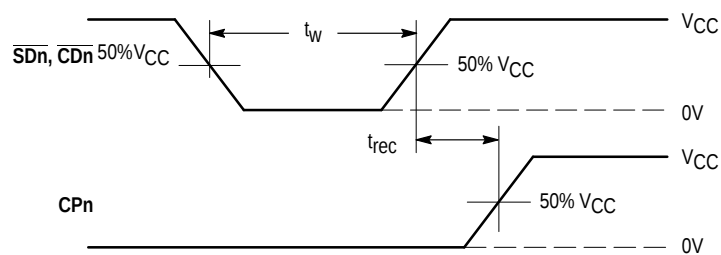
**WAVEFORM 1 – PROPAGATION DELAYS, SETUP AND HOLD TIMES**

$t_R = t_F = 2.5\text{ns}$ , 10% to 90%;  $f = 1\text{MHz}$ ;  $t_W = 500\text{ns}$



**WAVEFORM 2 – PROPAGATION DELAYS**

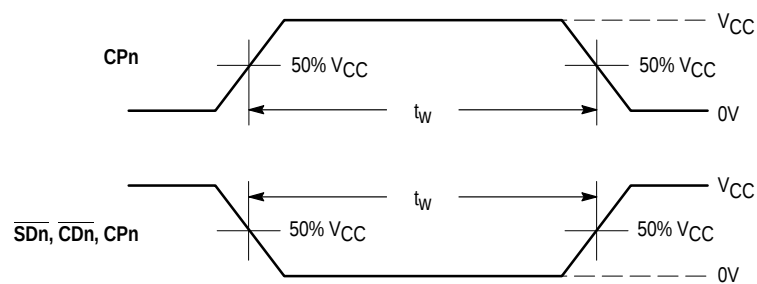
$t_R = t_F = 2.5\text{ns}$ , 10% to 90%;  $f = 1\text{MHz}$ ;  $t_W = 500\text{ns}$



**WAVEFORM 3 – RECOVERY TIME**

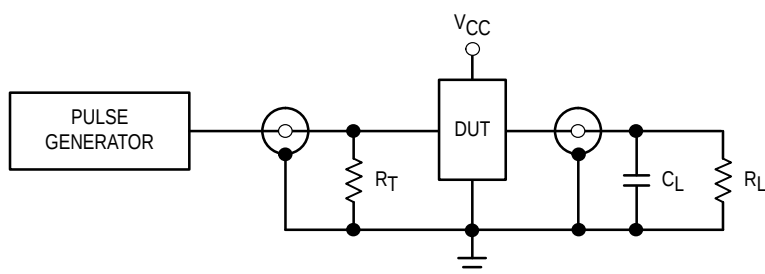
$t_R = t_F = 2.5\text{ns}$  from 10% to 90%;  $f = 1\text{MHz}$ ;  $t_W = 500\text{ns}$

**Figure 1. AC Waveforms**



**WAVEFORM 4 - PULSE WIDTH**  
 $t_R = t_F = 2.5\text{ns}$  (or fast as required) from 10% to 90%;  
 Output requirements:  $V_{OL} \leq 0.8\text{V}$ ,  $V_{OH} \geq 2.0\text{V}$

**Figure 1. AC Waveforms** (continued)

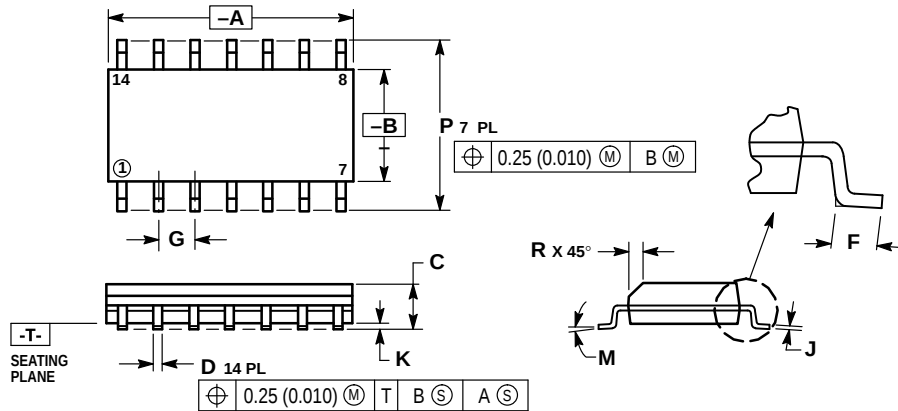


$C_L = 50\text{pF}$  or equivalent (Includes jig and probe capacitance)  
 $R_L = R_1 = 500\Omega$  or equivalent  
 $R_T = Z_{OUT}$  of pulse generator (typically  $50\Omega$ )

**Figure 2. Test Circuit**

## OUTLINE DIMENSIONS

**D SUFFIX**  
**PLASTIC SOIC PACKAGE**  
CASE 751A-03  
ISSUE F

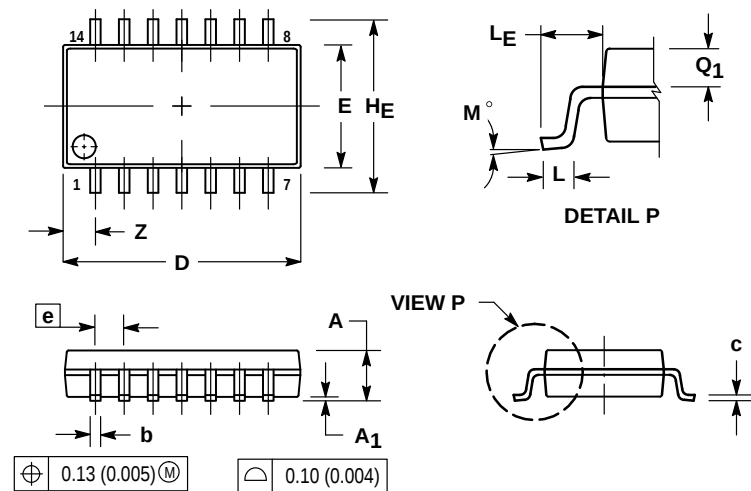


## NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 8.55        | 8.75 | 0.337     | 0.344 |
| B   | 3.80        | 4.00 | 0.150     | 0.157 |
| C   | 1.35        | 1.75 | 0.054     | 0.068 |
| D   | 0.35        | 0.49 | 0.014     | 0.019 |
| F   | 0.40        | 1.25 | 0.016     | 0.049 |
| G   | 1.27 BSC    |      | 0.050 BSC |       |
| J   | 0.19        | 0.25 | 0.008     | 0.009 |
| K   | 0.10        | 0.25 | 0.004     | 0.009 |
| M   | 0°          | 7°   | 0°        | 7°    |
| P   | 5.80        | 6.20 | 0.228     | 0.244 |
| R   | 0.25        | 0.50 | 0.010     | 0.019 |

**M SUFFIX**  
**PLASTIC SOIC EIAJ PACKAGE**  
CASE 965-01  
ISSUE O



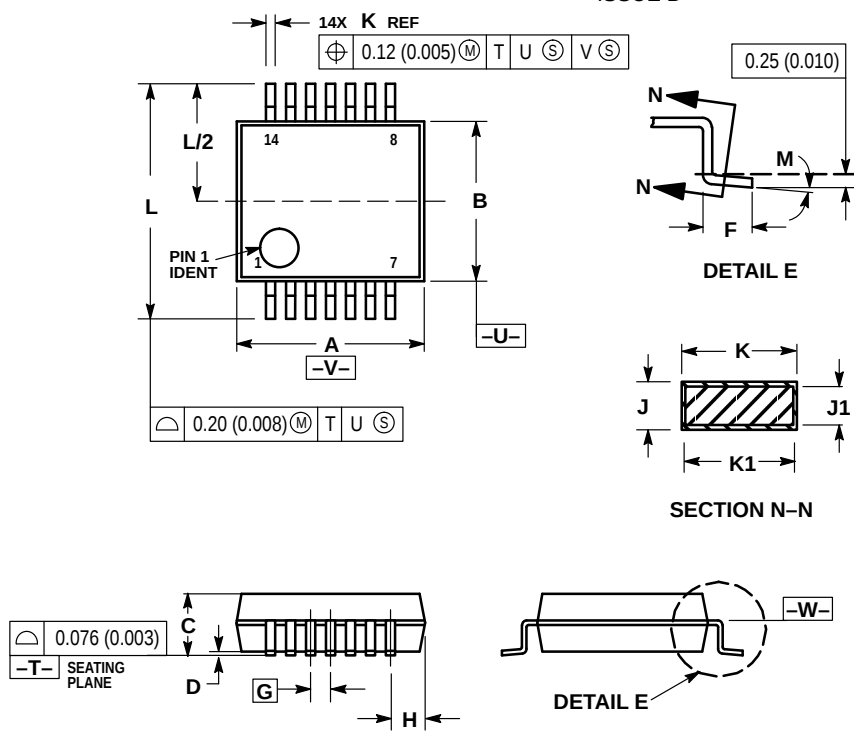
## NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

| DIM            | MILLIMETERS |       | INCHES    |       |
|----------------|-------------|-------|-----------|-------|
|                | MIN         | MAX   | MIN       | MAX   |
| A              | ---         | 2.05  | ---       | 0.081 |
| A <sub>1</sub> | 0.05        | 0.20  | 0.002     | 0.008 |
| b              | 0.35        | 0.50  | 0.014     | 0.020 |
| c              | 0.18        | 0.27  | 0.007     | 0.011 |
| D              | 9.90        | 10.50 | 0.390     | 0.413 |
| E              | 5.10        | 5.45  | 0.201     | 0.215 |
| e              | 1.27 BSC    |       | 0.050 BSC |       |
| H <sub>E</sub> | 7.40        | 8.20  | 0.291     | 0.323 |
| L              | 0.50        | 0.85  | 0.020     | 0.033 |
| L <sub>E</sub> | 1.10        | 1.50  | 0.043     | 0.059 |
| M              | 0°          | 10°   | 0°        | 10°   |
| Q <sub>1</sub> | 0.70        | 0.90  | 0.028     | 0.035 |
| Z              | ---         | 1.42  | ---       | 0.056 |

## OUTLINE DIMENSIONS

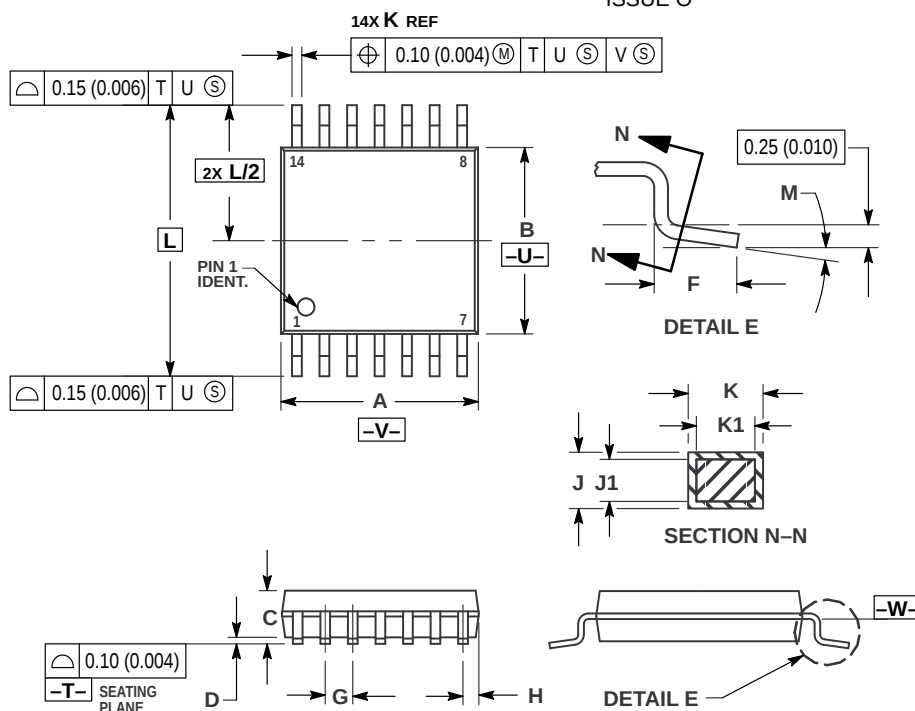
**SD SUFFIX**  
PLASTIC SSOP PACKAGE  
CASE 940A-03  
ISSUE B



- NOTES:
- 6 DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  - 7 CONTROLLING DIMENSION: MILLIMETER.
  - 8 DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
  - 9 DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
  - 10 DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION/INTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF K DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR INTRUSION SHALL NOT REDUCE DIMENSION K BY MORE THAN 0.07 (0.002) AT LEAST MATERIAL CONDITION.
  - 11 TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
  - 12 DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 6.07        | 6.33 | 0.238     | 0.249 |
| B   | 5.20        | 5.38 | 0.205     | 0.212 |
| C   | 1.73        | 1.99 | 0.068     | 0.078 |
| D   | 0.05        | 0.21 | 0.002     | 0.008 |
| F   | 0.63        | 0.95 | 0.024     | 0.037 |
| G   | 0.65 BSC    |      | 0.026 BSC |       |
| H   | 1.08        | 1.22 | 0.042     | 0.048 |
| J   | 0.09        | 0.20 | 0.003     | 0.008 |
| J1  | 0.09        | 0.16 | 0.003     | 0.006 |
| K   | 0.25        | 0.38 | 0.010     | 0.015 |
| K1  | 0.25        | 0.33 | 0.010     | 0.013 |
| L   | 7.65        | 7.90 | 0.301     | 0.311 |
| M   | 0°          | 8°   | 0°        | 8°    |

**DT SUFFIX**  
PLASTIC TSSOP PACKAGE  
CASE 948G-01  
ISSUE O



- NOTES:**
- 1 DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  - 2 CONTROLLING DIMENSION: MILLIMETER.
  - 3 DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
  - 4 DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
  - 5 DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
  - 6 TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
  - 7 DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

| DIM | MILLIMETERS |      | INCHES    |       |
|-----|-------------|------|-----------|-------|
|     | MIN         | MAX  | MIN       | MAX   |
| A   | 4.90        | 5.10 | 0.193     | 0.200 |
| B   | 4.30        | 4.50 | 0.169     | 0.177 |
| C   | —           | 1.20 | —         | 0.047 |
| D   | 0.05        | 0.15 | 0.002     | 0.006 |
| F   | 0.50        | 0.75 | 0.020     | 0.030 |
| G   | 0.65 BSC    |      | 0.026 BSC |       |
| H   | 0.50        | 0.60 | 0.020     | 0.024 |
| J   | 0.09        | 0.20 | 0.004     | 0.008 |
| J1  | 0.09        | 0.16 | 0.004     | 0.006 |
| K   | 0.19        | 0.30 | 0.007     | 0.012 |
| K1  | 0.19        | 0.25 | 0.007     | 0.010 |
| L   | 6.40 BSC    |      | 0.252 BSC |       |
| M   | 0°          | 8°   | 0°        | 8°    |

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