

Advance Information

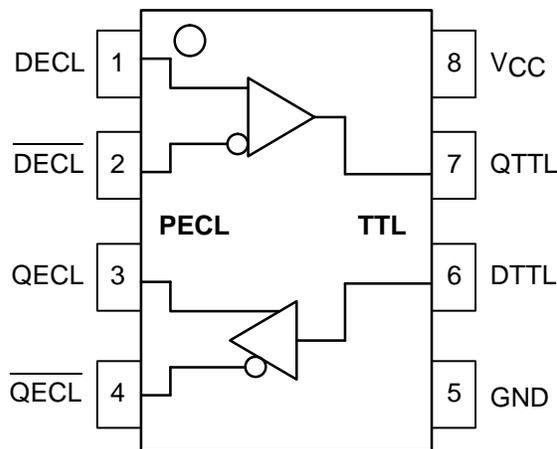
TTL to Differential PECL/Differential PECL to TTL Translator

The MC10ELT/100ELT28 is a differential PECL to TTL translator and a TTL to differential PECL translator in a single package. Because PECL (Positive ECL) levels are used only +5V and ground are required. The small outline 8-lead SOIC package and the dual translation design of the ELT28 makes it ideal for applications which are sending and receiving signals across a backplane. Because the mature MOSAIC 1.5 process is used, low cost can be added to the list of features.

The ELT28 is available in both ECL standards: the 10ELT is compatible with positive MECL 10H logic levels while the 100ELT is compatible with positive ECL 100K logic levels.

- 3.5ns Typical PECL to TTL Propagation Delay
- 1.2ns Typical TTL to PECL Propagation Delay
- Differential PECL Inputs/Outputs
- Small Outline SOIC Package
- PNP TTL Inputs for Minimal Loading
- 24mA TTL Outputs
- Flow Through Pinouts

LOGIC DIAGRAM AND PINOUT ASSIGNMENT



MC10ELT28 MC100ELT28



D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751-05

PIN DESCRIPTION

PIN	FUNCTION
QTTL	TTL Output
DTTL	TTL Inputs
QECL	Diff ECL Outputs
DECL	Diff ECL Inputs
VCC	+5.0V Supply
GND	Ground

MAXIMUM RATINGS*

Symbol	Parameter	Value	Unit
VCC	DC Supply Voltage (Referenced to GND)	7.0	V
T _A	Operating Temperature Range (In Free-Air)	-40 to 85	°C
T _{STG}	Storage Temperature Range	-55 to +150	°C

* Maximum Ratings are those values beyond which damage to the device may occur. Functional operation should be restricted to the Recommended Operating Conditions.

This document contains information on a new product. Specifications and information herein are subject to change without notice.



MC10ELT28 MC100ELT28

TTL OUTPUT DC CHARACTERISTICS ($V_{CC} = 4.75V$ to $5.25V$; $T_A = -40^{\circ}C$ to $85^{\circ}C$)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
V_{OH}	Output HIGH Voltage	2.4			V	$I_{OH} = -3.0mA$
V_{OL}	Output LOW Voltage			0.5	V	$I_{OL} = 24mA$
I_{CCH}	Power Supply Current		27	40	mA	
I_{CCL}	Power Supply Current		29	42	mA	
I_{OS}	Output Short Circuit Current	-150		-60	mA	

TTL INPUT DC CHARACTERISTICS ($V_{CC} = 4.75V$ to $5.25V$; $T_A = -40^{\circ}C$ to $85^{\circ}C$)

Symbol	Characteristic	Min	Typ	Max	Unit	Condition
I_{IH}	Input HIGH Current			20	μA	$V_{IN} = 2.7V$
I_{IHH}	Input HIGH Current			100	μA	$V_{IN} = 7.0V$
I_{IL}	Input LOW Current			-0.6	mA	$V_{IN} = 0.5V$
V_{IK}				-1.2	V	$I_{IN} = -18mA$
V_{IH}	Input HIGH Voltage	2.0			V	
V_{IL}	Input LOW Voltage			0.8	V	

PECL OUTPUT DC CHARACTERISTICS ($V_{CC} = 4.75V$ to $5.25V$; $T_A = -40^{\circ}C$ to $85^{\circ}C$)

Symbol	Characteristic	$-40^{\circ}C$		$0^{\circ}C$		$25^{\circ}C$			$85^{\circ}C$		Unit	Condition
		Min	Max	Min	Max	Min	Typ	Max	Min	Max		
V_{OH}	Output HIGH Voltage	10ELT ¹ 3.920	4.11	3.980	4.16	4.020	4.10	4.19	4.080	4.27	V	$V_{CC} = 5.0V$
		100ELT ¹ 3.915	4.12	3.975	4.12	3.975	4.05	4.12	3.975	4.12		
V_{OL}	Output LOW Voltage	10ELT ¹ 3.05	3.350	3.05	3.37	3.05	3.25	3.37	3.05	3.40	V	$V_{CC} = 5.0V$
		100ELT ¹ 3.17	3.445	3.19	3.38	3.19	3.30	3.38	3.19	3.35		

1. Levels will vary 1:1 with V_{CC} .

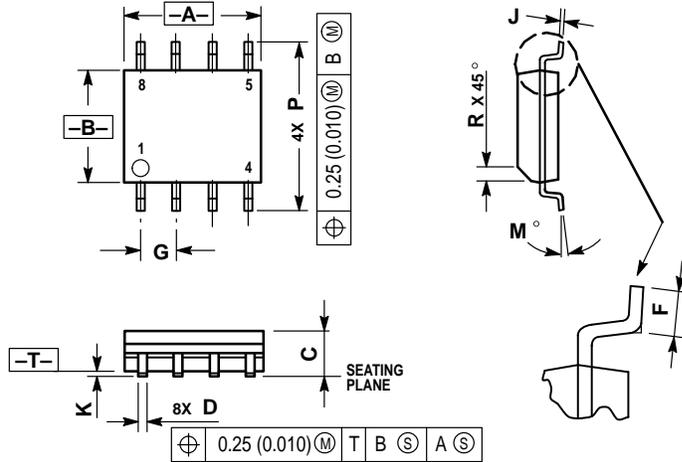
PECL INPUT DC CHARACTERISTICS ($V_{CC} = 4.75V$ to $5.25V$; $T_A = -40^{\circ}C$ to $85^{\circ}C$)

Symbol	Characteristic	$-40^{\circ}C$		$0^{\circ}C$		$25^{\circ}C$			$85^{\circ}C$		Unit	Condition
		Min	Max	Min	Max	Min	Typ	Max	Min	Max		
I_{IH}	Input HIGH Current		150		150			150		150	μA	
I_{IL}	Input LOW Current	0.5		0.5		0.5			0.5		μA	
V_{CMR}	Common Mode Range	2.2	V_{CC}	2.2	V_{CC}	2.2		V_{CC}	2.2	V_{CC}	V	
V_{PP}	Minimum Peak-to-Peak Input ¹	200		200		200			200		mV	
V_{IH}	Input HIGH Voltage	10ELT 3.770	4.110	3.830	4.16	3.870		4.19	3.930	4.265	V	$V_{CC} = 5.0V$
		100ELT 3.835	4.120	3.835	4.12	3.835		4.12	3.835	4.120		
V_{IL}	Input LOW Voltage	10ELT 3.05	3.500	3.05	3.520	3.05		3.520	3.05	3.550	V	$V_{CC} = 5.0V$
		100ELT 3.19	3.525	3.19	3.525	3.19		3.525	3.19	3.525		
t_{PLH}	Prop Delay DECL to QTTL DTTL to QECL	2.0 0.6	5.5 1.2	2.0 0.65	5.5 1.45	2.0 0.9	1.2	5.5 1.5	2.0 0.6	5.5 1.35	ns	$C_L = 20pF$
t_{PHL}	Prop Delay DECL to QTTL DTTL to QECL	2.0 0.4	5.5 1.0	2.0 0.45	5.5 1.05	2.0 0.5	0.8	5.5 1.1	2.0 0.7	5.5 1.3	ns	$C_L = 20pF$
t_r, t_f	Rise/Fall Times	QECL 0.15	1.5	0.15	1.5	0.15		1.5	0.15	1.5	ns	20% – 80%

1. 200mV input guarantees full logic swing at the output.

OUTLINE DIMENSIONS

D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751-05
ISSUE P



NOTES:

1. DIMENSIONS A AND B ARE DATUMS AND T IS A DATUM SURFACE.
2. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
3. DIMENSIONS ARE IN MILLIMETER.
4. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
5. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
6. DIMENSION D DOES NOT INCLUDE MOLD PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	4.80	5.00
B	3.80	4.00
C	1.35	1.75
D	0.35	0.49
F	0.40	1.25
G	1.27 BSC	
J	0.18	0.25
K	0.10	0.25
M	0°	7°
P	5.80	6.20
R	0.25	0.50

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How to reach us:

USA/EUROPE/Locations Not Listed: Motorola Literature Distribution; P.O. Box 20912; Phoenix, Arizona 85036. 1-800-441-2447 or 602-303-5454

JAPAN: Nippon Motorola Ltd.; Tatsumi-SPD-JLDC, 6F Seibu-Butsuryu-Center, 3-14-2 Tatsumi Koto-Ku, Tokyo 135, Japan. 03-81-3521-8315

MFAX: RMFAX0@email.sps.mot.com - TOUCHTONE 602-244-6609
INTERNET: http://Design-NET.com

ASIA/PACIFIC: Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park, 51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852-26629298

