

PowerMOS transistor
Voltage clamped logic level FET
with temperature sensing diodes

BUK9120-48TC

GENERAL DESCRIPTION

Protected N-channel enhancement mode logic level field-effect power transistor in a plastic envelope suitable for surface mounting. Using 'trench' technology the device features very low on-state resistance and has integral zener diodes giving ESD protection up to 2kV and active drain voltage clamping. Temperature sensitive diodes are incorporated for monitoring chip temperature. The device is intended for use in automotive and general purpose switching applications.

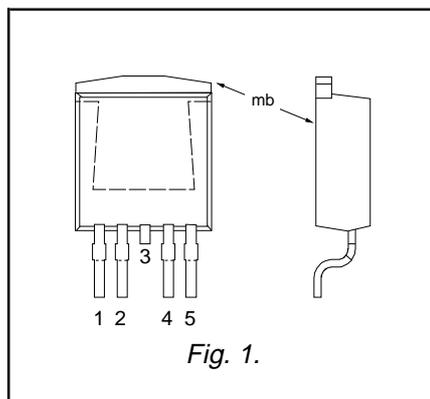
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MIN.	TYP.	MAX.	UNIT
$V_{(CL)DSR}$	Drain-source clamp voltage	40	45	55	V
I_D	Drain current (DC)			52	A
P_{tot}	Total power dissipation			116	W
T_j	Junction temperature			175	°C
$R_{DS(ON)}$	Drain-source on-state resistance; $V_{GS} = 5\text{ V}$			20	mΩ
V_F	Forward voltage, temperature sense diodes	685	710	735	mV
$-S_F$	Negative temperature coefficient, temperature sense diodes	1.26	1.4	1.54	mV/K

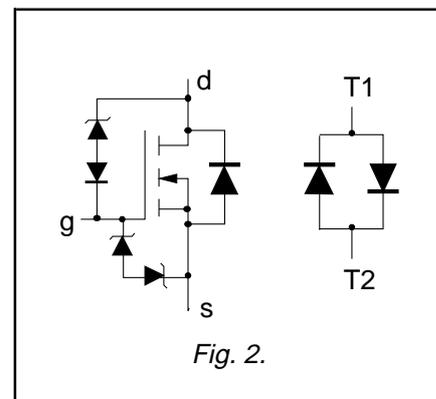
PINNING - SOT426

PIN	DESCRIPTION
1	gate
2	T1
3	(connected to mb)
4	T2
5	source
mb	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	continuous	-	40	V
V_{DG}	Drain-gate voltage	continuous	-	38	V
$\pm V_{GS}$	Gate-source voltage	-	-	10	V
I_D	Drain current (DC)	$T_{mb} = 25\text{ °C}$	-	52	A
I_D	Drain current (DC)	$T_{mb} = 100\text{ °C}$	-	37	A
I_D	Drain current (DC)	$T_{mb} = 140\text{ °C}$	-	25	A
I_{DM}	Drain current (pulse peak value)	$T_{mb} = 25\text{ °C}$	-	208	A
P_{tot}	Total power dissipation	$T_{mb} = 25\text{ °C}$	-	116	W
I_{GD}	Drain-gate clamp current	5ms pulse; $\Delta = 0.01$	-	50	mA
I_{GS}	Gate-source clamp current	5ms pulse; $\Delta = 0.01$	-	50	mA
V_{TS}	Source T1/T2 voltage	-	-	± 100	V
T_{stg}	Storage temperature	-	- 55	175	°C
T_j	Junction temperature	-	- 55	175	°C

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ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge voltage, pins 1,3,5	Human body model (100pF,1.5K Ω)	-	2	kV

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$R_{th\ j-mb}$	Thermal resistance junction to mounting base		-	-	1.29	K/W
$R_{th\ j-a}$	Thermal resistance junction to ambient	minimum footprint, FR4 board	-	50	-	K/W

STATIC CHARACTERISTICS

 $T_j = 25\text{ }^\circ\text{C}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DG}$	Drain-gate zener voltage	250 μ A; $-55\text{ }^\circ\text{C} \leq T_j \leq 175\text{ }^\circ\text{C}$	38	43		V
$V_{GS(TO)}$	Gate threshold voltage	$V_{DS} = V_{GS}$; $I_D = 1\text{ mA}$; $T_j = 175\text{ }^\circ\text{C}$	1.0	1.5	2.0	V
		$T_j = -55\text{ }^\circ\text{C}$	0.5	-	-	V
I_{DSS}	Zero gate voltage drain current	$V_{DS} = +35\text{ V}$; $V_{GS} = 0\text{ V}$; $T_j = 175\text{ }^\circ\text{C}$	-	0.1	100	μ A
			-	-	250	μ A
I_{DSS}	Zero gate voltage drain current	$V_{DS} = +15\text{ V}$; $V_{GS} = 0\text{ V}$; $T_j = 175\text{ }^\circ\text{C}$	-	0.004	2	μ A
			-	-	250	μ A
I_{GSS}	Gate source leakage current	$V_{GS} = \pm 5\text{ V}$; $V_{DS} = 0\text{ V}$; $T_j = 175\text{ }^\circ\text{C}$	-	0.02	1	μ A
			-	-	10	μ A
$\pm V_{(BR)GSS}$	Gate source breakdown voltage	$\pm 1\text{ mA}$;	10	-	-	V
$R_{DS(ON)}$	Drain-source on-state resistance	$V_{GS} = 5\text{ V}$; $I_D = 20\text{ A}$; $T_j = 175\text{ }^\circ\text{C}$	-	16	20	m Ω
			-	-	42	m Ω
V_F	Forward voltage, temperature sense diodes	$I_F = 250\text{ }\mu\text{A}$;	685	710	735	V
						mV
$-S_F$	Negative temperature coefficient, temperature sense diodes from $25\text{ }^\circ\text{C}$ to $140\text{ }^\circ\text{C}$	$I_F = 250\text{ }\mu\text{A}$	1.26	1.4	1.54	mV/K
V_{HYS}	Forward voltage hysteresis; temperature sense diodes	$I_F = 125\text{ }\mu\text{A}$ to $250\text{ }\mu\text{A}$	25		50	mV

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DYNAMIC CHARACTERISTICS $T_j = 25\text{ }^\circ\text{C}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(CL)DSR}$	Drain source clamp voltage (peak value)	$R_G = 10\text{ k}\Omega$; $I_D = 10\text{ A}$; $-55 \leq T_j \leq 175\text{ }^\circ\text{C}$	40	45	55	V
g_{fs}	Forward transconductance	$V_{DS} = 25\text{ V}$; $I_D = 10\text{ A}$	20	53	-	S
C_{iss}	Input capacitance	$V_{GS} = 0\text{ V}$; $V_{DS} = 25\text{ V}$; $f = 1\text{ MHz}$	-	2200	2900	pF
C_{oss}	Output capacitance		-	400	500	pF
C_{rss}	Feedback capacitance		-	215	300	pF
t_{don}	Turn-on delay time	$V_{DD} = 30\text{ V}$; $I_D = 25\text{ A}$; $V_{GS} = 5\text{ V}$; $R_G = 10\text{ k}\Omega$;	-	12	18	μs
t_r	Turn-on rise time		-	55	80	μs
t_{doff}	Turn-off delay time		-	60	85	μs
t_f	Turn-off fall time		-	45	60	μs
L_d	Internal drain inductance	Measured from upper edge of drain tab to centre of die	-	2.5	-	nH
L_s	Internal source inductance	Measured from source lead soldering point to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS $T_j = 25\text{ }^\circ\text{C}$ unless otherwise specified

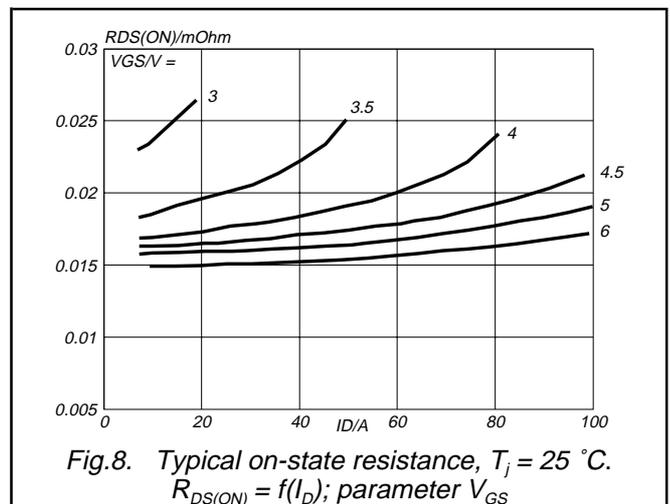
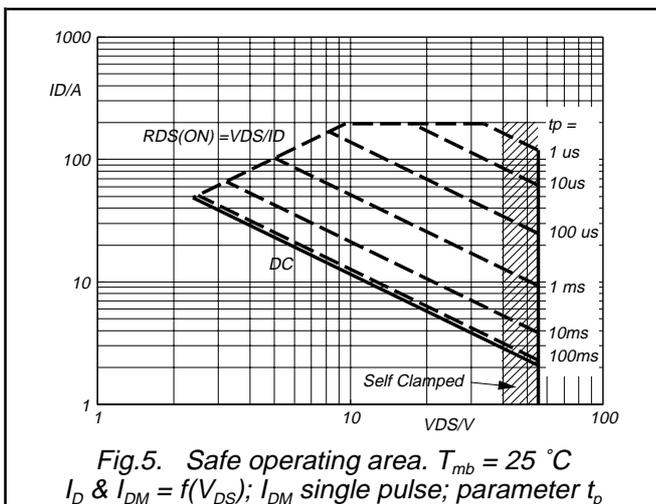
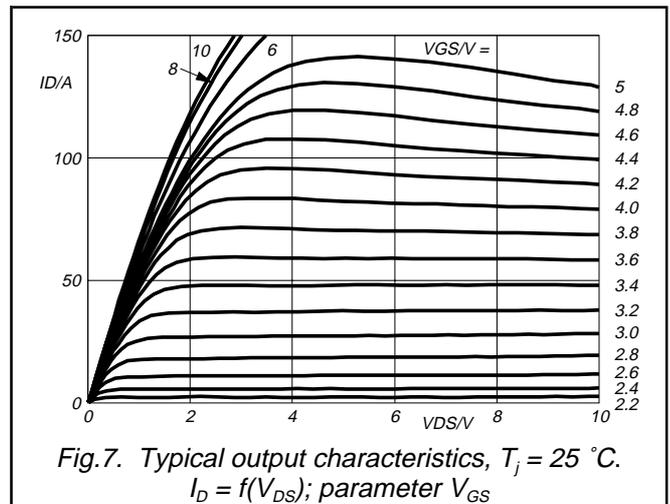
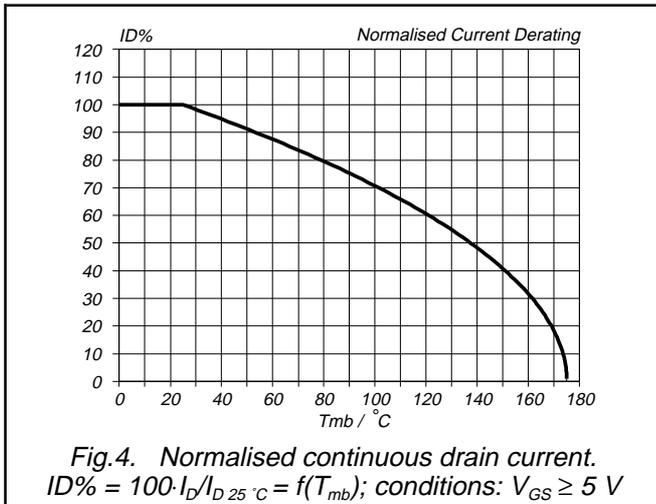
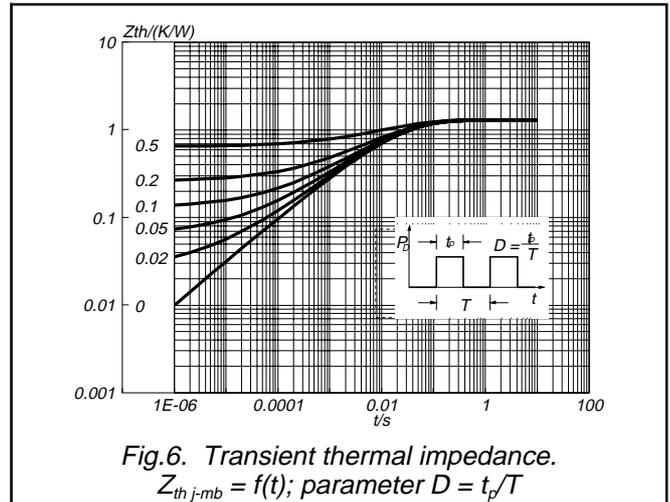
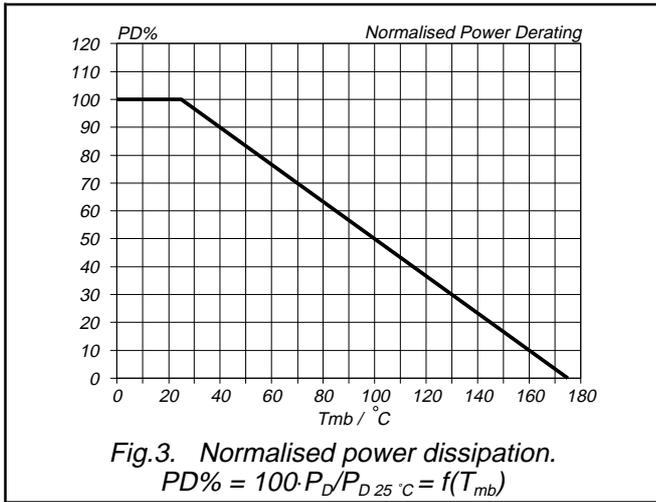
SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current	-	-	-	52	A
I_{DRM}	Pulsed reverse drain current	-	-	-	208	A
V_{SD}	Diode forward voltage	$I_F = 20\text{ A}$; $V_{GS} = 0\text{ V}$	-	0.95	1.2	V
		$I_F = 40\text{ A}$; $V_{GS} = 0\text{ V}$	-	1	-	V

CLAMPED ENERGY LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
W_{DSRS}	Non-repetitive drain-source clamped inductive turn off energy	$T_j = 25\text{ }^\circ\text{C}$ prior to clamping; $I_D = 20\text{ A}$; $V_{DD} \leq 16\text{ V}$; $V_{GS} = 5\text{ V}$; $R_G = 10\text{ k}\Omega$; inductive load	-	450	mJ

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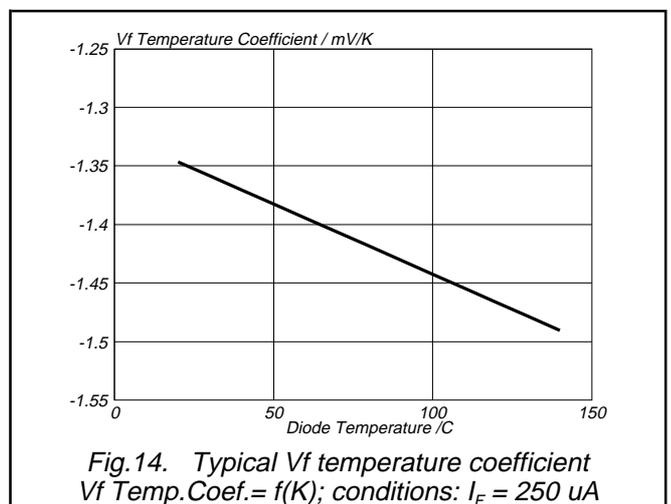
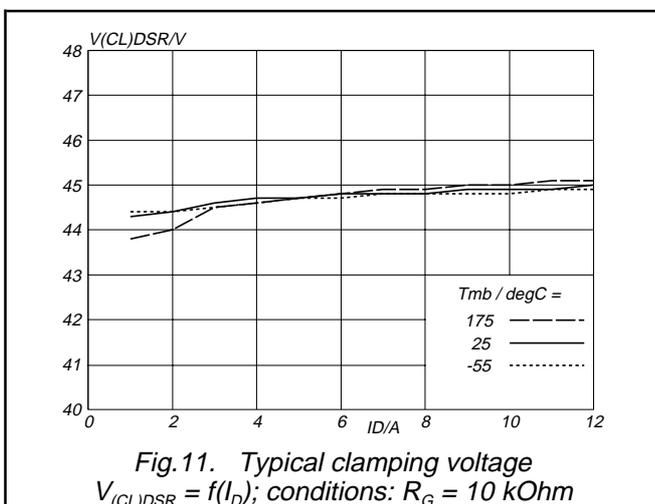
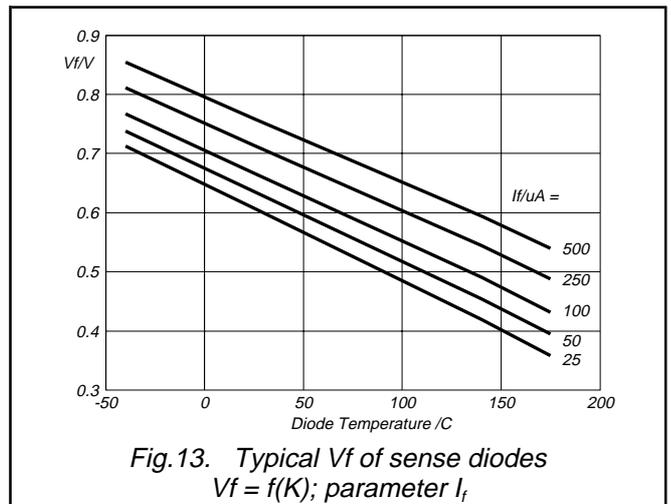
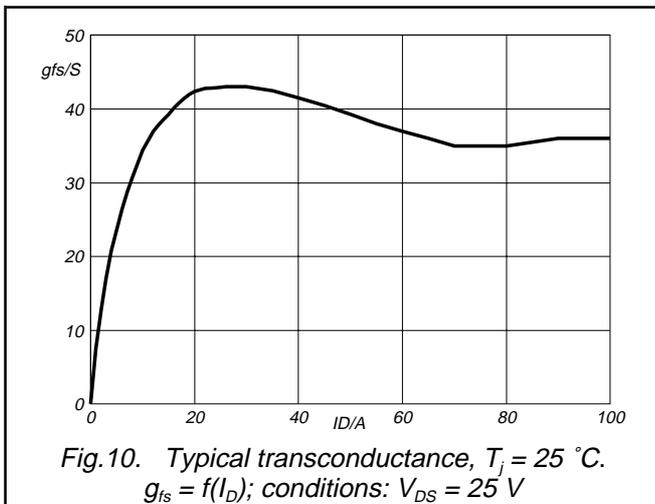
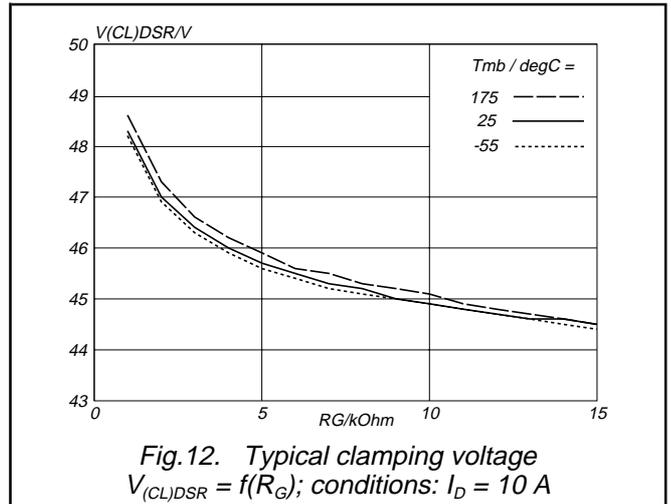
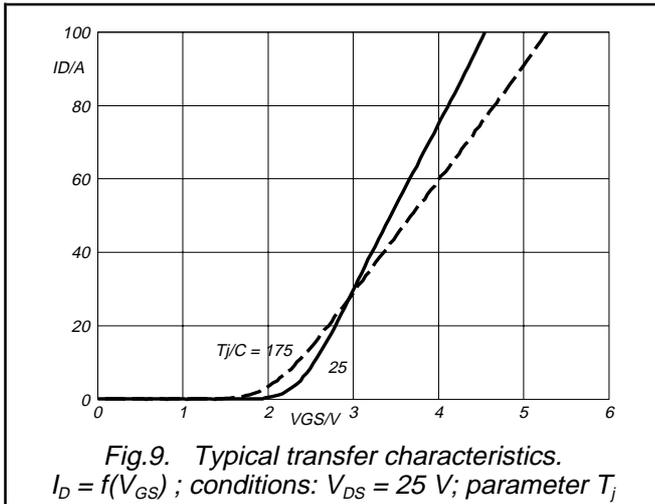
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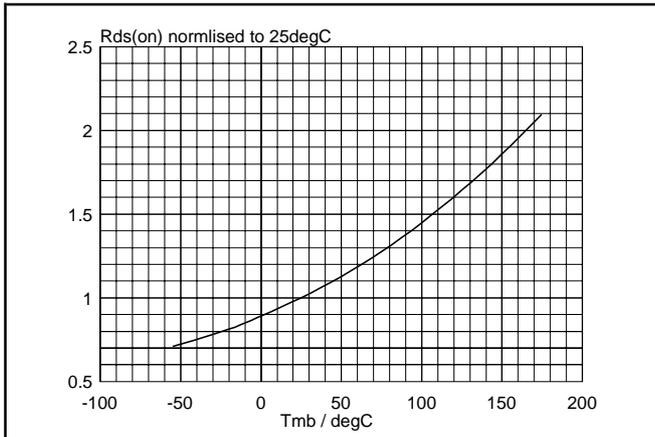


Fig.15. Normalised drain-source on-state resistance.
 $a = R_{DS(ON)}/R_{DS(ON)25\text{ }^\circ\text{C}} = f(T_j)$; $I_D = 25\text{ A}$; $V_{GS} = 5\text{ V}$

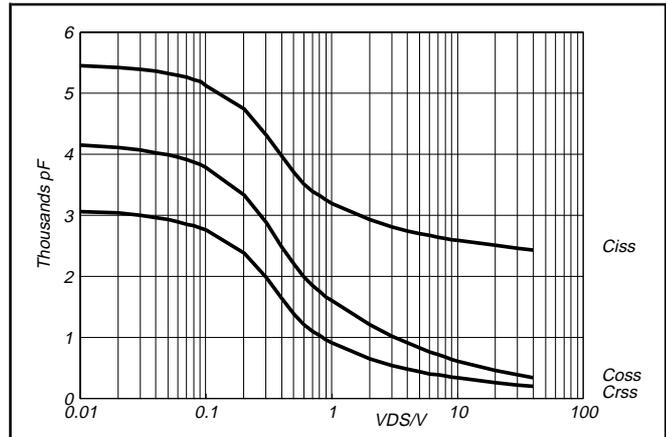


Fig.18. Typical capacitances, C_{iss} , C_{oss} , C_{rss} .
 $C = f(V_{DS})$; conditions: $V_{GS} = 0\text{ V}$; $f = 1\text{ MHz}$

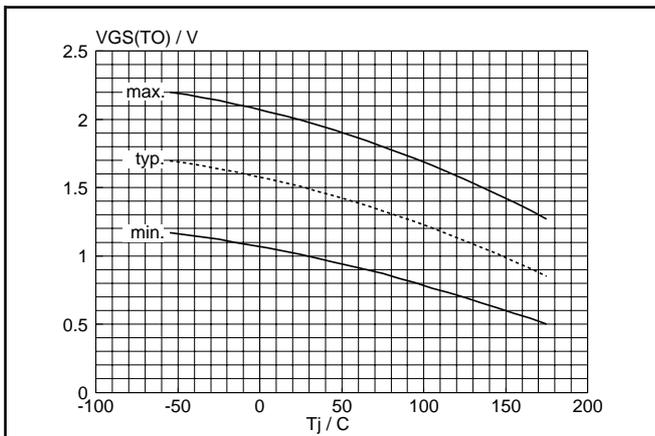


Fig.16. Gate threshold voltage.
 $V_{GS(TO)} = f(T_j)$; conditions: $I_D = 1\text{ mA}$; $V_{DS} = V_{GS}$

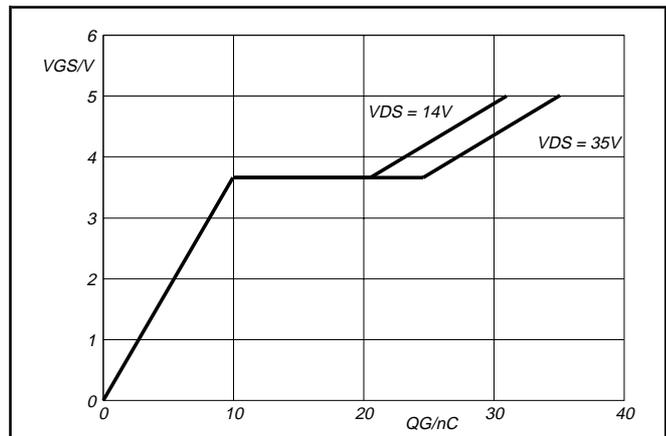


Fig.19. Typical turn-on gate-charge characteristics.
 $V_{GS} = f(Q_G)$; conditions: $I_D = 50\text{ A}$; parameter V_{DS}

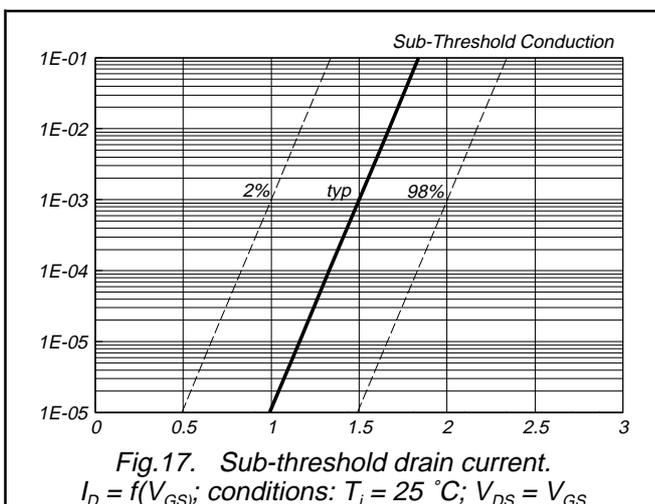


Fig.17. Sub-threshold drain current.
 $I_D = f(V_{GS})$; conditions: $T_j = 25\text{ }^\circ\text{C}$; $V_{DS} = V_{GS}$

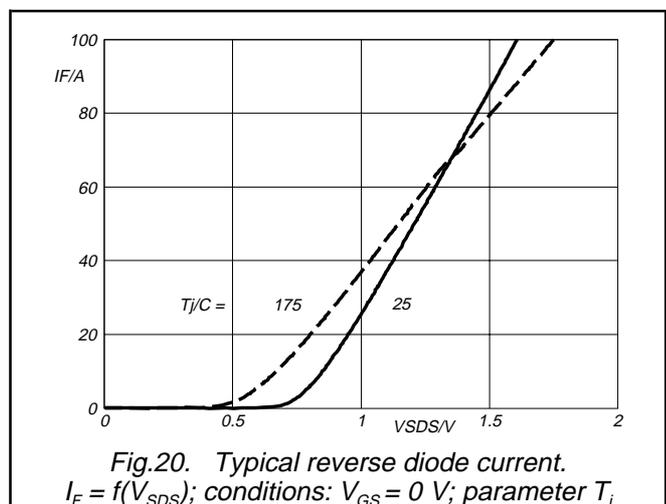
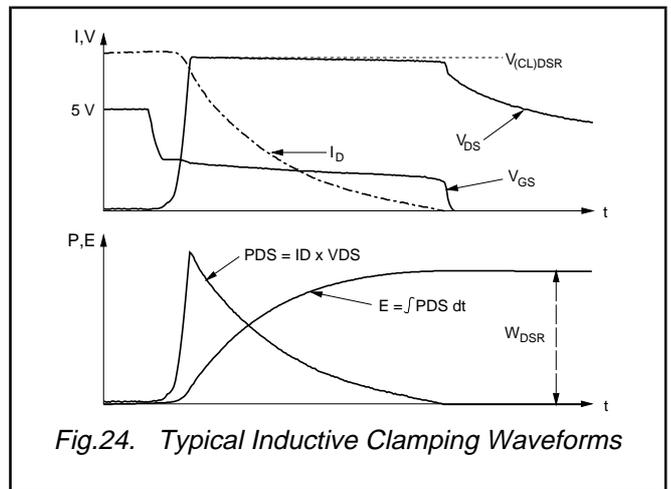
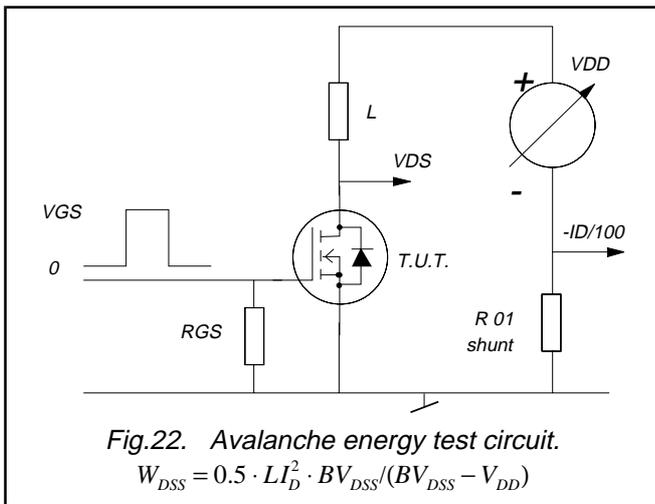
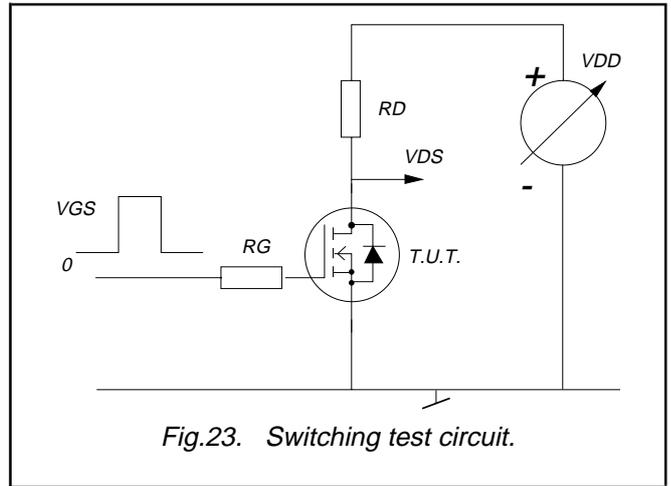
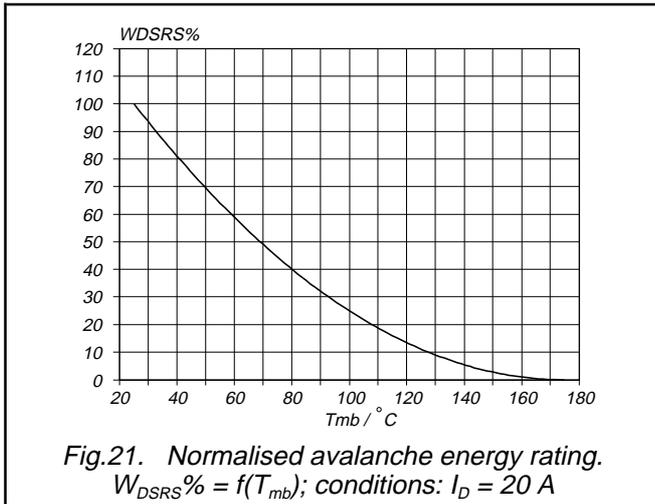


Fig.20. Typical reverse diode current.
 $I_F = f(V_{SDS})$; conditions: $V_{GS} = 0\text{ V}$; parameter T_j

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MECHANICAL DATA

Dimensions in mm

Net Mass: 1.4 g

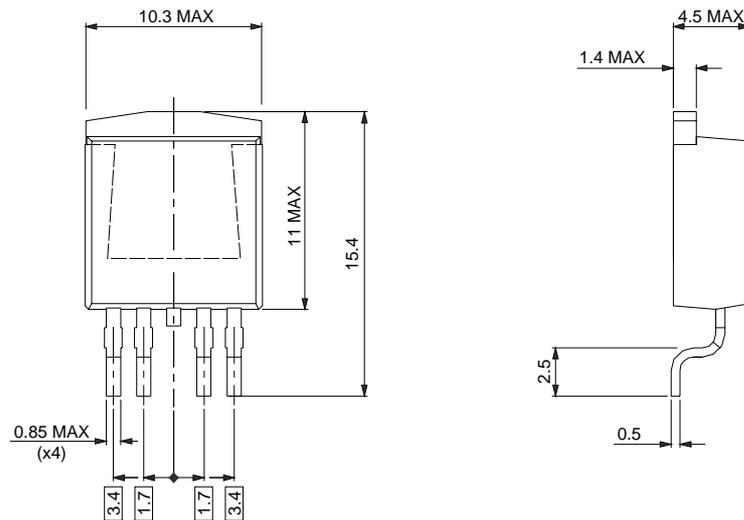


Fig.25. SOT426 : centre pin connected to mounting base.

MOUNTING INSTRUCTIONS

Dimensions in mm

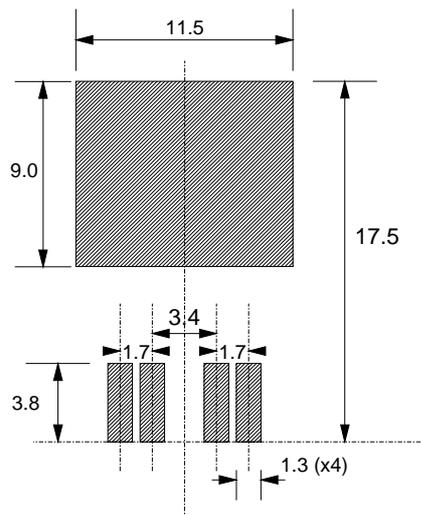


Fig.26. SOT426 : soldering pattern for surface mounting.

Notes

1. Observe the general handling precautions for electrostatic-discharge sensitive devices (ESDs) to prevent damage to MOS gate oxide.
2. Epoxy meets UL94 V0 at 1/8".

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BUK9120-48TC**DEFINITIONS**

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	
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