TrenchMOS™ transistor Standard level FET

BUK7621-30

GENERAL DESCRIPTION

N-channel enhancement mode standard level field-effect power transistor in a plastic envelope suitable for surface mounting using '**trench**' technology. The device features very low on-state resistance and has integral zener diodes giving ESD protection up to 2kV. It is intended for use in automotive and general purpose switching applications.

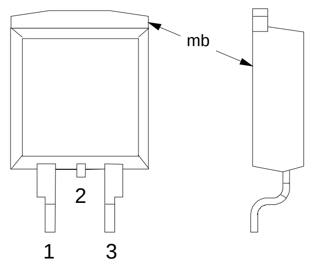
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	30	V
I_D	Drain current (DC)	50	A
P_{tot}	Total power dissipation	94	W
T_j	Junction temperature	175	˚C
$R_{DS(ON)}$	Drain-source on-state resistance V_{GS} = 10 V	21	mΩ

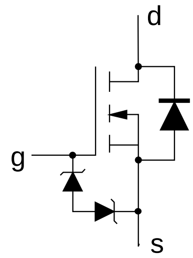
PINNING - SOT404 (D²PAK)

PIN	DESCRIPTION
1	gate
2	drain
3	source
mb	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	30	V
V_{DGR}	Drain-gate voltage	R_{GS} = 20 kΩ	-	30	V
$\pm V_{GS}$	Gate-source voltage	-	-	20	V
I_D	Drain current (DC)	T_{mb} = 25 ˚C	-	50	A
I_D	Drain current (DC)	T_{mb} = 100 ˚C	-	29	A
I_{DM}	Drain current (pulse peak value)	T_{mb} = 25 ˚C	-	200	A
P_{tot}	Total power dissipation	T_{mb} = 25 ˚C	-	94	W
T_{stg}, T_j	Storage & operating temperature	-	- 55	175	˚C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j\text{-}mb}$	Thermal resistance junction to mounting base	-	-	1.6	K/W
$R_{th\ j\text{-}a}$	Thermal resistance junction to ambient	pcb mounted, minimum footprint	50	-	K/W

ESD LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_C	Electrostatic discharge capacitor voltage, all pins	Human body model (100 pF, 1.5 kΩ)	-	2	kV

STATIC CHARACTERISTICS

T_j = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	V_{GS} = 0 V; I_D = 0.25 mA;	30	-	-	V
		T_j = -55˚C	27	-	-	V
$V_{GS(TO)}$	Gate threshold voltage	V_{DS} = V_{GS}; I_D = 1 mA	2.0	3.0	4.0	V
		T_j = 175˚C	1.0	-	-	V
		T_j = -55˚C	-	-	4.4	V
I_{DSS}	Zero gate voltage drain current	V_{DS} = 30 V; V_{GS} = 0 V;	-	0.05	10	µA
		T_j = 175˚C	-	-	500	µA
I_{GSS}	Gate source leakage current	V_{GS} = ±10 V; V_{DS} = 0 V	-	0.02	1	µA
		T_j = 175˚C	-	-	20	µA
$\pm V_{(BR)GSS}$	Gate source breakdown voltage	I_G = ±1 mA;	16	-	-	V
$R_{DS(ON)}$	Drain-source on-state resistance	V_{GS} = 10 V; I_D = 25 A	-	19	21	mΩ
		T_j = 175˚C	-	-	39	mΩ

DYNAMIC CHARACTERISTICS

T_j = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
g_{fs}	Forward transconductance	V_{DS} = 25 V; I_D = 25 A	6	19	-	S
$Q_{g(tot)}$	Total gate charge	I_D = 25 A; V_{DD} = 30 V; V_{GS} = 10 V	-	28	-	nC
Q_{gs}	Gate-source charge		-	7	-	nC
Q_{gd}	Gate-drain (Miller) charge		-	11	-	nC
C_{iss}	Input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz	-	974	-	pF
C_{oss}	Output capacitance		-	325	-	pF
C_{rss}	Feedback capacitance		-	152	-	pF
$t_{d\,on}$	Turn-on delay time	V_{DD} = 30 V; I_D = 25 A;	-	10	-	ns
t_r	Turn-on rise time	V_{GS} = 10 V; R_G = 10 Ω	-	45	-	ns
$t_{d\,off}$	Turn-off delay time	Resistive load	-	30	-	ns
t_f	Turn-off fall time		-	32	-	ns
L_d	Internal drain inductance	Measured from tab to centre of die	-	3.5	-	nH
L_d	Internal drain inductance	Measured from drain lead solder point to centre of die	-	4.5	-	nH
L_s	Internal source inductance	Measured from source lead solder point to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

T_j = 25˚C unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current		-	-	50	A
I_{DRM}	Pulsed reverse drain current		-	-	200	A
V_{SD}	Diode forward voltage	I_F = 25 A; V_{GS} = 0 V	-	0.95	1.2	V
		I_F = 50 A; V_{GS} = 0 V	-	1.0	-	
t_{rr}	Reverse recovery time	I_F = 25 A; -dI_F/dt = 100 A/µs;	-	100	-	ns
Q_{rr}	Reverse recovery charge	V_{GS} = -10 V; V_R = 25 V	-	0.4	-	µC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	I_D = 25 A; V_{DD} ≤ 25 V; V_{GS} = 10 V; R_{GS} = 50 Ω; T_{mb} = 25 ˚C	-	-	70	mJ

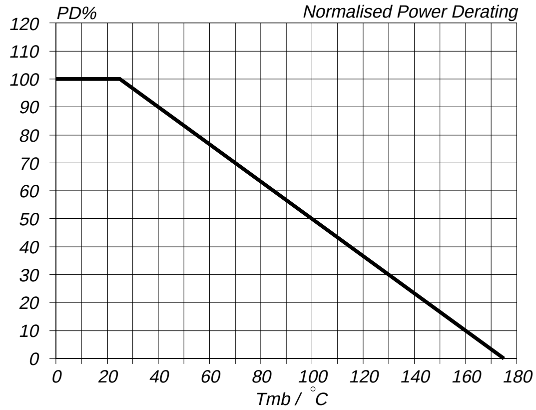


Fig.1. Normalised power dissipation.
$PD\% = 100 \cdot P_D/P_{D\ 25\ ˚C} = f(T_{mb})$

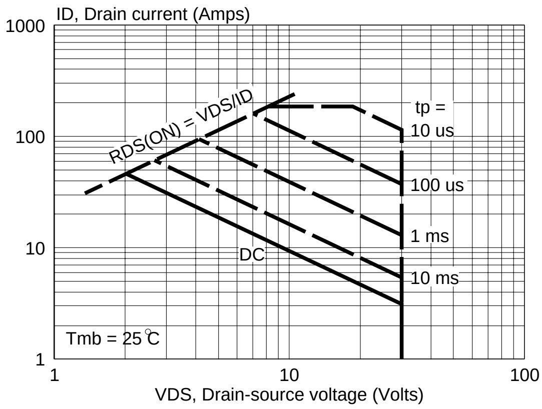


Fig.3. Safe operating area. T_{mb} = 25 ˚C
I_D & $I_{DM} = f(V_{DS})$; I_{DM} single pulse; parameter t_p

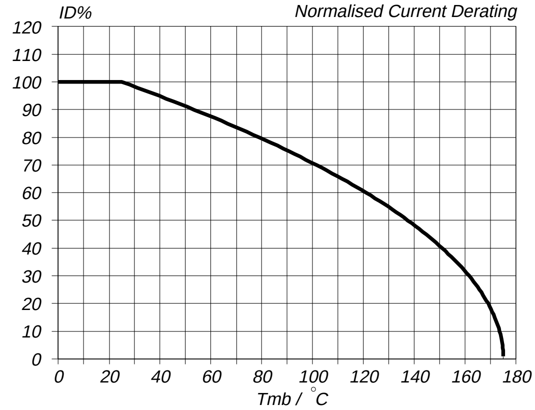


Fig.2. Normalised continuous drain current.
$ID\% = 100 \cdot I_D/I_{D\ 25\ ˚C} = f(T_{mb})$; conditions: $V_{GS} \geq 5$ V

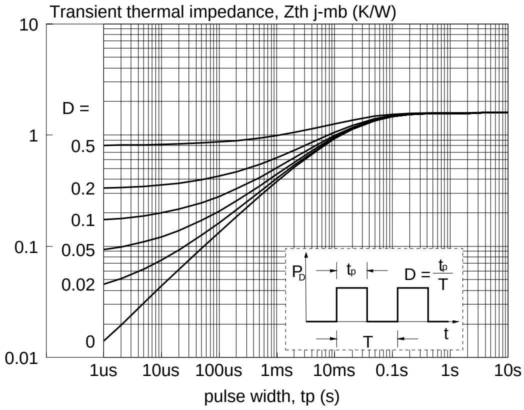


Fig.4. Transient thermal impedance.
$Z_{th\ j-mb} = f(t)$; parameter $D = t_p/T$

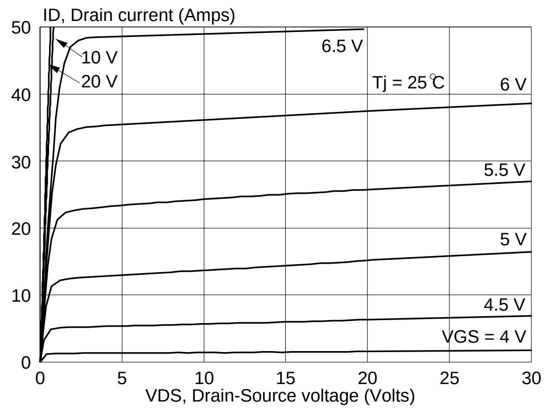


Fig.5. Typical output characteristics, T_j = 25 ˚C.
$I_D = f(V_{DS})$; parameter V_{GS}

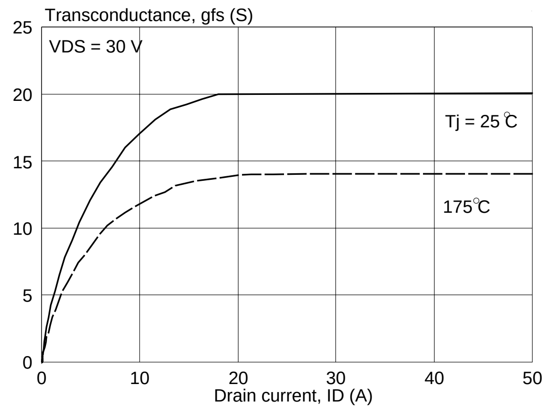


Fig.8. Typical transconductance, T_j = 25 ˚C.
$g_{fs} = f(I_D)$

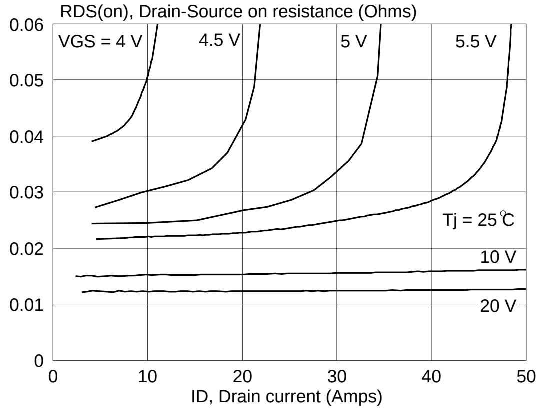


Fig.6. Typical on-state resistance, T_j = 25 ˚C.
$R_{DS(ON)} = f(I_D)$; parameter V_{GS}

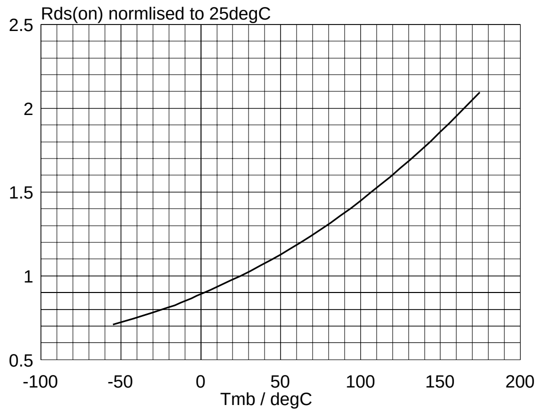


Fig.9. Normalised drain-source on-state resistance.
$a = R_{DS(ON)}/R_{DS(ON)25\ ^{\circ}C} = f(T_j)$; I_D = 25 A; V_{GS} = 5 V

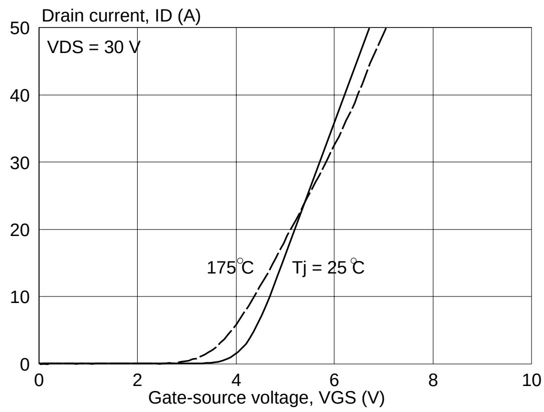


Fig.7. Typical transfer characteristics.
$I_D = f(V_{GS})$; parameter T_j

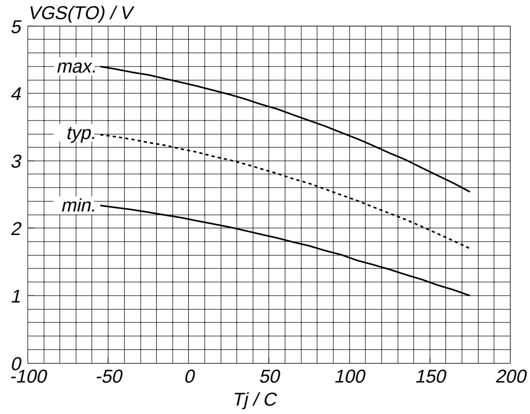


Fig.10. Gate threshold voltage.
$V_{GS(TO)} = f(T_j)$; conditions: I_D = 1 mA; $V_{DS} = V_{GS}$

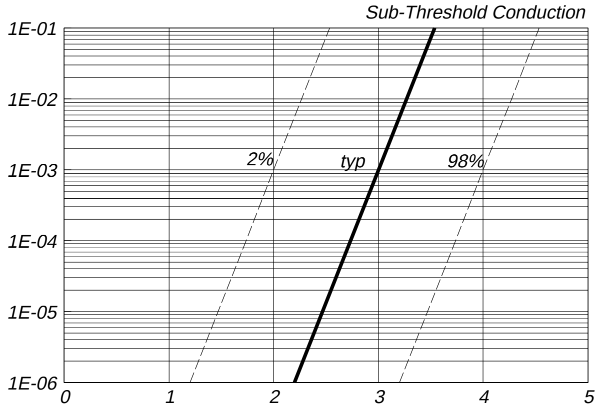


Fig.11. Sub-threshold drain current.
$I_D = f(V_{GS})$; conditions: $T_j = 25$ ˚C; $V_{DS} = V_{GS}$

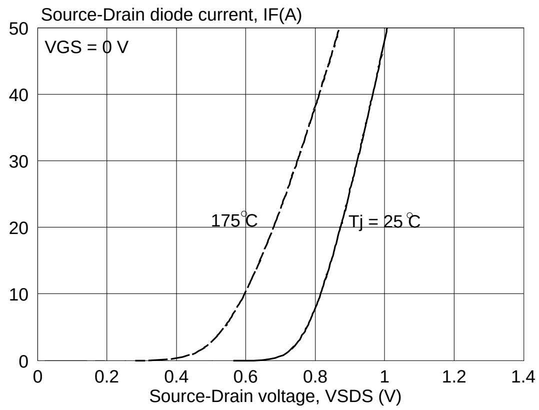


Fig.14. Typical reverse diode current.
$I_F = f(V_{SDS})$; parameter T_j

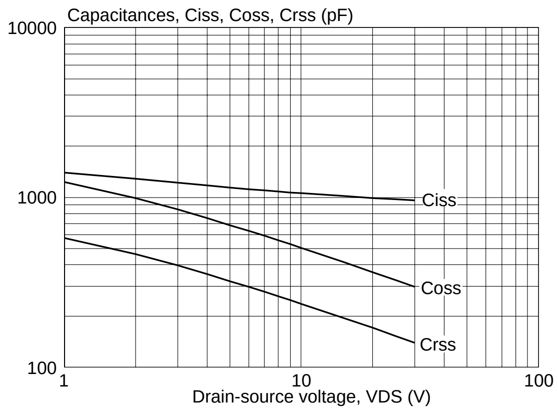


Fig.12. Typical capacitances, C_{iss}, C_{oss}, C_{rss}.
$C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; f = 1 MHz

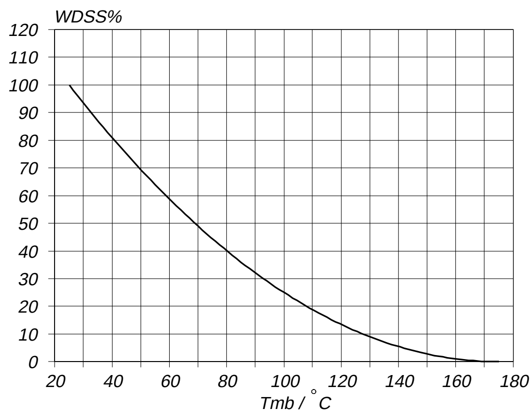


Fig.15. Normalised avalanche energy rating.
$W_{DSS}\% = f(T_{mb})$

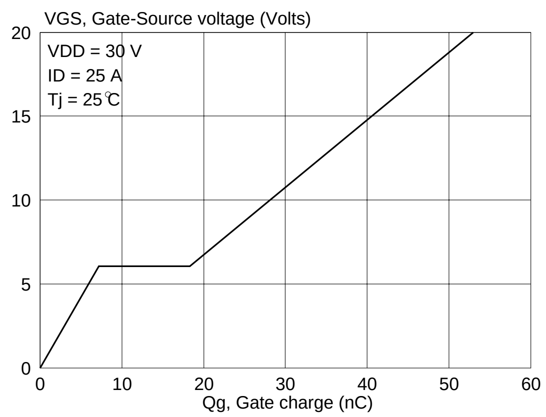


Fig.13. Typical turn-on gate-charge characteristics.
$V_{GS} = f(Q_G)$; parameter V_{DS}

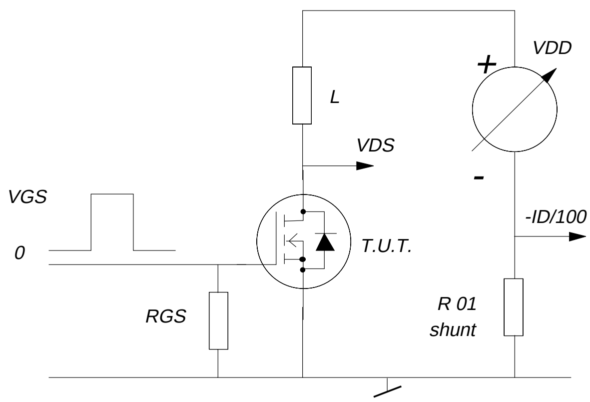
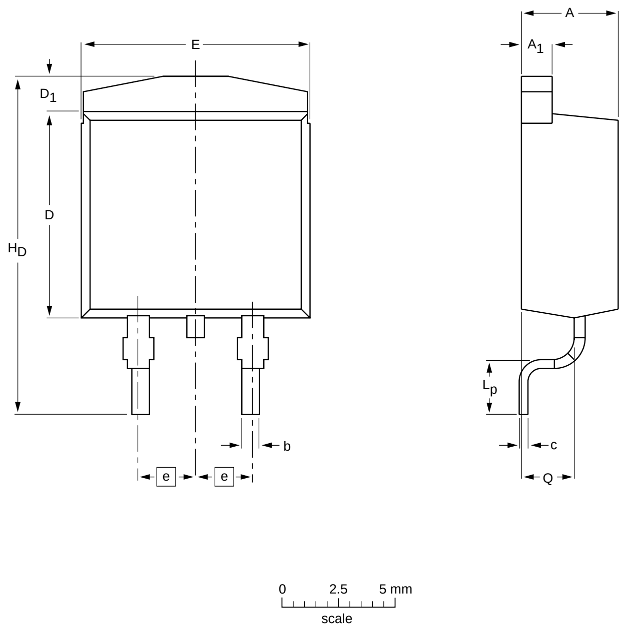


Fig.16. Avalanche energy test circuit.
$$W_{DSS} = 0.5 \cdot LI_D^2 \cdot BV_{DSS}/(BV_{DSS} - V_{DD})$$

MECHANICAL DATA

Plastic single-ended package (Philips version of D2-PAK); 2 leads **SOT404**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b	c	D	D_1	E	e	L_p	H_D	Q
mm	4.5 4.1	1.40 1.27	0.85 0.60	0.64 0.46	9.65 8.65	1.6 1.2	10.3 9.7	2.54	2.9 2.1	15.4 14.8	2.60 2.20

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT404						97-06-16

Fig.17. SOT404 surface mounting package. Centre pin connected to mounting base.

Notes

1. This product is supplied in anti-static packaging. The gate-source input must be protected against static discharge during transport or handling.
2. Refer to SMD Footprint Design and Soldering Guidelines, Data Handbook SC18.
3. Epoxy meets UL94 V0 at 1/8".

MOUNTING INSTRUCTIONS

Dimensions in mm

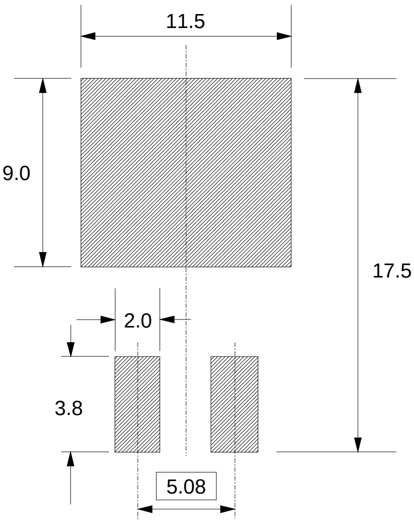


Fig.18. SOT404 : soldering pattern for surface mounting.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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