

TrenchMOS™ transistor

Standard level FET

BUK7606-55A

GENERAL DESCRIPTION

N-channel enhancement mode standard level field-effect power transistor in a plastic envelope suitable for surface mounting. Using 'trench' technology the device features very low on-state resistance. It is intended for use in automotive and general purpose switching applications.

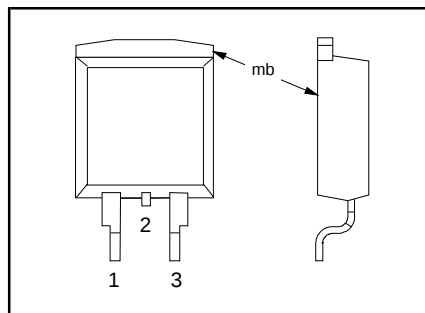
QUICK REFERENCE DATA

SYMBOL	PARAMETER	MAX.	UNIT
V_{DS}	Drain-source voltage	55	V
I_D	Drain current (DC)	75	A
P_{tot}	Total power dissipation	230	W
T_j	Junction temperature	175	°C
$R_{DS(ON)}$	Drain-source on-state resistance $V_{GS} = 10\text{ V}$	6.3	mΩ

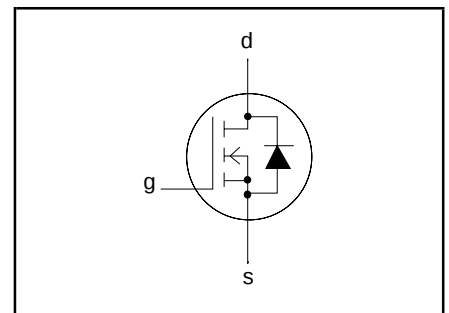
PINNING - SOT404

PIN	DESCRIPTION
1	gate
2	drain (no connection possible)
3	source
mb	drain

PIN CONFIGURATION



SYMBOL



LIMITING VALUES

Limiting values in accordance with the Absolute Maximum System (IEC 134)

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{DS}	Drain-source voltage	-	-	55	V
V_{DGR}	Drain-gate voltage	$R_{GS} = 20\text{ k}\Omega$	-	55	V
$\pm V_{GS}$	Gate-source voltage	-	-	20	V
I_D	Drain current (DC)	$T_{mb} = 25\text{ °C}$	-	75	A
I_D	Drain current (DC)	$T_{mb} = 100\text{ °C}$	-	75	A
I_{DM}	Drain current (pulse peak value)	$T_{mb} = 25\text{ °C}$	-	240	A
P_{tot}	Total power dissipation	$T_{mb} = 25\text{ °C}$	-	230	W
T_{stg}, T_j	Storage & operating temperature	-	- 55	175	°C

THERMAL RESISTANCES

SYMBOL	PARAMETER	CONDITIONS	TYP.	MAX.	UNIT
$R_{th\ j-mb}$	Thermal resistance junction to mounting base	-	-	0.65	K/W
$R_{th\ j-a}$	Thermal resistance junction to ambient	Minimum footprint, FR4 board	50	-	K/W

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STATIC CHARACTERISTICS

 $T_j = 25^\circ\text{C}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	Drain-source breakdown voltage	$V_{GS} = 0\text{ V}; I_D = 0.25\text{ mA}; T_j = -55^\circ\text{C}$	55 50	- -	- -	V V
$V_{GS(TO)}$	Gate threshold voltage	$V_{DS} = V_{GS}; I_D = 1\text{ mA}$	2	3.0	4.0	V
		$T_j = 175^\circ\text{C}$	1	-	-	V
		$T_j = -55^\circ\text{C}$	-	-	4.4	V
I_{DSS}	Zero gate voltage drain current	$V_{DS} = 55\text{ V}; V_{GS} = 0\text{ V}; T_j = 175^\circ\text{C}$	-	0.05	10	μA
I_{GSS}	Gate source leakage current	$V_{GS} = \pm 20\text{ V}; V_{DS} = 0\text{ V}$	-	2	100	nA
$R_{DS(ON)}$	Drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 25\text{ A}; T_j = 175^\circ\text{C}$	-	5.3	6.3	m Ω
			-	-	13.2	m Ω

DYNAMIC CHARACTERISTICS

 $T_{mb} = 25^\circ\text{C}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{iss}	Input capacitance	$V_{GS} = 0\text{ V}; V_{DS} = 25\text{ V}; f = 1\text{ MHz}$	-	4500	6000	pF
C_{oss}	Output capacitance		-	1000	1200	pF
C_{rss}	Feedback capacitance		-	620	820	pF
$t_{d\text{ on}}$	Turn-on delay time	$V_{DD} = 30\text{ V}; R_{load} = 1.2\Omega;$	-	35	55	ns
t_r	Turn-on rise time	$V_{GS} = 10\text{ V}; R_G = 10\Omega$	-	115	175	ns
$t_{d\text{ off}}$	Turn-off delay time		-	155	230	ns
t_f	Turn-off fall time		-	110	155	ns
L_d	Internal drain inductance	Measured from upper edge of drain tab to centre of die	-	2.5	-	nH
L_s	Internal source inductance	Measured from source lead soldering point to source bond pad	-	7.5	-	nH

REVERSE DIODE LIMITING VALUES AND CHARACTERISTICS

 $T_j = 25^\circ\text{C}$ unless otherwise specified

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
I_{DR}	Continuous reverse drain current		-	-	75	A
I_{DRM}	Pulsed reverse drain current		-	-	240	A
V_{SD}	Diode forward voltage	$I_F = 25\text{ A}; V_{GS} = 0\text{ V}$	-	0.85	1.2	V
		$I_F = 75\text{ A}; V_{GS} = 0\text{ V}$	-	1.1	-	V
t_{rr}	Reverse recovery time	$I_F = 75\text{ A}; -dI_F/dt = 100\text{ A}/\mu\text{s};$	-	80	-	ns
Q_{rr}	Reverse recovery charge	$V_{GS} = -10\text{ V}; V_R = 30\text{ V}$	-	0.2	-	μC

AVALANCHE LIMITING VALUE

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
W_{DSS}	Drain-source non-repetitive unclamped inductive turn-off energy	$I_D = 75\text{ A}; V_{DD} \leq 25\text{ V};$ $V_{GS} = 10\text{ V}; R_{GS} = 50\Omega; T_{mb} = 25^\circ\text{C}$	-	-	500	mJ

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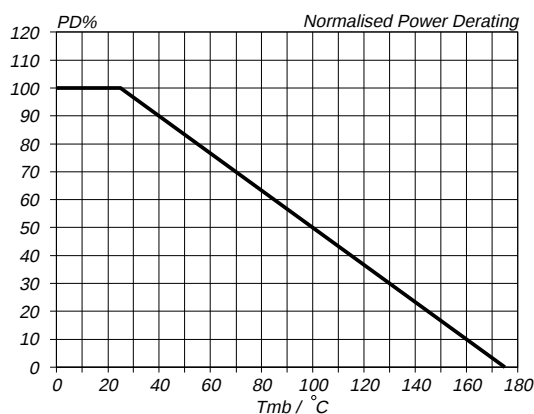


Fig.1. Normalised power dissipation.
 $PD\% = 100 \cdot P_D / P_{D, 25^\circ\text{C}} = f(T_{mb})$

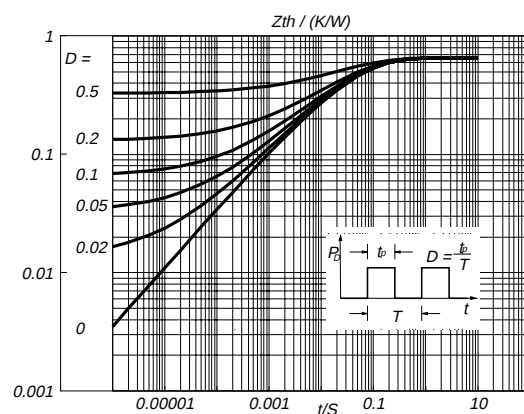


Fig.4. Transient thermal impedance.
 $Z_{th\ j-mb} = f(t)$; parameter $D = t_p / T$

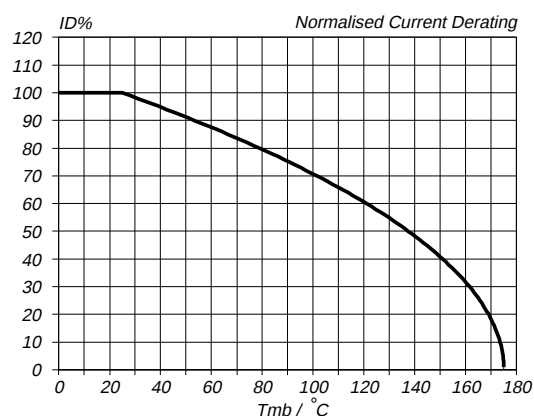


Fig.2. Normalised continuous drain current.
 $ID\% = 100 \cdot I_D / I_{D, 25^\circ\text{C}} = f(T_{mb})$; conditions: $V_{GS} \geq 5\text{ V}$

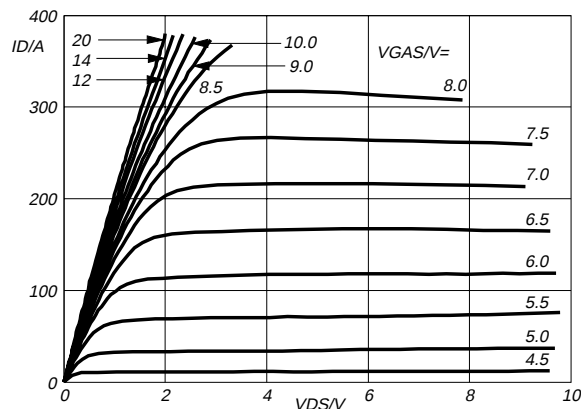


Fig.5. Typical output characteristics, $T_j = 25^\circ\text{C}$.
 $I_D = f(V_{DS})$; parameter V_{GS}

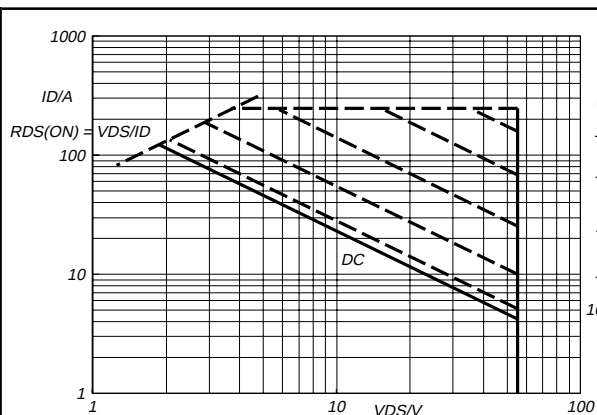


Fig.3. Safe operating area. $T_{mb} = 25^\circ\text{C}$
 I_D & $I_{DM} = f(V_{DS})$; I_{DM} single pulse; parameter t_p

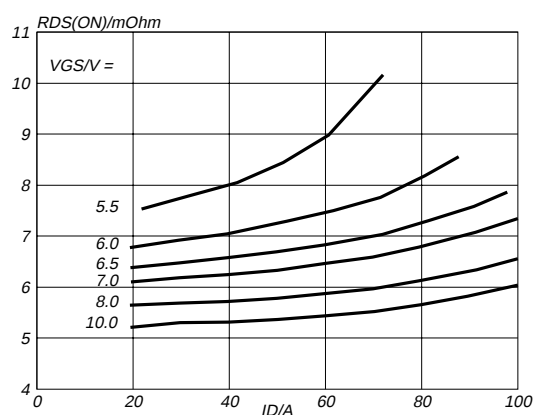


Fig.6. Typical on-state resistance, $T_j = 25^\circ\text{C}$.
 $R_{DS(ON)} = f(I_D)$; parameter V_{GS}

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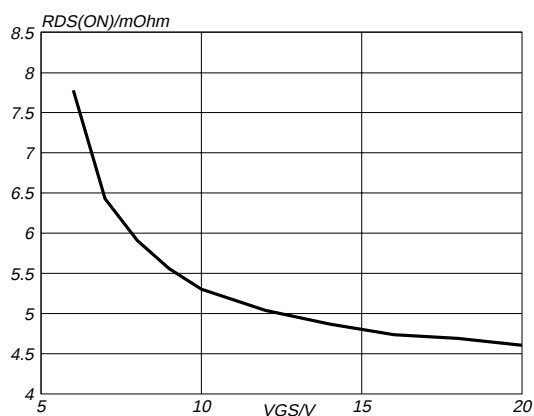


Fig.7. Typical on-state resistance, $T_j = 25\text{ °C}$.
 $R_{DS(ON)} = f(V_{GS})$; conditions $I_D = 25\text{ A}$;

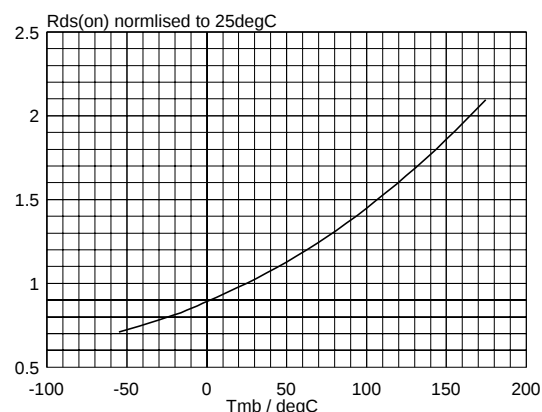


Fig.10. Normalised drain-source on-state resistance.
 $a = R_{DS(ON)}/R_{DS(ON)25\text{ °C}} = f(T_j)$; $I_D = 25\text{ A}$; $V_{GS} = 5\text{ V}$

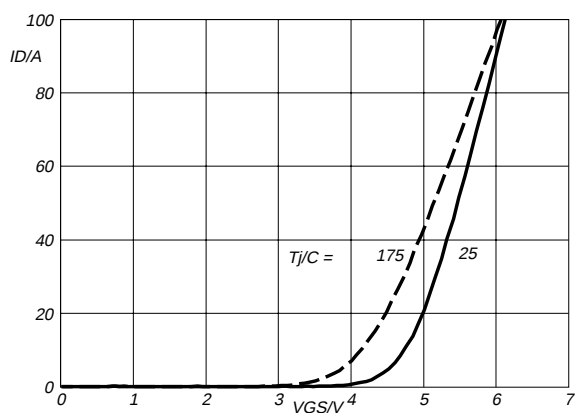


Fig.8. Typical transfer characteristics.
 $I_D = f(V_{GS})$; conditions: $V_{DS} = 25\text{ V}$; parameter T_j

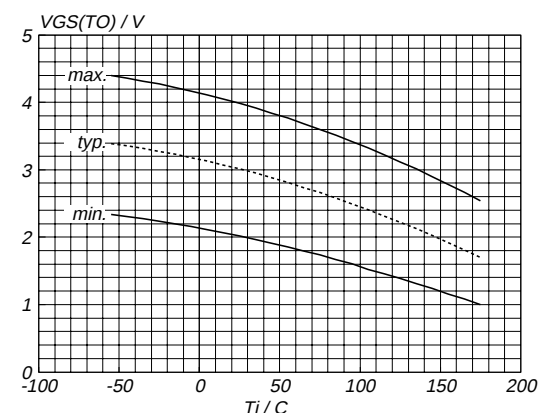


Fig.11. Gate threshold voltage.
 $V_{GS(T0)} = f(T_j)$; conditions: $I_D = 1\text{ mA}$; $V_{DS} = V_{GS}$

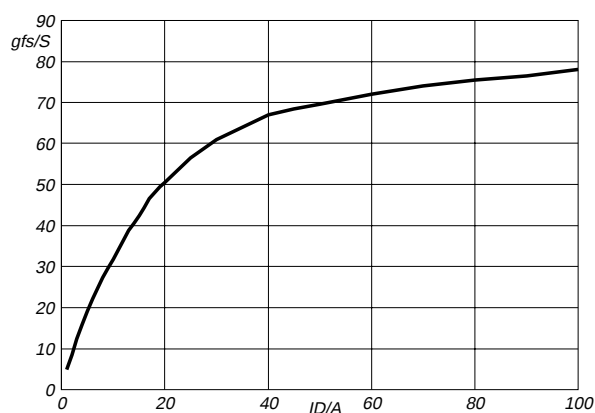


Fig.9. Typical transconductance, $T_j = 25\text{ °C}$.
 $g_{fs} = f(I_D)$; conditions: $V_{DS} = 25\text{ V}$

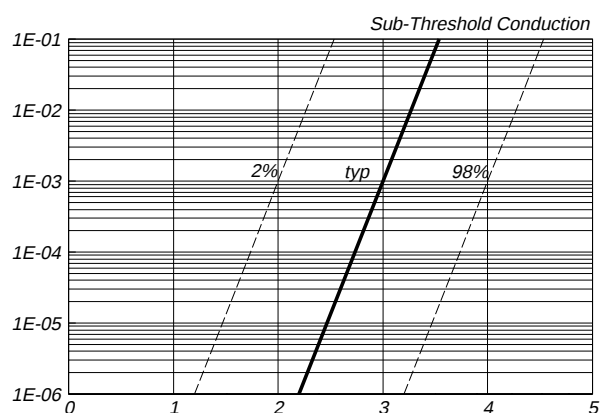


Fig.12. Sub-threshold drain current.
 $I_D = f(V_{GS})$; conditions: $T_j = 25\text{ °C}$; $V_{DS} = V_{GS}$

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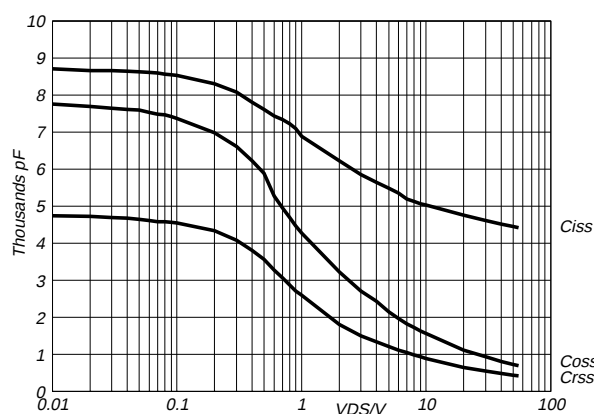


Fig.13. Typical capacitances, C_{iss} , C_{oss} , C_{rss} .
 $C = f(V_{DS})$; conditions: $V_{GS} = 0$ V; $f = 1$ MHz

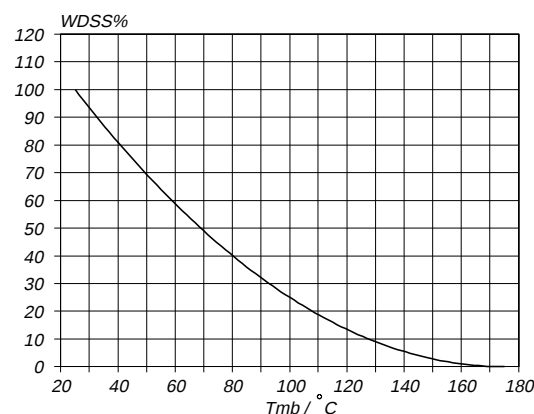


Fig.16. Normalised avalanche energy rating.
 $W_{DSS}\% = f(T_{mb})$; conditions: $I_D = 75$ A

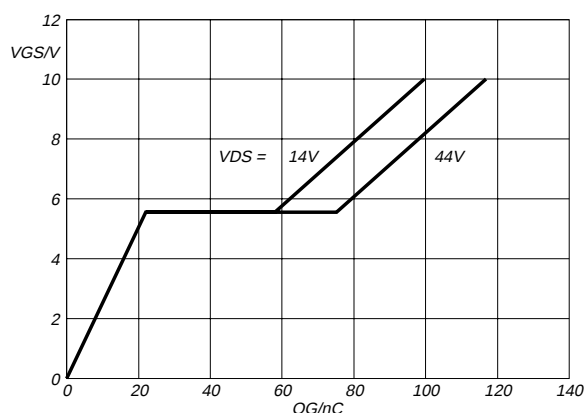


Fig.14. Typical turn-on gate-charge characteristics.
 $V_{GS} = f(Q_G)$; conditions: $I_D = 50$ A; parameter V_{DS}

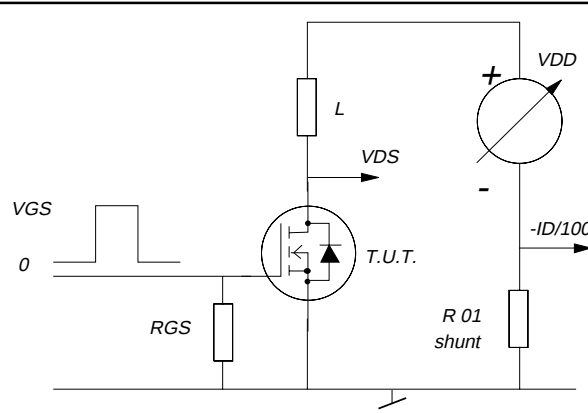


Fig.17. Avalanche energy test circuit.
 $W_{DSS} = 0.5 \cdot L I_D^2 \cdot BV_{DSS}' / (BV_{DSS}' - V_{DD})$

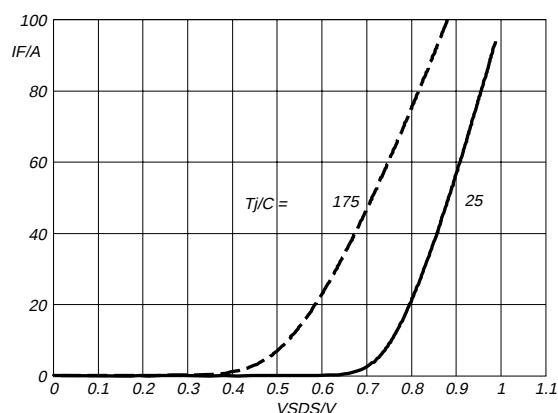


Fig.15. Typical reverse diode current.
 $I_F = f(V_{SDS})$; conditions: $V_{GS} = 0$ V; parameter T_j

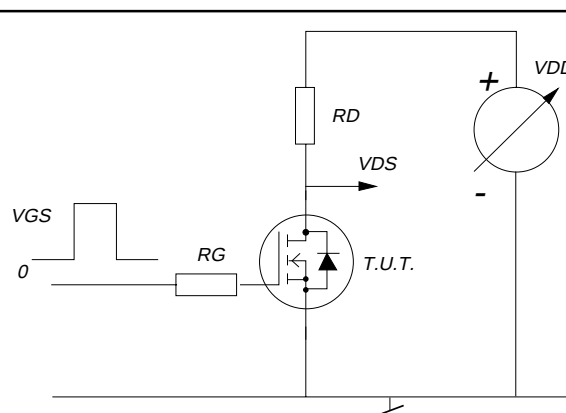
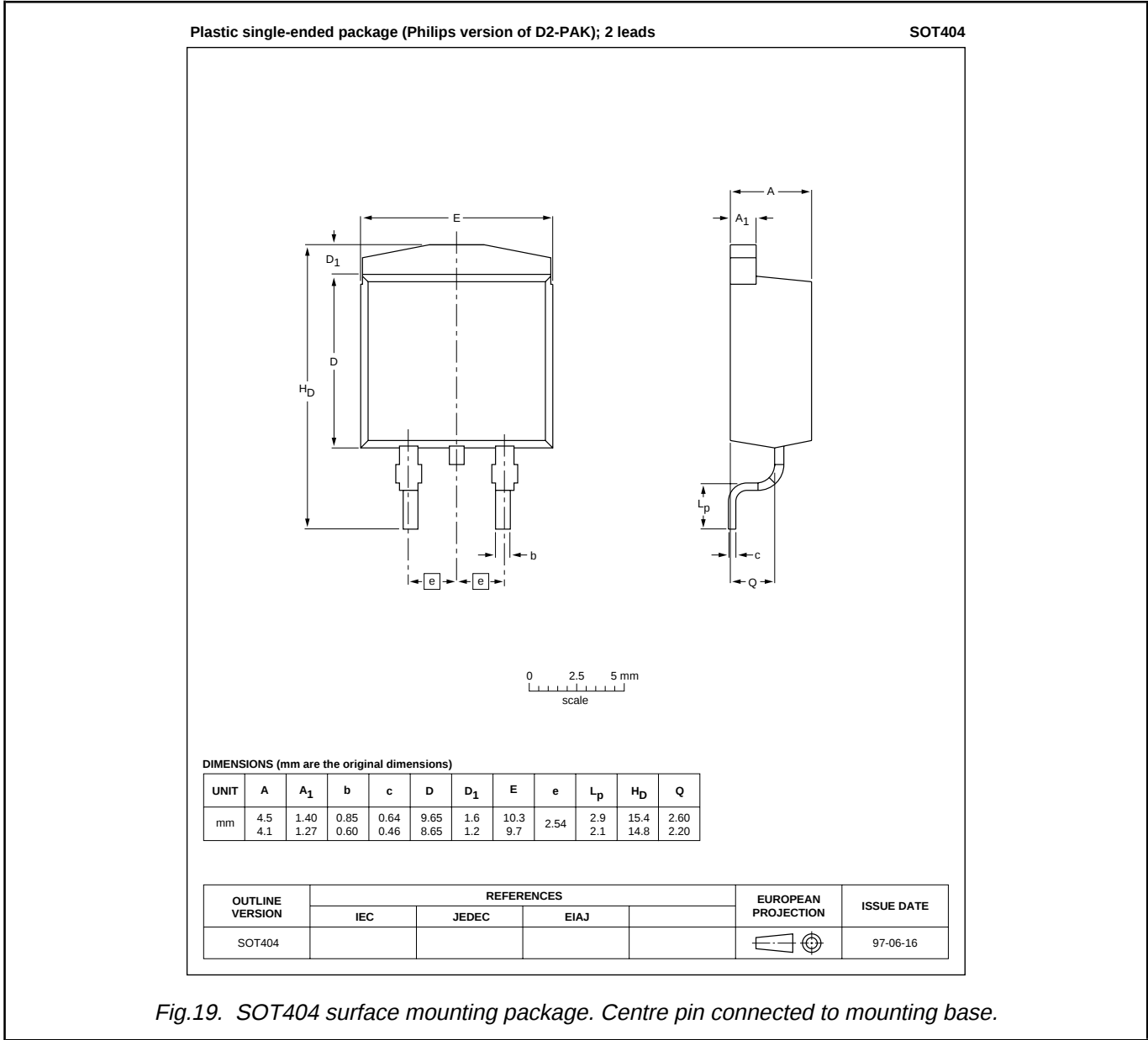


Fig.18. Switching test circuit.

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MECHANICAL DATA



Notes

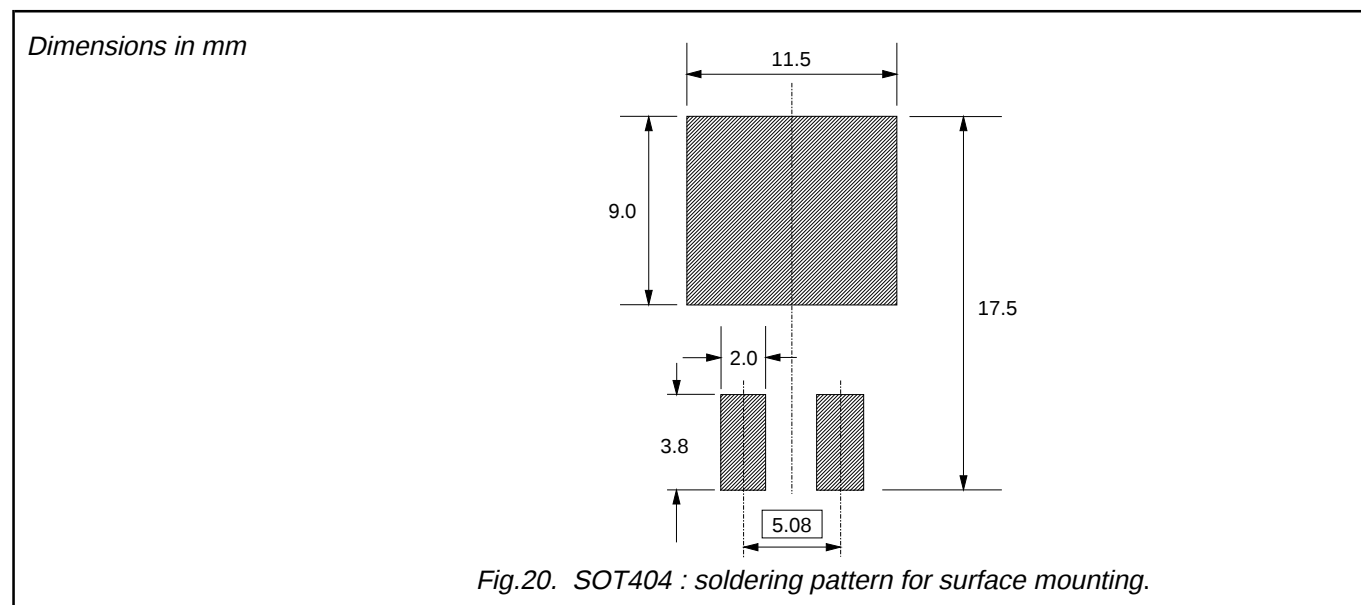
- 1. This product is supplied in anti-static packaging. The gate-source input must be protected against static discharge during transport or handling.
- 2. Refer to SMD Footprint Design and Soldering Guidelines, Data Handbook SC18.
- 3. Epoxy meets UL94 V0 at 1/8".

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MOUNTING INSTRUCTIONS



DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values are given in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of this specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	
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