Audio Digital Delay (KARAOKE Echo) BU9252S/BU9252F

The BU9252S and BU9252F are digital delays specifically for KARAOKE systems. Each has an internal sample hold circuit, an 8-bit A/D and D/A converter and 2KB SRAM, and allows for the selection of one of eight delay times just by attaching an inexpensive ceramic resonator.

A digital echo system can be formed by using either of these ICs together with the BA7725S or BA7725FS.

Applications

KARAOKE echo system

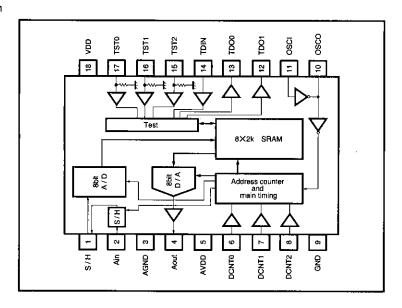
Electronic circuits that require signal delays

Features

- 1) Internal digital delay circuit.
- Internal 8-bit A/D converter (sample rate = 14.22kHz when fosc = 455kHz).
- 3) Internal 2 K bytes data SRAM.

- 4) Internal 8-bit D/A converter.
- 5) CMOS design for low power consumption.
- Internal sample hold circuit.
- Internal feedback resistors and capacitors for oscillator circuits.

Block diagram



●Pin descriptions

Pin No.	Name	Function	Pin No.	Pin name	Function
1	S/H	For attaching sample-and-hold capacitor	10	osco	Oscillator pin 2
2	Ain	Analog input	11	OSCI	Oscillator pin 1
3	AGND	Analog circuit ground	12	TDO1	Test pin (output)
4	Aout	Analog output	13	TDO0	Test pin (output)
5	AVDD	Analog circuit power supply	14	TDIN	Test pin (input)
6	DCNT0	Delay setting input	15	TST2	Test mode setting
7	DCNT1	Delay setting input	16	TST1	Test mode setting
8	DCNT2	Delay setting input	17	TST0	Test mode setting
9	GND	Digital circuit ground	18	VDD	Digital circuit power supply

●Input/output circuits

BU9252S	/ F					
Name	Pin	Internal equivalent circuit	Name	Pin	Internal equivalent circuit	
S/H	1				т.	
Ain	2 OSCI OSCO	11 10				
TDIN DCNT0 DCNT1 DCNT2	14 6 7 8					
TDO0 TDO1	13 12		Aout	4	D/A	
TST0 TST1 TST2	17 16 15				Bulli-in 0.875x amplifier as output buffer.	

●Absolute maximum ratings (Ta=25℃)

	Parameter	Symbol	Limits	Unit	
Power supp	Power supply voltage		-0.3~7.0	V	
Power	BU9252S	D.I	600 * 1		
dissipation	BU9252F	Pd	450* ²	mW	
Storage tem	Storage temperature		−55 ~125	Ç	
Input voltage		Vin	-0.3~V _{DD} +0.3	٧	
Output voltage		Vouт	-0.3~VDD+0.3	V	

^{* 1} IC only. Reduce by $\sim\!\!6$ mW/ $^{\circ}\!C$ for each degree above 25 $^{\circ}\!C$.

Recommended operating conditions

Parameter	Symbol	Limits	Unit
Power supply voltage	Voo	4.5~5.5	V
Analog power supply voltage	AVDD	V _{DD}	V
Input "L" voltage	VIL	0.0~0.2Vpp	V
Input "H" voltage	ViH	0.8Vpp~Vpp	V
Analog input voltage	Vain	0~AVDD	V
Clock frequency	fosc	200~1000	kHz
Operating temperature	Topr	−10~70	ç

●Electrical characteristics (unless otherwise noted, Ta=25°C, VDD=AVDD=5V)

Parameter	Symbol	Min.	Тур.	Max.	Unit	Conditions
Circuit current	loo	_	3.5	12	mA	Vain=AVDD, fosc=455kHz
Anatas autorit arment	laout	1	4	_	mA	VAOUT=1V, VAIN=0V
Analog output current		0.3	0.8		mA	VAOUT=0.5VDD, VAIN=VDD
Analog input impedance	RAIN	12	25	60	kΩ	*
A/D to D/A precision	RES		2	_	L\$B	
OSCO output "L" voltage	VLosc	_	0.6	1.2	V	IoL=100 μ A
OSCO output "H" voltage	VHOSC	3.8	4.4		٧	loκ=-100 μ A
OSCI feedback loop current	losci	1	6	20	μΑ	Vosci=VDD
Oscillation capacity		_	150	_	PF	

^{*} The bias circuit is impedance.

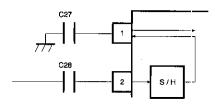
Circuit operation

· External capacitor for signal input pin

Audio signals compressed by the BA7725S or BA7725FS have their DC component removed by an AC coupling capacitor and are then input to pin 2 of BU9252S or BU9252F. At this stage, level deviations occur because the input signal is capacitor-divided by this AC coupling capacitor C28 and by sampling hold capacitor C27 connected to pin 1.

To prevent this, make sure that C27 is much lower than C28.

(Note: The numbers of external components are the numbers used in the system application example.)



The sample-held analog signal is converted to digital by the serial 8-bit A/D converter and then temporarily stored in the internal SRAM (2K bytes).

• Relationship between oscillation frequency (CLK) and delay time

Sample rate F = fosc/32 (fosc : oscillation frequency)

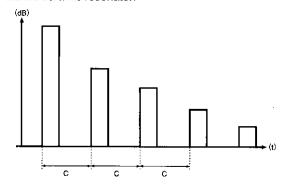
F = 14.22kHz at fosc = 455kHz)

Sample period T = 1/F

Delay time $Dtime = T \times number of counts$

· Delay timer settings

The delay time (i.e., the length of time the signal is stored in the SRAM) can be set to any of eight settings between the maximum and minimum delay times by setting pins 6, 7 and 8 to the combination of logic signal inputs that results in the corresponding number of counts. The maximum and minimum delay times are determined by the oscillation frequency of the attached ceramic resonator.



C: Delay time (ms)

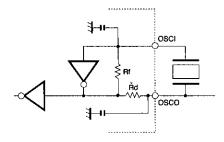
The delay time can be set to any of the eight settings shown below by setting the logic inputs of terminals DCNT0 through DCNT2.

	Logic input		Count	Delay time (ms) (when fosc=455kHz)		
DCNT1	DCNT2	DCNT0	BU9252S / F	BU9252\$ / F		
0	0	0	256	18.00		
0	0	1	512	36.01		
0	1	0	768	54.01		
0	1	1	1024	72.02		
1	0	0	1280	90.02		
1	0	1	1536	108.03		
1	1	0	1792	126.03		
1	1	1	2048	144.04		

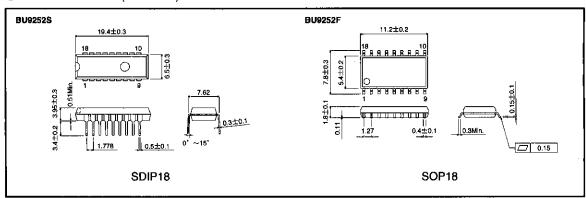
Maximum and minimum delay times when using 300kHz, 375kHz and 455kHz ceramic oscillators

Delay time (ms)							
300	kHz	375	kHz	455kHz			
Max.	Max. Min.		Min.	Max.	Min.		
218.45	218.45 27.30		174.76 21.85		18.00		

Peripheral components of the ceramic oscillator
 An oscillator circuit can be configured simply by attaching a 455kHz ceramic resonator.



●External dimensions (Units: mm)



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