Quad D latch

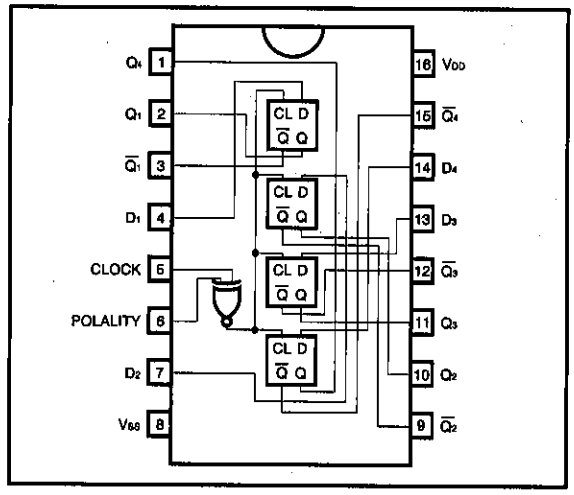
BU4042B

The BU4042B is a four-circuit D latch with a common clock line and separate data input terminals.
When the polarity input is set to "H", input (D) is presented to output (Q) as is, as long as the clock input is rising, and when the clock input falls, output (Q) holds input (D) at that point. While the clock input is falling, output (Q) does not change even if input (D) changes.
Also, if the polarity input is set to "L", input (D) is presented to output (Q) as is, as long as the clock input is at "L" level, and when the clock input goes to "H" level, latching takes place.

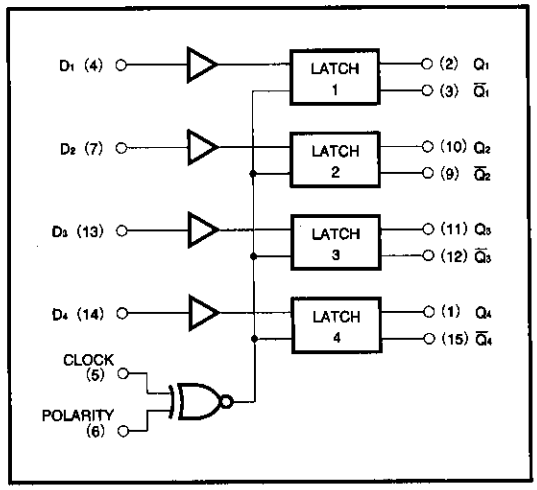
●Features

1) Low power consumption.
2) Wide range of operating power supply voltages.
3) High input impedance.
4) High fan-out.
5) Direct drive of 2 L-TTL inputs and 1 LS-TTL input.

●Block diagram



●Logic diagram



●Truth table

CLOCK	POLARITY	Q
L	L	D
H	L	LATCH
H	H	D
L	H	LATCH

●Absolute maximum ratings (Ta=25℃)

Parameter	Symbol	Limits	Unit
Power supply voltage	V_{DD}	−0.3~18	V
Power dissipation	Pd	1000 (DIP)	mW
Operating temperature	Topr	−40~85	℃
Storage temperature	Tstg	−55~150	℃
Input voltage	V_{IN}	−0.3~V_{DD}+0.3	V

●Electrical characteristics

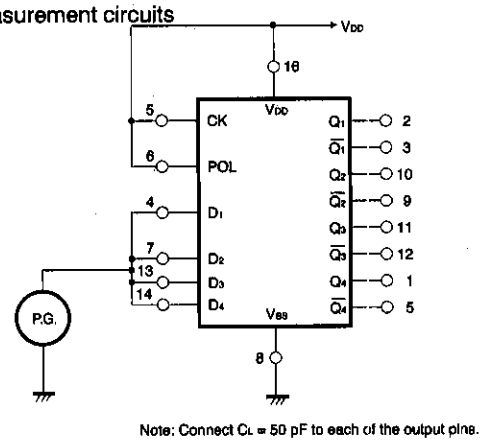
DC characteristics (unless otherwise noted, Ta=25℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit	V_{DD} (V)	Conditions
"H" input voltage (DATA)	V_{IH}	3.5	—	—	V	5	—
		7.0	—	—		10	
		11.0	—	—		15	
"H" input voltage (CLOCK POLARITY)	V_{IH}	3.5	—	—	V	5	—
		7.0	—	—		10	
		11.25	—	—		15	
"L" input voltage (DATA)	V_{IL}	—	—	1.5	V	5	—
		—	—	3.0		10	
		—	—	4.0		15	
"L" input voltage (CLOCK POLARITY)	V_{IL}	—	—	1.5	V	5	—
		—	—	3.0		10	
		—	—	3.75		15	
"H" input current	I_{IH}	—	—	0.3	μA	15	V_{IH}=15V
"L" input current	I_{IL}	—	—	−0.3	μA	15	V_{IL}=0V
"H" output voltage	V_{OH}	4.95	—	—	V	5	I_O=0mA
		9.95	—	—		10	
		14.95	—	—		15	
"L" output voltage	V_{OL}	—	—	0.05	V	5	I_O=0mA
		—	—	0.05		10	
		—	—	0.05		15	
"H" output current	I_{OH}	−0.16	—	—	mA	5	V_{OH}=4.6V
		−0.4	—	—		10	V_{OH}=9.5V
		−1.2	—	—		15	V_{OH}=13.5V
"L" output current	I_{OL}	0.44	—	—	mA	5	V_{OL}=0.4V
		1.1	—	—		10	V_{OL}=0.5V
		3.0	—	—		15	V_{OL}=1.5V
Quiescent supply current	I_{DD}	—	—	4.0	μA	5	V_I=V_{DD} or GND
		—	—	8.0		10	
		—	—	16.0		15	

Switching characteristics (unless otherwise noted, Ta=25℃, C_L=50pF)

Parameter	Symbol	Min.	Typ.	Max.	Unit	V_{DD} (V)	Conditions	Measurement Circuit
Output rise time	t_{TLH}	—	180	—	ns	5	—	Fig.1
		—	90	—		10		
		—	65	—		15		
Output fall time	t_{THL}	—	100	—	ns	5	—	Fig.1
		—	50	—		10		
		—	40	—		15		
Propagation delay time D→Q, $\overline{Q}$	t_{PLH} t_{PHL}	—	220	—	ns	5	—	Fig.1
		—	90	—		10		
		—	70	—		15		
Propagation delay time CLOCK→Q, $\overline{Q}$	t_{PLH} t_{PHL}	—	220	—	ns	5	—	Fig.2
		—	90	—		10		
		—	70	—		15		
Minimum clock pulse width	t_{WH} t_{WL}	—	150	—	ns	5	—	Fig.2
		—	50	—		10		
		—	40	—		15		
Hold time	t_H	—	50	—	ns	5	—	Fig.2
		—	25	—		10		
		—	20	—		15		
Setup time	t_{SU}	—	50	—	ns	5	—	Fig.2
		—	20	—		10		
		—	5	—		15		
Input capacitance	C_{IN}	—	5	—	pF	—	—	—

●Measurement circuits



Note: Connect C_L = 50 pF to each of the output pins.

Fig. 1 (a) Switching characteristics measurement circuit 1

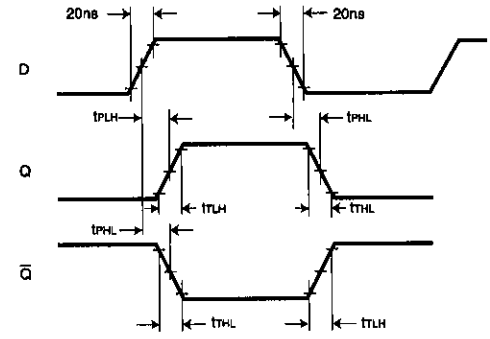
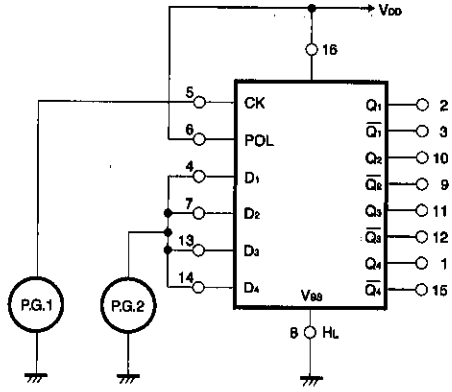


Fig. 1 (b) Switching time measurement waveform 1

●Measurement circuits



Note: Connect C_L = 50 pF to each of the output pins.

Fig. 2 (a) Switching characteristics measurement circuit 2

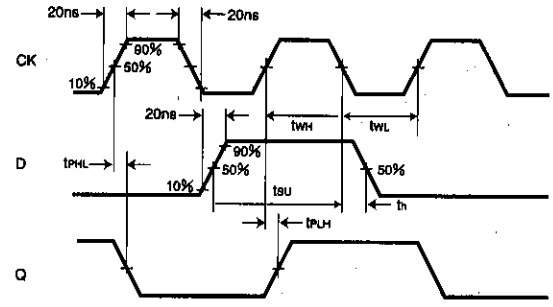


Fig. 2 (b) Switching time measurement waveform 2

●Electrical characteristic curve

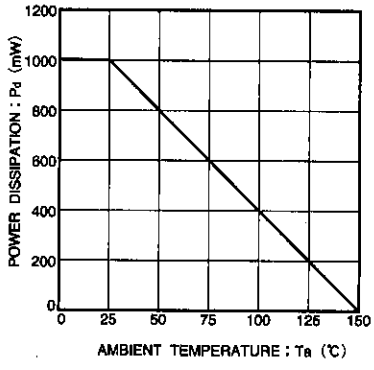
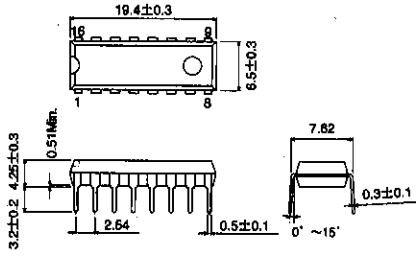


Fig.3 Power dissipation - Ta characteristic

●External dimensions (Units: mm)



DIP16

Series Standard
BU4000B

The BU4000 Series are CMOS ICs featuring low voltage and low power consumption. The wide range of operating power supply voltages is compatible with the general-purpose 4000B Series, and when a 5V power supply voltage is used, the LS-TTL IC can be driven directly.
These ICs are available in SOP and SSOP packages as well as the standard DIP package.

●Features

1) Low power consumption.
2) Wide range of operating power supply voltages.
3) High input impedance.
4) High fan-out.
5) Direct drive of 2 L-TTL inputs and 1 LS-TTL input.

●Absolute maximum ratings (Ta = 25℃)

Parameter	Symbol	Limits	Unit
Power supply voltage	V_{DD}	18 *1	V
Input voltage	V_{IN}	−0.3~V_{DD}+0.3	V
Power dissipation *2	Pd	Please refer to specifications for individual package	mW
Storage temperature	Tstg	−55~150	℃

*1 For the BU4XXXBC type, V_{DD} = 20 V.
*2 The values for the SOP and SSOP packages are the values when mounted on a glass epoxy PCB (50 mm x 50 mm x 1.6 mm).

●Recommended operating conditions (Ta = 25℃)

Parameter	Symbol	Limits	Unit
Power supply voltage	V_{DD}	3~16 *	V
Input voltage	V_{IN}	0~V_{DD}	V
Operating temperature	Topr	−40~85	℃

* For the BU4XXXBC type, V_{DD} = 3 to 18 V.

●Electrical characteristic curves

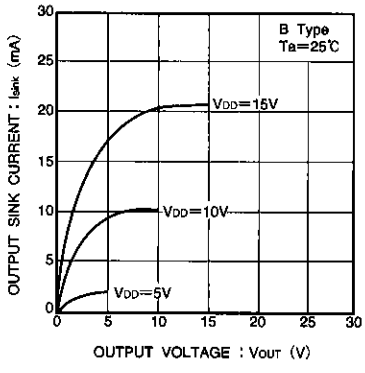


Fig.1 Output sink current - output voltage characteristic

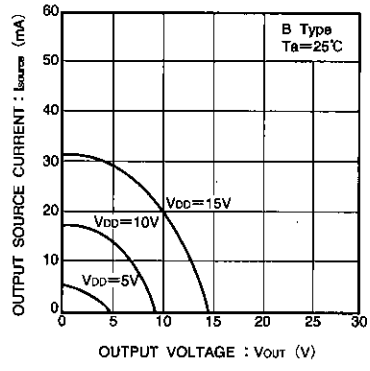


Fig.2 Output source current - output voltage characteristic

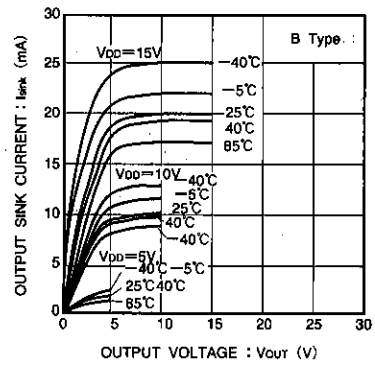


Fig.3 Output SINK current - output voltage characteristic

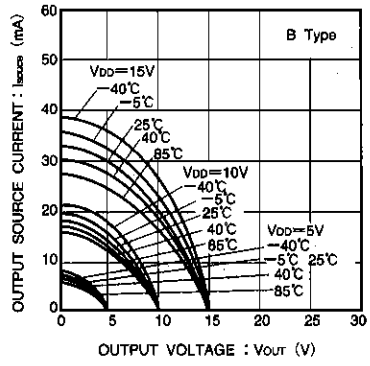


Fig.4 Output source current - output voltage characteristic

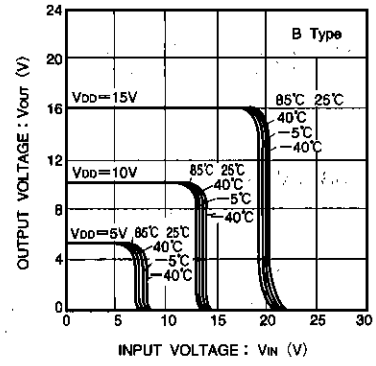


Fig.5 Output voltage - input voltage characteristic

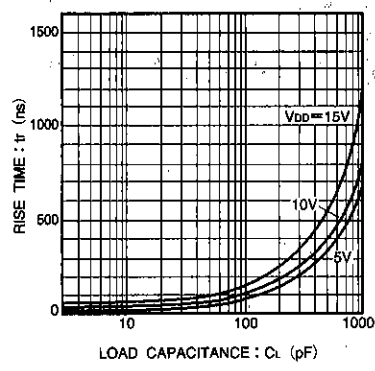


Fig.6 Rise time - load capacitance characteristic

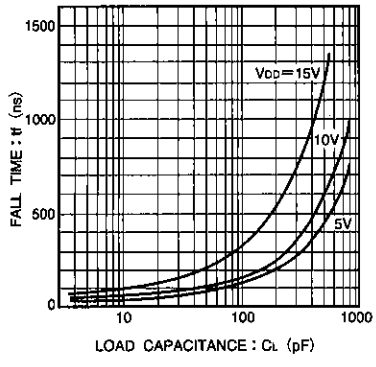


Fig.7 Fall time - load capacitance characteristic

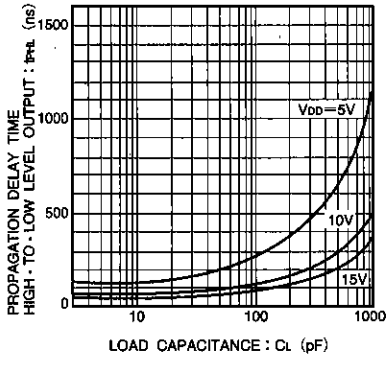


Fig.8 "H" to "L" propagation delay time - load capacitance characteristic

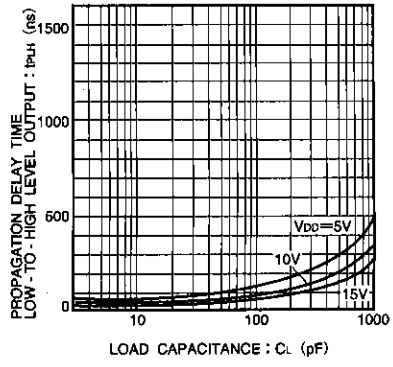


Fig.9 "L" to "H" propagation delay time - load capacitance characteristic

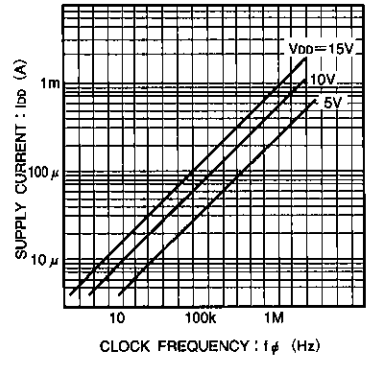


Fig.10 Supply current - clock frequency characteristic

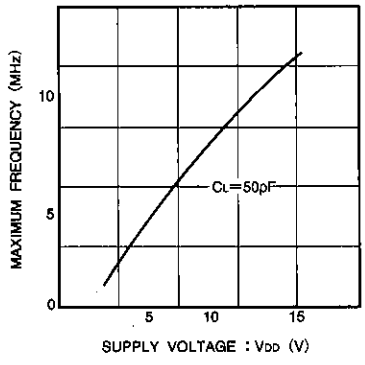


Fig.11 Maximum clock frequency - power supply voltage characteristic

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