DATA SHEET

BLV958; BLV958FL
UHF power transistors

Product specification
Supersedes data of 2000 Jan 12

2000 Nov 02

Philips
Semiconductors

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UHF power transistors BLV958; BLV958FL

FEATURES

- Internal input and output matching for easy matching, high gain and efficiency
- Poly-silicon emitter ballasting resistors for an optimum temperature profile
- Gold metallization ensures excellent reliability.

DESCRIPTION

NPN silicon planar epitaxial transistors primarily intended for common emitter class-AB operation. The transistors have internal input and output matching by means of MOS capacitors. The encapsulations are a 2-lead rectangular SOT391A flange package and a SOT391B flangeless package, both with a ceramic cap.

APPLICATIONS

- Base stations in the 800 to 960 MHz frequency range.

PINNING - SOT391A

PIN	SYMBOL	DESCRIPTION
1	c	collector
2	b	base
3	e	emitter; connected to flange

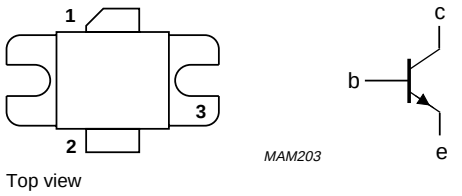


Fig.1 Simplified outline (SOT391A) and symbol.

PINNING - SOT391B

PIN	SYMBOL	DESCRIPTION
1	c	collector
2	b	base
Ground plane	e	emitter

Fig.2 Simplified outline (SOT391B) and symbol.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a common emitter test circuit.

MODE OF OPERATION	f (MHz)	V_{CE} (V)	P_L (W)	G_p (dB)	η_C (%)
CW, class-AB	900	26	75	≥8	≥50
	960	26	75	≥8.5	≥50

WARNING

Product and environmental safety - toxic materials

This product contains beryllium oxide. The product is entirely safe provided that the BeO disc is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	70	V
V_{CEO}	collector-emitter voltage	open base	–	30	V
V_{EBO}	emitter-base voltage	open collector	–	3	V
I_C	collector current (DC)		–	15	A
$I_{C(AV)}$	average collector current		–	15	A
P_{tot}	total power dissipation	$T_{mb} \leq 25$ °C	–	250	W
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	200	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	P_{tot} = 250 W; T_{mb} = 25 °C; note 1	0.7	K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink		0.2	K/W

Note

1. Thermal resistance is determined under specified RF operating conditions.

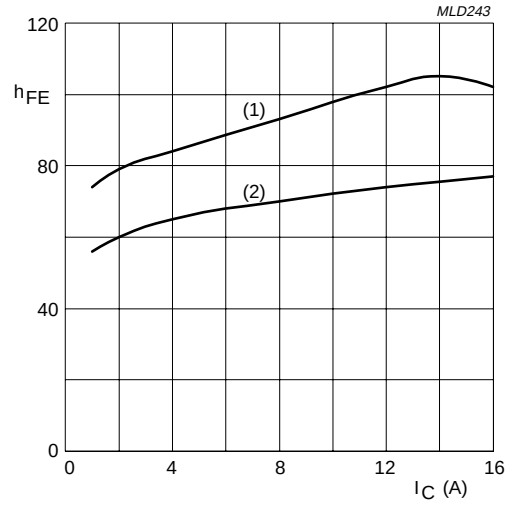
CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)CBO}$	collector-base breakdown voltage	open emitter; I_C = 60 mA	70	–	–	V
$V_{(BR)CEO}$	collector-emitter breakdown voltage	open base; I_C = 150 mA	30	–	–	V
$V_{(BR)EBO}$	emitter-base breakdown voltage	open collector; I_E = 3 mA	3	–	–	V
I_{CES}	collector leakage current	V_{BE} = 0; V_{CE} = 28 V	–	–	5	mA
h_{FE}	DC current gain	V_{CE} = 10 V; I_C = 4.5 A; note 1; see Fig 3	30	–	120	
C_c	collector capacitance	V_{CB} = 26 V; $I_E = i_e$ = 0; f = 1 MHz; note 2; see Fig 4	–	75	–	pF

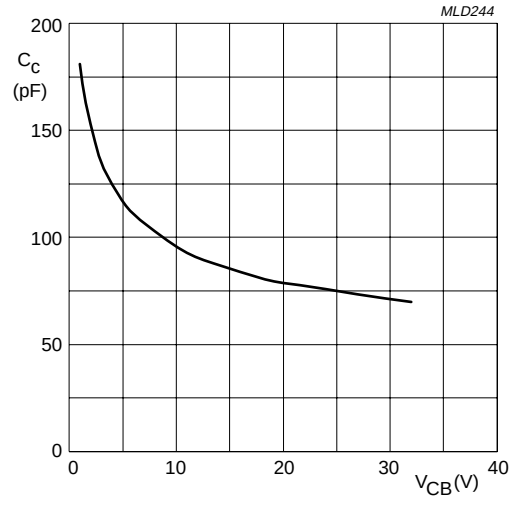
Notes

1. Measured under pulsed conditions: $t_p \leq 500$ μs; $\delta \leq 0.01$.
2. Value of C_c is that of the die only, it is not measurable because of internal matching network.



Measured under pulsed conditions; $t_p \leq 500$ μs; $\delta \leq 0.01$.
(1) V_{CE} = 26 V.
(2) V_{CE} = 10 V.

Fig.3 DC current gain as a function of collector current; typical values.



Value C_c is that of the die only, it is not measurable because of internal matching network.
$I_E = i_e$ = 0; f = 1 MHz.

Fig.4 Collector capacitance as a function of collector-base voltage; typical values.

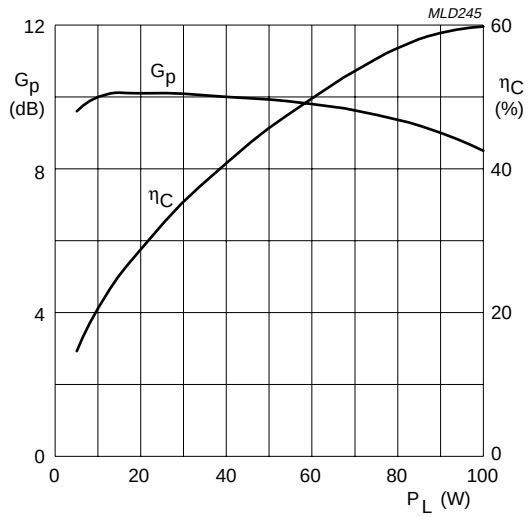
APPLICATION INFORMATION

RF performance at T_h = 25 °C in a common emitter, class-AB test circuit; $R_{th\ mb\text{-}h}$ = 0.2 K/W.

MODE OF OPERATION	f (MHz)	V_{CE} (V)	I_{CQ} (mA)	P_L (W)	G_p (dB)	η_C (%)
CW, class-AB	900	26	200	75	≥8 typ. 9.5	≥50 typ. 55
	960	26	200	75	≥8.5 typ. 9.5	≥50 typ. 55

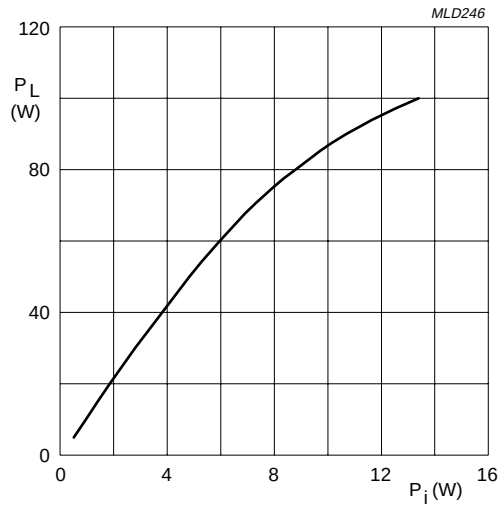
Ruggedness in class-AB operation

The transistors are capable of withstanding a load mismatch corresponding to VSWR = 4 : 1 through all phases at rated output power, under the following conditions: V_{CE} = 26 V; f = 960 MHz; I_{CQ} = 200 mA; T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.2 K/W.



V_{CE} = 26 V; I_{CQ} = 200 mA; f = 960 MHz.

Fig.5 Power gain and collector efficiency as functions of load power; typical values.



V_{CE} = 26 V; I_{CQ} = 200 mA; f = 960 MHz.

Fig.6 Load power as a function of input power; typical values.

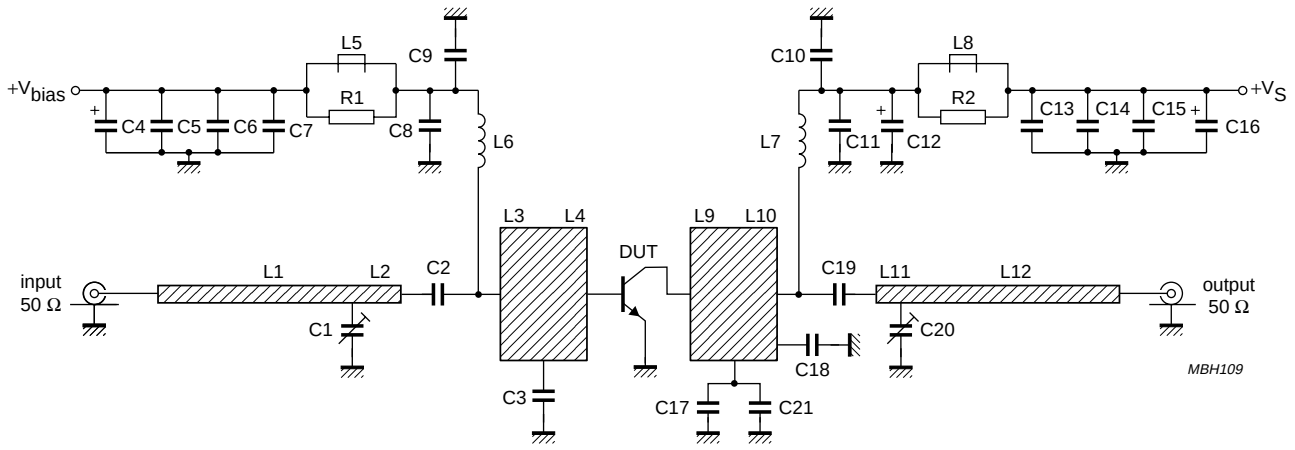


Fig.7 Class-AB test circuit at f = 960 MHz.

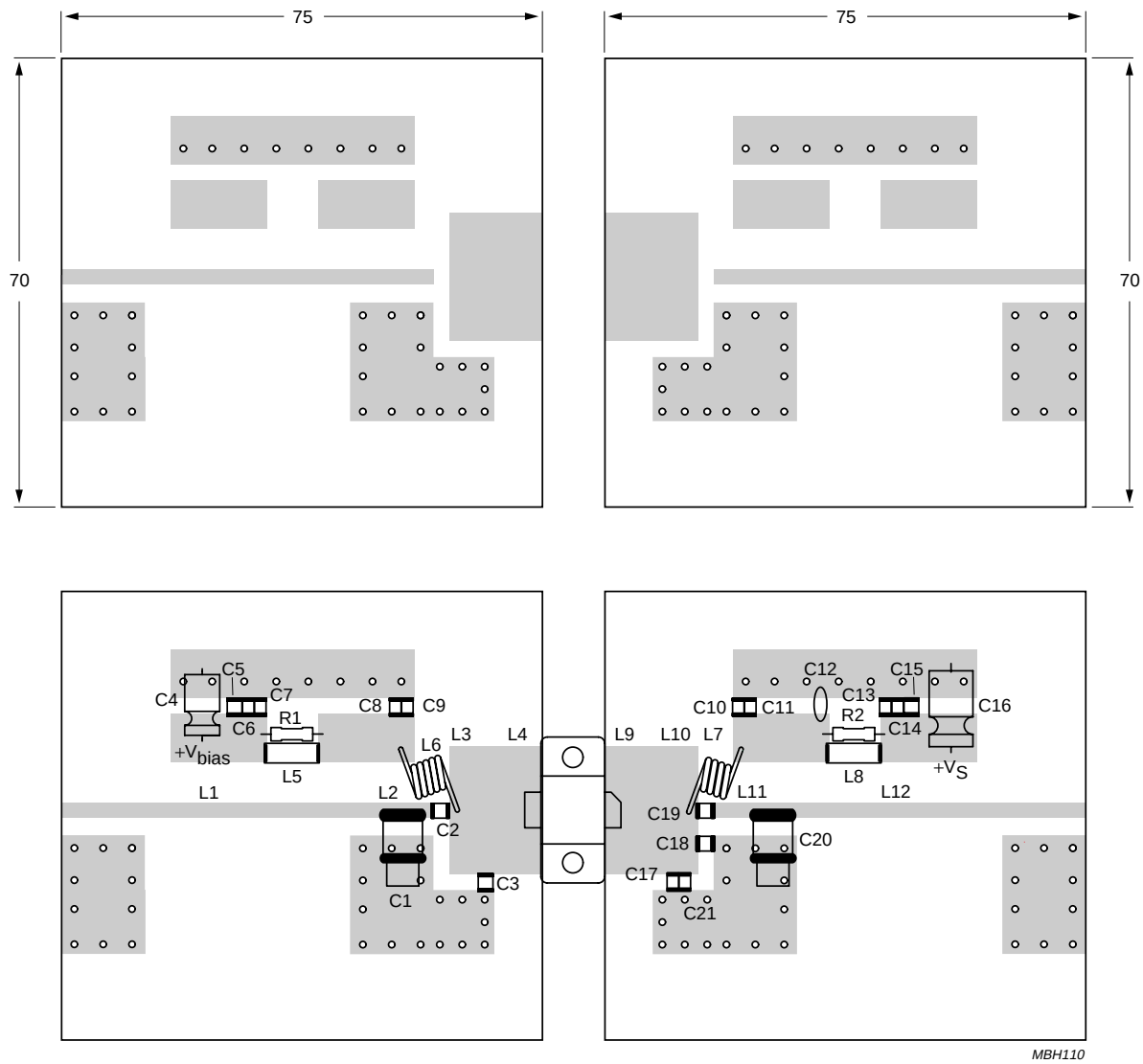
List of components (see Figs 7 and 8)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE No.
C1, C20	Tekelec, type 5201	0.8 to 10 pF		
C2, C19	multilayer ceramic chip capacitor; note 1	15 pF; 500 V		
C3	multilayer ceramic chip capacitor; note 1	6.2 pF; 500 V		
C4	electrolytic capacitor	10 μF; 63 V		
C5	multilayer ceramic chip capacitor	22 nF; 50 V		
C6	multilayer ceramic chip capacitor; note 1	1 nF; 500 V		
C7	multilayer ceramic chip capacitor; note 1	33 pF; 500 V		2222 030 28109
C8, C11, C14	multilayer ceramic chip capacitor; note 1	100 pF; 500 V		
C9, C10, C13	multilayer ceramic chip capacitor; note 1	20 pF; 500 V		
C12	solid tantalum capacitor	1 μF; 35 V		
C15	multilayer ceramic chip capacitor	100 nF; 50 V		
C16	electrolytic capacitor	47 μF; 40 V		2222 036 68479

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE No.
C17	multilayer ceramic chip capacitor; note 1	4.7 pF; 500 V		
C18	multilayer ceramic chip capacitor; note 1	3.3 pF; 500 V		
C21	multilayer ceramic chip capacitor; note 1	2.7 pF; 500 V		
L1	stripline; note 2		length 51 mm width 2.2 mm	
L2	stripline; note 2		length 7 mm width 2.2 mm	
L3	stripline; note 2		length 5.5 mm width 20 mm	
L4	stripline; note 2		length 9 mm width 20 mm	
L5, L8	Ferroxcube chip-bead grade 4S2			4330 030 36300
L6	5 turns enamelled 1 mm copper wire		int. diameter 4 mm close wound	
L7	4 turns enamelled 1 mm copper wire		int. diameter 4 mm close wound	
L9	stripline; note 2		length 12.5 mm width 20 mm	
L10	stripline; note 2		length 2 mm width 20 mm	
L11	stripline; note 2		length 17 mm width 2.2 mm	
L12	stripline; note 2		length 41 mm width 2.2 mm	
R1, R2	metal film resistor	100 Ω; 0.4 W		

Notes

1. American Technical Ceramics type 100B or capacitor of same quality.
2. The striplines are on double-clad printed-circuit board with PTFE fibre-glass dielectric (ε_r = 2.25); thickness $^1/_{32}$ inch.

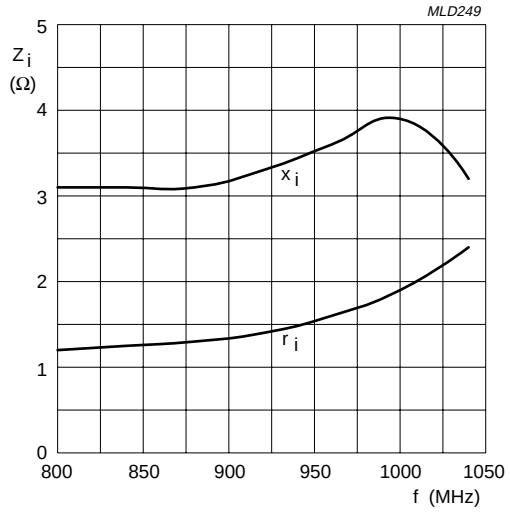


The same printed-circuit board can also be used for the flangeless version FL.

Dimensions in mm.

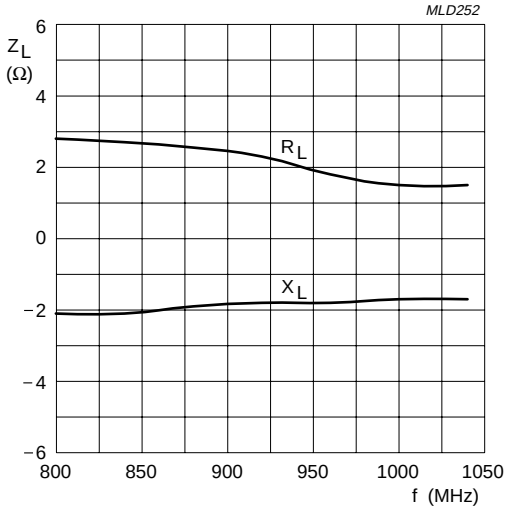
The components are located on one side of the copper-clad PTFE microfibre-glass board, the other side is unetched and serves as a ground plane. Earth connections from the component side to the ground plane are made by through metallization.

Fig.8 Component layout and printed-circuit board for 960 MHz class-AB test circuit.



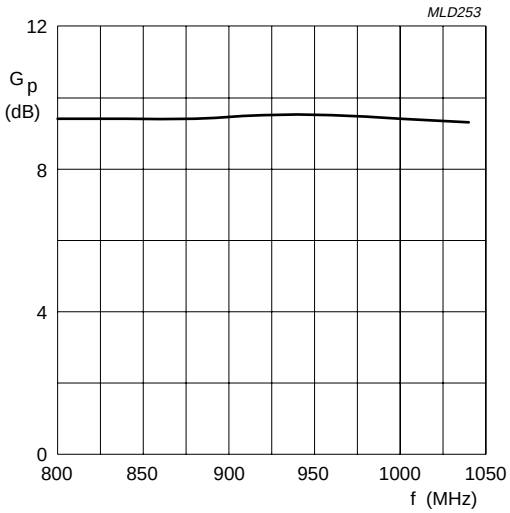
V_{CE} = 26 V; I_{CQ} = 200 mA; P_L = 75 W;
T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.2 K/W.

Fig.9 Input impedance as a function of frequency (series components); typical values.



V_{CE} = 26 V; I_{CQ} = 200 mA; P_L = 75 W;
T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.2 K/W.

Fig.10 Load impedance as a function of frequency (series components); typical values.



V_{CE} = 26 V; I_{CQ} = 200 mA; P_L = 75 W;
T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.2 K/W.

Fig.11 Power gain as a function of frequency; typical values.

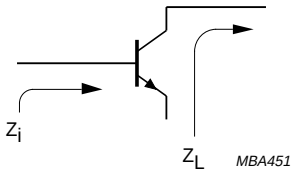
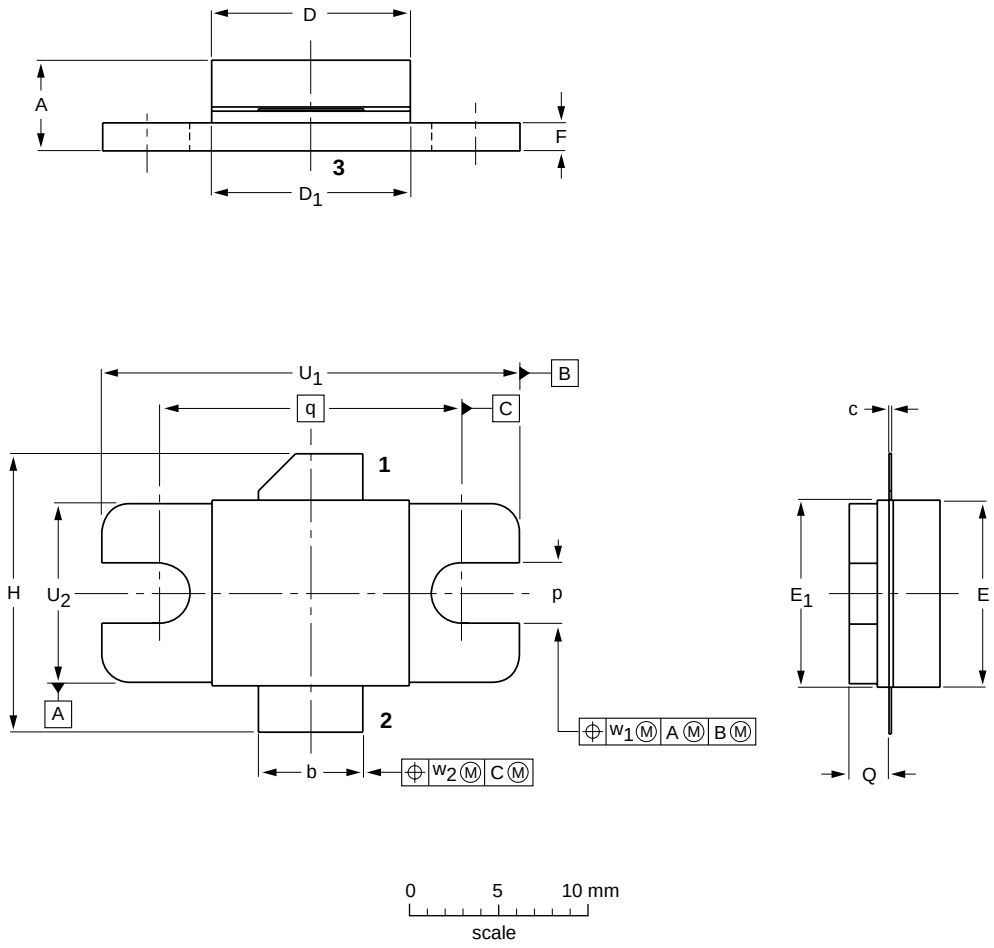


Fig.12 Definition of transistor impedance.

PACKAGE OUTLINES

Flanged ceramic package; 2 mounting holes; 2 leads **SOT391A**

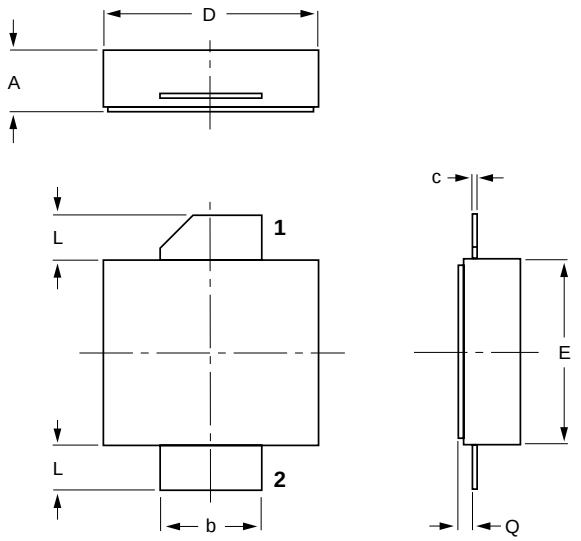


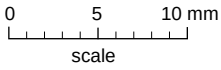
DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	E	E_1	F	H	p	Q	q	U_1	U_2	w_1	w_2
mm	5.21 4.45	5.84 5.59	0.15 0.10	10.87 10.67	10.92 10.67	10.26 10.06	10.29 10.03	1.65 1.40	15.75 14.73	3.43 3.18	2.29 2.03	16.51	22.99 22.73	9.91 9.65	0.25	0.51
inches	0.205 0.175	0.230 0.220	0.006 0.004	0.428 0.420	0.430 0.420	0.404 0.396	0.405 0.395	0.065 0.055	0.620 0.580	0.135 0.125	0.090 0.080	0.650	0.905 0.895	0.390 0.380	0.010	0.020

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT391A						~~99-12-08~~ 00-11-01

Flangeless ceramic package; 2 leads **SOT391B**





DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	E	L	Q
mm	4.09 3.02	5.85 5.58	0.16 0.10	11.54 10.51	10.93 9.90	2.79 2.29	1.02 0.76

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT391B						97-05-29

DATA SHEET STATUS

DATA SHEET STATUS	PRODUCT STATUS	DEFINITIONS [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

Note

1. Please consult the most recently issued data sheet before initiating or completing a design.

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Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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