DATA SHEET

BLV857
UHF linear push-pull power transistor

Product specification
Supersedes data of 1995 Oct 04

1997 Jan 16

Philips Semiconductors

PHILIPS

UHF linear push-pull power transistor BLV857

FEATURES

- Internal input matching for an optimum wideband capability and high gain
- Polysilicon emitter ballasting resistors for an optimum temperature profile
- Gold metallization ensures excellent reliability.

APPLICATION

- Common emitter class-A operation in linear transposers/transmitters (television) in the 470 to 860 MHz frequency band.

DESCRIPTION

NPN silicon planar transistor with two sections in push-pull configuration. The device is encapsulated in a SOT324B 4-lead rectangular flange package with a ceramic cap. The common emitters are connected to the flange.

PINNING SOT324B

PIN	SYMBOL	DESCRIPTION
1	c1	collector 1
2	c2	collector 2
3	b1	base 1
4	b2	base 2
5	e	common emitters

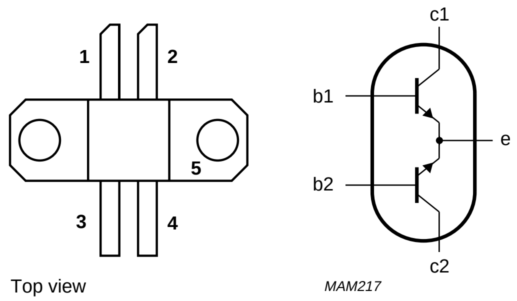


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a common emitter push-pull test circuit.

MODE OF OPERATION	f (MHz)	V_{CE} (V)	I_{CQ} (A)	$P_{o\ sync}$ (W)	G_p (dB)
CW class-A	860	25	2 × 1.1	≥10(1)	≥10(1)

Note

1. Three-tone test signal (–8, –16 and –10 dB); d_{im} = –54 dB.

WARNING
Product and environmental safety - toxic materials
This product contains beryllium oxide. The product is entirely safe provided that the BeO discs are not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

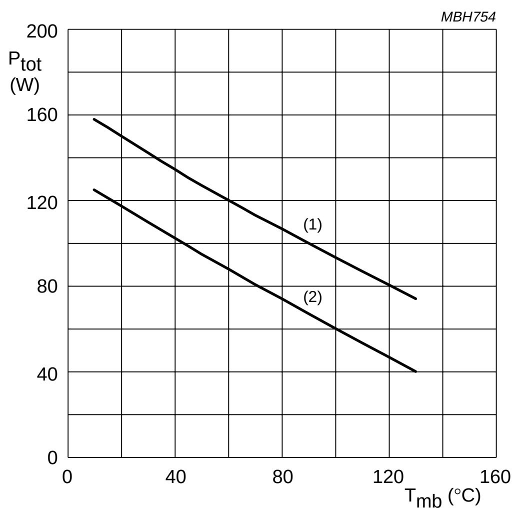
SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	60	V
V_{CEO}	collector-emitter voltage	open base	–	28	V
V_{EBO}	emitter-base voltage	open collector	–	2.5	V
I_C	collector current (DC)		–	7.4	A
$I_{C(AV)}$	average collector current		–	7.4	A
P_{tot}	total power dissipation	T_{mb} = 70 °C; note 1; see Fig.2	–	80	W
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	200	°C

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting-base	P_{tot} = 80 W; T_{mb} = 70 °C note 1	1.6	K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting-base to heatsink	note 1	0.4	K/W

Note to Limiting values and Thermal characteristics

1. Total device; both sections equally loaded.



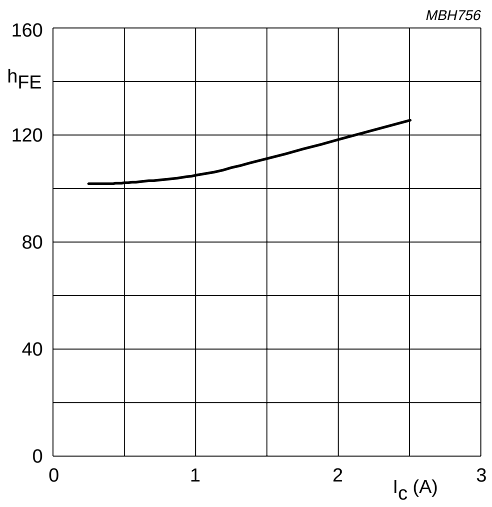
(1) Short-time operation during mismatch.
(2) Continuous operation.

Fig.2 Power derating curve.

CHARACTERISTICS

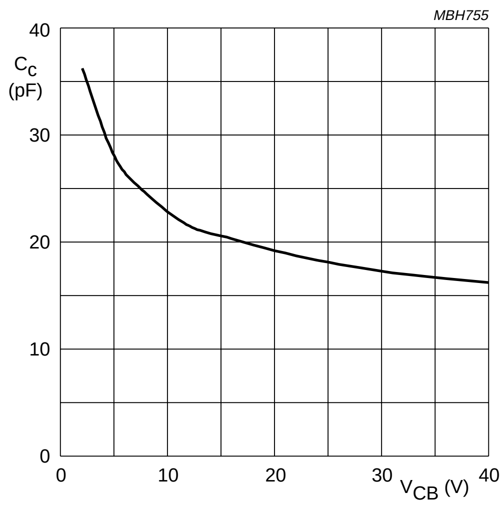
Values apply to either transistor section; T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)CBO}$	collector-base breakdown voltage	I_C = 15 mA; I_E = 0	60	–	–	V
$V_{(BR)CEO}$	collector-emitter breakdown voltage	I_C = 30 mA; I_B = 0	28	–	–	V
$V_{(BR)EBO}$	emitter-base breakdown voltage	I_E = 0.6 mA; I_C = 0	2.5	–	–	V
I_{CBO}	collector-base leakage current	V_{CB} = 27 V; V_{BE} = 0	–	–	1.5	mA
I_{CEO}	collector-emitter leakage current	V_{CE} = 20 V	–	–	3	mA
h_{FE}	DC current gain	V_{CE} = 25 V; I_C = 1.1 A; see Fig.3	30	–	140	
C_c	collector capacitance	V_{CB} = 25 V; I_E = i_e = 0; f = 1 MHz; see Fig.4	–	18	–	pF
C_{re}	feedback capacitance	V_{CE} = 25 V; I_C = 0; f = 1 MHz	–	11	–	pF



V_{CE} = 25 V; t_p = 500 µs; δ = <1 %.

Fig.3 DC current gain as a function of collector current; typical values.



I_E = i_e = 0; f = 1 MHz.

Fig.4 Collector capacitance as a function of collector-base voltage; typical values.

APPLICATION INFORMATION

RF performance at T_h = 25 °C in a common emitter push-pull class-A test circuit.

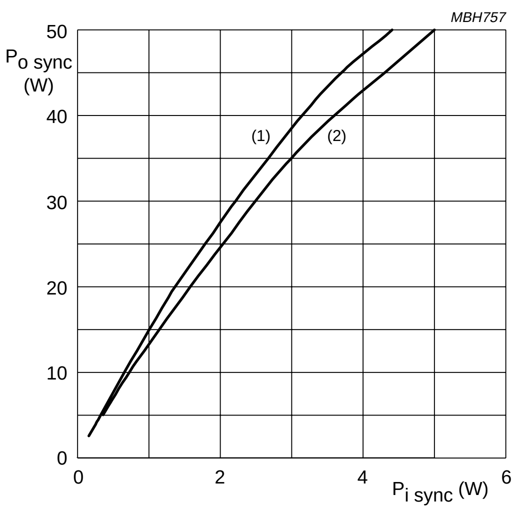
MODE OF OPERATION	f (MHz)	V_{CE} (V)	I_{CQ} (A)	$P_{o\ sync}$ (W)	G_p (dB)	d_{im} (dB)
CW class-A	860	25	2 × 1.1	≥10(1)	≥10(1)	≤–54(1)
CW class-A	860	25	2 × 1.1	≥10(2)	≥10(2)	≤–51(2)

Notes

1. Three-tone test method: f_{vision} = 855.25 MHz (vision carrier –8 dB); f_{sound} = 860.75 MHz (sound carrier –10 dB); $f_{sideband}$ = 859.68 MHz (sideband signal –16 dB); 0 dB corresponds to peak sync level.
2. Three-tone test method: f_{vision} = 855.25 MHz (vision carrier –8 dB); f_{sound} = 860.75 MHz (sound carrier –7 dB); $f_{sideband}$ = 859.68 MHz (sideband signal –16 dB); 0 dB corresponds to peak sync level.

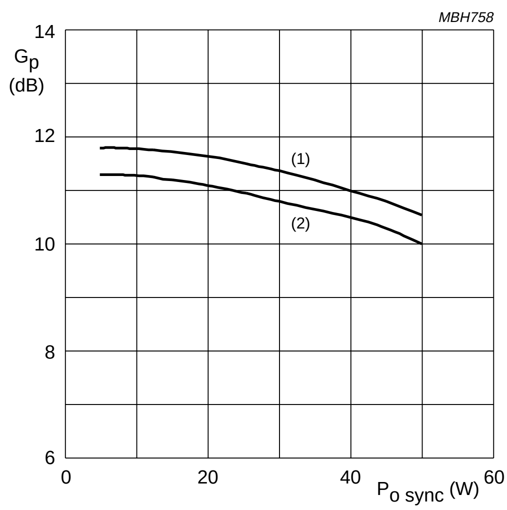
Ruggedness in class-A operation

The BLV857 is capable of withstanding a load mismatch corresponding to VSWR = 50 : 1 through all phases under the conditions: V_{CE} = 25 V; I_{CQ} = 2 × 1.1 A; f = 860 MHz; T_h = 25 °C; $P_{o\ sync}$ = 10 W.



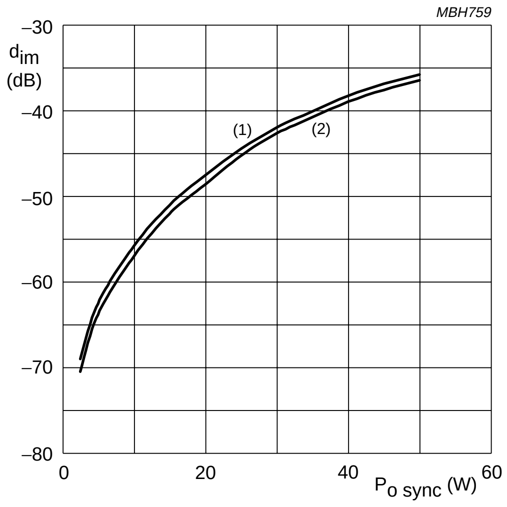
V_{CE} = 25 V; I_{CQ} = 2 × 1.1 A; f = 860 MHz; (3-tone; –8/–16/–10 dB).
(1) T_h = 25 °C.
(2) T_h = 70 °C.

Fig.5 Output power as a function of input power; typical values.



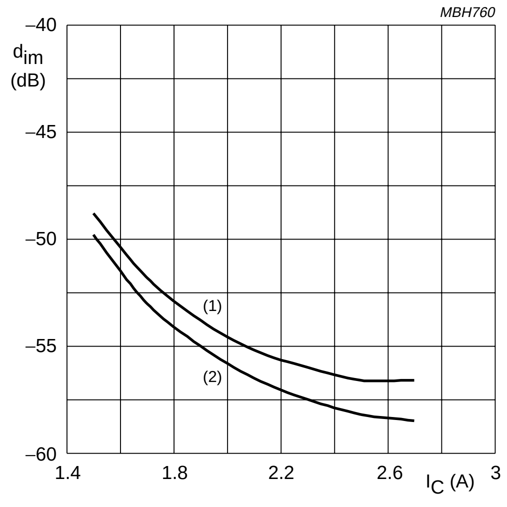
V_{CE} = 25 V; I_{CQ} = 2 × 1.1 A; f = 860 MHz; (3-tone; –8/–16/–10 dB).
(1) T_h = 25 °C.
(2) T_h = 70 °C.

Fig.6 Power gain as a function of output power; typical values.



V_{CE} = 25 V; I_{CQ} = 2 × 1.1 A; f = 860 MHz; (3-tone; –8/–16/–10 dB).
(1) T_h = 70 °C.
(2) T_h = 25 °C.

Fig.7 Intermodulation distortion as a function of output power; typical values.



V_{CE} = 25 V; f = 860 MHz; (3-tone; –8/–16/–10 dB).
(1) T_h = 70 °C.
(2) T_h = 25 °C.

Fig.8 Intermodulation distortion as a function of collector current; typical values.

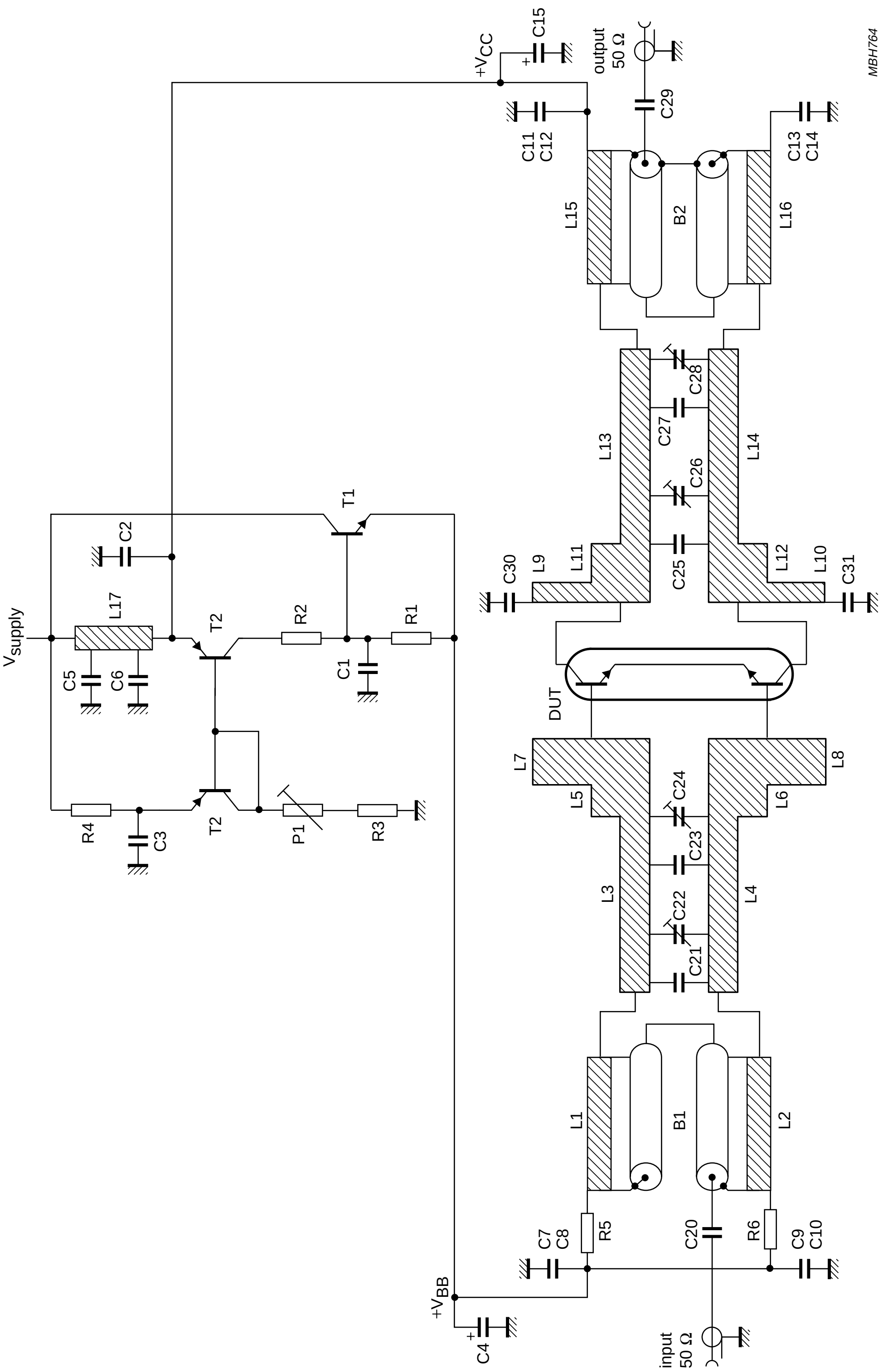
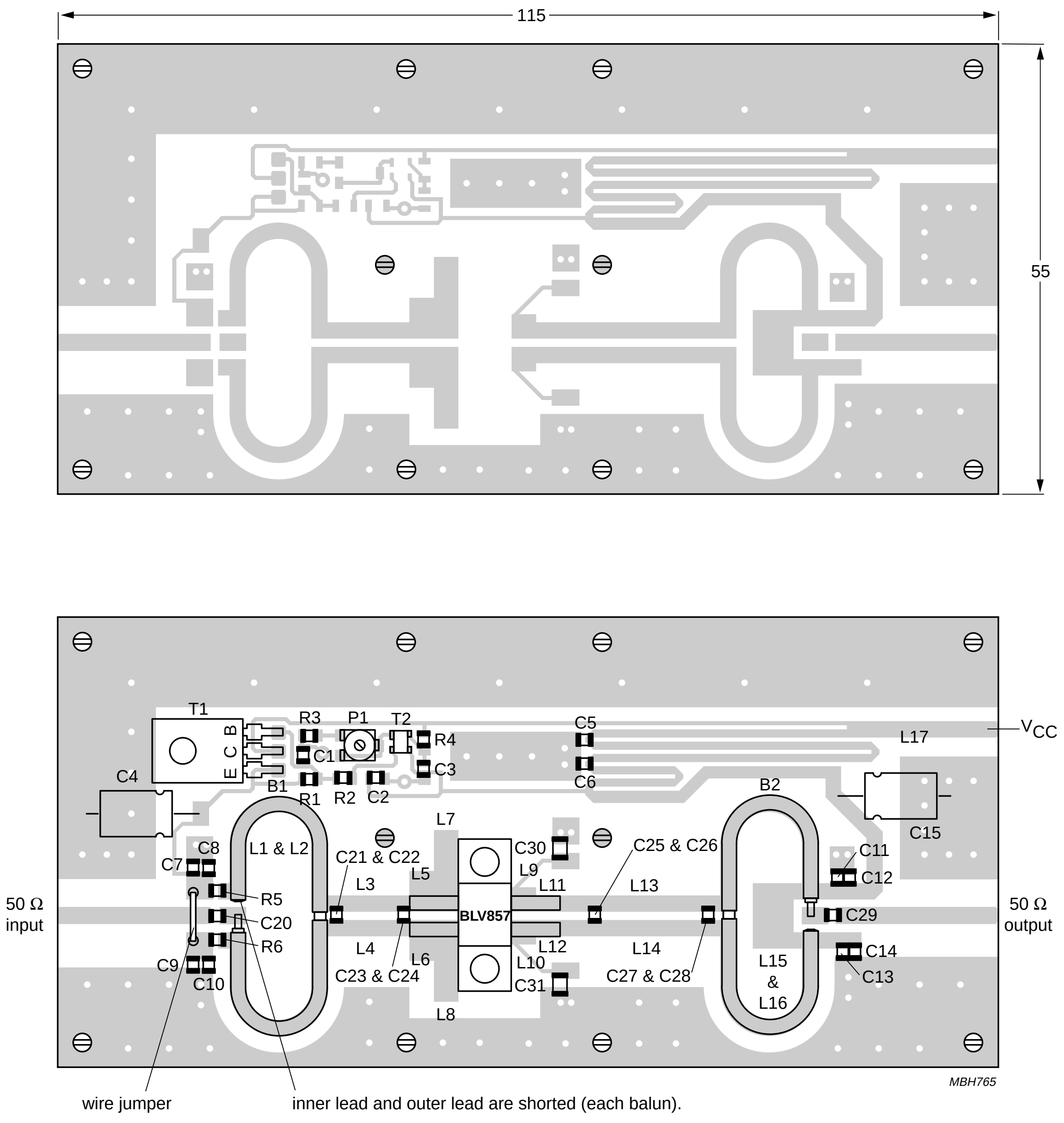


Fig.9 Class-A test circuit at f = 860 MHz.



Dimensions in mm.

The components are situated on one side of the copper-clad epoxy fibre-glass board, the other side is unetched and serves as a ground plane. Earth connections from the component side to the ground plane are made by through metallization.

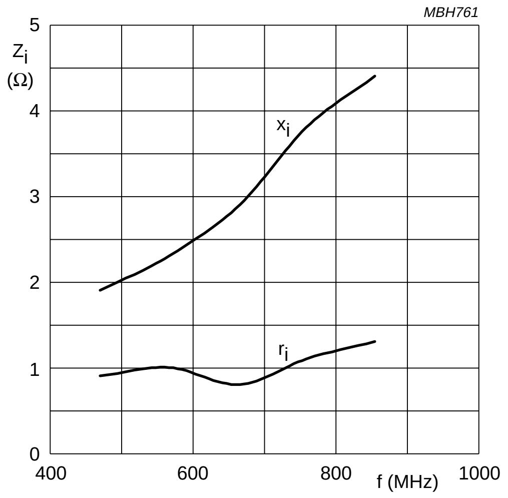
Fig.10 Printed-circuit board and component lay-out for 860 MHz class-A test circuit.

List of components

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE No.
C1, C2, C3, C5, C6, C7, C8, C9, C10	multilayer ceramic chip capacitor	10 nF	805	2222 590 16627
C4	solid aluminium capacitor	47 µF; 25 V		2222 030 36479
C11, C12, C13, C14, C30, C31	multilayer ceramic chip capacitor	100 nF	1206	2222 591 16641
C15	solid aluminium capacitor	10 µF; 63 V		2222 030 38109
C20	multilayer ceramic chip capacitor; note 1	18 pF		
C21	multilayer ceramic chip capacitor; note 1	3 pF		
C22, C24, C26, C28	Tekelec Giga trim 37271; note 3	0.6 to 4.5 pF		
C23	multilayer ceramic chip capacitor; note 1	7.5 pF		
C25	multilayer ceramic chip capacitor; notes 1 and 3	11 pF		
C27	multilayer ceramic chip capacitor; notes 1 and 3	9.1 pF		
C29	multilayer ceramic chip capacitor; note 1	100 pF		
L1, L2, L15, L16	stripline; note 2	50 Ω	30.6 × 2 mm	
L3, L4	stripline; note 2	50 Ω	10 × 2 mm	
L5, L6	stripline; note 2	26.5 Ω	3 × 5 mm	
L7, L8	stripline; note 2	15 Ω	3 × 10 mm	
L9, L10	stripline; note 2	104 Ω	6 × 0.5 mm	
L11, L12	stripline; note 2	38.8 Ω	3 × 3 mm	
L13, L14	stripline; note 2	50 Ω	22.5 × 2 mm	
L17	stripline; notes 2 and 4	76.2 Ω	120 × 1 mm	
B1, B2	Semi rigid coax balun UT70-25	Z = 25 Ω ±1.5 Ω	70 mm	
R1	SMD resistor	220 Ω	805	2322 734 22201
R2	SMD resistor	1.8 Ω	805	2322 734 21808
R3	SMD resistor	4.3 kΩ	805	2322 734 24302
R4	SMD resistor	33 Ω	805	2322 734 23309
R5, R6	SMD resistor	3.3 Ω	805	2322 734 23308
P1	potentiometer	2 kΩ		
T1	NPN transistor	BD139		9330 912 20112
T2	double PNP transistor	BCV62		5322 130 60505

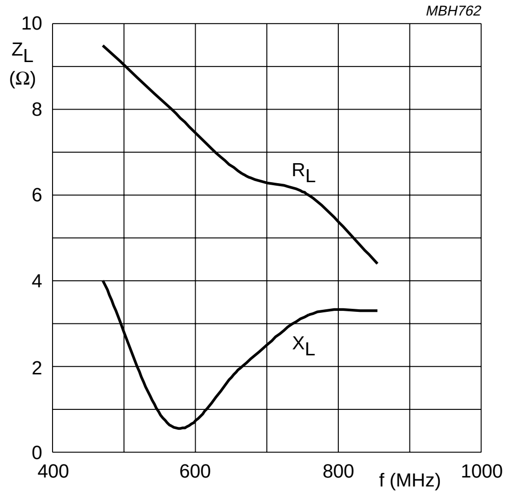
Notes

1. American Technical Ceramics type 100A or capacitor of same quality.
2. The striplines are on a double copper-clad printed-circuit board: Rogers ULTRALAM 2000 (B0300M1046QB) (ε_r = 2.55); thickness 0.76 mm.
3. Position of C25 and C26: distance of centre capacitor to transistor BLV857 = 7.5 mm.
   Position of C27 and C28: distance of centre capacitor to balun B2 = 1.5 mm.
4. The sense resistor on the bias unit is implemented as a stripline L17, in this way we obtain a small sense resistor (approximately 80 mΩ) which can handle the dissipated power.



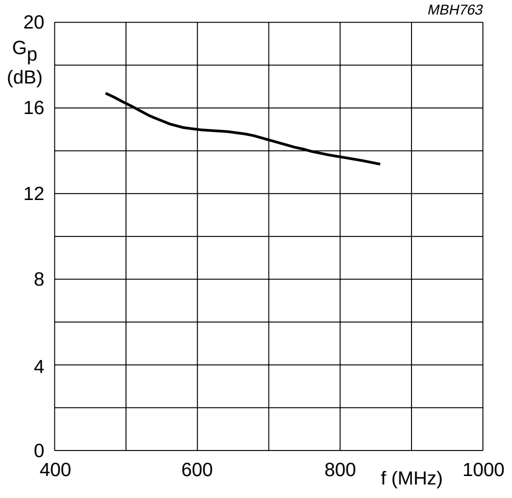
V_{CE} = 25 V; I_{CQ} = 2 × 1.1 A; $P_{o\ sync}$ = 10 W (total device); T_h = 25 °C.

Fig.11 Input impedance (per section) as a function of frequency (series components); typical values.



V_{CE} = 25 V; I_{CQ} = 2 × 1.1 A; $P_{o\ sync}$ = 10 W (total device); T_h = 25 °C.

Fig.12 Load impedance (per section) as a function of frequency (series components); typical values.



V_{CE} = 25 V; I_{CQ} = 2 × 1.1 A; $P_{o\ sync}$ = 10 W (total device); T_h = 25 °C.

Fig.13 Gain as a function of frequency; typical values.

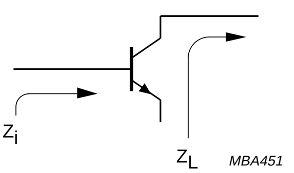
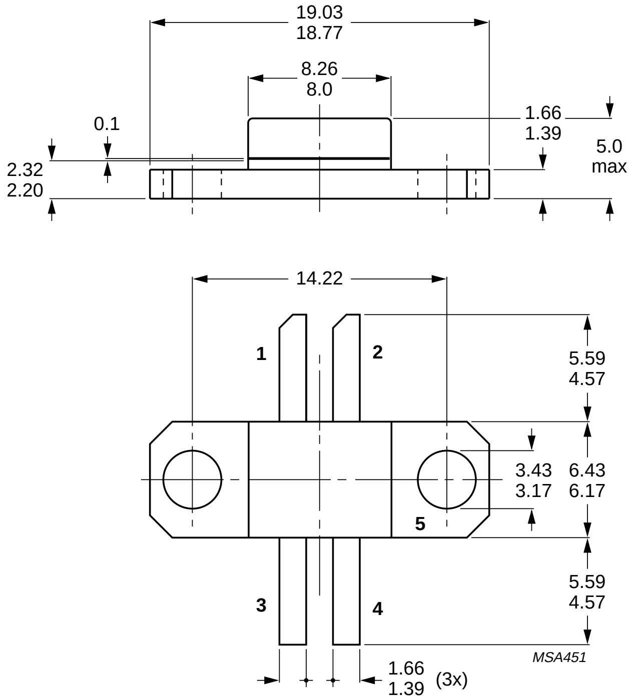


Fig.14 Definition of transistor impedance.

PACKAGE OUTLINE



Dimensions in mm.

Recommended screw: cheese-head 4-40 UNC/2A. Torque on screw: min. 0.6 Nm; max. 0.75 Nm.
Heatsink compound must be applied sparingly and evenly distributed.

Fig.15 SOT324B.

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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Argentina: see South America

Australia: 34 Waterloo Road, NORTH RYDE, NSW 2113, Tel. +61 2 9805 4455, Fax. +61 2 9805 4466

Austria: Computerstr. 6, A-1101 WIEN, P.O. Box 213, Tel. +43 1 60 101, Fax. +43 1 60 101 1210

Belarus: Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6, 220050 MINSK, Tel. +375 172 200 733, Fax. +375 172 200 773

Belgium: see The Netherlands

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Bulgaria: Philips Bulgaria Ltd., Energoproject, 15th floor, 51 James Bourchier Blvd., 1407 SOFIA, Tel. +359 2 689 211, Fax. +359 2 689 102

Canada: PHILIPS SEMICONDUCTORS/COMPONENTS, Tel. +1 800 234 7381

China/Hong Kong: 501 Hong Kong Industrial Technology Centre, 72 Tat Chee Avenue, Kowloon Tong, HONG KONG, Tel. +852 2319 7888, Fax. +852 2319 7700

Colombia: see South America

Czech Republic: see Austria

Denmark: Prags Boulevard 80, PB 1919, DK-2300 COPENHAGEN S, Tel. +45 32 88 2636, Fax. +45 31 57 1949

Finland: Sinikalliontie 3, FIN-02630 ESPOO, Tel. +358 9 615800, Fax. +358 9 61580/xxx

France: 4 Rue du Port-aux-Vins, BP317, 92156 SURESNES Cedex, Tel. +33 1 40 99 6161, Fax. +33 1 40 99 6427

Germany: Hammerbrookstraße 69, D-20097 HAMBURG, Tel. +49 40 23 53 60, Fax. +49 40 23 536 300

Greece: No. 15, 25th March Street, GR 17778 TAVROS/ATHENS, Tel. +30 1 4894 339/239, Fax. +30 1 4814 240

Hungary: see Austria

India: Philips INDIA Ltd, Shivsagar Estate, A Block, Dr. Annie Besant Rd. Worli, MUMBAI 400 018, Tel. +91 22 4938 541, Fax. +91 22 4938 722

Indonesia: see Singapore

Ireland: Newstead, Clonskeagh, DUBLIN 14, Tel. +353 1 7640 000, Fax. +353 1 7640 200

Israel: RAPAC Electronics, 7 Kehilat Saloniki St, TEL AVIV 61180, Tel. +972 3 645 0444, Fax. +972 3 649 1007

Italy: PHILIPS SEMICONDUCTORS, Piazza IV Novembre 3, 20124 MILANO, Tel. +39 2 6752 2531, Fax. +39 2 6752 2557

Japan: Philips Bldg 13-37, Kohnan 2-chome, Minato-ku, TOKYO 108, Tel. +81 3 3740 5130, Fax. +81 3 3740 5077

Korea: Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL, Tel. +82 2 709 1412, Fax. +82 2 709 1415

Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR, Tel. +60 3 750 5214, Fax. +60 3 757 4880

Mexico: 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905, Tel. +9-5 800 234 7381

Middle East: see Italy

Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB, Tel. +31 40 27 82785, Fax. +31 40 27 88399

New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND, Tel. +64 9 849 4160, Fax. +64 9 849 7811

Norway: Box 1, Manglerud 0612, OSLO, Tel. +47 22 74 8000, Fax. +47 22 74 8341

Philippines: Philips Semiconductors Philippines Inc., 106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI, Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

Poland: Ul. Lukiska 10, PL 04-123 WARSZAWA, Tel. +48 22 612 2831, Fax. +48 22 612 2327

Portugal: see Spain

Romania: see Italy

Russia: Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW, Tel. +7 095 755 6918, Fax. +7 095 755 6919

Singapore: Lorong 1, Toa Payoh, SINGAPORE 1231, Tel. +65 350 2538, Fax. +65 251 6500

Slovakia: see Austria

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South Africa: S.A. PHILIPS Pty Ltd., 195-215 Main Road Martindale, 2092 JOHANNESBURG, P.O. Box 7430 Johannesburg 2000, Tel. +27 11 470 5911, Fax. +27 11 470 5494

South America: Rua do Rocio 220, 5th floor, Suite 51, 04552-903 São Paulo, SÃO PAULO - SP, Brazil, Tel. +55 11 821 2333, Fax. +55 11 829 1849

Spain: Balmes 22, 08007 BARCELONA, Tel. +34 3 301 6312, Fax. +34 3 301 4107

Sweden: Kottbygatan 7, Akalla, S-16485 STOCKHOLM, Tel. +46 8 632 2000, Fax. +46 8 632 2745

Switzerland: Allmendstrasse 140, CH-8027 ZÜRICH, Tel. +41 1 488 2686, Fax. +41 1 481 7730

Taiwan: Philips Semiconductors, 6F, No. 96, Chien Kuo N. Rd., Sec. 1, TAIPEI, Taiwan Tel. +886 2 2134 2870, Fax. +886 2 2134 2874

Thailand: PHILIPS ELECTRONICS (THAILAND) Ltd., 209/2 Sanpavuth-Bangna Road Prakanong, BANGKOK 10260, Tel. +66 2 745 4090, Fax. +66 2 398 0793

Turkey: Talatpasa Cad. No. 5, 80640 GÜLTEPE/ISTANBUL, Tel. +90 212 279 2770, Fax. +90 212 282 6707

Ukraine: PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7, 252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

United Kingdom: Philips Semiconductors Ltd., 276 Bath Road, Hayes, MIDDLESEX UB3 5BX, Tel. +44 181 730 5000, Fax. +44 181 754 8421

United States: 811 East Arques Avenue, SUNNYVALE, CA 94088-3409, Tel. +1 800 234 7381

Uruguay: see South America

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Yugoslavia: PHILIPS, Trg N. Pasica 5/v, 11000 BEOGRAD, Tel. +381 11 625 344, Fax.+381 11 635 777

For all other countries apply to: Philips Semiconductors, Marketing & Sales Communications, Building BE-p, P.O. Box 218, 5600 MD EINDHOVEN, The Netherlands, Fax. +31 40 27 24825

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