DATA SHEET

BLV33
VHF linear power transistor

Product specification
Supersedes data of November 1995

1996 Oct 10

Philips
Semiconductors

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VHF linear power transistor BLV33

FEATURES

- Diffused emitter ballasting resistors for an optimum temperature profile
- Gold sandwich metallization ensures excellent reliability.

APPLICATIONS

- Primarily intended for use in linear VHF amplifiers for television transmitters and transposers.

DESCRIPTION

NPN silicon planar epitaxial transistor encapsulated in a ¹⁄₁₆" 4 fslead SOT147 capstan package with ceramic cap. All leads are isolated from the stud.

PINNING - SOT147

PIN	SYMBOL	DESCRIPTION
1	c	collector
2	e	emitter
3	b	base
4	e	emitter

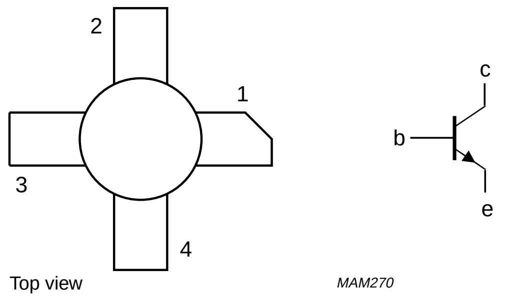


Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

RF performance in a common emitter push-pull test circuit.

MODE OF OPERATION	f_{vision} (MHz)	V_{CE} (V)	I_C, $I_{C(ZS)}$ (A)	T_h (°C)	d_{im}(1) (dB)	$P_{o\ sync}$(1) (W)	G_P (dB)	sync compr.(2) sync in/sync out (%)
CW, class-A	224.25	25	3.2	70	–55	>16.5	>9	
				25	–55	typ. 26	typ. 9.7	
CW, class-AB	224.25	28	0.1	70		typ. 90	typ. 6.5	30/25

Notes

1. Three-tone test method (vision carrier –8 dB, sound carrier –7 dB, sideband signal –16 dB), zero dB corresponds to peak sync level.
2. Television service (negative modulation, C.C.I.R. system).

WARNING
Product and environmental safety - toxic materials
This product contains beryllium oxide. The product is entirely safe provided that the BeO disc is not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

VHF linear power transistor BLV33

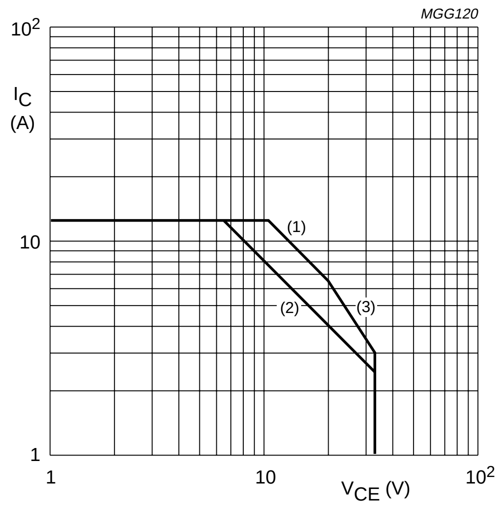
LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CESM}	collector-emitter voltage	$V_{BE} = 0$	–	65	V
V_{CEO}	collector-emitter voltage	open base	–	33	V
V_{EBO}	emitter-base voltage	open collector	–	4	V
I_C	collector current (DC)		–	12.5	A
$I_{C(AV)}$	average collector current		–	12.5	A
I_{CM}	peak collector current	f > 1 MHz	–	20	A
P_{tot}	total power dissipation (DC)	T_{mb} = 25 °C	–	132	W
P_{rf}	RF power dissipation	f > 1 MHz; T_{mb} = 25 °C	–	165	W
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	200	°C

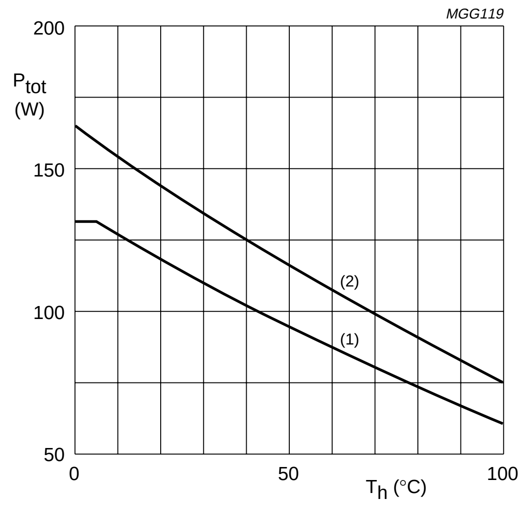
THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}mb(dc)}$	thermal resistance from junction to mounting base (DC dissipation)	P_{diss} = 80 W; T_{mb} = 82 °C; T_h = 70 °C	1.46	K/W
$R_{th\ j\text{-}mb(rf)}$	thermal resistance from junction to mounting base (RF dissipation)	P_{diss} = 80 W; T_{mb} = 82 °C; T_h = 70 °C	1.17	K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink	P_{diss} = 80 W; T_{mb} = 82 °C; T_h = 70 °C	0.15	K/W



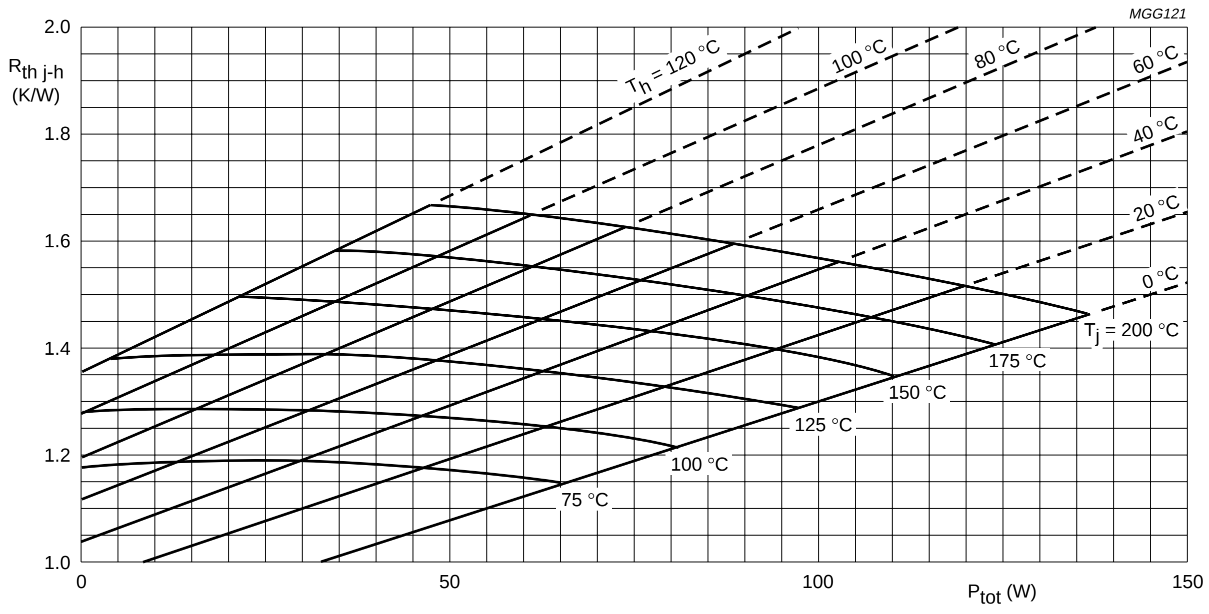
(1) T_{mb} = 25 °C.
(2) T_h = 70 °C.
(3) Second breakdown limit (independent of temperature).

Fig.2 DC SOAR.



(1) Continuous DC (including RF class-A) operation.
(2) Continuous RF operation.

Fig.3 Power derating curves.



$R_{th\ mb\text{-}h}$ = 0.15 K/W.

Fig.4 Maximum thermal resistance from junction to heatsink as a function of power dissipation, with heatsink and junction temperature as parameters.

Example

Nominal class-A operation: V_{CE} = 25 V; I_C = 3.2 A; T_h = 70 °C.

Figure 4 shows:

$R_{th\ j\text{-}h}$ = max. 1.60 K/W

T_j = max. 198 °C.

Typical device:

$R_{th\ j\text{-}h}$ = typ.1.50 K/W

T_j = typ. 190 °C.

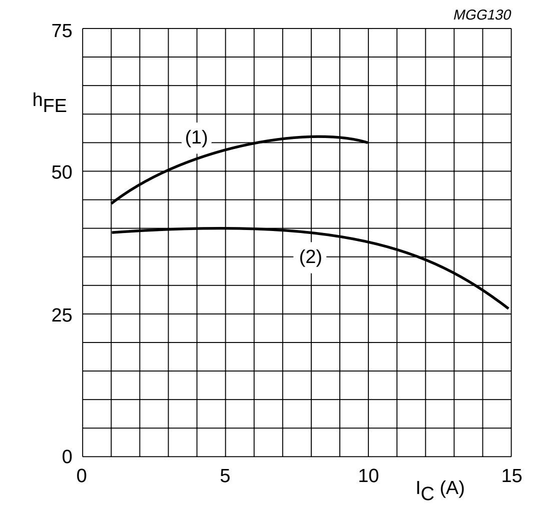
CHARACTERISTICS

T_j = 25 °C; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)CES}$	collector-emitter breakdown voltage	V_{BE} = 0; I_C = 25 mA	65	–	–	V
$V_{(BR)CEO}$	collector-emitter breakdown voltage	open base; I_C = 100 mA	33	–	–	V
$V_{(BR)EBO}$	emitter-base breakdown voltage	open collector; I_E = 10 mA	4	–	–	V
I_{CES}	collector cut-off current	V_{BE} = 0; V_{CE} = 30 V	–	–	1	mA
h_{FE}	DC current gain	V_{CE} = 25 V; I_C = 3 A; note 1	15	50	100	
V_{CEsat}	collector-emitter saturation voltage	I_C = 6 A; I_B = 0.6 A; note 1	–	0.75	–	V
f_T	transition frequency	V_{CB} = 25 V; I_E = –3 A; f = 100 MHz; note 2	–	680	–	MHz
	transition frequency	V_{CB} = 25 V; I_E = –6 A; f = 100 MHz; note 2	–	750	–	MHz
C_c	collector capacitance	V_{CB} = 25 V; I_E = i_e = 0; f = 1 MHz	–	155	–	pF
C_{re}	feedback capacitance	I_C = 100 mA; V_{CE} = 25 V; f = 1 MHz	–	88	–	pF
C_{cs}	collector-stud capacitance		–	3	–	pF

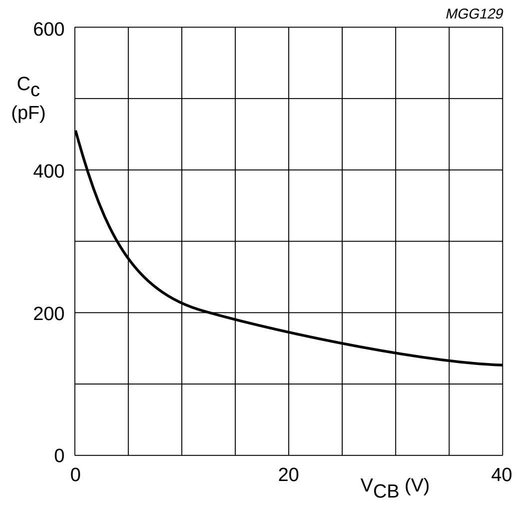
Notes

1. Measured under pulse conditions: $t_p \leq 300\ \mu s$; $\delta \leq 0.02$.
2. Measured under pulse conditions: $t_p \leq 50\ \mu s$; $\delta \leq 0.01$.



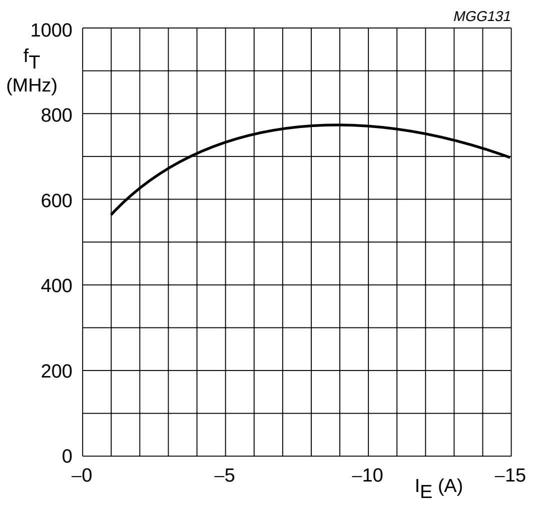
T_j = 25 °C.
(1) V_{CE} = 25 V.
(2) V_{CE} = 5 V.

Fig.5 DC current gain as a function of collector current; typical values.



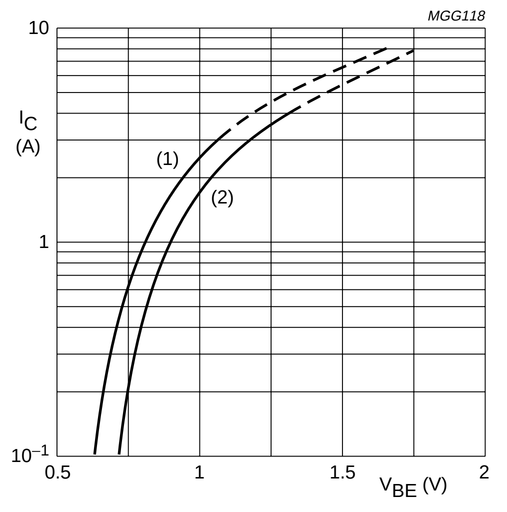
$I_E = i_e = 0$; f = 1 MHz; T_j = 25 °C.

Fig.6 Collector capacitance as a function of collector-base voltage; typical values.



V_{CB} = 25 V; f = 100 MHz; T_j = 25 °C.

Fig.7 Transition frequency as a function of emitter current; typical values.



V_{CE} = 25 V.
(1) T_h = 70 °C.
(2) T_h = 25 °C.

Fig.8 Collector current as a function of base-emitter voltage; typical values.

APPLICATION INFORMATION

RF performance in VHF class-A operation (linear power amplifier)

MODE OF OPERATION	f_{vision} (MHz)	V_{CE} (V)	I_C (A)	T_h (°C)	d_{im}(1) (dB)	$P_{o\ sync}$(1) (W)	G_P (dB)
CW, class-A	224.25	25	3.2	70	–55	>16.5	>9
				70	–55	typ. 17.5	typ. 9.3
				70	–52	typ. 26.5	typ. 9.3
				25	–55	typ. 23	typ. 9.7

Note

1. Three-tone test method (vision carrier –8 dB, sound carrier –7 dB, sideband signal –16 dB), zero dB corresponds to peak sync level.

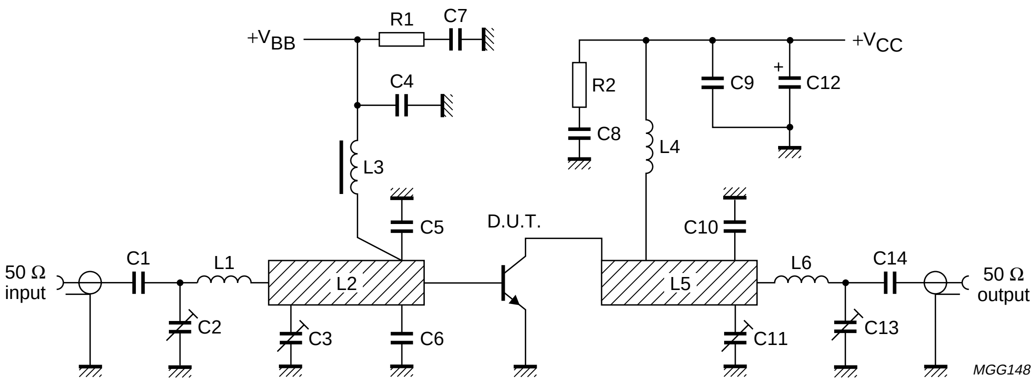


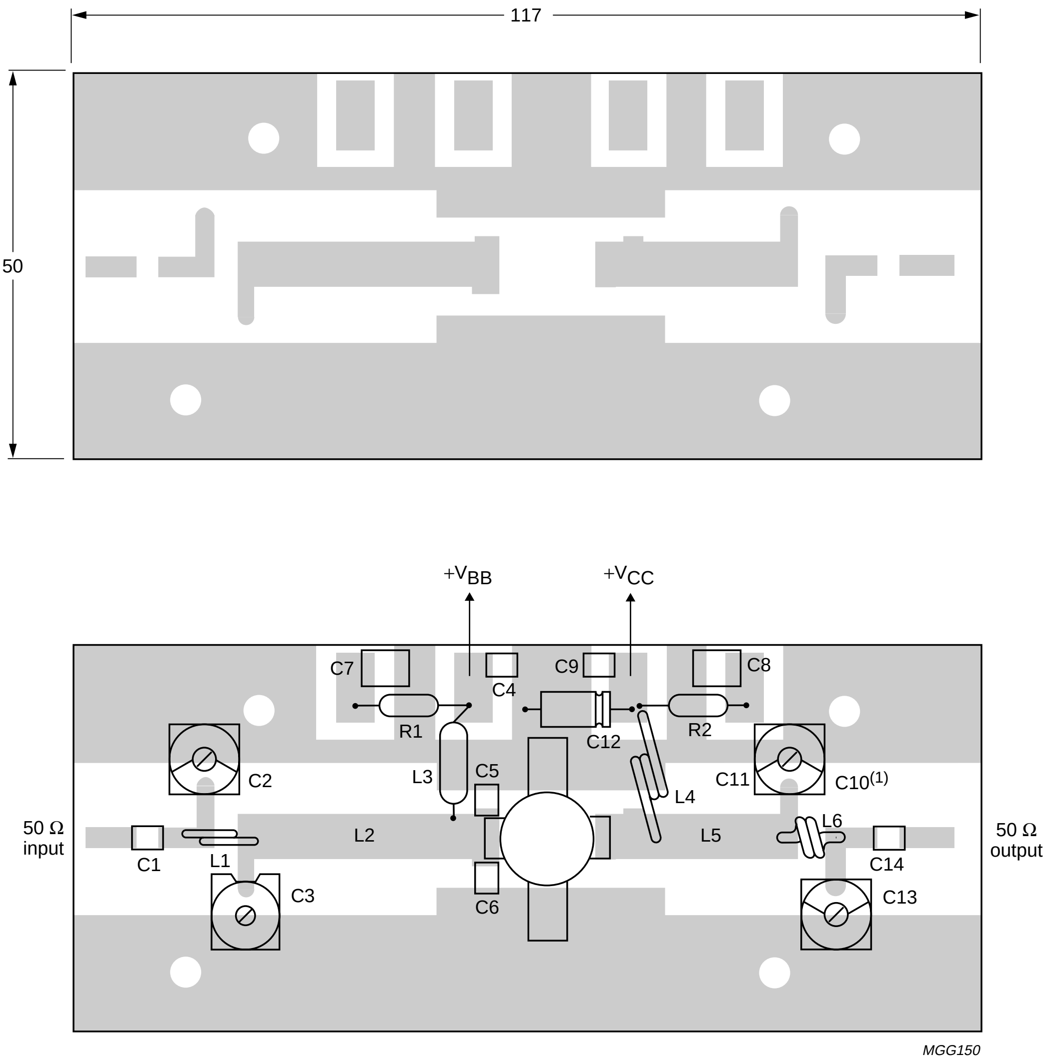
Fig.9 Class-A test circuit at f_{vision} = 224.25 MHz.

List of components used in test circuit (see Figs 9 and 10)**.**

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE No.
C1, C14	multilayer ceramic chip capacitor; note 1	680 pF, 500 V		
C2, C11, C13	film dielectric trimmer	4 to 40 pF		2222 809 08002
C3	film dielectric trimmer	2 to 18 pF		2222 809 09003
C4, C9	multilayer ceramic chip capacitor	680 pF, 50 V		2222 852 13681
C5, C6	multilayer ceramic chip capacitor; note 1	68 pF, 500 V	placed 2 mm from transistor edge	
C7, C8	multilayer ceramic chip capacitor	470 nF, 50 V		2222 856 48474
C10	multilayer ceramic chip capacitor; note 1	24 pF, 500 V		
C12	solid aluminium electrolytic capacitor	10 μF, 40 V		
L1	1½ turns of closely wound 1.6 mm enamelled Cu wire		int. diameter 4.5 mm leads 2 × 3 mm	
L2	stripline	30 Ω	6 mm × 32.7 mm	
L3	microchoke	1 μH		4322 057 01080
L4	2 turns of 1.1 mm enamelled Cu wire	27 nH	int. diameter 4.5 mm length 2.9 mm leads 2 × 5 mm	
L5	stripline	30 Ω	6 mm × 24 mm	
L6	2 turns of 1.1 mm enamelled Cu wire	19 nH	int. diameter 3.5 mm length 3.5 mm leads 2 × 5 mm	
L2, L5	stripline; note 2			
R1, R2	carbon resistor	10 Ω		

Notes

1. American Technical Ceramics type 100B or capacitor of same quality.
2. The striplines are on a double Cu-clad printed-circuit board, with epoxy fibre-glass dielectric (ε_r = 4.5); thickness 1⁄16".

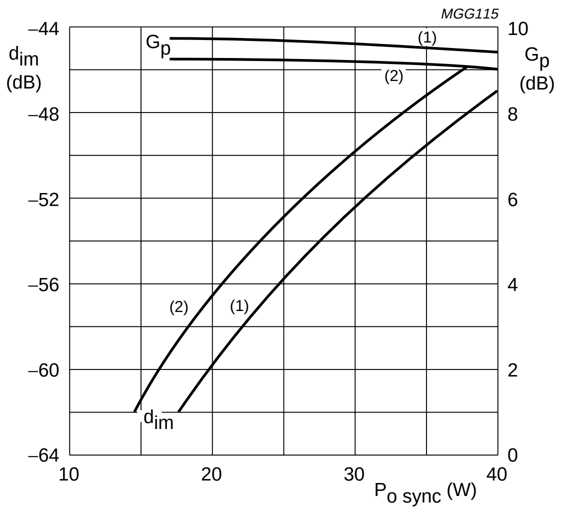


Dimensions in mm.

The circuit and the components are on one side of the epoxy fibre-glass board, the other side is unetched copper to serve as earth. Earth connections are made by hollow rivets. Additionally copper straps are used under the emitters and at the input and output to provide direct contact between the copper on the component side and the ground-plane.

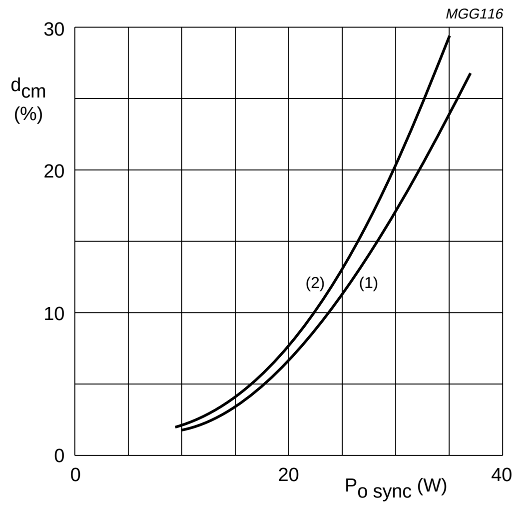
(1) C10 positioned under C11.

Fig.10 Component layout and printed-circuit board for 224.25 MHz class-A test circuit.



V_{CE} = 25 V; I_C = 3.2 A; f_{vision} = 224.25 MHz.
(1) T_h = 25 °C.
(2) T_h = 70 °C.

Fig.11 Intermodulation distortion and power gain as a functions of output power.



V_{CE} = 25 V; I_C = 3.2 A; f_{vision} = 224.25 MHz.
(1) T_h = 25 °C.
(2) T_h = 70 °C.

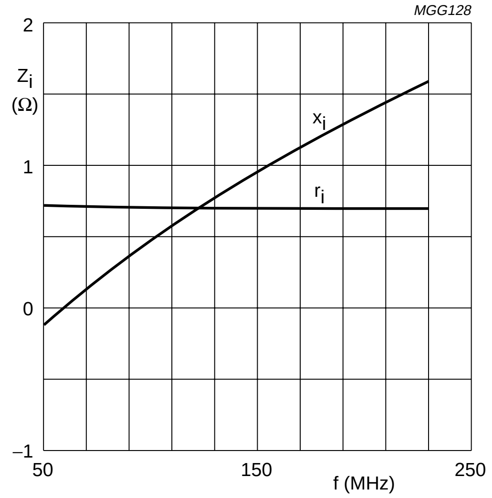
Fig.12 Cross-modulation distortion as a function of output power.

Three-tone test method (vision carrier –8 dB, sound carrier –7 dB, sideband signal –16 dB), zero dB corresponds to peak sync level (see Fig.11).

Two-tone test method (vision carrier 0 dB, sound carrier –7 dB), zero dB corresponds to peak sync level. Cross-modulation distortion (d_{cm}) is the voltage variation (%) of sound carrier when vision carrier is switched from 0 dB to –20 dB (see Fig.12).

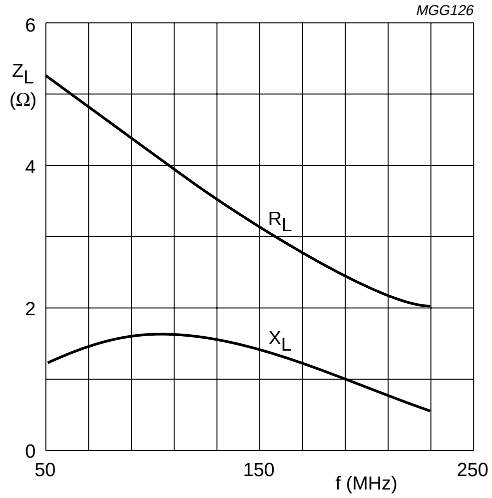
Ruggedness in class-A operation

The BLV33 is capable of withstanding a full load mismatch corresponding to VSWR = 50 : 1 through all phases up to 30 W (RMS) or 40 W (PEP) under the following conditions: V_{CE} = 25 V; I_C = 3.2 A; T_h = 70 °C; f = 224.25 MHz; $R_{th\ mb-h}$ = 0.15 K/W.



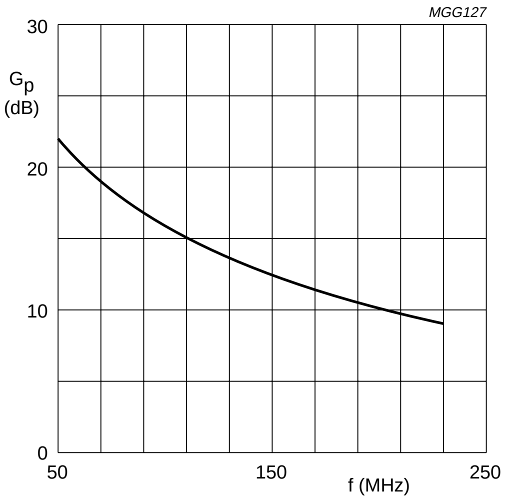
Class-A operation; V_{CE} = 25 V; I_C = 3.2 A; T_h = 70 °C.

Fig.13 Input impedance as a function of frequency (series components); typical values.



Class-A operation; V_{CE} = 25 V; I_C = 3.2 A; T_h = 70 °C.

Fig.14 Load impedance as a function of frequency (series components); typical values.



Class-A operation; V_{CE} = 25 V; I_C = 3.2 A; T_h = 70 °C.

Fig.15 Power gain as a function of frequency; typical values.

RF performance in VHF class-AB operation (C.W)

MODE OF OPERATION	f (MHz)	V_{CE} (V)	I_C, $I_{C(ZS)}$ (A)	T_h (°C)	P_L (W)	I_C (A)	η_C (%)	G_P (dB)[(1)]
CW, class-AB	224.25	28	0.1	70	40	typ. 2.60	typ. 55	typ. 7.5
					90	typ. 4.46	typ. 72	typ. 6.5

Note

1. Gain compression point of 1 dB is at typical 90 W (minimum 80 W). Using a 3rd-order amplitude transfer characteristic, 1 dB compression corresponds with 30 % sync input / 25 % sync output compression in television service (negative modulation, C.C.I.R. system).

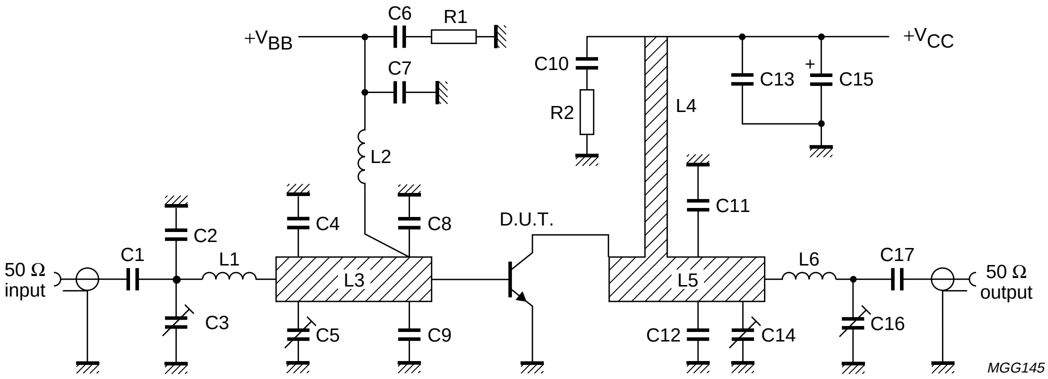


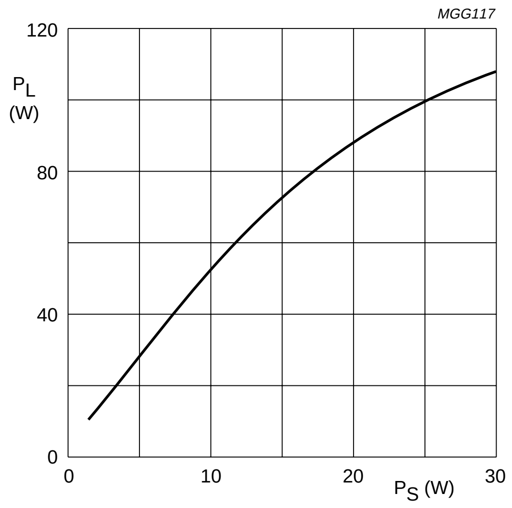
Fig.16 Class-AB test circuit at f_{vision} = 224.25 MHz.

List of components used in test circuit (see Fig.16)**.**

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE No.
C1, C17	multilayer ceramic chip capacitor; note 1	680 pF, 500 V		
C2	multilayer ceramic chip capacitor; note 1	39 pF, 500 V		
C3, C16	film dielectric trimmer	2 to 18 pF		2222 809 09003
C4	multilayer ceramic chip capacitor; note 1	43 pF, 500 V		
C5	film dielectric trimmer	4 to 40 pF		2222 809 08002
C6, C10	polyester capacitor	330 nF		
C7, C13	multilayer ceramic chip capacitor	680 pF, 50 V		2222 852 13681
C8, C9	multilayer ceramic chip capacitor; note 1	68 pF, 500 V	placed 2.5 mm from transistor edge	
C11, C12	multilayer ceramic chip capacitor; note 1	27 pF, 500 V	placed 7 mm from transistor edge	
C14	film dielectric trimmer	5 to 60 pF		2222 809 08003
C15	solid aluminium electrolytic capacitor	10 μF, 40 V		
L1	2 turns of 1.6 mm enamelled Cu wire	25 nH	int. diameter 4.3 mm length 3.4 mm leads 2 × 5 mm	
L2	4 turns closely wound 1.1 mm enamelled Cu wire	120 nH	int. diameter 6 mm leads 2 × 5 mm	
L3	stripline; note 2	30 Ω	6 mm × 48.8 mm	
L4	stripline; note 2	48 Ω	3 mm × 27 mm at 3 mm from transistor edge	
L5	stripline; note 2	30 Ω	6 × 42.9 mm	
L6	2 turns of 1.6 mm enamelled Cu wire	24 nH	int. diameter 4 mm length 3.4 mm leads 2 × 5 mm	
R1, R2	carbon resistor	10 Ω		

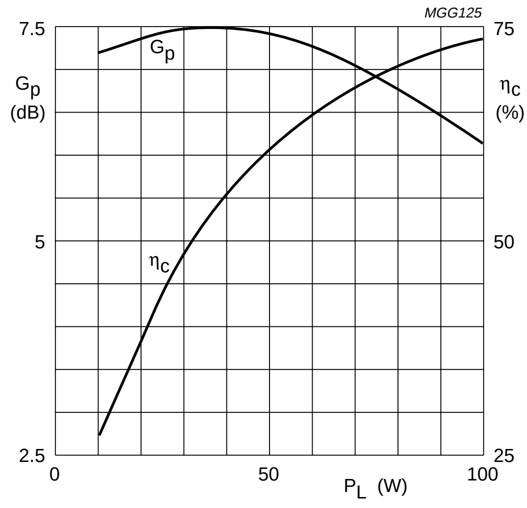
Notes

1. American Technical Ceramics type 100B or capacitor of same quality.
2. The striplines are on a double Cu-clad printed-circuit board, with epoxy fibre-glass dielectric (ε_r = 4.5); thickness $^1\!/_{16}$".



V_{CE} = 28 V; $I_{C(ZS)}$ = 0.1 A; T_h = 70 °C; f_{vision} = 224.25 MHz.

Fig.17 Load power as a function of source power; typical values.

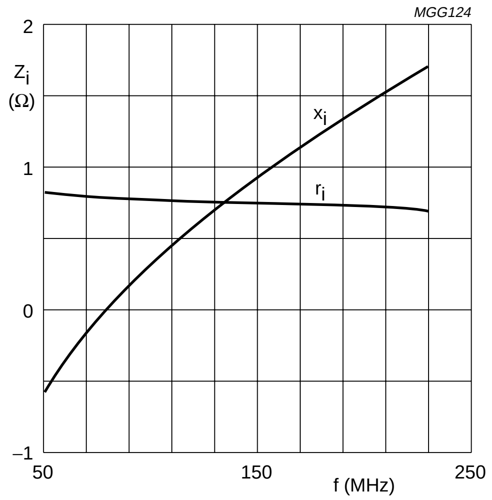


V_{CE} = 28 V; $I_{C(ZS)}$ = 0.1 A; T_h = 70 °C; f_{vision} = 224.25 MHz.

Fig.18 Power gain and efficiency as functions of load power; typical values.

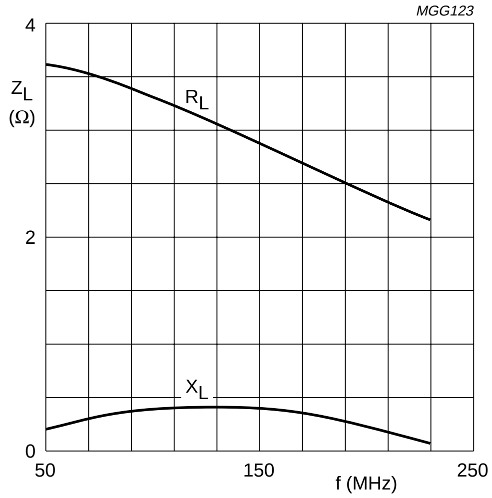
Ruggedness in class-AB operation

The BLV33 is capable of withstanding a full load mismatch corresponding to VSWR ≤ 2 through all phases) up to 60 W (RMS) and 90 W (PEP) under the following conditions: V_{CE} = 28 V; T_h = 70 °C; f = 224.25 MHz; $R_{th\ mb-h}$ = 0.15 K/W.



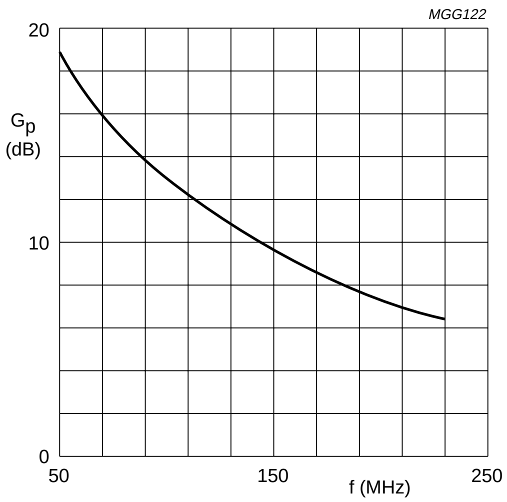
Class-AB operation; V_{CE} = 28 V; P_L = 80 W (PEP); T_h = 70 °C.

Fig.19 Input impedance (series components); typical values.



Class-AB operation; V_{CE} = 28 V; P_L = 80 W (PEP); T_h = 70 °C.

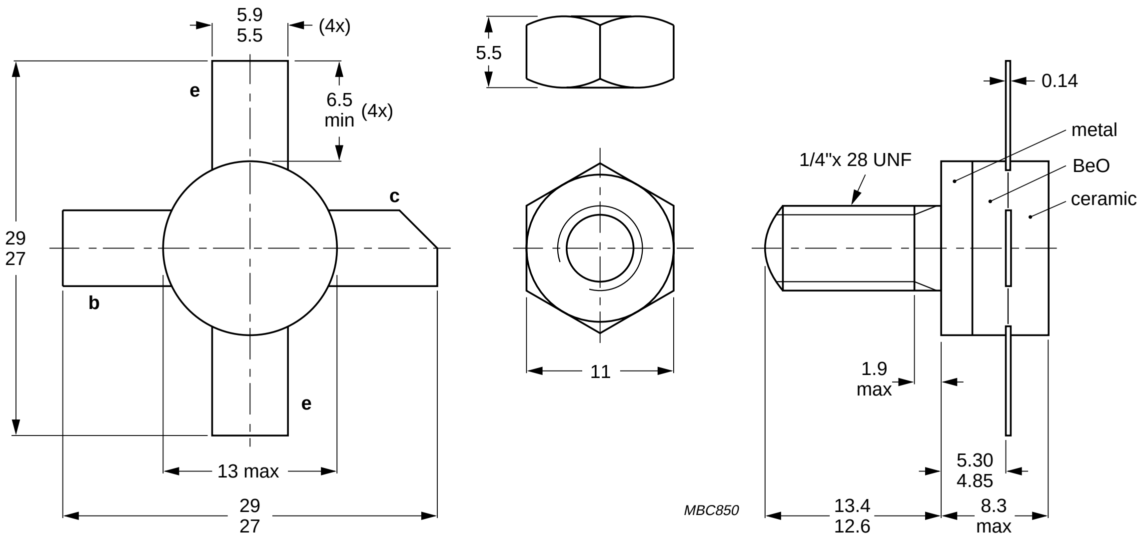
Fig.20 Load impedance (series components); typical values.



Class-AB operation; V_{CE} = 28 V; P_L = 80 W (PEP); T_h = 70 °C.

Fig.21 Power gain as a function of frequency; typical values.

PACKAGE OUTLINE



Dimensions in mm.
Torque on nut: min. 2.3 Nm; max. 2.7 Nm.
Diameter of clearance hole in heatsink: max. 6.4 mm.
Mounting hole to have no burrs at either end.
De-burring must leave surface flat; do not chamfer or countersink either end of hole.
When locking is required an adhesive is preferred instead of a lock washer.

Fig.22 SOT147.

DEFINITIONS

Data Sheet Status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

NOTES

NOTES

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