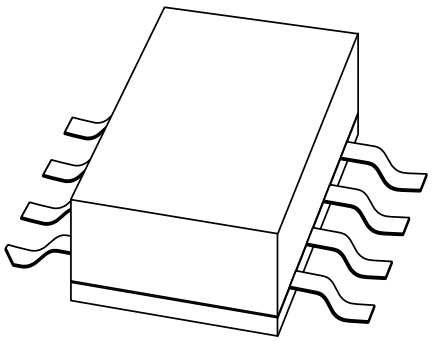
DATA SHEET



BLV2042
UHF power transistor

Product specification
Supersedes data of 1997 July 11

2000 May 08

Philips
Semiconductors

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UHF power transistor BLV2042

FEATURES

- Emitter ballasting resistors for optimum temperature profile
- Gold metallization ensures excellent reliability
- Internal input matching to achieve high power gain and easy design of wideband circuits.

APPLICATIONS

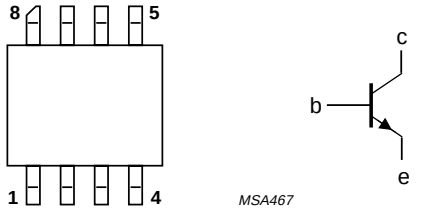
- Common emitter class-AB operation in base stations in the 1800 to 1990 MHz frequency range.

DESCRIPTION

NPN silicon planar epitaxial power transistor in an 8-lead SOT409A SMD package with ceramic cap.
All leads are isolated from the mounting base.

PINNING - SOT409A

PIN	DESCRIPTION
1, 4, 5 and 8	emitter
2 and 3	base
6 and 7	collector



Top view

Fig.1 Simplified outline and symbol.

QUICK REFERENCE DATA

RF performance at T_{mb} = 25 °C in a common emitter test circuit.

MODE OF OPERATION	f (MHz)	V_{CE} (V)	P_L (W)	G_p (dB)	η_C (%)	d_{im} (dBc)
CW, class-AB	1950	26	4	≥11	≥40	–
CW, class-AB	1990	26	4	≥11	≥40	–
2-tone, class-AB	f_1 = 1950; f_2 = 1950.1	26	4 (PEP)	typ. 14	typ. 35	typ. –30

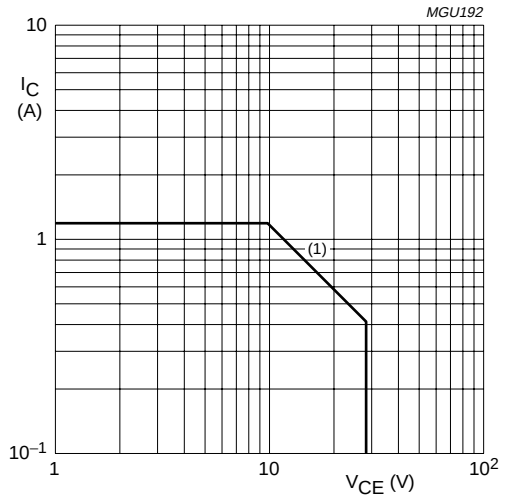
LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 60134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
V_{CBO}	collector-base voltage	open emitter	–	60	V
V_{CEO}	collector-emitter voltage	open base	–	28	V
V_{EBO}	emitter-base voltage	open collector	–	4	V
I_C	collector current (DC)		–	1.2	A
$I_{C(AV)}$	collector current (average)		–	1.2	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; note 1	–	14.6	W
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	200	°C

Note

1. Transistor with metallized ground plane mounted on a printed-circuit board, see *"Mounting and soldering recommendations in the General part of the associated handbook"*.



(1) T_s = 60 °C.

Fig.2 DC SOAR.

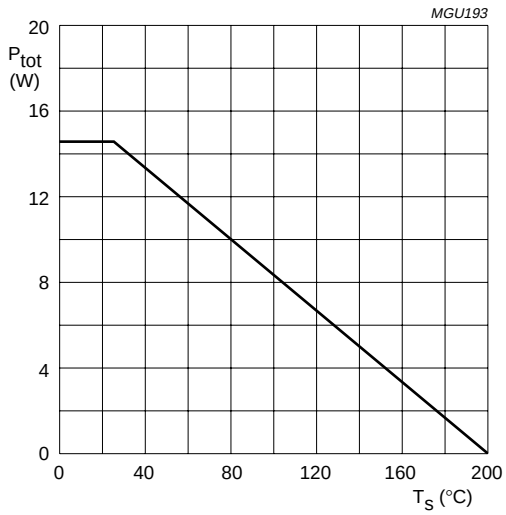


Fig.3 Total power dissipation as a function of the soldering point temperature.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	P_{tot} = 14.6 W; T_{mb} = 25 °C; note 1	12	K/W

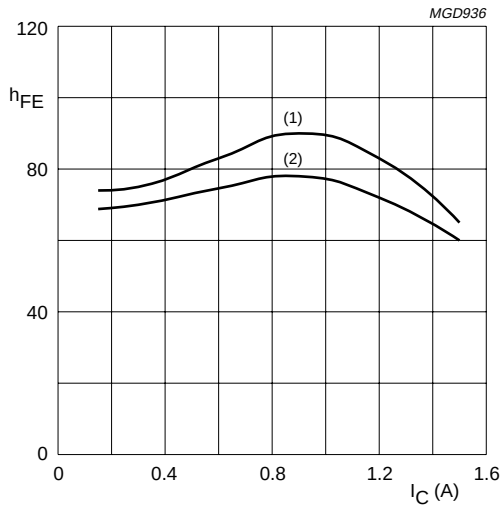
Note

1. Transistor with metallized ground plane mounted on a printed-circuit board, see *"Mounting and soldering recommendations in the General part of the associated handbook"*.

CHARACTERISTICS

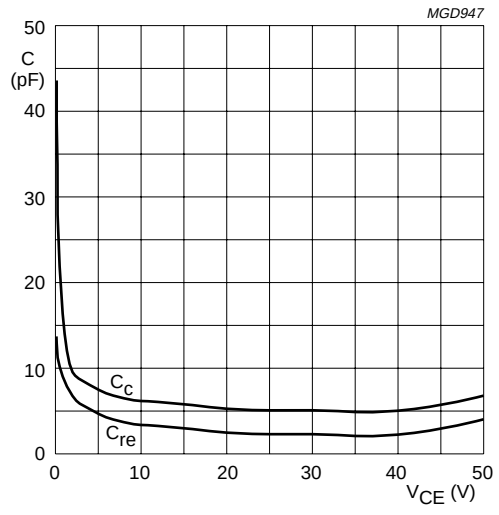
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)CBO}$	collector-base breakdown voltage	open emitter; I_C = 5 mA	60	–	–	V
$V_{(BR)CEO}$	collector-emitter breakdown voltage	open base; I_C = 10 mA	28	–	–	V
$V_{(BR)EBO}$	emitter-base breakdown voltage	open collector; I_E = 0.5 mA	4	–	–	V
I_{CES}	collector leakage current	V_{CE} = 26 V; V_{BE} = 0	–	–	1.3	mA
h_{FE}	DC current gain	V_{CE} = 26 V; I_C = 600 mA	30	–	120	
C_c	collector capacitance	V_{CB} = 26 V; I_E = i_e = 0; f = 1 MHz	–	6	–	pF
C_{re}	feedback capacitance	V_{CE} = 26 V; I_C = 0; f = 1 MHz	–	2.5	–	pF



(1) V_{CE} = 26 V; t_p = 500 μs; δ = < 1 %.
(2) V_{CE} = 10 V.

Fig.4 DC current gain as a function of collector current; typical values.



f = 1 MHz.

Fig.5 Capacitance as a function of collector-emitter voltage; typical values.

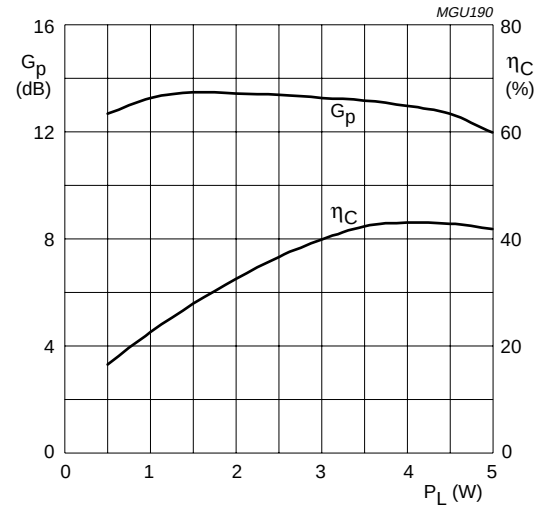
APPLICATION INFORMATION

RF performance at T_{mb} = 25 °C in a common emitter test circuit.

MODE OF OPERATION	f (MHz)	V_{CE} (V)	I_{CQ} (mA)	P_L (W)	G_p (dB)	η_C (%)	d_{im} (dBc)
CW, class-AB	1950	26	15	4	≥11 typ. 13	≥40 typ. 43	–
CW, class-AB	1990	26	15	4	≥11	≥40	–
2-tone, class-AB	f_1 = 1950; f_2 = 1950.1	26	15	4 (PEP)	typ. 14	typ. 35	typ. –30

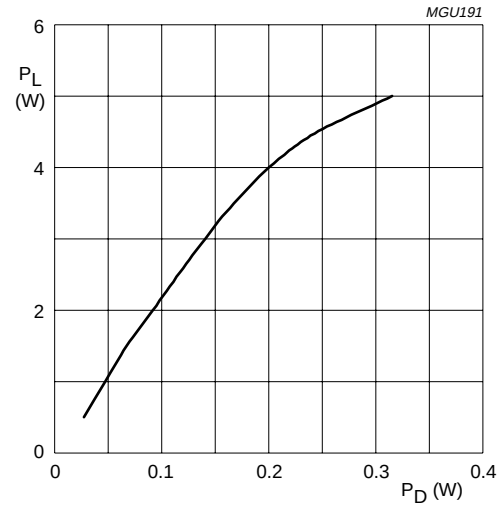
Ruggedness in class-AB operation

The BLV2042 is capable of withstanding a load mismatch corresponding to VSWR = 20 : 1 through all phases under the following conditions: f = 1950 MHz; V_{CE} = 26 V; I_{CQ} = 15 mA; P_L = 4 W; T_{mb} = 25 °C.



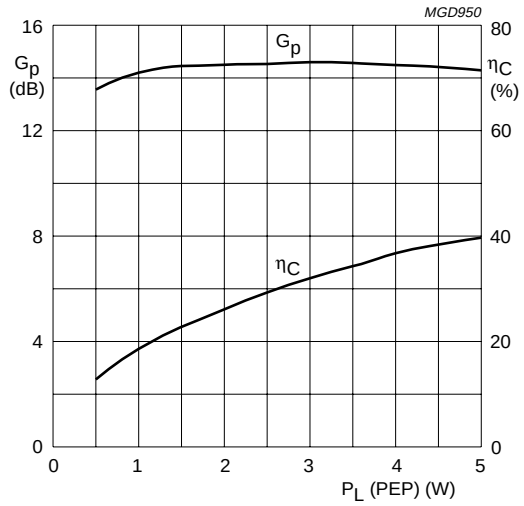
CW, class-AB; V_{CE} = 26 V; I_{CQ} = 15 mA; f = 1950 MHz; T_{mb} = 25 °C.

Fig.6 Power gain and collector efficiency as functions of load power; typical values.



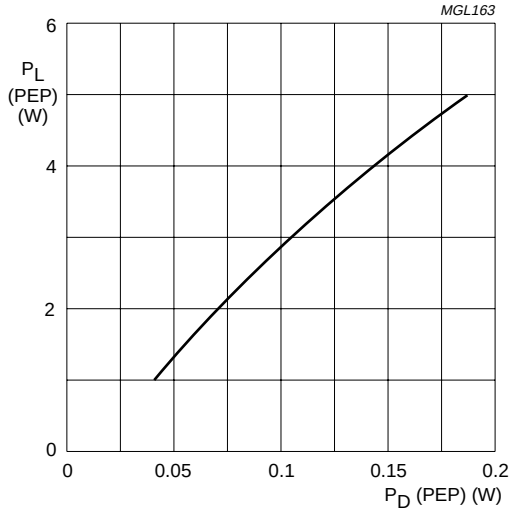
CW, class-AB; V_{CE} = 26 V; I_{CQ} = 15 mA; f = 1950 MHz; T_{mb} = 25 °C.

Fig.7 Load power as a function of drive power; typical values.



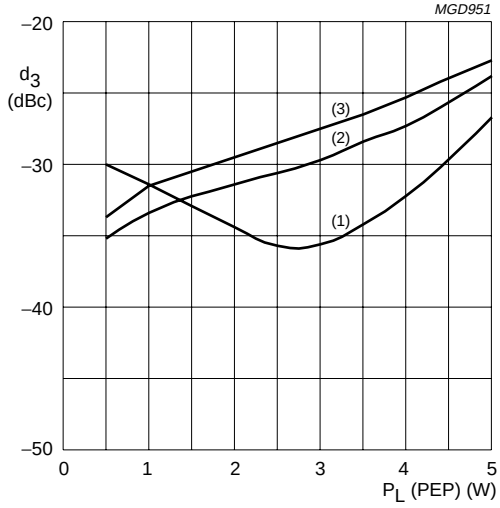
V_{CE} = 26 V; I_{CQ} = 15 mA; f_1 = 1950 MHz; f_2 = 1950.1 MHz.

Fig.8 Power gain and collector efficiency as functions of peak envelope load power; typical values.



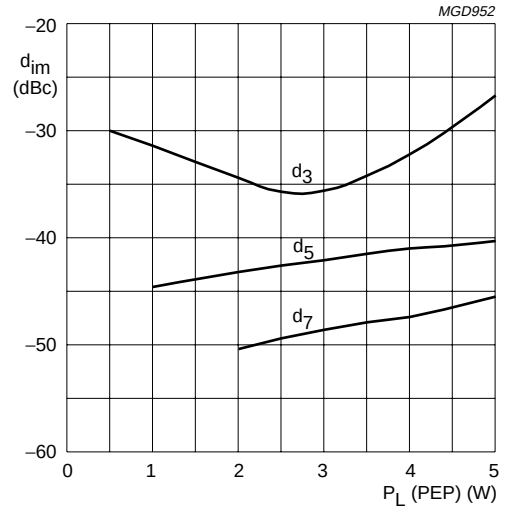
V_{CE} = 26 V; I_{CQ} = 15 mA; f_1 = 1950 MHz; f_2 = 1950.1 MHz.

Fig.9 Peak envelope load power as a function of peak envelope drive power; typical values.



V_{CE} = 26 V; f_1 = 1950 MHz; f_2 = 1950.1 MHz.
(1) I_{CQ} = 15 mA. (2) I_{CQ} = 40 mA. (3) I_{CQ} = 60 mA.

Fig.10 Third order intermodulation distortion as a function of peak envelope load power; typical values.



V_{CE} = 26 V; I_{CQ} = 15 mA; f_1 = 1950 MHz; f_2 = 1950.1 MHz.

Fig.11 Intermodulation distortion as a function of peak envelope load power; typical values.

Test circuit information

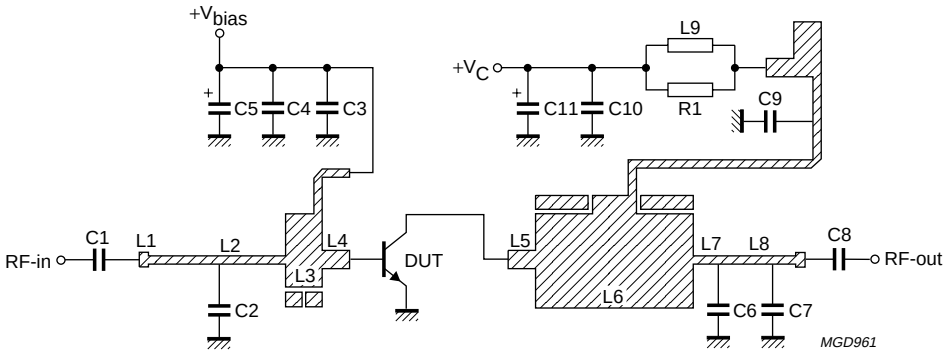


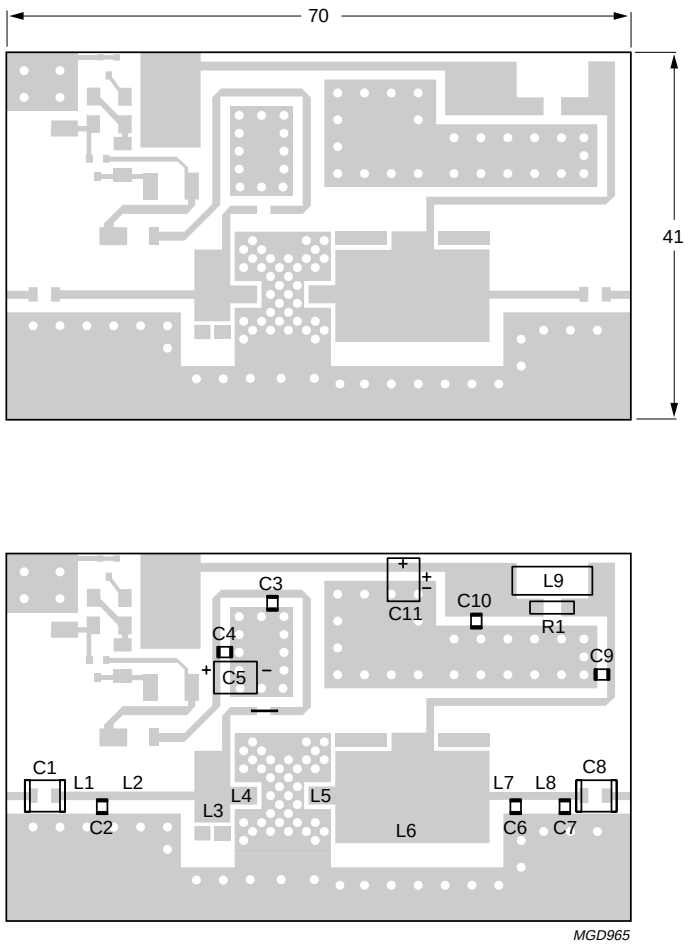
Fig.12 Class-AB test circuit at 1950 MHz.

List of components (see Figs 12 and 13)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE No.
C1, C9	multilayer ceramic chip capacitor; note 1	100 pF		
C2, C6	multilayer ceramic chip capacitor; note 2	3 pF		
C3, C8	multilayer ceramic chip capacitor; note 2	27 pF		
C4, C10	multilayer ceramic chip capacitor	100 nF		2222 581 16641
C5, C11	tantalum SMD capacitor	47 μF; 35 V		
C7	multilayer ceramic chip capacitor; note 2	1.2 pF		
L1	stripline; note 3	50 Ω	length 9.9 mm width 0.91 mm	
L2	stripline; note 3	50 Ω	length 6.66 mm width 0.91 mm	
L3	stripline; note 3	10 Ω	length 4 mm width 8 mm	
L4	stripline; note 3	31 Ω	length 3 mm width 2 mm	
L5	stripline; note 3	31 Ω	length 3 mm width 2 mm	
L6	stripline; note 3	8.3 Ω	length 17.25 mm width 10.3 mm	
L7	stripline; note 3	50 Ω	length 2.42 mm width 0.91 mm	
L8	stripline; note 3	50 Ω	length 6.14 mm width 0.91 mm	
L9	grade 4S2 ferroxcube chip-bead			4330 030 36301
R1	metal film resistor	100 Ω; 0.4 W		

Notes

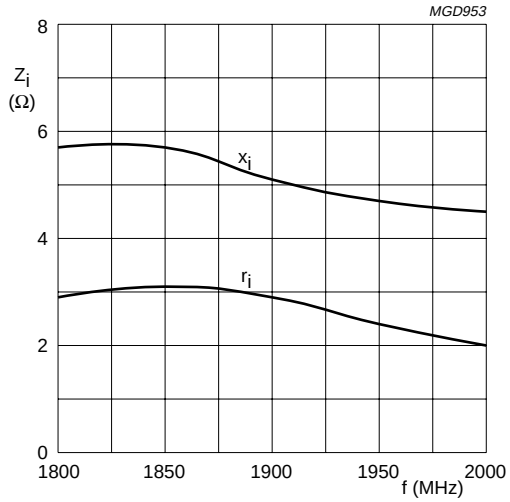
1. American Technical Ceramics type 100B or capacitor of the same quality.
2. American Technical Ceramics type 100A or capacitor of the same quality.
3. The striplines are on a double copper-clad printed-circuit board with epoxy fibreglass dielectric (ε_r = 6.15); thickness 0.64 mm.



Dimensions in mm.

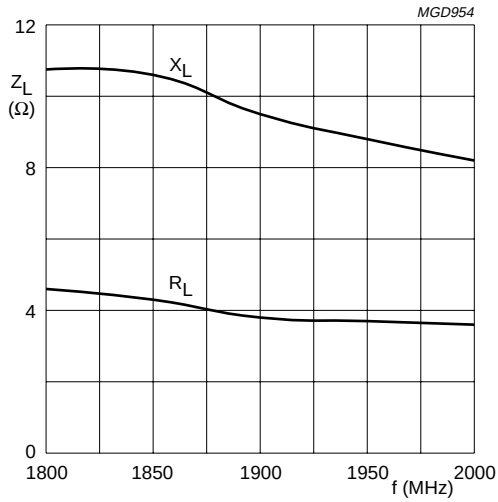
The components are situated on one side of the copper-clad epoxy fibreglass board, the other side is not etched and serves as a ground plane. Earth connections from the component side to the ground plane are made by through metallization.

Fig.13 Component layout for 1950 MHz class-AB test circuit.



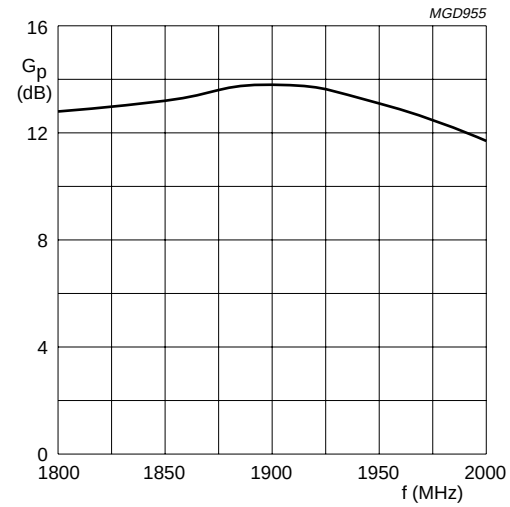
V_{CE} = 26 V; I_{CQ} = 15 mA; P_L = 4 W; T_{mb} = 25 °C.

Fig.14 Input impedance as a function of frequency (series components); typical values.



V_{CE} = 26 V; I_{CQ} = 15 mA; P_L = 4 W; T_{mb} = 25 °C.

Fig.15 Load impedance as a function of frequency (series components); typical values.



V_{CE} = 26 V; I_{CQ} = 15 mA; P_L = 4 W; T_{mb} = 25 °C.

Fig.16 Power gain as a function of frequency; typical values.

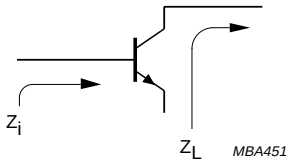


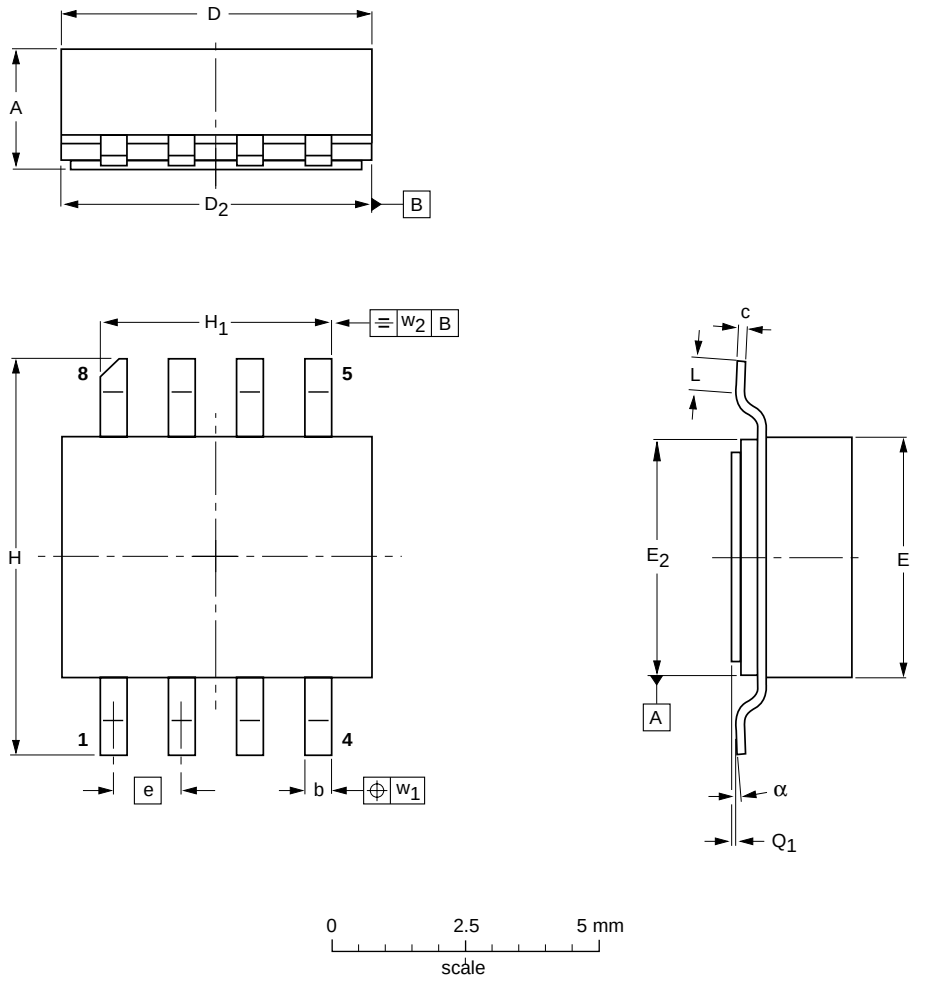
Fig.17 Definition of transistor impedance.

MOUNTING RECOMMENDATIONS

Heat from the device is transferred via the leads and the metallized underside. For optimum heat transfer it is recommended that the transistor be mounted on a grounded metallized area on the component side of the printed-circuit board. This metallized area should contain a large number of metallized, solder-filled through-holes. The non-component side of the printed-circuit board forms a ground plane. When the printed-circuit board is mounted on the heatsink using heatsink compound, a thermal resistance from mounting base to heatsink of 0.9 K/W can be attained.

PACKAGE OUTLINE

Ceramic surface mounted package; 8 leads **SOT409A**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_2	E	E_2	e	H	H_1	L	Q_1	w_1	w_2	α
mm	2.36 2.06	0.58 0.43	0.23 0.18	5.94 5.03	5.16 5.00	4.93 4.01	4.14 3.99	1.27	7.47 7.26	4.39 4.24	1.02 0.51	0.10 0.00	0.25	0.25	7° 0°
inches	0.093 0.081	0.023 0.017	0.009 0.007	0.234 0.198	0.203 0.197	0.194 0.158	0.163 0.157	0.050	0.294 0.286	0.173 0.167	0.040 0.020	0.004 0.000	0.010	0.010	7° 0°

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT409A						98-01-27

DATA SHEET STATUS

DATA SHEET STATUS	PRODUCT STATUS	DEFINITIONS [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

Note

1. Please consult the most recently issued data sheet before initiating or completing a design.

DEFINITIONS

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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