DATA SHEET

BLF247B
VHF push-pull power MOS transistor

Product specification

August 1994

Philips Semiconductors

PHILIPS

VHF push-pull power MOS transistor BLF247B

FEATURES

- High power gain
- Easy power control
- Good thermal stability
- Withstands full load mismatch.

APPLICATIONS

- Large signal applications in the VHF frequency range.

DESCRIPTION

Silicon N-channel enhancement mode vertical D-MOS push-pull transistor encapsulated in a 4-lead, SOT262A1 balanced flange type package with two ceramic caps. The mounting flange provides the common source connection for the transistor.

PIN CONFIGURATION

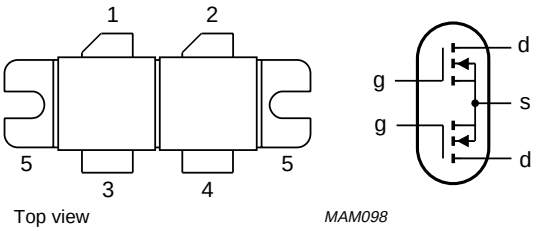


Fig.1 Simplified outline and symbol.

CAUTION

The device is supplied in a antistatic package. The gate-source input must be protected against static charge during transport or handling.

PINNING - SOT262A1

PIN	DESCRIPTION
1	drain 1
2	drain 2
3	gate 1
4	gate 2
5	source

WARNING

Product and environmental safety - toxic materials
This product contains beryllium oxide. The product is entirely safe provided that the BeO discs are not damaged. All persons who handle, use or dispose of this product should be aware of its nature and of the necessary safety precautions. After use, dispose of as chemical or special waste according to the regulations applying at the location of the user. It must never be thrown out with the general or domestic waste.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)
CW, class-B	225	28	150	≥12	≥55

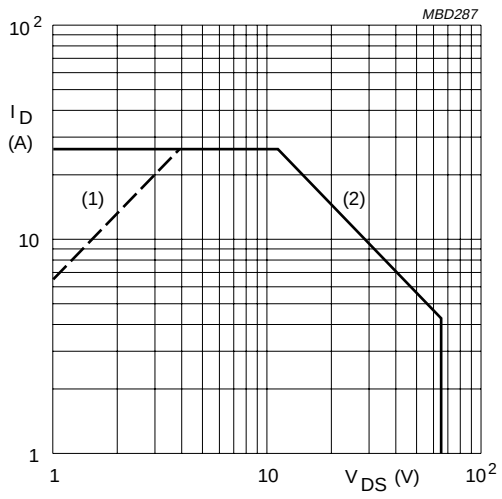
LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
Per transistor section					
V_{DS}	drain-source voltage (DC)		–	65	V
V_{GS}	gate-source voltage		–	±20	V
I_D	drain current (DC)		–	13	A
P_{tot}	total power dissipation	up to T_{mb} = 25 °C; total device; both sections equally loaded	–	280	W
T_{stg}	storage temperature		–65	+150	°C
T_j	operating junction temperature		–	+200	°C

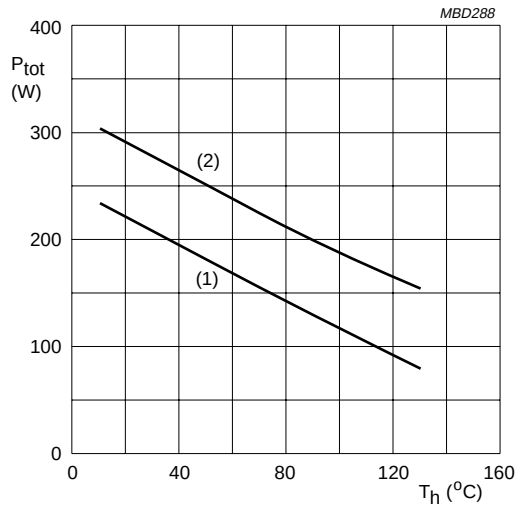
THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}mb}$	thermal resistance from junction to mounting base	total device; both sections equally loaded	0.63	K/W
$R_{th\ mb\text{-}h}$	thermal resistance from mounting base to heatsink	total device; both sections equally loaded	0.15	K/W



Total device; both sections equally loaded.
(1) Current in this area may be limited by R_{DSon}.
(2) T_{mb} = 25 °C.

Fig.2 DC SOAR.



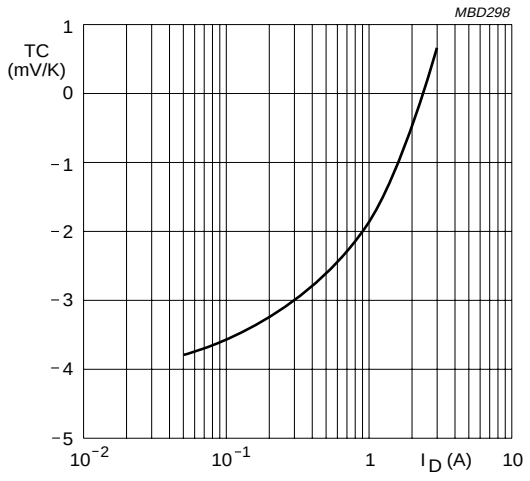
Total device; both sections equally loaded.
(1) Continuous operation.
(2) Short-time operation during mismatch.

Fig.3 Power derating curves.

CHARACTERISTICS

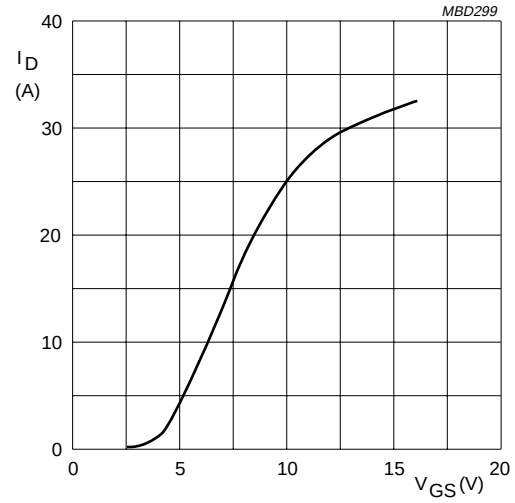
T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Per transistor section						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 50 mA; V_{GS} = 0	65	–	–	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 28 V	–	–	2.5	mA
I_{GSS}	gate-source leakage current	V_{GS} = ±20 V; V_{DS} = 0	–	–	1	µA
V_{GSth}	gate-source threshold voltage	I_D = 50 mA; V_{DS} = 10 V	2	–	4.5	V
g_{fs}	forward transconductance	I_D = 5 A; V_{GS} = 10 V	3	4.2	–	S
R_{DSon}	drain-source on-state resistance	I_D = 5 A; V_{GS} = 10 V	–	0.2	0.3	Ω
I_{DSX}	drain cut-off current	V_{GS} = 10 V; V_{DS} = 10 V	–	22	–	A
C_{is}	input capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	225	–	pF
C_{os}	output capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	180	–	pF
C_{rs}	reverse transfer capacitance	V_{GS} = 0; V_{DS} = 28 V; f = 1 MHz	–	25	–	pF



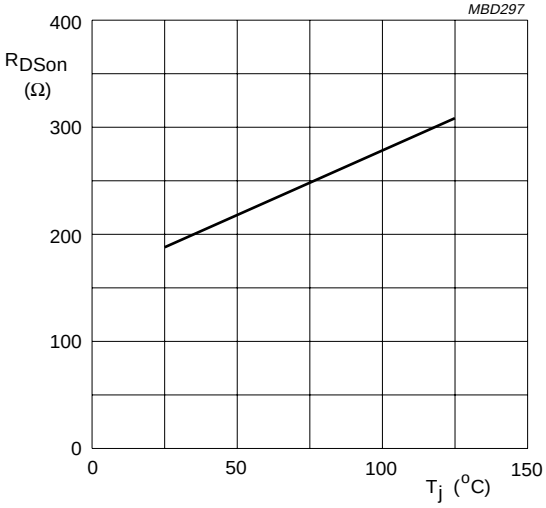
V_{DS} = 10 V.

Fig.4 Temperature coefficient of gate-source voltage as a function of drain current, typical values per section.



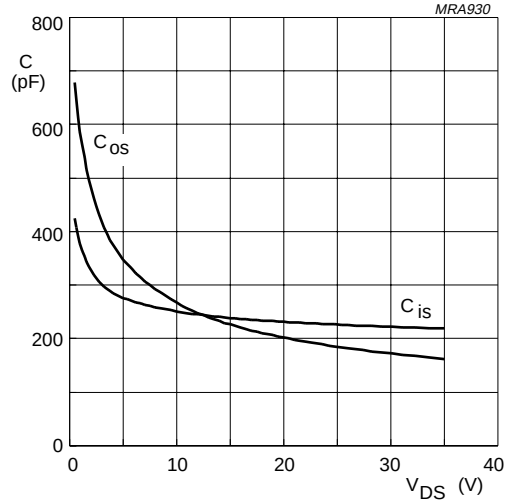
V_{DS} = 10 V.

Fig.5 Drain current as a function of gate-source voltage, typical values per section.



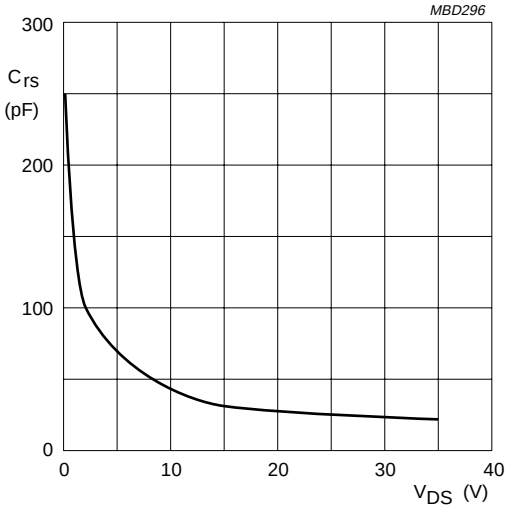
I_D = 5 A; V_{GS} = 10 V.

Fig.6 Drain-source on-state resistance as a function of junction temperature, typical values per section.



V_{GS} = 0; f = 1 MHz.

Fig.7 Input and output capacitance as functions of drain-source voltage, typical values per section.



V_{GS} = 0; f = 1 MHz.

Fig.8 Reverse transfer capacitance as a function of drain-source voltage, typical values per section.

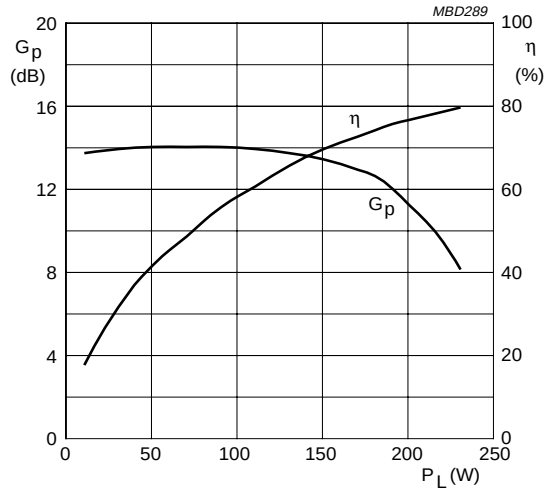
APPLICATION INFORMATION

RF performance in a push-pull, common source, class-B test circuit: T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.15 K/W.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (mA)	P_L (W)	G_p (dB)	η_D (%)
CW, class-B	225	28	2 × 100	150	≥12 typ. 13.5	≥55 typ. 70

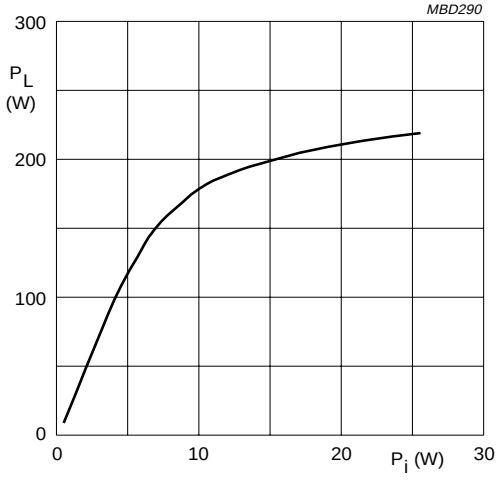
Ruggedness in class-B operation

The BLF247B is capable of withstanding a full load mismatch corresponding to VSWR = 50 through all phases under the following conditions: V_{DS} = 28 V; f = 175 MHz; T_h = 25 °C; P_L = 150 W; $R_{th\ mb\text{-}h}$ = 0.15 K/W.



Class-B operation.
V_{DS} = 28 V.
I_{DQ} = 2 × 100 mA.
Z_L = 1.3 + j0.6 Ω per section.
f = 225 MHz.

Fig.9 Power gain and efficiency as functions of load power; typical values.



Class-B operation.
V_{DS} = 28 V.
I_{DQ} = 2 × 100 mA.
Z_L = 1.3 + j0.6 Ω per section.
f = 225 MHz.

Fig.10 Load power as a function of input power; typical values.

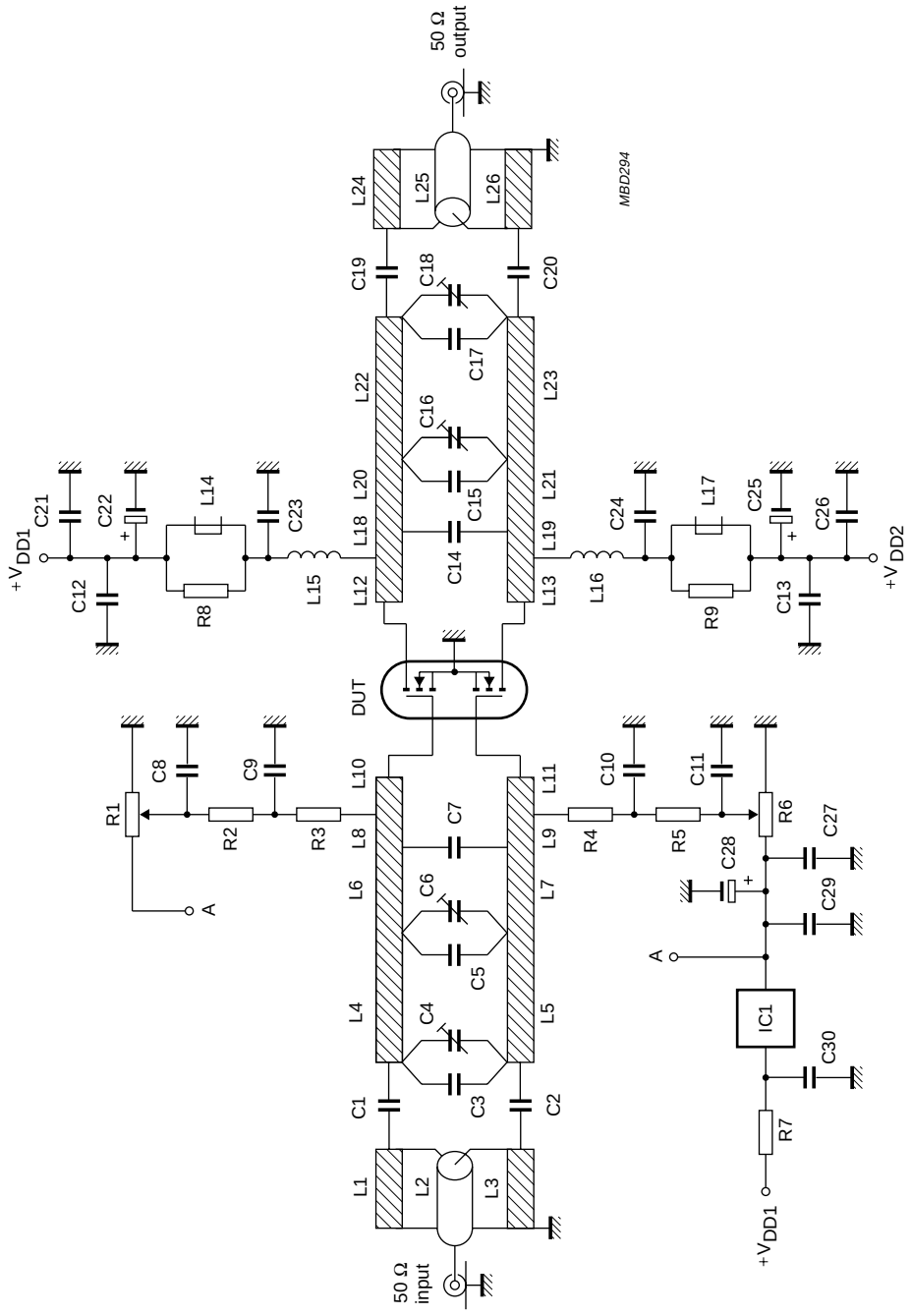


Fig.11 Test circuit for Class-B operation at 225 MHz.

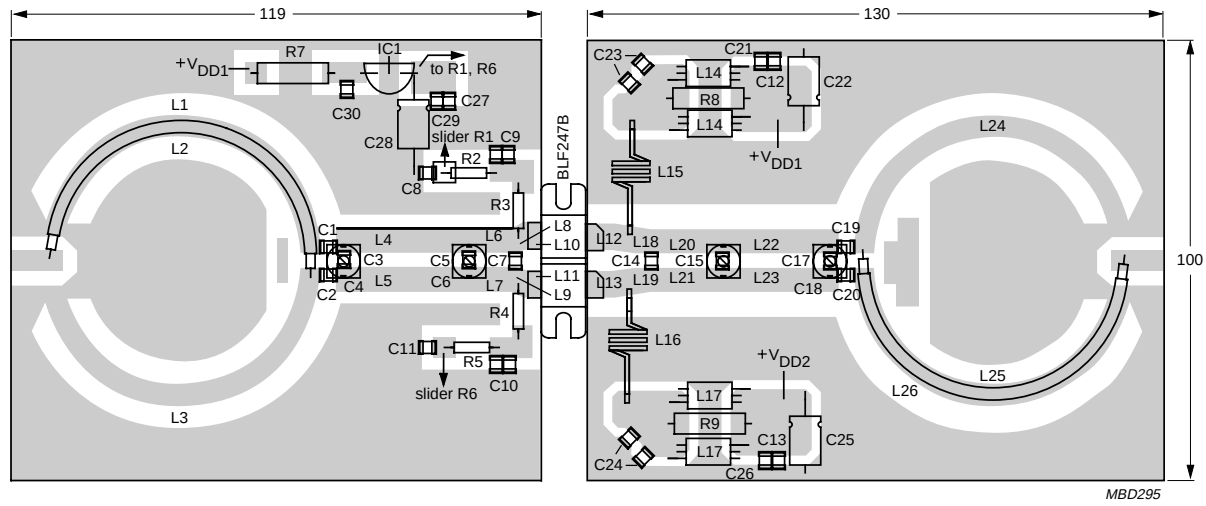
List of components (see Figs 11 and 12)

COMPONENT	DESCRIPTION	VALUE	DIMENSION	CATALOGUE NO.
C1, C2	multilayer ceramic chip capacitor; note 1	200 pF		
C3	multilayer ceramic chip capacitor; note 1	27 pF		
C4, C6, C18	film dielectric trimmer	2 to 9 pF		2222 809 09005
C5	multilayer ceramic chip capacitor; note 1	39 pF		
C7	multilayer ceramic chip capacitor; note 1	91 pF		
C8, C11, C12, C13, C27	multilayer ceramic chip capacitor	100 nF; 50 V		2222 852 47104
C9, C10	multilayer ceramic chip capacitor; note 1	2×1 nF in parallel		
C14	multilayer ceramic chip capacitor; note 1	2×36 pF in parallel		
C15	multilayer ceramic chip capacitor; note 1	18 pF		
C16	film dielectric trimmer	2 to 18 pF		2222 809 09006
C17	multilayer ceramic chip capacitor; note 1	6.8 pF		
C19, C20	multilayer ceramic chip capacitor; note 1	47 pF		
C21, C26, C29, C30	multilayer ceramic chip capacitor; note 1	1 nF		
C22, C25, C28	electrolytic capacitor	10 μF; 63 V		2222 030 38109
C23, C24	multilayer ceramic chip capacitor; note 1	2×470 nF in parallel		
L1, L3, L24, L26	stripline; note 2	50 Ω	length 80 mm width 4.8 mm	
L2, L25	semi-rigid cable; note 3	50 Ω	ext. conductor: length 80 mm diameter 3.6 mm	
L4, L5	stripline; note 2	43 Ω	length 30 mm width 6 mm	
L6, L7	stripline; note 2	43 Ω	length 10 mm width 6 mm	
L8, L9	stripline; note 2	43 Ω	length 2 mm width 6 mm	
L10, L11	stripline; note 2	43 Ω	length 4 mm width 6 mm	
L12, L13	stripline; note 2	43 Ω	length 10 mm width 6 mm	
L14, L17	Ferroxcube grade 3B wideband HF choke	2 in parallel		4312 02036642

COMPONENT	DESCRIPTION	VALUE	DIMENSION	CATALOGUE NO.
L15, L16	3 turns enamelled 1.6 mm copper wire	50 nH	length 7.8 mm internal diameter 6 mm leads 2 × 10 mm	
L18, L19	stripline; note 2	43 Ω	length 6 mm width 6 mm	
L20, L21	stripline; note 2	43 Ω	length 15 mm width 6 mm	
L22, L23	stripline; note 2	43 Ω	length 26.5 mm width 6 mm	
R1, R6	10 turns potentiometer	50 kΩ		
R2, R3, R4, R5	metal film resistor	1 kΩ; 0.4 W		
R7	metal film resistor	5.11 kΩ; 1 W		
R8, R9	metal film resistor	10 Ω; 1 W		
IC1	voltage regulator			78L05

Notes

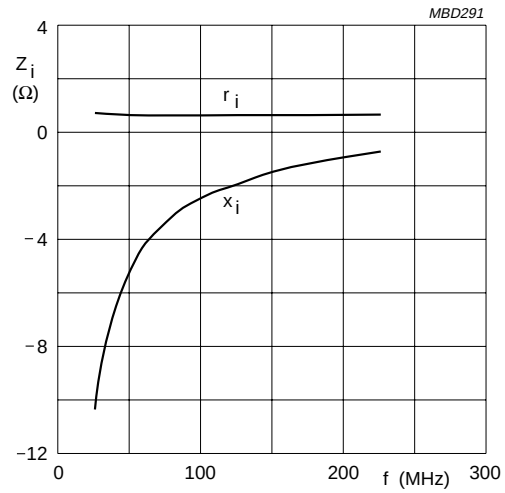
1. American Technical Ceramics type 100B or capacitor of same quality.
2. The striplines are on a double copper-clad printed-circuit board with glass microfibre PTFE dielectric (ε_r = 2.2); thickness $^1/_{16}$ inch; thickness of the copper sheet 2 × 35 μm.
3. Semi-rigid cables L2 and L25 are soldered onto striplines L1 and L26.



Dimensions in mm.

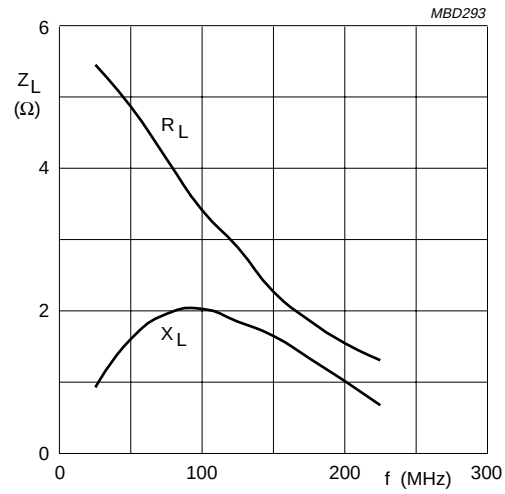
The circuit and components are situated on one side of the printed-circuit board, the other side being fully metallized to serve as a ground plane. Earth connections are made by means of copper straps and hollow rivets for a direct contact between upper and lower sheets.

Fig.12 Component layout for 225 MHz class-B test circuit.



V_{DS} = 28 V.
I_{DQ} = 2 × 100 mA.
T_h = 25 °C.
P_L = 150 W (total device).

Fig.13 Input impedance as a function of frequency (series components), typical values per section.



V_{DS} = 28 V.
I_{DQ} = 2 × 100 mA.
T_h = 25 °C.
P_L = 150 W (total device).

Fig.14 Load impedance as a function of frequency (series components), typical values per section.

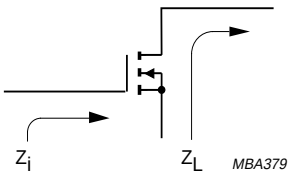
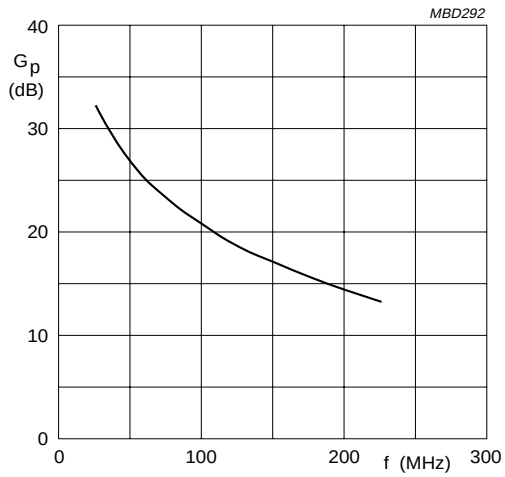


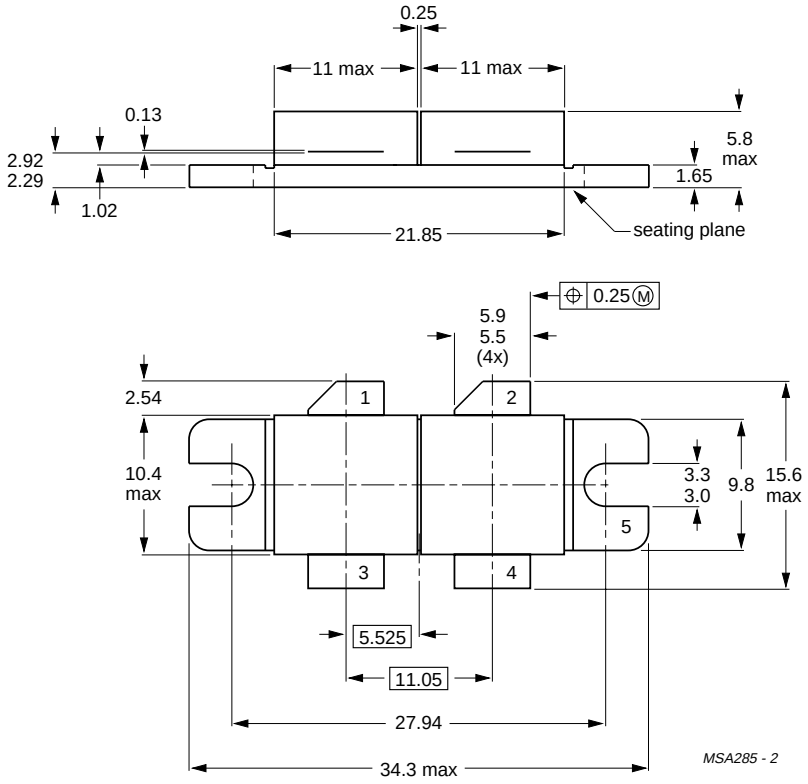
Fig.15 Definition of MOS impedances.



V_{DS} = 28 V.
I_{DQ} = 2 × 100 mA.
T_h = 25 °C.
P_L = 150 W (total device).

Fig.16 Power gain as a function of frequency, typical values per section.

PACKAGE OUTLINE



Dimensions in mm.

Fig.17 SOT262A1.

DEFINITIONS

Data Sheet Status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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