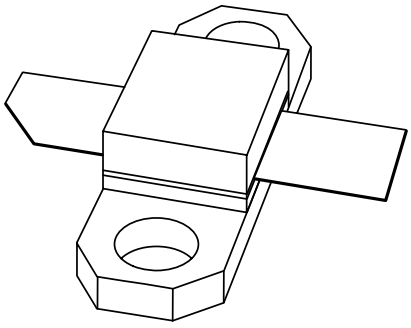
DATA SHEET



BLF2045
UHF power LDMOS transistor

Product specification
Supersedes data of 2000 Jan 04

2000 Feb 17

Philips
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UHF power LDMOS transistor BLF2045

FEATURES

- High power gain
- Easy power control
- Excellent ruggedness
- Source on underside eliminates DC isolators, reducing common mode inductance
- Designed for broadband operation.

APPLICATIONS

- Communication transmitter applications (PCN/PCS) in the 1.8 to 2.2 GHz frequency range.

DESCRIPTION

Silicon N-channel enhancement mode lateral D-MOS transistor encapsulated in a 2-lead flange package (SOT467C) with a ceramic cap. The common source is connected to the mounting flange.

PINNING - SOT467C

PIN	DESCRIPTION
1	drain
2	gate
3	source, connected to flange

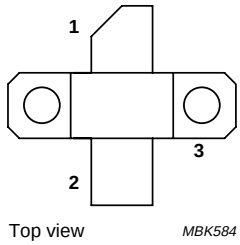


Fig.1 Simplified outline.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in a common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)	d_{im} (dBc)
2-tone, class-AB	f_1 = 2000; f_2 = 2000.1	26	30 (PEP)	>10	>30	≤–25

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage	–	65	V
V_{GS}	gate-source voltage	–	±15	V
I_D	drain current (DC)	–	4.5	A
T_{stg}	storage temperature	–65	150	°C
T_j	junction temperature	–	200	°C

CAUTION
This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A and SNW-FQ-302B.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}h}$	thermal resistance from junction to heatsink	P_{tot} = 87.5 W; T_h = 25 °C; note 1	2.1	K/W

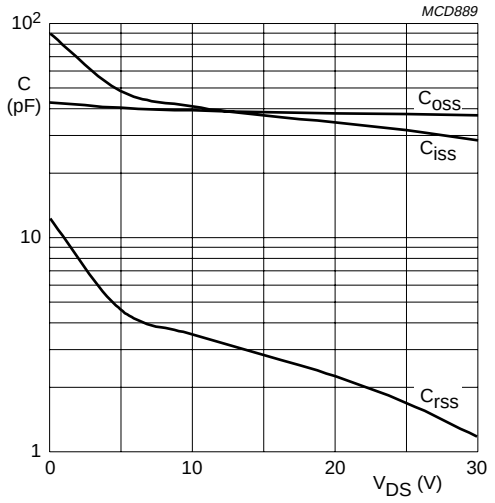
Note

1. Thermal resistance is determined under specified RF operating conditions.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 0.7 mA	65	–	–	V
V_{GSth}	gate-source threshold voltage	V_{DS} = 10 V; I_D = 70 mA	1.5	–	3.5	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 26 V	–	–	5	μA
I_{DSX}	drain cut-off current	V_{GS} = V_{GSth} + 9 V; V_{DS} = 10 V	9	–	–	A
I_{GSS}	gate leakage current	V_{GS} = ±15 V; V_{DS} = 0	–	–	125	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 2.5 A	–	2	–	S
R_{DSon}	drain-source on-state resistance	V_{GS} = V_{GSth} + 9 V; I_D = 2.5 A	–	340	–	mΩ
C_{iss}	input capacitance	V_{GS} = 0; V_{DS} = 26 V; f = 1 MHz	–	38	–	pF
C_{oss}	output capacitance	V_{GS} = 0; V_{DS} = 26 V; f = 1 MHz	–	31	–	pF
C_{rss}	feedback capacitance	V_{GS} = 0; V_{DS} = 26 V; f = 1 MHz	–	1.7	–	pF



V_{GS} = 0; f = 1 MHz.

Fig.2 Input, output and feedback capacitance as functions of drain-source voltage, typical values.

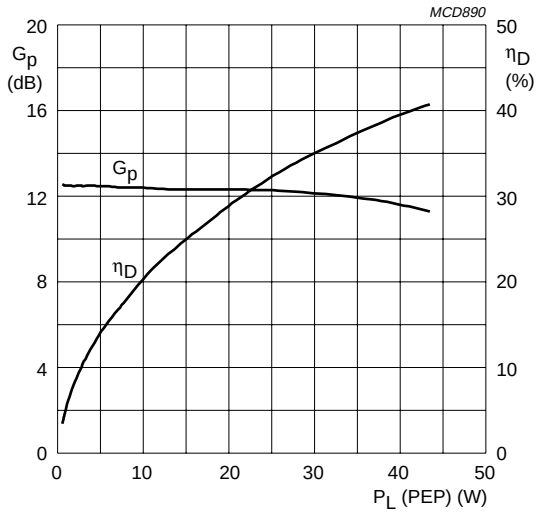
APPLICATION INFORMATION

RF performance in a common source class-AB circuit. T_h = 25 °C; $R_{th\ mb\text{-}h}$ = 0.65 K/W, unless otherwise specified.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (mA)	P_L (W)	G_p (dB)	η_D (%)	d_{im} (dBc)
2-tone, class-AB	f_1 = 2000; f_2 = 2000.1	26	180	30 (PEP)	>10	>30	≤–25

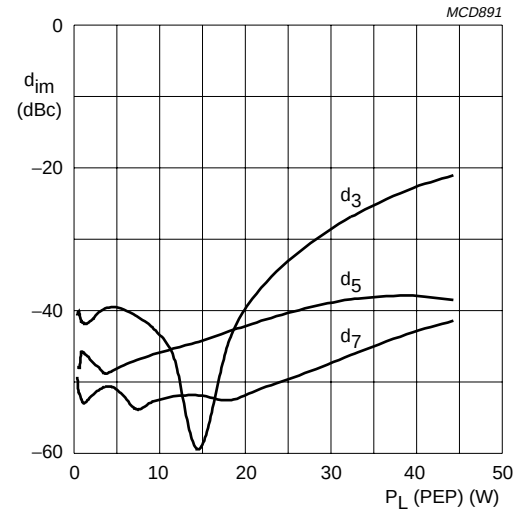
Ruggedness in class-AB operation

The BLF2045 is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 26 V; P_L = 30 W (CW); f = 2000 MHz.



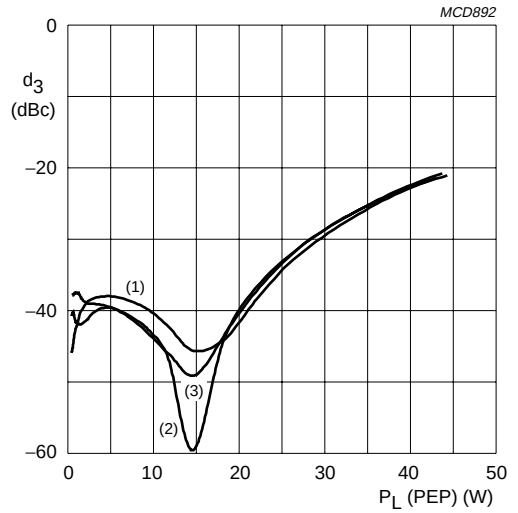
Class-AB operation; V_{DS} = 26 V; I_{DQ} = 180 mA; f_1 = 2000 MHz; f_2 = 2000.1 MHz.

Fig.3 Power gain and efficiency as functions of peak envelope load power, typical values.



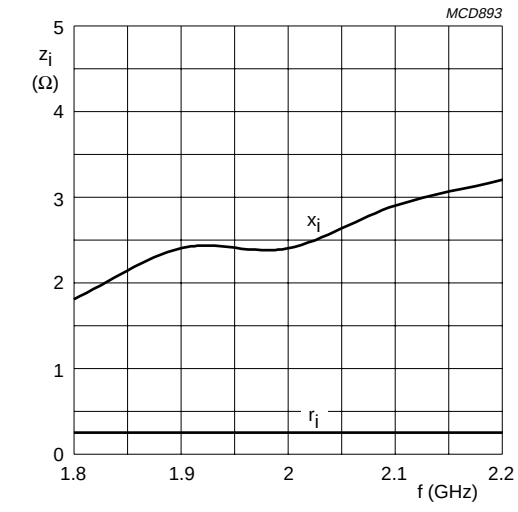
V_{DS} = 26 V; I_{DQ} = 180 mA; $T_h \leq 25$ °C;
f_1 = 2000 MHz; f_2 = 2000.1 MHz.

Fig.4 Intermodulation distortion as a function of peak envelope load power; typical values.



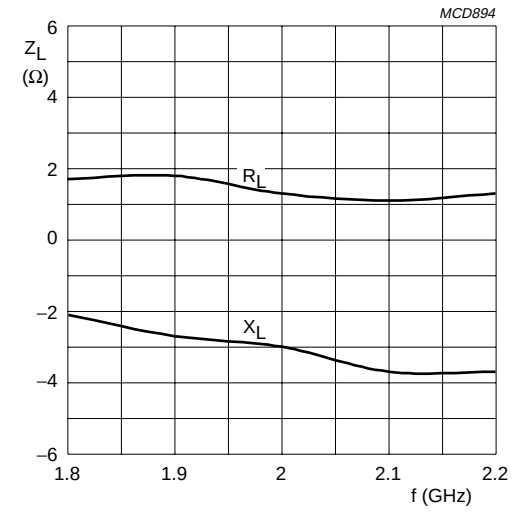
V_{DS} = 26 V; $T_h \leq 25$ °C; f_1 = 2000 MHz; f_2 = 2000.1 MHz.
(1) I_{DQ} = 140 mA.
(2) I_{DQ} = 180 mA.
(3) I_{DQ} = 220 mA.

Fig.5 Intermodulation distortion as a function of peak envelope load power; typical values.



V_{DS} = 26 V; I_{DQ} = 180 mA; P_L = 45 W; $T_h \leq 25$ °C.

Fig.6 Input impedance as a function of frequency (series components); typical values.



V_{DS} = 26 V; I_{DQ} = 180 mA; P_L = 45 W; $T_h \leq 25$ °C.

Fig.7 Load impedance as a function of frequency (series components); typical values.

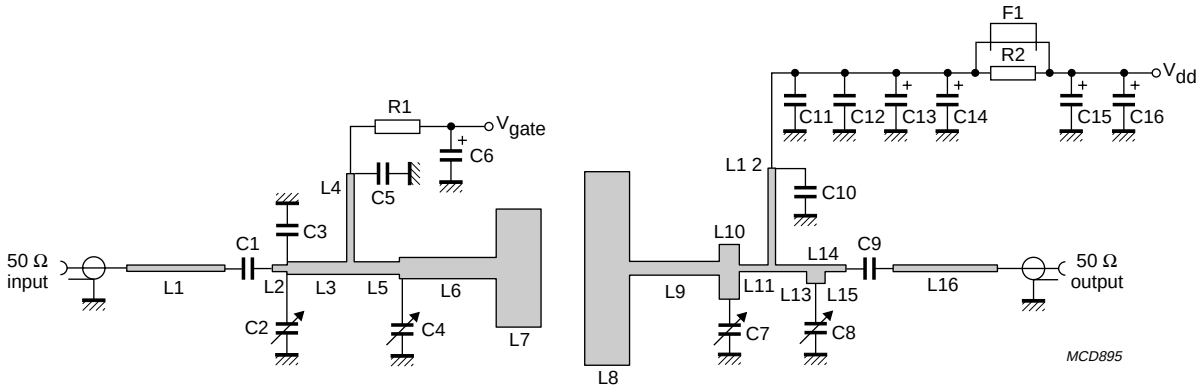


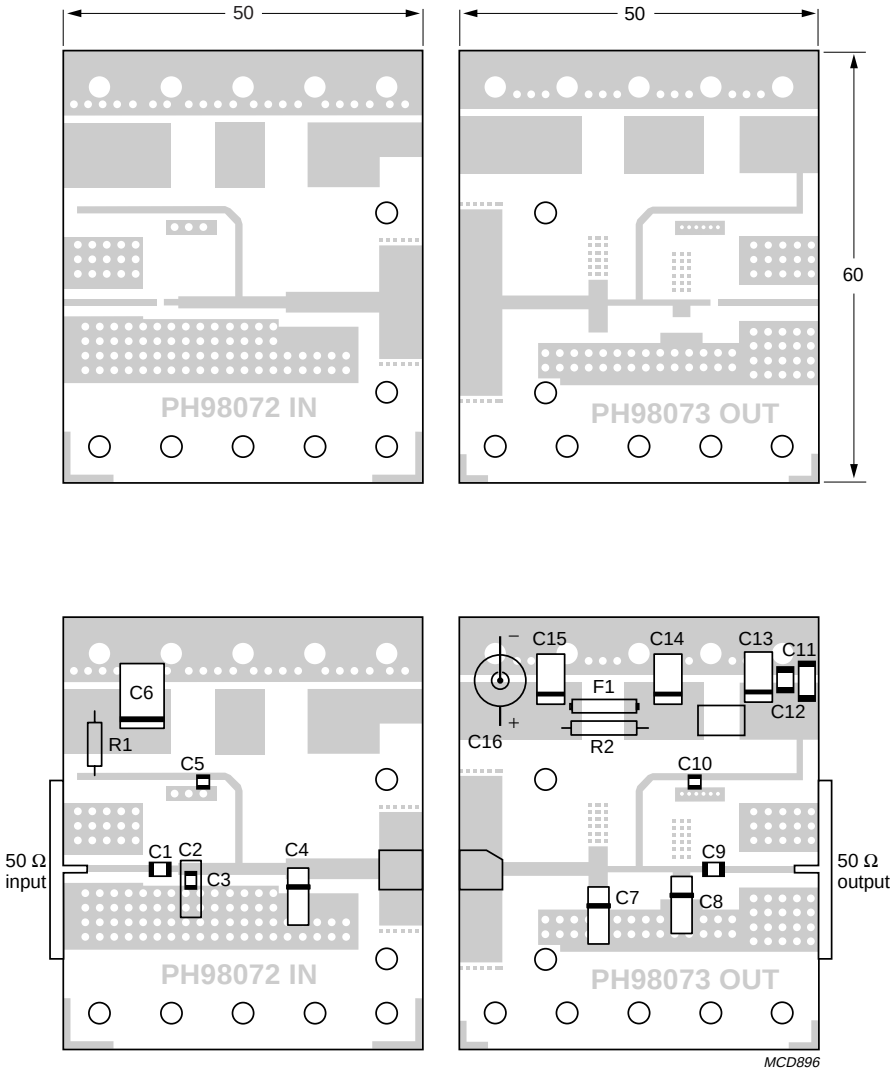
Fig.8 Class-AB test circuit for 2 GHz.

List of components (see Figs 8 and 9)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C2, C4, C7 and C8	Tekelec variable capacitor; type 37281	0.4 to 2.5 pF		
C3	multilayer ceramic chip capacitor; note 1	2.4 pF		
C1, C5, C9 and C10	multilayer ceramic chip capacitor; note 1	11 pF		
C11	multilayer ceramic chip capacitor; note 2	1 nF		
C12	multilayer ceramic chip capacitor	100 nF		2222 581 16641
C6, C13, C14 and C15	tantalum SMD capacitor	4.5 μF; 50 V		
C16	electrolytic capacitor	100 μF; 63 V		2222 037 58101
F1	Ferroxcube chip-bead 8DS3/3/8/9-4S2			4330 030 36301
L1	stripline; note 3	50 Ω	13 × 0.9 mm	
L2	stripline; note 3	50 Ω	2 × 0.9 mm	
L3	stripline; note 3	34.3 Ω	15 × 1.7 mm	
L4 and L12	stripline; note 3	50 Ω	37 × 0.9 mm	
L5	stripline; note 3	34.3 Ω	6 × 1.7 mm	
L6	stripline; note 3	23.6 Ω	13 × 2.9 mm	
L7	stripline; note 3	5.6 Ω	6 × 15.8 mm	
L8	stripline; note 3	3.5 Ω	6 × 26 mm	
L9	stripline; note 3	31.9 Ω	12 × 1.9 mm	
L10	stripline; note 3	24.9 Ω	7.4 × 2.7 mm	
L11	stripline; note 3	50 Ω	3 × 0.9 mm	
L13	stripline; note 3	50 Ω	4.15 × 0.9 mm	
L14	stripline; note 3	26.3 Ω	2.5 × 2.5 mm	
L15	stripline; note 3	50 Ω	2.8 × 0.9 mm	
L16	stripline; note 3	50 Ω	14 × 0.9 mm	
R1 and R2	metal film resistor	10 Ω, 0.6 W		2322 156 11009

Notes

1. American Technical Ceramics type 100A or capacitor of same quality.
2. American Technical Ceramics type 100B or capacitor of same quality.
3. The striplines are on a double copper-clad printed-circuit board with Teflon dielectric (ε_r = 6.15); thickness 0.64 mm.



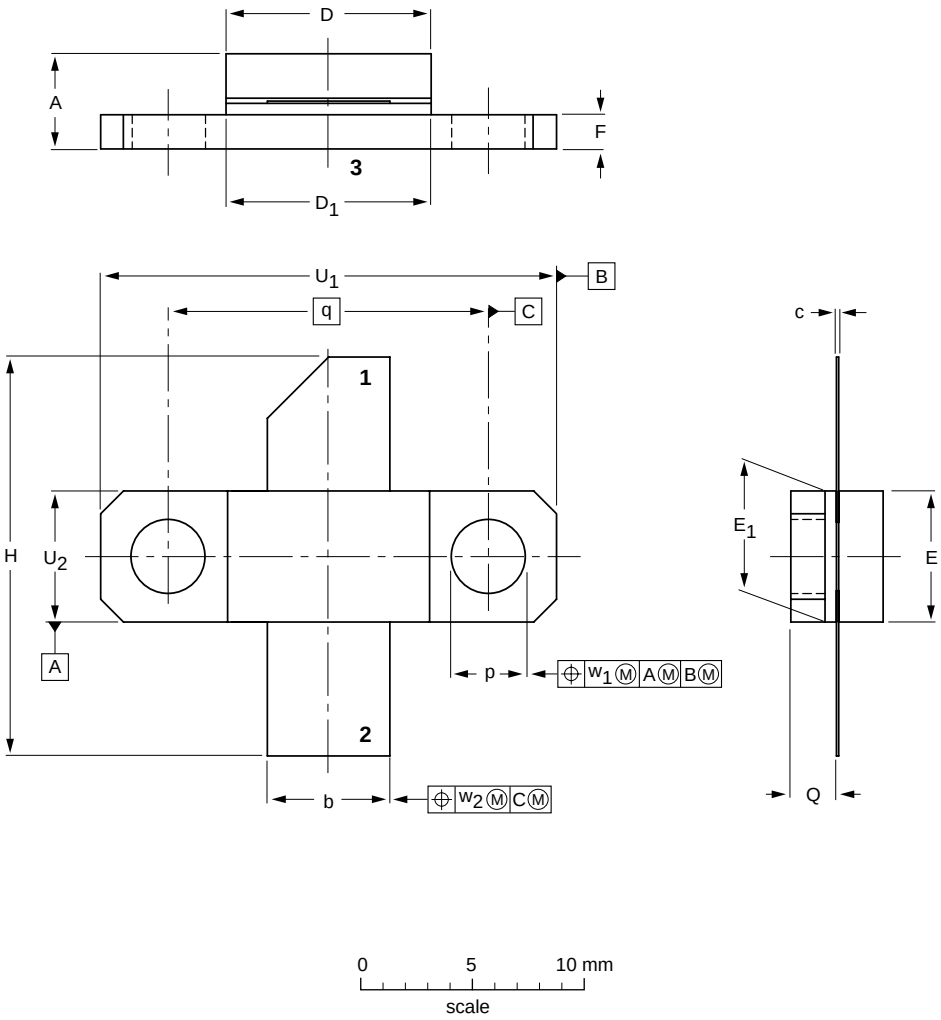
Dimensions in mm.

The components are situated on one side of the copper-clad printed-circuit board with Teflon dielectric (ε_r = 6.15), thickness 0.64 mm. The other side is unetched and serves as a ground plane.

Fig.9 Component layout for 2 GHz class-AB test circuit.

PACKAGE OUTLINE

Flanged LDMOST ceramic package; 2 mounting holes; 2 leads **SOT467C**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	E	E_1	F	H	p	Q	q	U_1	U_2	w_1	w_2
mm	4.67 3.94	5.59 5.33	0.15 0.10	9.25 9.04	9.27 9.02	5.92 5.77	5.97 5.72	1.65 1.40	18.54 17.02	3.43 3.18	2.21 1.96	14.27	20.45 20.19	5.97 5.72	0.25	0.51
inch	0.184 0.155	0.220 0.210	0.006 0.004	0.364 0.356	0.365 0.355	0.233 0.227	0.235 0.225	0.065 0.055	0.73 0.67	0.135 0.125	0.087 0.077	0.562	0.805 0.795	0.235 0.225	0.010	0.020

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT467C						~~99-12-06~~ 99-12-28

DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

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