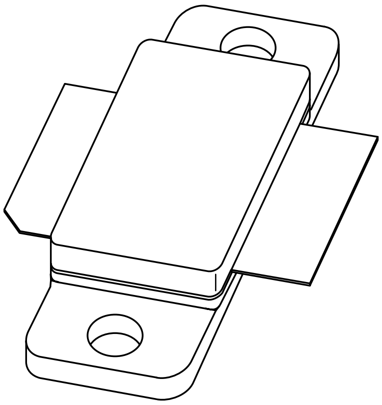
DATA SHEET



BLF1047
UHF power LDMOS transistor

Preliminary specification 2000 Oct 23

Philips
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FEATURES

- High power gain
- Easy power control
- Excellent ruggedness
- Source on underside eliminates DC isolators, reducing common mode inductance
- Designed for broadband operation (800 MHz to 1 GHz).

APPLICATIONS

- Communication transmitter applications in the UHF frequency range.

DESCRIPTION

Silicon N-channel enhancement mode lateral D-MOS transistor encapsulated in a 2-lead flange package (SOT541A) with a ceramic cap. The common source is connected to the mounting flange.

PINNING - SOT541A

PIN	DESCRIPTION
1	drain
2	gate
3	source, connected to flange

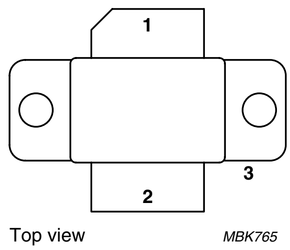


Fig.1 Simplified outline.

QUICK REFERENCE DATA

RF performance at T_h = 25 °C in the common source broadband test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)	d_{im} (dBc)
CW, class-AB (2-tone)	f_1 = 960; f_2 = 960.1	26	70 (PEP)	>14	>35	≤–26
CW, class-AB (1-tone)	960	26	70	>14	>45	–

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage	–	65	V
V_{GS}	gate-source voltage	–	±20	V
I_D	drain current (DC)	–	9	A
T_{stg}	storage temperature	–65	+150	°C
T_j	junction temperature	–	200	°C

CAUTION
This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A and SNW-FQ-302B.

THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j\text{-}h}$	thermal resistance from junction to heatsink	T_h = 25 °C, P_{dis} = 100 W; note 1	1.15	K/W

Note

1. Determined under specified RF operating conditions, based on maximum peak junction temperature.

CHARACTERISTICS

T_j = 25 °C unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	V_{GS} = 0; I_D = 1.4 mA	65	–	–	V
V_{GSth}	gate-source threshold voltage	V_{DS} = 10 V; I_D = 140 mA	4	–	5	V
I_{DSS}	drain-source leakage current	V_{GS} = 0; V_{DS} = 26 V	–	–	10	μA
I_{DSX}	drain cut-off current	V_{GS} = V_{GSth} + 9 V; V_{DS} = 10 V	20	–	–	A
I_{GSS}	gate leakage current	V_{GS} = ±20 V; V_{DS} = 0	–	–	250	nA
g_{fs}	forward transconductance	V_{DS} = 10 V; I_D = 5 A	–	3	–	S
R_{DSon}	drain-source on-state resistance	V_{GS} = V_{GSth} + 9 V; I_D = 5 A	–	200	–	mΩ
C_{is}	input capacitance	V_{GS} = 0; V_{DS} = 26 V; f = 1 MHz	–	75	–	pF
C_{os}	output capacitance	V_{GS} = 0; V_{DS} = 26 V; f = 1 MHz	–	65	–	pF
C_{rs}	feedback capacitance	V_{GS} = 0; V_{DS} = 26 V; f = 1 MHz	–	2.5	–	pF

APPLICATION INFORMATION

RF performance in the common source class-AB broadband test circuit. T_h = 25 °C; $R_{th\ j\text{-}h}$ = 1.15 K/W, unless otherwise specified.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)	d_{im} (dBc)
CW, class-AB (2-tone)	f_1 = 960; f_2 = 960.1	26	70 (PEP)	>14	>35	≤–26
CW, class-AB (1-tone)	960	26	70	>14	>45	–

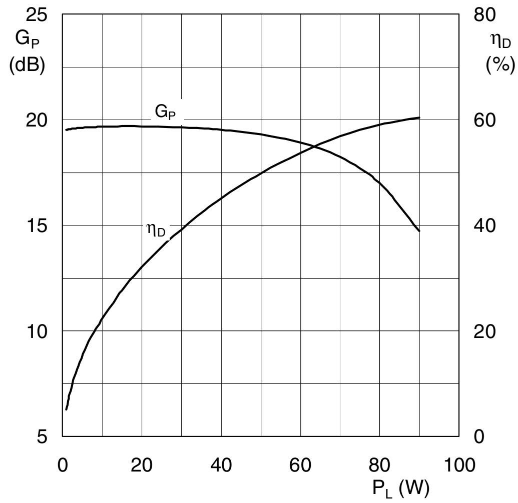
Ruggedness in class-AB operation

The BLF1047 is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: V_{DS} = 26 V; f = 960 MHz at rated load power.

Tuning Procedure

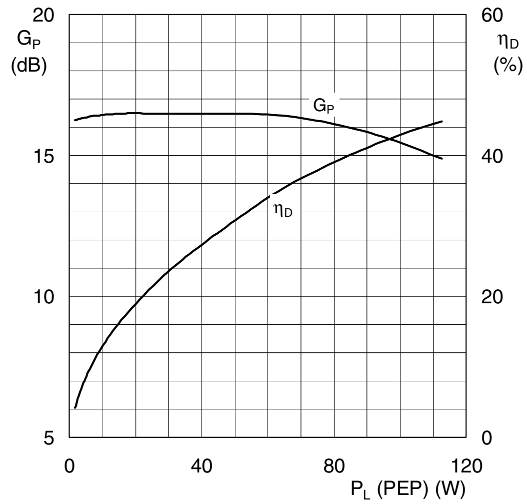
For high gain and efficiency:
In CW mode (P_D = 1 W; f = 960 MHz) tune C2 and C16 (see Figs. 13 and 14) until IRL < –15 dB, then adjust C6 and C8 for high gain until G_P > 14 dB at P_L = 50 W.

For linear mode:
Tune for high gain and efficiency mode, then apply two tone signal (f_1 = 960 MHz; f_2 = 960.1 MHz) at P_L = 45 W (PEP) and tune first C2 and then C6 and C8 for lowest d_3 (below –28 dBc).



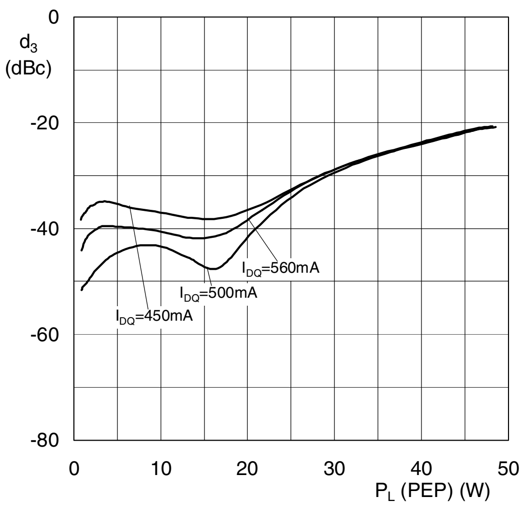
V_{DS} = 26 V; I_{DQ} = 500 mA; $T_h \leq 25$ °C;
f = 960 MHz; tuned for high efficiency; see tuning procedure.

Fig.2 Power gain and drain efficiency as functions of the load power; typical values.



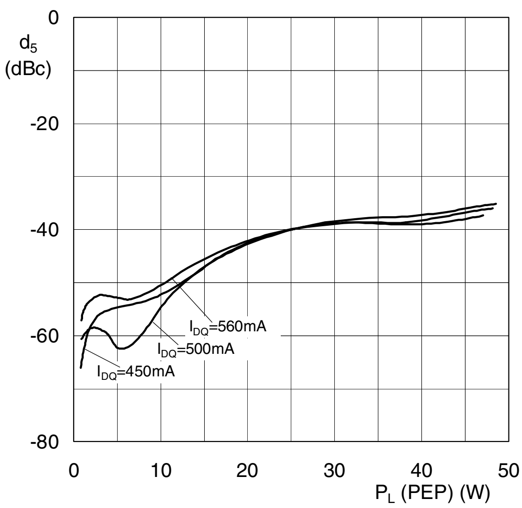
V_{DS} = 26 V; I_{DQ} = 500 mA; $T_h \leq 25$ °C; f_1 = 960 MHz; f_2 = 960.1 MHz;
tuned for high linearity; see tuning procedure

Fig.3 Power gain and drain efficiency as functions of peak envelope power; typical values.



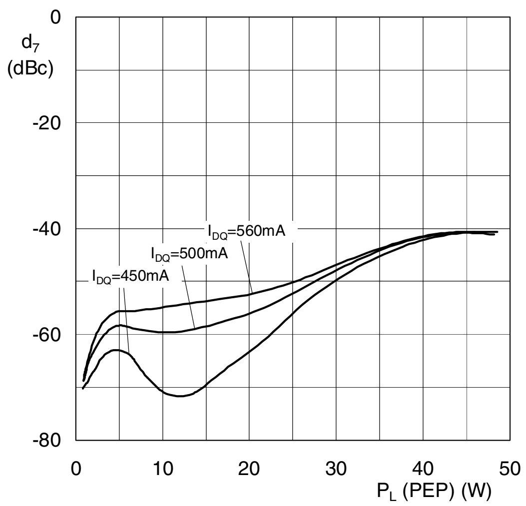
V_{DS} = 26 V; $T_h \leq 25$ °C; f_1 = 960 MHz; f_2 = 960.1 MHz
tuned for high linearity; see tuning procedure.

Fig.4 Third order intermodulation distortion as a function of peak envelope load power; typical values.



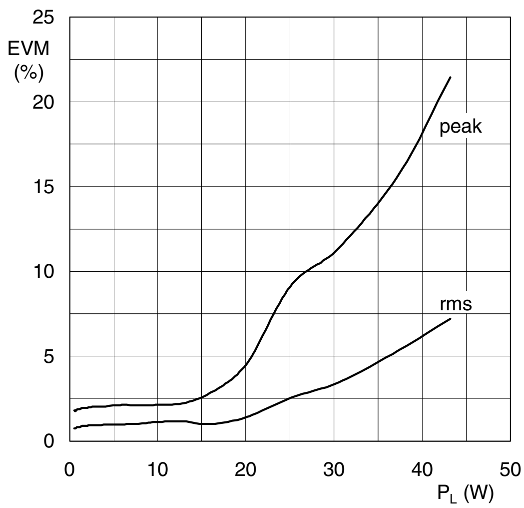
V_{DS} = 26 V; $T_h \leq 25$ °C; f_1 = 960 MHz; f_2 = 960.1 MHz
tuned for high linearity; see tuning procedure.

Fig.5 Fifth order intermodulation distortion as a function of peak envelope load power; typical values.



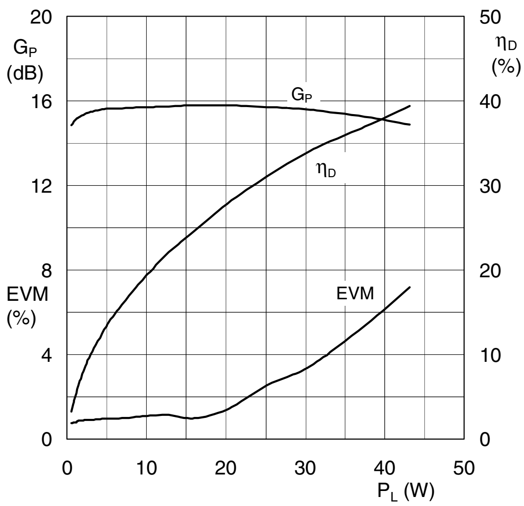
V_{DS} = 26 V; $T_h \leq 25$ °C; f_1 = 960 MHz; f_2 = 960.1 MHz
tuned for high linearity; see tuning procedure.

Fig.6 Seventh order intermodulation distortion as a function of peak envelope load power; typical values.



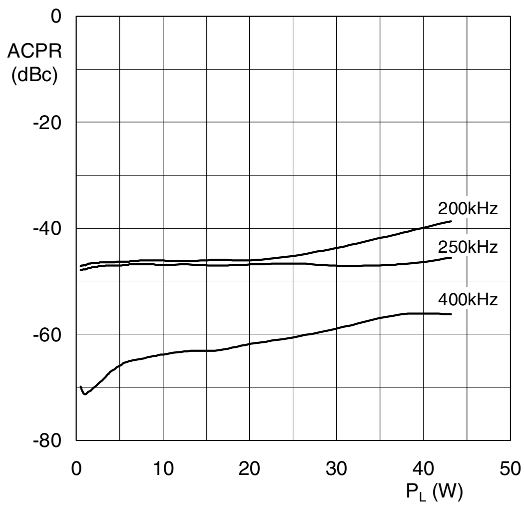
V_{DS} = 26 V; I_{DQ} = 470 mA; $T_h \leq 25$ °C; f = 960 MHz;
tuned for high linearity; see tuning procedure.

Fig.7 Error vector magnitude (EVM) / EDGE 8PSK as a function of load power; typical values.



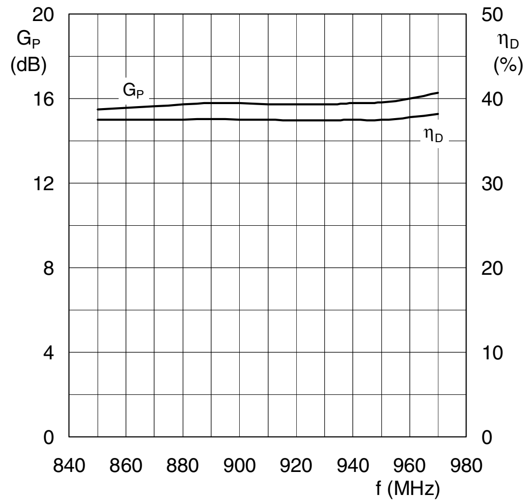
V_{DS} = 26 V; I_{DQ} = 470 mA; $T_h \leq 25$ °C; f = 960 MHz
tuned for high linearity; see tuning procedure.

Fig.8 EDGE 8PSK EVM, gain and efficiency as function of load power; typical values.



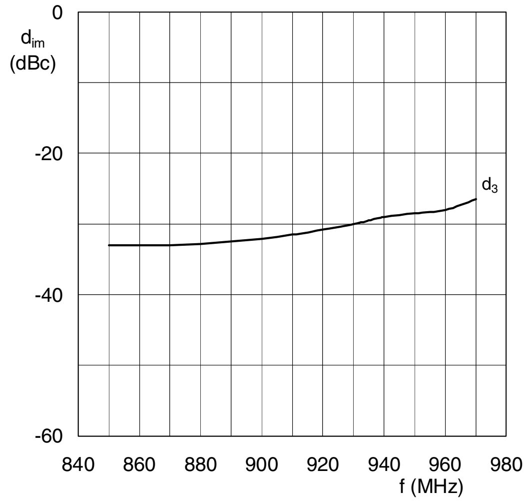
V_{DS} = 26 V; I_{DQ} = 300 mA; $T_h \leq 25$ °C; f = 960 MHz;
tuned for high linearity; see tuning procedure.
Measured EDGE channel bandwidth 270 kHz and adjacent channels bandwidth 30 kHz.

Fig.9 EDGE 8PSK adjacent channel power as function of load power; typical values.



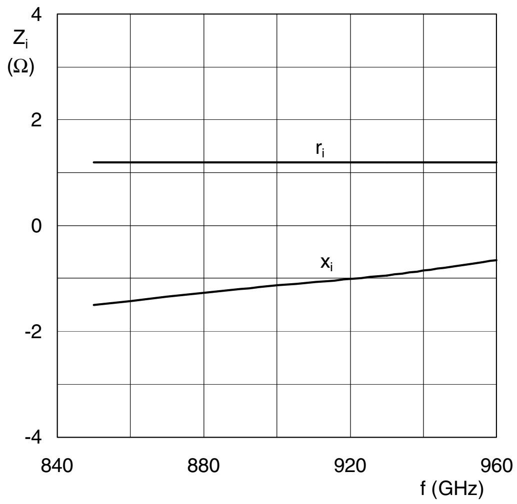
V_{DS} = 26 V; I_{DQ} = 500 mA; P_L = 70 W (PEP); $T_h \leq 25$ °C;
tuned for high linearity; see tuning procedure

Fig.10 Power gain and drain efficiency as functions of frequency; typical values.



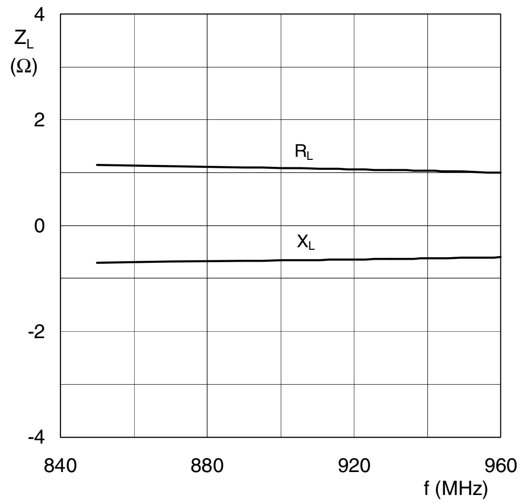
V_{DS} = 26 V; I_{DQ} = 500 mA; P_L = 70 W (PEP); $T_h \leq 25$ °C;
tuned for high linearity; see tuning procedure

Fig.11 Intermodulation distortion as function of frequency; typical values.



V_{DS} = 26 V; I_{DQ} = 470 mA; P_L = 45 W; $T_h \leq 25$ °C
tuned for high linearity; see tuning procedure.

Fig.12 Optimal source impedance as a function of frequency (series components); typical values.



V_{DS} = 26 V; I_{DQ} = 470 mA; P_L = 45 W; $T_h \leq 25$ °C
tuned for high linearity; see tuning procedure.

Fig.13 Optimal load impedance as a function of frequency (series components); typical values.

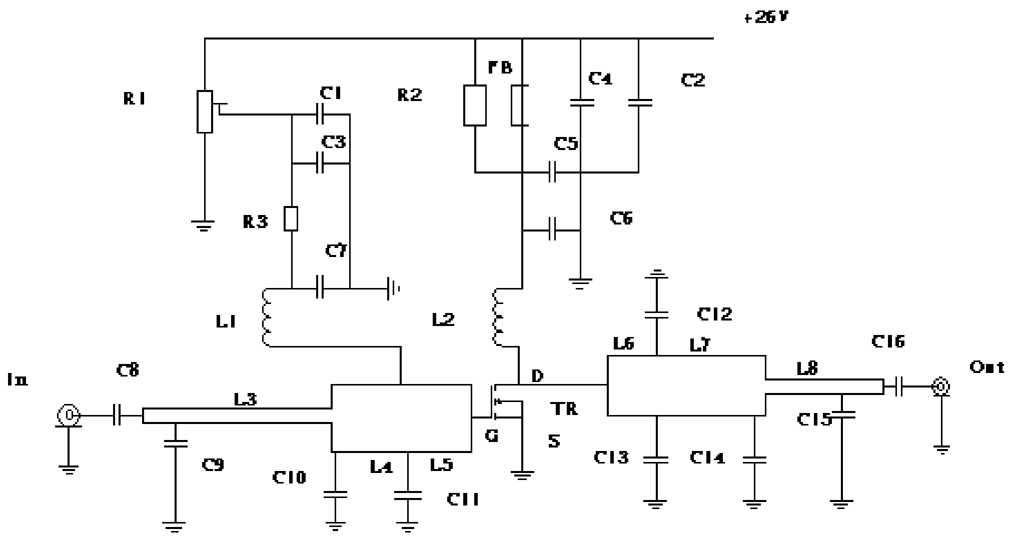
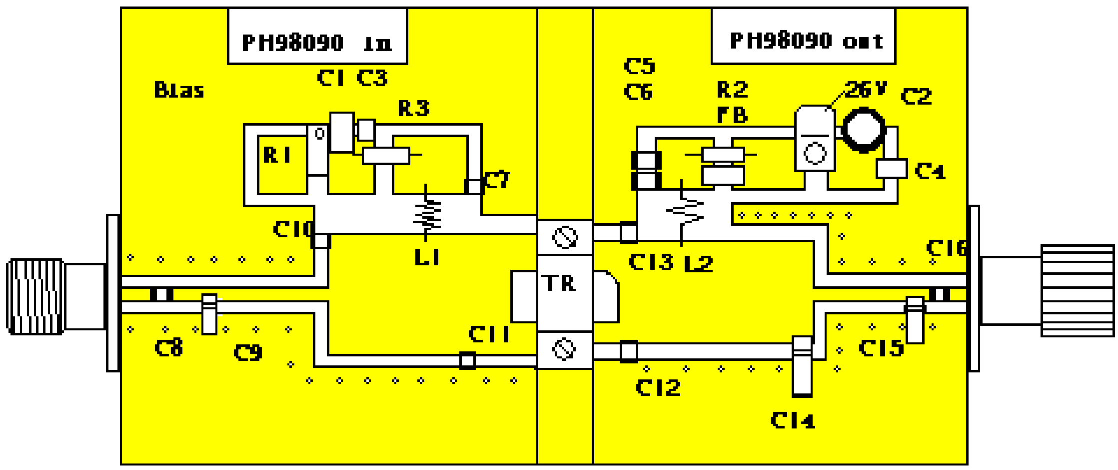


Fig.14 Class-AB broadband test circuit at f = 800 - 1000 MHz.



Dimensions in mm.

The components are situated on one side of the copper-clad printed-circuit board with Teflon dielectric (ε_r = 2.2), thickness 0.79 mm.

Fig.15 Component layout for 800 - 1000 MHz class-AB broadband test circuit.

List of components (See Figs 13 and 14)

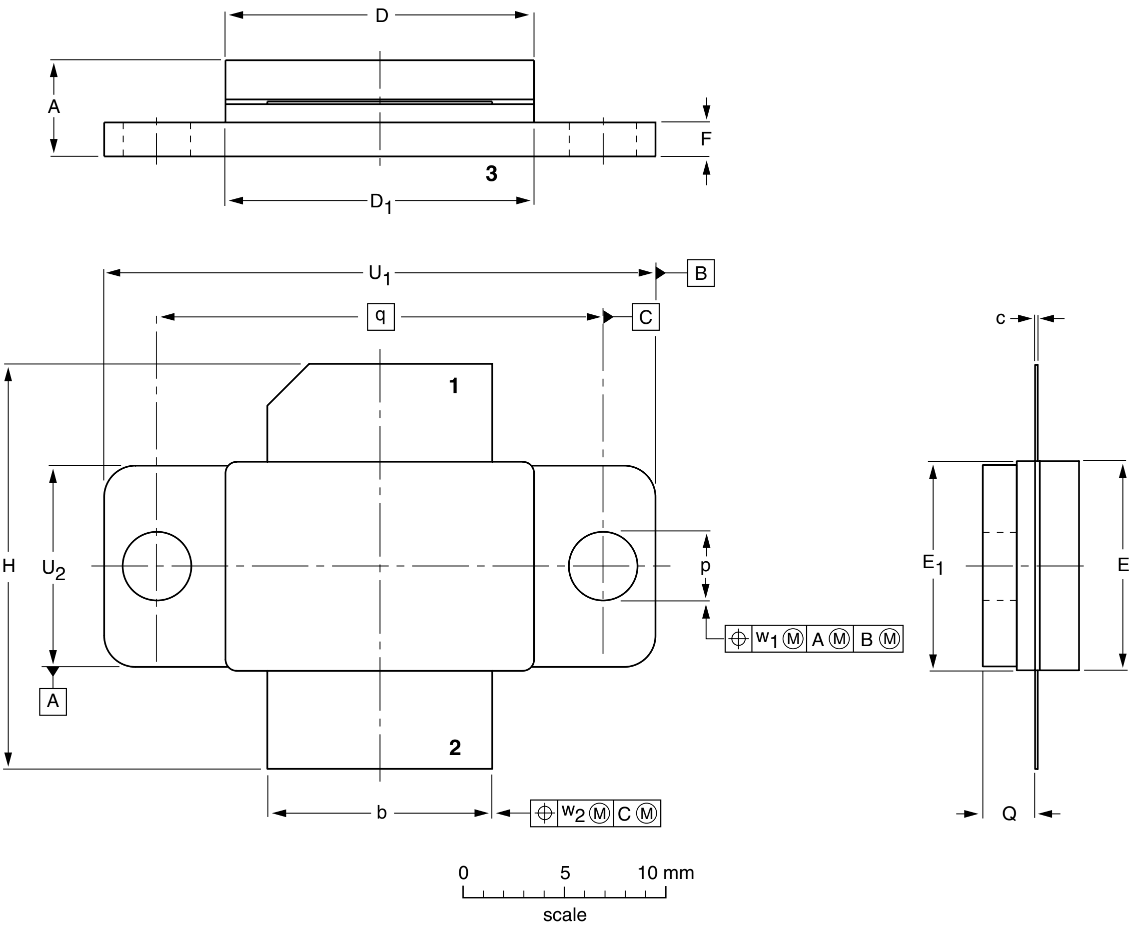
COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1	electrolytic capacitor	10 µF; 63 V		
C2	electrolytic capacitor	100 µF; 63 V		
C3, C4	multilayer ceramic chip capacitor; note 1	100 pF		
C5, C7	multilayer ceramic chip capacitor; note 1	150 pF		
C6, C8, C16	multilayer ceramic chip capacitor; note 1	33 pF		
C9, C14, C15	Tekelec variable capacitor	0.6 to 4.6 pF		
C10	multilayer ceramic chip capacitor; note 1	2.7 pF		
C11	multilayer ceramic chip capacitor; note 1	9.1 pF		
C12, C13	multilayer ceramic chip capacitor; note 1	15 pF		
FB	Ferroxcube chip-bead grade 4B1			
L1	5 turns enamelled 0.4 mm copper wire		int. dia. = 5 mm; length = 4 mm	
L2	2 turns enamelled 0.4 mm copper wire		int. dia. = 5 mm; length = 2 mm	
L3	stripline; note 2	50 Ω	22 × 2.36 mm	
L4	stripline; note 2	8.26 Ω	19 × 22 mm	
L5	stripline; note 2	8.26 Ω	11 × 22 mm	
L6	stripline; note 2	9 Ω	5 × 20 mm	
L7	stripline; note 2	9 Ω	33 × 20 mm	
L8	stripline; note 2	50 Ω	13 × 2.36 mm	
R1	variable resistor	10 kΩ		
R2	metal film resistor	3 Ω, 0.6 W		
R3	metal film resistor	10 kΩ, 0.6 W		

Notes

1. American Technical Ceramics type 100B or capacitor of same quality.
2. The striplines are on a double copper-clad printed-circuit board with Teflon dielectric (εr = 2.2); thickness 0.79 mm.

PACKAGE OUTLINE

Flanged LDMOST ceramic package; 2 mounting holes; 2 leads **SOT541A**



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D_1	E	E_1	F	H	p	Q	q	U_1	U_2	w_1	w_2
mm	5.74 4.60	11.05 10.80	0.18 0.10	15.39 15.09	15.39 15.09	10.26 10.06	10.29 10.03	1.78 1.52	20.83 19.81	3.43 3.18	2.69 2.44	22.10	27.31 27.05	9.91 9.65	0.25	0.51
inches	0.226 0.181	0.435 0.425	0.007 0.004	0.606 0.594	0.606 0.594	0.404 0.396	0.405 0.395	0.070 0.060	0.820 0.780	0.135 0.125	0.106 0.096	0.87	1.075 1.065	0.390 0.380	0.01	0.02

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT541A						~~00-01-13~~ 00-03-03

DATA SHEET STATUS

DATA SHEET STATUS	PRODUCT STATUS	DEFINITIONS (1)
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
Product specification	Production	This data sheet contains final specifications. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.

Note

1. Please consult the most recently issued data sheet before initiating or completing a design.

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