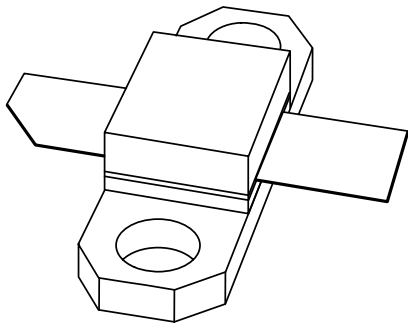


DATA SHEET



BLF1046

UHF power LDMOS transistor

Preliminary specification

2000 Sep 20

UHF power LDMOS transistor

BLF1046

FEATURES

- High power gain
- Easy power control
- Excellent ruggedness
- Source on underside eliminates DC isolators, reducing common mode inductance
- Designed for broadband operation (HF to 1 GHz).

APPLICATIONS

- Communication transmitter applications in the UHF frequency range.

DESCRIPTION

Silicon N-channel enhancement mode lateral D-MOS transistor encapsulated in a 2-lead flange package (SOT467C) with a ceramic cap. The common source is connected to the mounting flange.

PINNING - SOT467C

PIN	DESCRIPTION
1	drain
2	gate
3	source, connected to flange

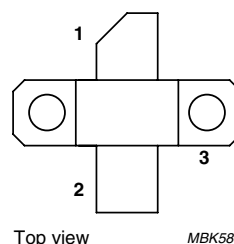


Fig.1 Simplified outline.

QUICK REFERENCE DATA

RF performance at $T_h = 25^\circ\text{C}$ in a common source test circuit.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	P_L (W)	G_p (dB)	η_D (%)	d_{im} (dBc)
CW, class-AB (2-tone)	$f_1 = 960; f_2 = 960.1$	26	45 (PEP)	>14	>35	≤ -28
CW, class-AB (1-tone)	960	26	45	>14	>46	—

LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DS}	drain-source voltage	—	65	V
V_{GS}	gate-source voltage	—	± 20	V
I_D	drain current (DC)	—	4.5	A
T_{stg}	storage temperature	-65	+150	$^\circ\text{C}$
T_j	junction temperature	—	200	$^\circ\text{C}$

CAUTION

This product is supplied in anti-static packing to prevent damage caused by electrostatic discharge during transport and handling. For further information, refer to Philips specs.: SNW-EQ-608, SNW-FQ-302A and SNW-FQ-302B.

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THERMAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j-mb}$	thermal resistance from junction to heatsink	$T_h = 25\ ^\circ\text{C}$, $P_{dis} = 97\ \text{W}$; note 1	1.22	K/W
$R_{th\ mb-h}$	thermal resistance from mounting base to heatsink		0.65	K/W

Note

1. Determined under specified RF operating conditions, based on maximum peak junction temperature.

CHARACTERISTICS

$T_j = 25\ ^\circ\text{C}$ unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{(BR)DSS}$	drain-source breakdown voltage	$V_{GS} = 0$; $I_D = 0.7\ \text{mA}$	65	–	–	V
V_{GSth}	gate-source threshold voltage	$V_{DS} = 10\ \text{V}$; $I_D = 70\ \text{mA}$	4	–	5	V
I_{DSS}	drain-source leakage current	$V_{GS} = 0$; $V_{DS} = 26\ \text{V}$	–	–	1	μA
I_{DSX}	drain cut-off current	$V_{GS} = V_{GSth} + 9\ \text{V}$; $V_{DS} = 10\ \text{V}$	12.5	–	–	A
I_{GSS}	gate leakage current	$V_{GS} = \pm 20\ \text{V}$; $V_{DS} = 0$	–	–	125	nA
g_{fs}	forward transconductance	$V_{DS} = 10\ \text{V}$; $I_D = 3.5\ \text{A}$	–	2	–	S
R_{DSon}	drain-source on-state resistance	$V_{GS} = V_{GSth} + 9\ \text{V}$; $I_D = 3.5\ \text{A}$	–	300	–	m Ω
C_{is}	input capacitance	$V_{GS} = 0$; $V_{DS} = 26\ \text{V}$; $f = 1\ \text{MHz}$	–	46	–	pF
C_{os}	output capacitance	$V_{GS} = 0$; $V_{DS} = 26\ \text{V}$; $f = 1\ \text{MHz}$	–	37	–	pF
C_{rs}	feedback capacitance	$V_{GS} = 0$; $V_{DS} = 26\ \text{V}$; $f = 1\ \text{MHz}$	–	1.5	–	pF

APPLICATION INFORMATION

RF performance in a common source class-AB circuit. $T_h = 25\ ^\circ\text{C}$; $R_{th\ mb-h} = 0.65\ \text{K/W}$, unless otherwise specified.

MODE OF OPERATION	f (MHz)	V_{DS} (V)	I_{DQ} (mA)	P_L (W)	G_p (dB)	η_D (%)	d_{im} (dBc)
CW, class-AB (2-tone)	$f_1 = 960$; $f_2 = 960.1$	26	300	45 (PEP)	>14	>35	≤ -28
CW, class-AB (1-tone)	960	26	300	45	>14	>46	–

Ruggedness in class-AB operation

The BLF1046 is capable of withstanding a load mismatch corresponding to VSWR = 10 : 1 through all phases under the following conditions: $V_{DS} = 26\ \text{V}$; $f = 960\ \text{MHz}$ at rated load power.

Tuning Procedure

For high gain and efficiency:

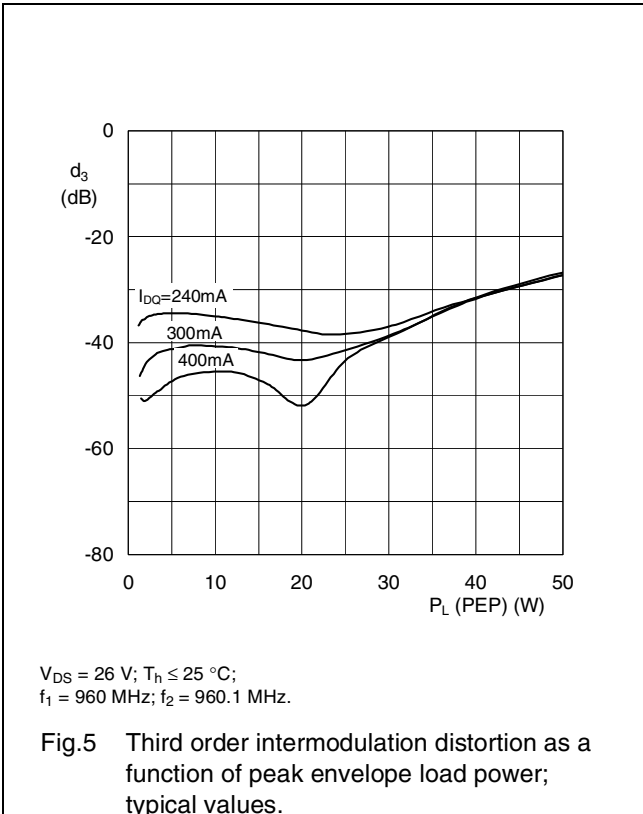
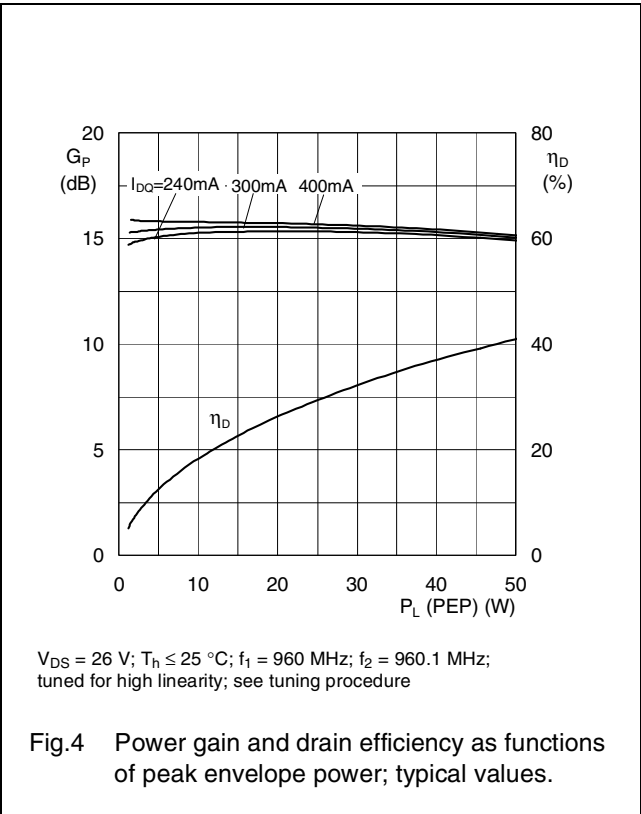
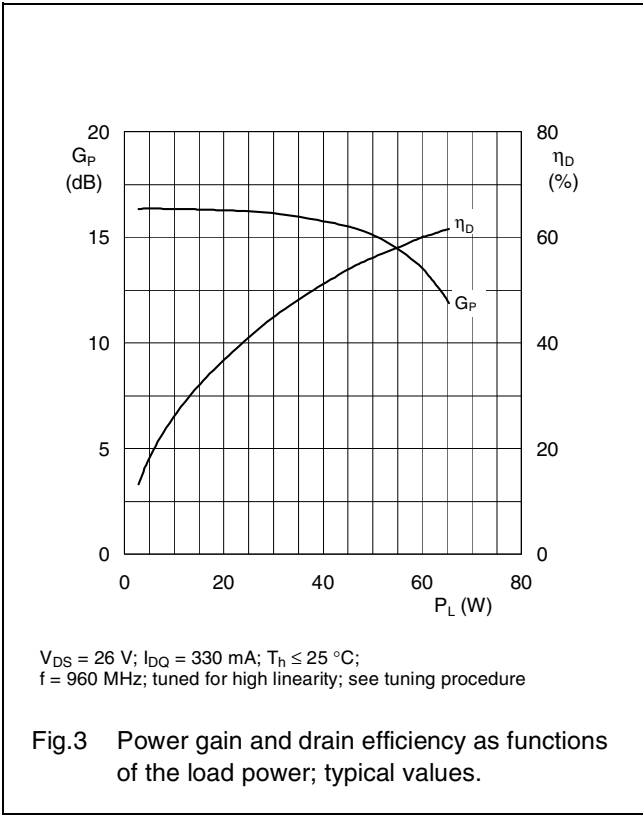
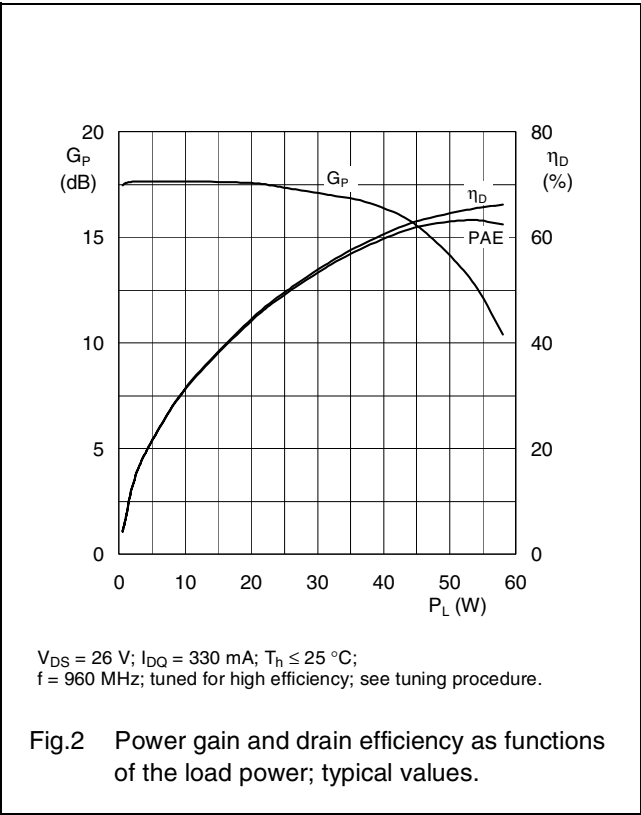
In CW mode ($P_D = 1\ \text{W}$; $f = 960\ \text{MHz}$) tune C2 and C16 (see Figs. 13 and 14) until IRL < –15 dB, then adjust C6 and C8 for high gain until $G_p > 14\ \text{dB}$ at $P_L = 50\ \text{W}$.

For linear mode:

Tune for high gain and efficiency mode, then apply two tone signal ($f_1 = 960\ \text{MHz}$; $f_2 = 960.1\ \text{MHz}$) at $P_L = 45\ \text{W}$ (PEP) and tune first C2 and then C6 and C8 for lowest d_3 (below –28 dBc).

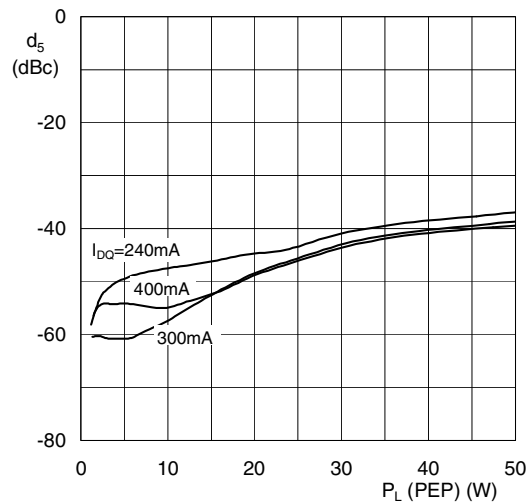
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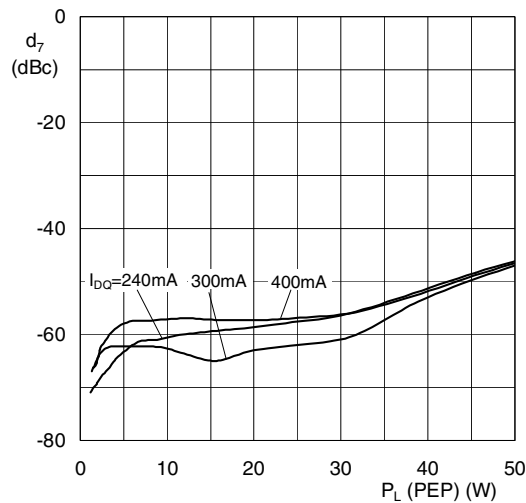
UHF power LDMOS transistor

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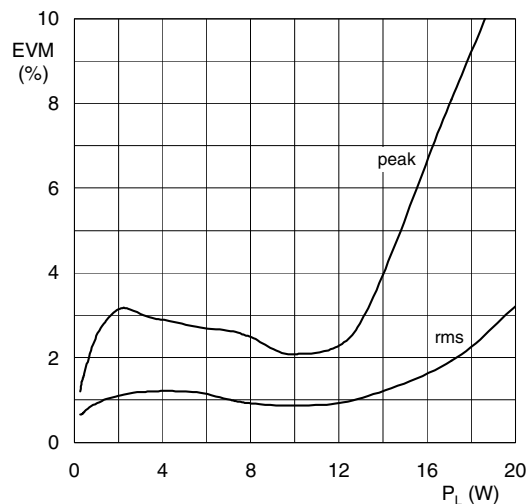
$V_{DS} = 26\text{ V}$; $T_h \leq 25\text{ }^\circ\text{C}$;
 $f_1 = 960\text{ MHz}$; $f_2 = 960.1\text{ MHz}$.

Fig.6 Fifth order intermodulation distortion as a function of peak envelope load power; typical values.



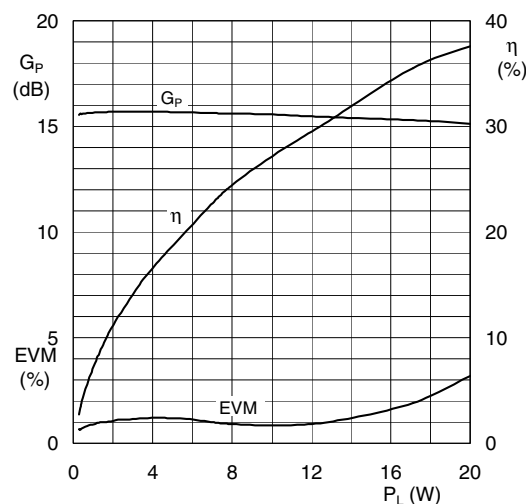
$V_{DS} = 26\text{ V}$; $T_h \leq 25\text{ }^\circ\text{C}$;
 $f_1 = 960\text{ MHz}$; $f_2 = 960.1\text{ MHz}$.

Fig.7 Seventh order intermodulation distortion as a function of peak envelope load power; typical values.



$V_{DS} = 26\text{ V}$; $I_{DQ} = 300\text{ mA}$; $T_h \leq 25\text{ }^\circ\text{C}$; $f = 960\text{ MHz}$.

Fig.8 Error vector magnitude (EVM) / EDGE 8PSK as a function of load power; typical values.

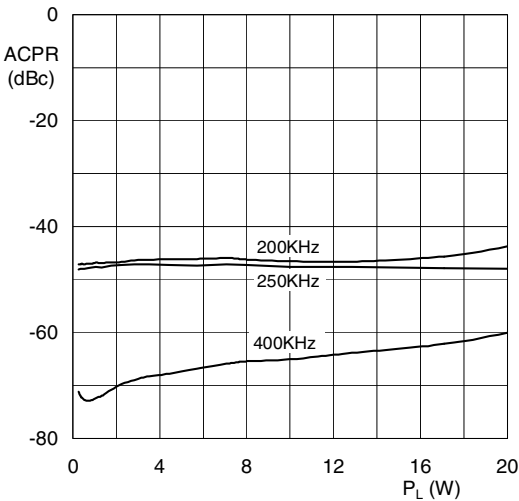


$V_{DS} = 26\text{ V}$; $I_{DQ} = 300\text{ mA}$; $T_h \leq 25\text{ }^\circ\text{C}$; $f = 960\text{ MHz}$.

Fig.9 EDGE 8PSK EVM, gain and efficiency as a function of load power; typical values.

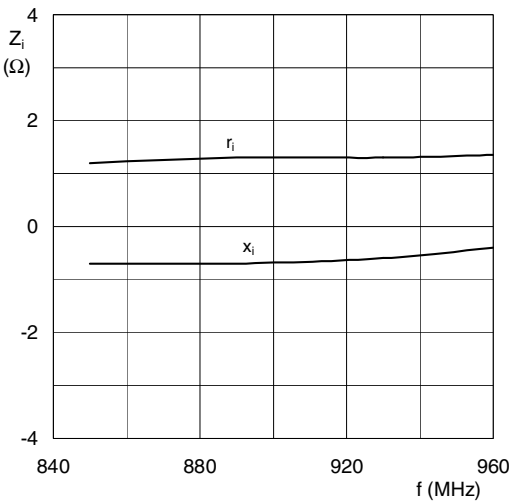
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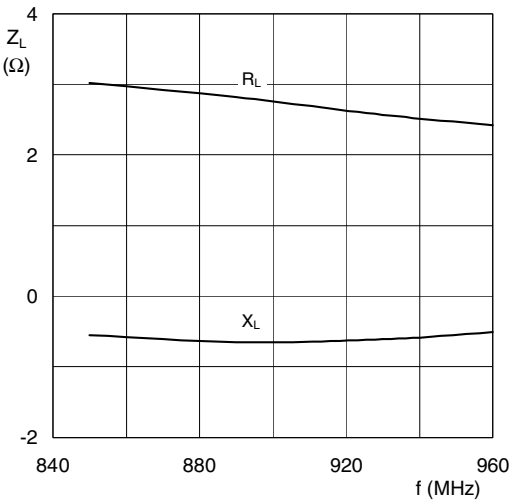
$V_{DS} = 26\text{ V}$; $I_{DQ} = 300\text{ mA}$; $T_h \leq 25\text{ }^{\circ}\text{C}$; $f = 960\text{ MHz}$.

Fig.10 EDGE 8PSK adjacent channel power as function of load power; typical values.



$V_{DS} = 26\text{ V}$; $I_{DQ} = 300\text{ mA}$; $P_L = 45\text{ W}$; $T_h \leq 25\text{ }^{\circ}\text{C}$.

Fig.11 Optimal source impedance for high linearity performance as a function of frequency (series components); typical values.

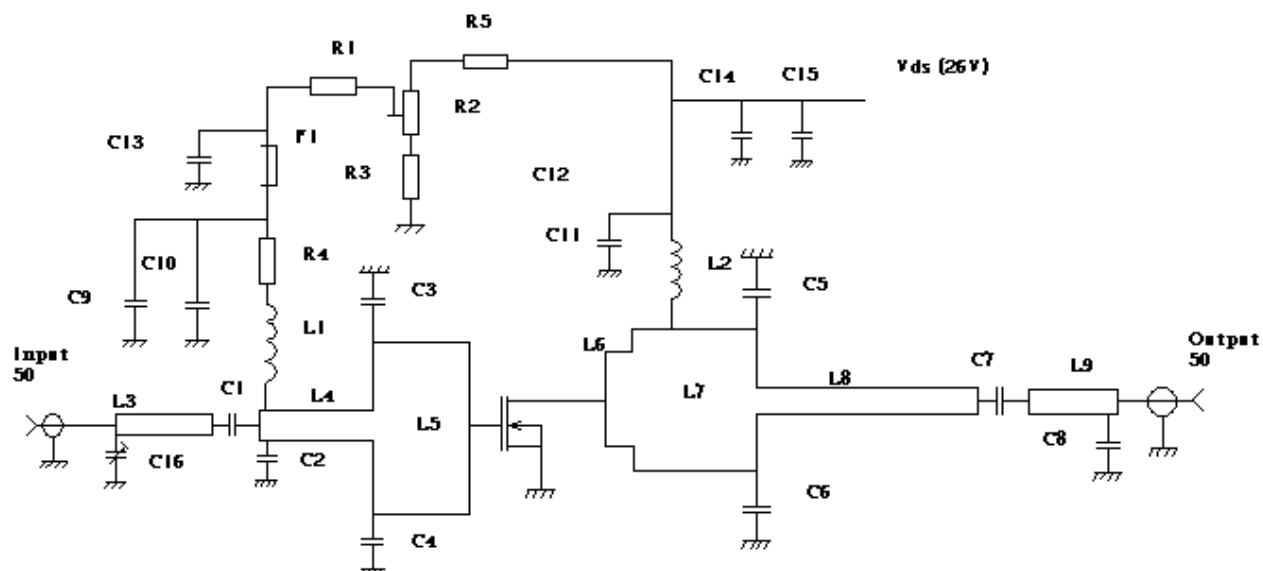
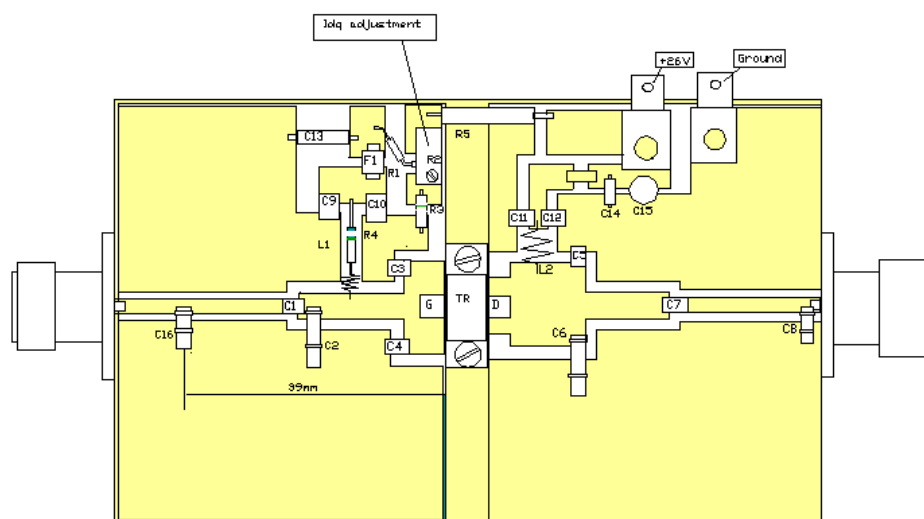


$V_{DS} = 26\text{ V}$; $I_{DQ} = 300\text{ mA}$; $P_L = 45\text{ W}$; $T_h \leq 25\text{ }^{\circ}\text{C}$.

Fig.12 Optimal load impedance for high linearity performance as a function of frequency (series components); typical values.

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Fig.13 Class-AB test circuit at $f = 960$ MHz.

Dimensions in mm.

The components are situated on one side of the copper-clad printed-circuit board with Teflon dielectric ($\epsilon_r = 2.2$), thickness 0.79 mm. The other side is unetched and serves as a ground plane.

Fig.14 Component layout for 960 MHz class-AB test circuit.

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List of components (See Figs 13 and 14)

COMPONENT	DESCRIPTION	VALUE	DIMENSIONS	CATALOGUE NO.
C1, C7	multilayer ceramic chip capacitor; note 1	33 pF		
C2, C6	Tekelec variable capacitor	0.8 to 8.2 pF		
C3, C4	multilayer ceramic chip capacitor; note 1	13 pF		
C5	multilayer ceramic chip capacitor; note 1	7.5 pF		
C8, C16	Tekelec variable capacitor	0.5 to 4.6 pF		
C9, C11	multilayer ceramic chip capacitor; note 1	33 pF		
C10, C12	multilayer ceramic chip capacitor; note 1	150 pF		
C13, C14	multilayer ceramic chip capacitor	33 nF		
C15	electrolytic capacitor	47 μ F; 63 V		
F1	Ferroxcube chip-bead 8DS3/3/8/9-4S2			4330 030 36301
L1	5 turns enamelled 0.6 mm copper wire		int. dia. = 4 mm; length = 5 mm	
L2	2 turns enamelled 0.6 mm copper wire		int. dia. = 4 mm; length = 1.6 mm	
L3	stripline; note 2	50 Ω	16 $\times$ 2.36 mm	
L4	stripline; note 2	42.5 Ω	16 $\times$ 3.1 mm	
L5	stripline; note 2	14.3 Ω	6 $\times$ 12 mm	
L6	stripline; note 2	20.2 Ω	3 $\times$ 8 mm	
L7	stripline; note 2	14.3 Ω	14 $\times$ 12 mm	
L8	stripline; note 2	40 Ω	17 $\times$ 3.4 mm	
L9	stripline; note 2	50 Ω	7 $\times$ 2.36 mm	
R1, R5	metal film resistor	10 k Ω , 0.6 W		
R2	variable resistor	10 k Ω		
R3	metal film resistor	1 k Ω , 0.6 W		
R4	metal film resistor	10 Ω , 0.6 W		

Notes

1. American Technical Ceramics type 100B or capacitor of same quality.
2. The striplines are on a double copper-clad printed-circuit board with Teflon dielectric ($\epsilon_r = 2.2$); thickness 0.79 mm.

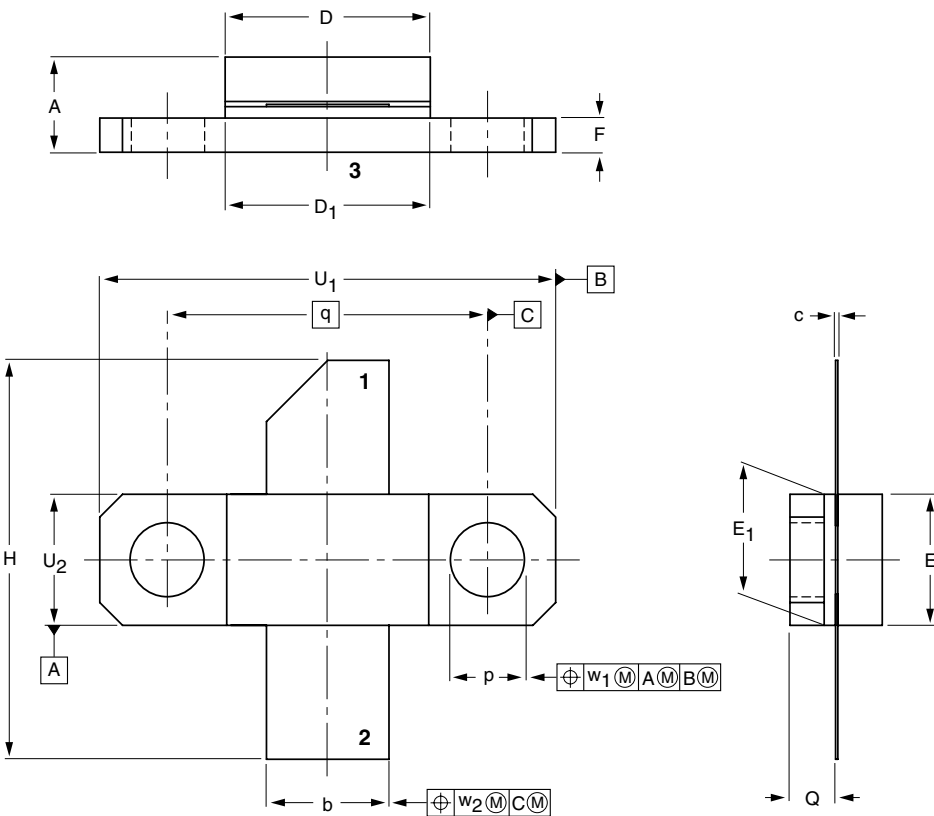
UHF power LDMOS transistor

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PACKAGE OUTLINE

Flanged LDMOST ceramic package; 2 mounting holes; 2 leads

SOT467C



DIMENSIONS (millimetre dimensions are derived from the original inch dimensions)

UNIT	A	b	c	D	D ₁	E	E ₁	F	H	p	Q	q	U ₁	U ₂	w ₁	w ₂
mm	4.67 3.94	5.59 5.33	0.15 0.10	9.25 9.04	9.27 9.02	5.92 5.77	5.97 5.72	1.65 1.40	18.54 17.02	3.43 3.18	2.21 1.96	14.27	20.45 20.19	5.97 5.72	0.25	0.51
inch	0.184 0.155	0.220 0.210	0.006 0.004	0.364 0.356	0.365 0.355	0.233 0.227	0.235 0.225	0.065 0.055	0.73 0.67	0.135 0.125	0.087 0.077	0.562	0.805 0.795	0.235 0.225	0.010	0.020

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT467C						99-12-06 99-12-28

UHF power LDMOS transistor

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DATA SHEET STATUS

DATA SHEET STATUS	PRODUCT STATUS	DEFINITIONS ⁽¹⁾
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
Preliminary specification	Qualification	This data sheet contains preliminary data, and supplementary data will be published at a later date. Philips Semiconductors reserves the right to make changes at any time without notice in order to improve design and supply the best possible product.
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Note

1. Please consult the most recently issued data sheet before initiating or completing a design.

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Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

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