# Read/Write Amplifier for FDD

## BH6625FS

The BH6625FS is a 4-mode read / write IC designed for floppy disk drives, and has an active filter that can be set according to transfer rate. Any of multiple write current settings can be selected, and inner edge / outer edge switching is done internally.

●Applications

Floppy disk drives (1MB, 1.6MB and 2MB)

●Features

1) Internal active filter with multiple settings that can be selected for multiple Q and $f_0$.
2) Time domain filter that is internally switchable according to transfer rate.
3) Any of multiple write current settings can be selected, and inner track / outer track switching is done internally.

●Absolute maximum ratings (unless otherwise noted, Ta=25℃)

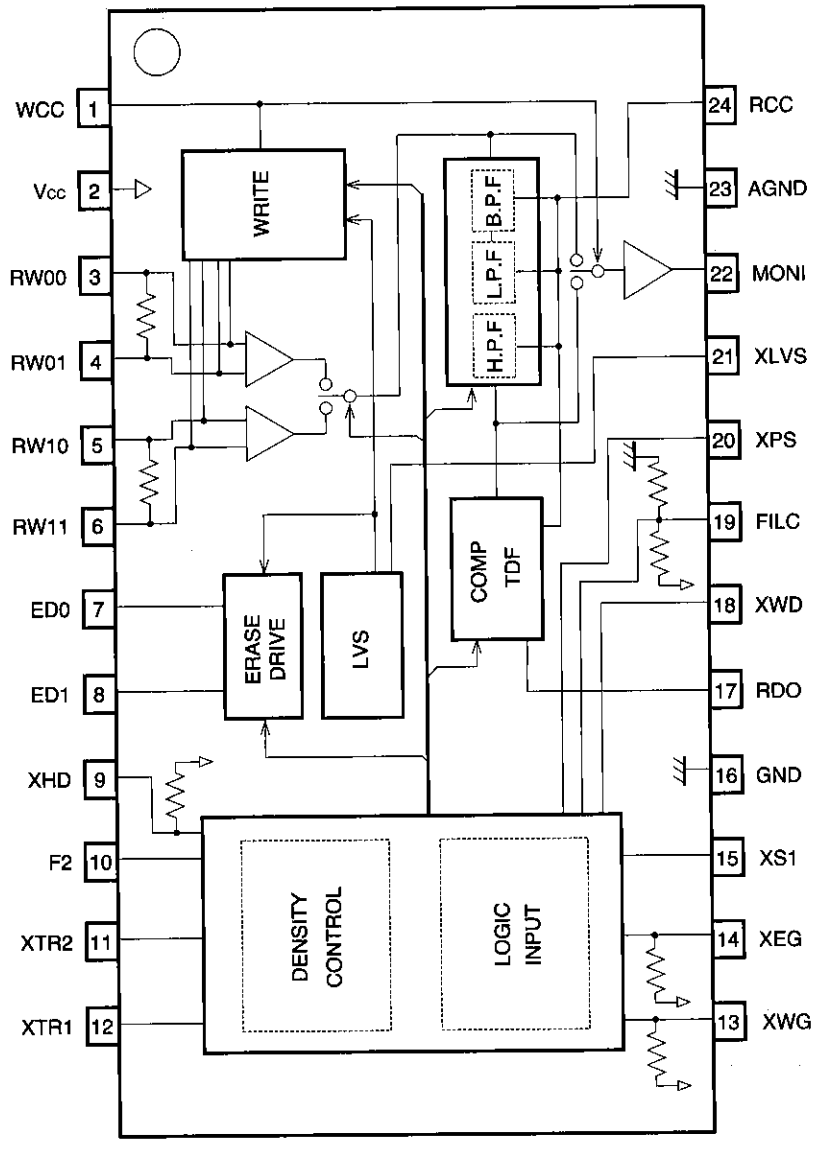
| Parameter | Symbol | Limits | Unit |
|---|---|---|---|
| Supply voltage | $V_{CC}$ | +7 | V |
| Operating temperature | $T_{OPR}$ | 0~+70 | ℃ |
| Storage temperature | $T_{STG}$ | −55~+125 | ℃ |
| Digital input voltage | VI | −0.5~$V_{CC}$+0.3 | V |
| RW pin voltage | VRW | +15 | V |
| LVS output voltage | VLVS | $V_{CC}$+0.3 | V |
| ED pin voltage | VER | $V_{CC}$+0.3 | V |
| Power dissipation | $P_D$ | 650* | mW |

* Reduced by 6.5mW for each increase in Ta of 1℃ over 25℃.

●Recommended operating conditions (Ta=25℃)

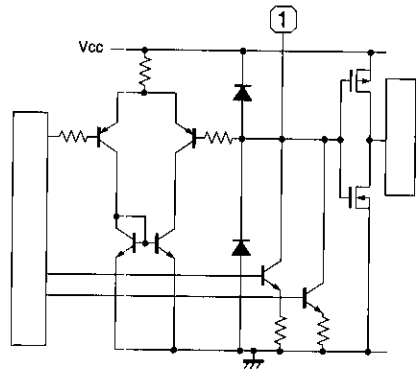
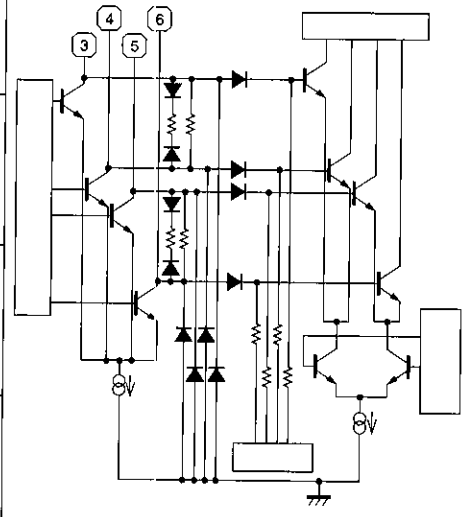
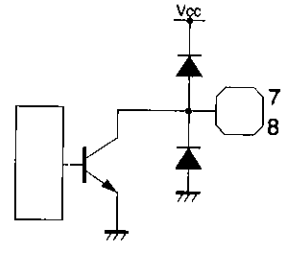
| Parameter | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Power supply voltage | $V_{CC}$ | 4.5 | 5.0 | 5.5 | V |

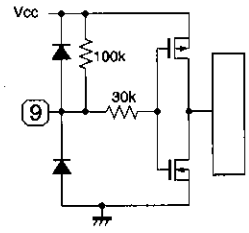
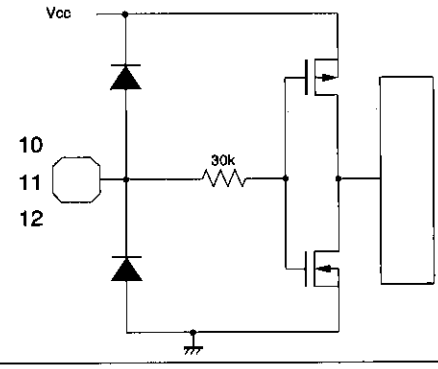
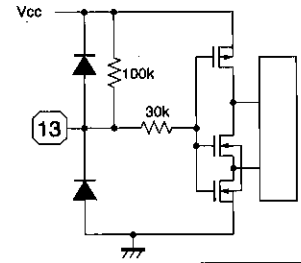
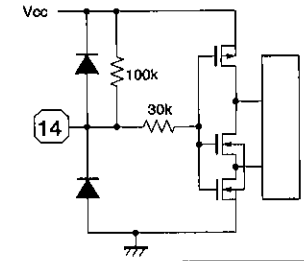
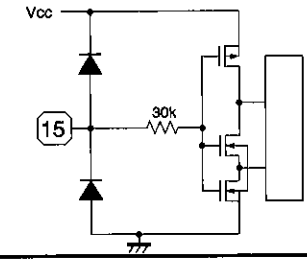
●Block diagram

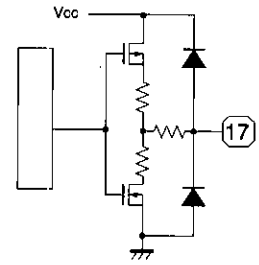
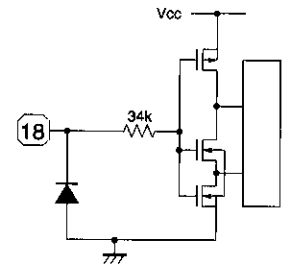
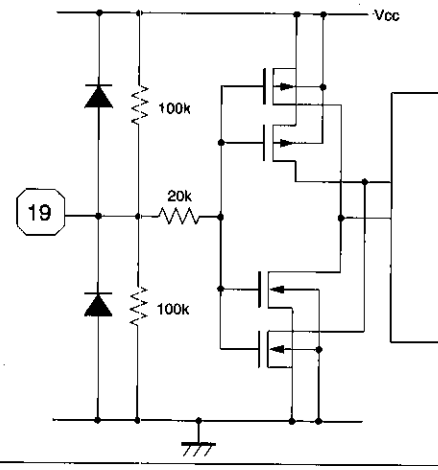
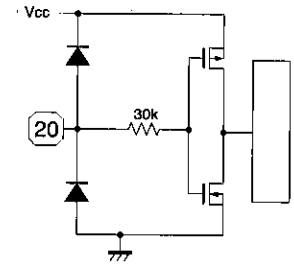


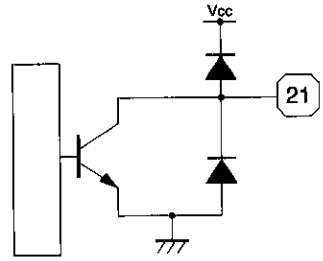
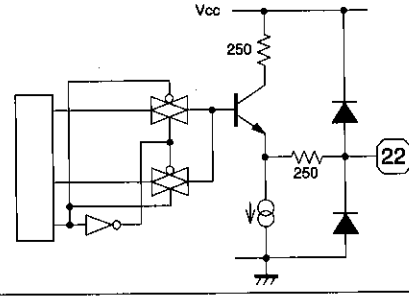
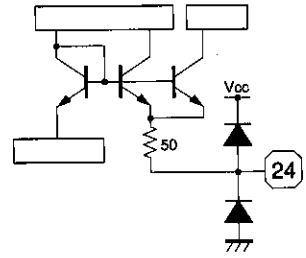

(Note) Use a short pattern for Vcc, and keep the impedance between Vcc and GND low by inserting a bypass capacitor.

●Pin description and input/output circuit

| Pin No. | Name | Equivalent circuit | Function |
|---|---|---|---|
| 1 | WCC |  | For connecting the write current adjustment resistor<br><br>Connect the write current adjustment resistor between this pin and Vcc.<br><br>Setting this pin to the low level during reading switches MONI to differentiator output. |
| 2 | Vcc | | Power supply pin |
| 3 | RW00 |  | Active when SIDE0 and the read/write head connecting pin (pin 15, XS1) is at the high level (side 0)<br><br>Starts at RW00 during the start of writing (from reading to writing) |
| 4 | RW01 | | |
| 5 | RW10 | | Active when the read/write head connecting pin (pin 15, XS1) is at the low level (side 1)<br><br>Starts at RW10 during the start of writing (from reading to writing) |
| 6 | RW11 | | |
| 7 | ED0 |  | Side 0 erase current sink |
| 8 | ED1 | | Side 1 erase current sink |

| Pin No. | Name | Equivalent circuit | Function |
|---|---|---|---|
| 9 | XHD |  | 1MB/2MB selector<br>High = 1MB<br>Low = 2MB |
| 10 | F2 |  | 1.6MB drive selector<br>Selector signal high level = active<br>High = 1.6MB drive, low = 2MB drive |
| 11 | XTR2 | | Inner track/outer track position setting<br>Controls the write current |
| 12 | XTR1 (XSWF) | | Inner track/outer track position setting<br>Controls the filter and write current |
| 13 | XWG |  | Write enable gate (Schmidt input)<br>Low = active |
| 14 | XEG |  | Erase enable gate (Schmidt input)<br>Low = active |
| 15 | XS1 |  | Head/side switching signal<br>Low = active (Schmidt input)<br>High = side 0, low = side 1 |

| Pin No. | Name | Equivalent circuit | Function |
|---|---|---|---|
| 16 | DGND | | Digital ground |
| 17 | RDO |  | Read data output<br>TTL high level = active |
| 18 | XWD |  | Write data input<br>Operates at falling edge<br>(Schmidt input) |
| 19 | FILC |  | Filter control ($f_0$, Q)<br>Used to switch filter cutoff frequency<br>(tri-state input) |
| 20 | XPS |  | Power save selector<br>Low = active |

| Pin No. | Name | Equivalent circuit | Function |
|---|---|---|---|
| 21 | XLVS |  | External low level voltage detection pin<br><br>Open collector output when low level voltage is detected.<br><br>Switches to low level when Vcc drops below the specified voltage |
| 22 | MONI |  | Preamplifier output and differentiator output monitoring<br><br>Monitor is switched with pin 1 (WCC) |
| 23 | AGND | | Analog ground |
| 24 | RCC |  | Filter (LPF, BPF) cutoff frequency and TDF 1st M/M pulse width setting resistor connection |

●Electrical characteristics (unless otherwise noted, Ta=25℃, Vcc=5V)

Current consumption

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Conditions |
|---|---|---|---|---|---|---|
| Current consumption, Standby | ICCST | — | 245 | 400 | μA | *1 |
| Current consumption, Read | ICCR | — | 28 | 42 | mA | *1 |
| Current consumption, Write | ICCW | — | 8.5 | 15 | mA | *2 |

*1 RRCC=2.0 [kΩ] (XHD=H)
*2 RWCC=2.4 [kΩ] (When 2MB inner edge, XTR2=high level, excluding IWR and IER)

Low level voltage detection circuit

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Conditions |
|---|---|---|---|---|---|---|
| Threshold voltage 1 | VTH1+ | — | 4.05 | 4.30 | V | When power supply voltage rises, internal LVS/write protect. |
| | VTH1− | 3.60 | 3.85 | 4.10 | V | When power supply voltage falls, internal LVS/write protect. |
| Threshold voltage 2 | VTH2+ | — | 3.95 | 4.20 | V | When power supply voltage rises, external LVS |
| | VTH2− | 3.50 | 3.75 | 4.00 | V | When power supply voltage falls, external LVS |
| Hysteresis voltage | VH | 50 | — | — | mV | |
| Output voltage, low level | VOL | — | — | 0.40 | V | Vcc=2.5 [V] IOL=0.2 [mA] |
| Output leakage current | IOH | — | — | 10 | μA | |

Recovery time

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Conditions |
|---|---|---|---|---|---|---|
| POWER·SAVE→READ | TR2 | — | — | 500 | μs | by XPS |
| READ→ERASE | TR3 | — | — | 6 | μs | by XEG |
| READ→WRITE | TR4 | — | — | 4 | μs | by XWG |
| WRITE→READ | TR5E | — | — | 20 | μs | by XEG |
| | TR5W | — | — | 160 | μs | by XWG |
| SIDE0↔SIDE1 | TR6 | — | — | 40 | μs | by XS1 |
| 1MB↔2MB | TR7 | — | — | 40 | μs | by XHD |

Preamplifier

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Conditions |
|---|---|---|---|---|---|---|
| Voltage gain (1) | GVD1 | 43 | 46 | 49 | dB | f=125[kHz], VIN=2.5[mVp-p] (XTR1=L) (differential) |
| Voltage gain (2) | GVD2 | 46 | 49 | 52 | dB | f=125[kHz], VIN=2.5[mVp-p] (XTR1=H) (differential) |
| SIDE0↔SIDE1 crosstalk | GCTLK | 50 | — | — | dB | f=125[kHz], VIN=100[mVp-p] (differential) *3 |
| Differential input resistance | RID | — | 3.3 | — | kΩ | 8.0 [kΩ] input resistance, //5.5 [kΩ] damping resistance |
| Input conversion noise voltage | VN | — | 2.5 | 3.7 | μVrms | f=500[Hz]~1[MHz] |
| Input sink current | ISINK | — | 180 | — | μA | |
| Differential input voltage amplitude tolerance (1) | VIN1 | — | — | 5.0 | mVp-p | 5% distortion (sinewave input) (XTR1=L) |
| Differential input voltage amplitude tolerance (2) | VIN2 | — | — | 3.5 | mVp-p | 5% distortion (sinewave input) (XTR1=H) |
| Common mode rejection ratio | CMRR | 50 | — | — | dB | f=125[kHz], VIN=100[mVp-p] *3 |
| Power supply rejection ratio | PSRR | 40 | — | — | dB | f=250[kHz], VIN=100[mVp-p] *3 |

Preamplifier/LPF/differentiator (BPF)

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Conditions |
|---|---|---|---|---|---|---|
| Filter time constant accuracy | EFIL | −10 | — | +10 | % | *3 |
| Total gain (preamplifier/ LPF/differentiator) (1) | GVDD1 | 40.5 | 44.5 | 48.5 | dB | f=250[kHz], VIN=2.5[mVp-p] (differential) (2MB, XTR1=L, FILC=H) |
| Total gain (preamplifier/ LPF/differentiator) (2) | GVDD2 | 43.5 | 47.5 | 51.5 | dB | f=250[kHz], VIN=2.5[mVp-p] (differential) (2MB, XTR1=H, FILC=H) |
| Differentiator output peaking frequency setting range | $f_0$ | 0.1 | — | 0.5 | MHz | Defined according to typical value in the settings |

*3 RRCC=2.0 [kΩ] (XHD=L, XTR1=H, F2=L, FILC=H)

Comparator and pulse shaper

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Conditions |
|---|---|---|---|---|---|---|
| TDF M/M pulse width accuracy (1) | TDF1 | −10 | — | +10 | % | XHD=H, F2=L (Typ. : 2470[ns]) f=62.5[kHz]~125[kHz] *4 |
| TDF M/M pulse width accuracy (2) | TDF2 | −10 | — | +10 | % | XHD=H, F2=H (Typ. : 2040[ns]) f=62.5[kHz]~125[kHz] *4 |
| TDF M/M pulse width accuracy (3) | TDF3 | −10 | — | +10 | % | XHD=L, F2=H/L (Typ. : 1230[ns]) f=125[kHz]~250[kHz] *4 |
| RD pulse width | TRD | 270 | 400 | 530 | ns | Judgment level 1.5 [V] |
| Rise time | TTLH | — | — | 70 | ns | Rise time till 0.4 [V] - 2.0 [V] |
| Fall time | TTHL | — | — | 70 | ns | Fall time till 2.0 [V] - 0.4 [V] |
| Peak shif | P. S. | — | — | 1.0 | % | f=250[kHz] , VIN=1[mVp-p] (differential) |
| Output "L" level voltage | VOL | — | — | 0.5 | V | |
| Output "H" level voltage | VOH | 2.7 | — | — | V | Rise level at 0.4 [V] to 70 [ns] |

*4 RRCC=2.0 [kΩ]

Write circuit

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Conditions |
|---|---|---|---|---|---|---|
| Write current adjust ment range | IWR | 2.0 | — | 20 | mA0-p | |
| Write current accuracy | ACIW | −7.0 | — | +7.0 | % | *5 |
| Write current pairability | △IWR | −1.0 | — | +1.0 | % | RWCC=2.4[kΩ] |
| Write current supply voltage dependency | PSIW | −4.0 | −0.8 | +3.0 | %/V | RWCC=2.4[kΩ] |
| Output saturation voltage | VSATRW | — | 0.4 | 1.0 | V | IWR=12[mA] |
| Off-state leakage current | ILKRW1 | — | — | 20 | μA | Unselected side |
| | ILKRW2 | — | — | 50 | μA | Selected side |
| Minimum write data pulse width | TWD | 70 | — | — | ns | |
| Write current inner track/ outer track ratio precision | ACIWTR | ±10× (Ratio of inner edge to outer edge) | | | % | *6 |

*5 RWCC=2.4 [kΩ] , adapted for desiredsetting of XTR1, XTR2
*6 Error in setting ratio (reference: XTR1=L, XTR2=L)

Erase output

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Conditions |
|---|---|---|---|---|---|---|
| Erase current adjustment range | IER | — | — | 40 | mA | |
| Output saturation voltage | VSATER | — | 0.2 | 0.6 | V | IER=40[mA] |
| Output leakage current | IOH | — | — | 10 | μA | OFF, ED0 = ED1 = Vcc |

Logic input

| Parameter | Symbol | Min. | Typ. | Max. | Unit | Conditions |
|---|---|---|---|---|---|---|
| Input voltage, high level | VIH | 2.0 | — | — | V | Excluding FILC |
| Input voltage, low level | VIL | — | — | 0.8 | V | Excluding FILC |
| Input voltage hysteresis | VH | 0.15 | — | — | V | Applies to XWD, XWG, XEG, XS1 |
| Input current, low level | IIL1 | — | 50 | 100 | μA | Vcc=5[V] VIL=GND<br>Applies to XWG, XEG, XHD |
| Tri-state interface | VIH | 4.2 | — | — | V | Applies to FILC |
| | VIM | 2.0 | 2.5 | 3.0 | V | Applies to FILC |
| | VIL | — | — | 0.8 | V | Applies to FILC |
| | IIH | — | 50 | 100 | μA | Vcc = 5[V], VIH = 5[V], applies to FILC |
| | IIL | — | 50 | 100 | μA | Vcc = 5[V], VIL = 0[V], applies to FILC |

●Read characteristics

| Density | | | | 1MB | | | | 1.6MB | | 2MB | |
|---|---|---|---|---|---|---|---|---|---|---|---|
| Transfer rate | | | FILC | 250[kbps] | | 300[kbps] | | 500[kbps] | | 500[kbps] | |
| Input | Mode | XHD | NO CARE | HI | | HI | | LOW | | LOW | |
| | | F2 | NO CARE | LOW | | HI | | HI | | LOW | |
| | Track | XTR1 (XSWF) | NO CARE | Outer track LOW | Inner track HI | Outer track LOW | Inner track HI | Outer track LOW | Inner track HI | Outer track LOW | Inner track HI |
| Output | Filter | $f_0$ [kHz] Characteristic *1 | HI | 144 | 162 | 171 | 192 | 324 | 422 | 384 | 358(C) |
| | | | OPEN | 167 | 182 | 201 | 216 | 309 | 400 | 336 | 361(B) |
| | | | LOW | 139 | 162 | 165 | 192 | 301 | 384 | 350 | 361(B) |
| | TDF | [nSEC] | NO CARE | 2470 | | 2040 | | 1230 | | 1230 | |

Note) *1 (B) Chebyshev characteristics. (However RRCC=2.0 [kΩ] )
(C) All are Butterworth characteristics except 2MB inner edges with high-ripple Chebyshev characteristics.

Total filter peak frequency setting

$f_0 = a / (RRCC\ [k\Omega] + 0.09)$ [kHz]

| FILC | "H" | "M" | "L" | |
|---|---|---|---|---|
| a = | 300 | 353 | 290 | 250 [kbps] outer track |
| | 339 | 380 | 339 | 250 [kbps] inner track |
| | 357 | 420 | 345 | 300 [kbps] outer track |
| | 401 | 451 | 401 | 300 [kbps] inner track |
| | 677 | 646 | 629 | 500 [kbps] outer track (when F2 = H) |
| | 882 | 836 | 732 | 500 [kbps] inner track (when F2 = H) |
| | 803 | 702 | 732 | 500 [kbps] outer track (when F2 = L) |
| | 748 | 754 | ← | 500 [kbps] inner track (when F2 = L) |

TDF time constant setting

250 [kbps] : $T = 940 \times RRCC\ [k\Omega] + 590$ [ns]
300 [kbps] : $T = 745 \times RRCC\ [k\Omega] + 550$ [ns]
500 [kbps] : $T = 377 \times RRCC\ [k\Omega] + 476$ [ns]

●Write current switching ratio

Track Outer edge ⟵ ⟶ Inner edge

| | XTR1 | L | | H | |
|---|---|---|---|---|---|
| | XTR2 | L | H | L | H |
| Density | 2MB | 0.450 | 0.400 | 0.350 | 0.300 |
| | 1.6MB | 0.500 | 0.450 | 0.400 | 0.350 |
| | 1MB (250kbps) | 0.933 | 0.833 | 0.766 | 0.677 |
| | 1MB (300kbps) | 1.000 | 0.900 | 0.800 | 0.700 |

Write current setting

$$Iwr = \frac{24.0}{RWCC\ [k\Omega]}\ [mA]$$

●Filter characteristics

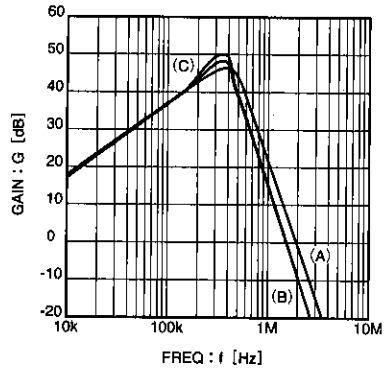
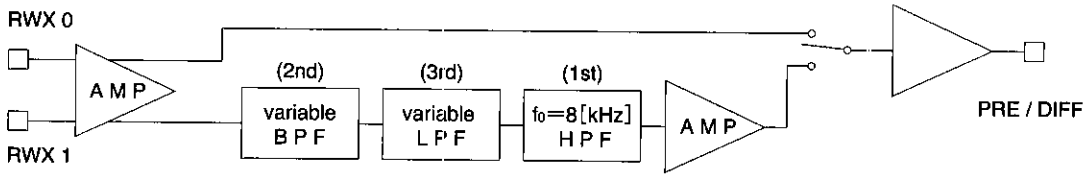
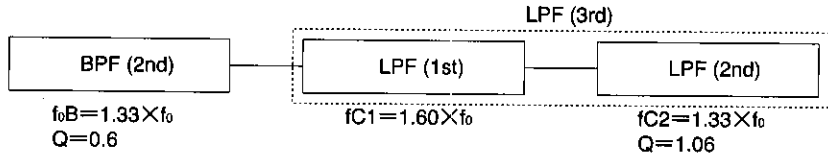



Fig. 1 PRE IN - DIFF OUT characteristic

Preamplifier-differentiator (BPF)-LPF

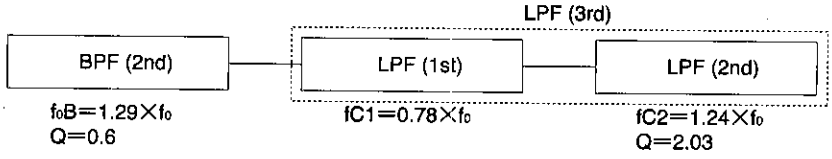



(A) Total characteristic peak frequency ($f_0$): 1M, 1.6M, 2M [outer edge]



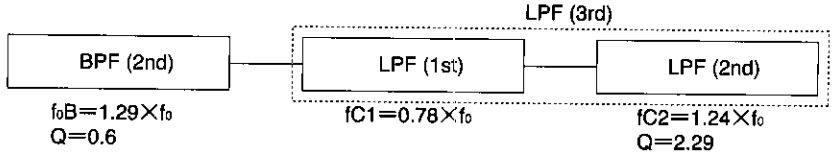

: Butterworth setting

(B) Total characteristic peak frequency ($f_0$) when FILC = low level or FILC = open, 2M [inner edge]




: Chebyshev setting

(C) Total characteristic peak frequency ($f_0$) when FILC = high level, 2M [inner edge]




: High ripple chebyshev setting

●Measurement circuit

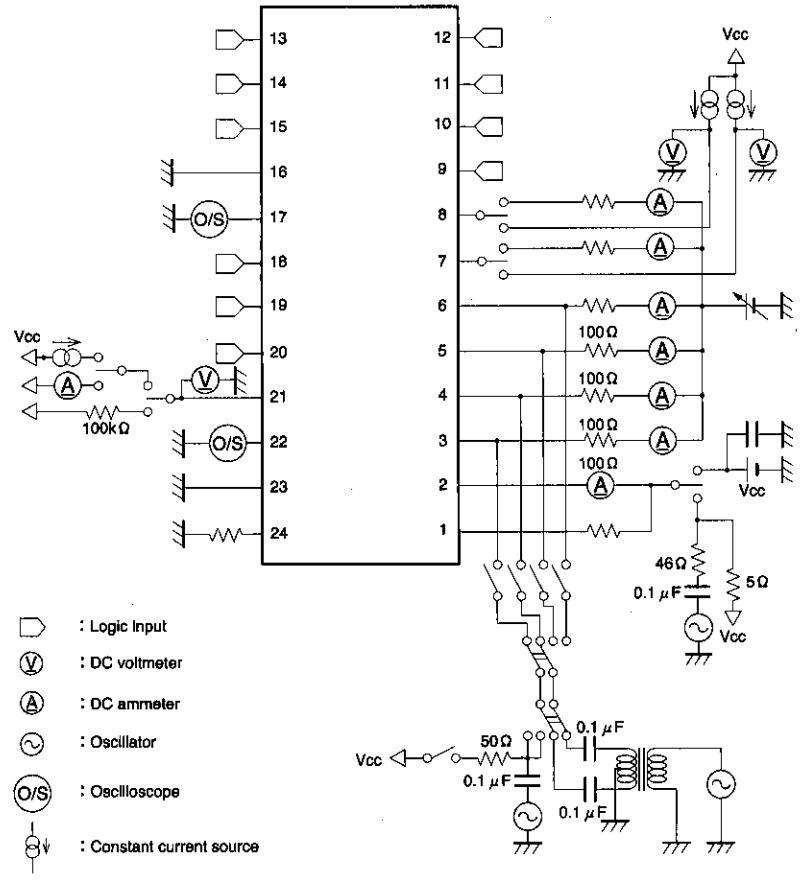



Fig. 2

●Circuit operation

(1) Read

The input signal from the head coils from each side of the disc is amplified by the preamplifier and then differentiated. The filter time constant can be set externally. After differentiation, the differential output is input to the comparator. The time domain filter detects zero cross, and the output is converted to read data. The monostable multivibrator width can be set externally, while the read data pulse width is a constant 400ns.

(2) Write

Input write data are converted to toggle movements by the internal flip-flops, operating the write driver. The write driver current is supplied by the write current generator, but the externally set current can be controlled according to density and by selecting inner track/outer track

(3) Erase

An open collector output pin is used, and the erase current is set with a resistor between it and the head.

(4) Power supply

When the low level voltage detector detects a drop in the supply voltage, writing and erasing are prohibited.

●Operation notes

(1) Use a short pattern for Vcc, and a sufficiently wide AGND and DGND. Keep the impedance between Vcc and GND low by inserting a bypass capacitor.

(2) Use a pattern that will minimize interference between digital signals and the head.

●Electrical characteristic curves

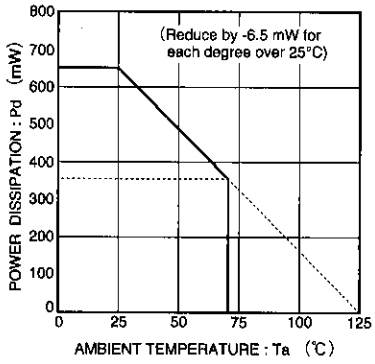



Fig. 3 Thermal derating curve

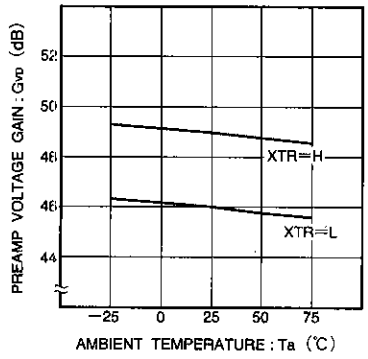



Fig. 4 Preamp voltage gain vs. ambient temperature

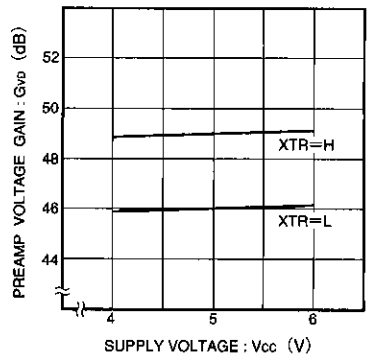



Fig. 5 Preamp voltage gain vs. supply voltage

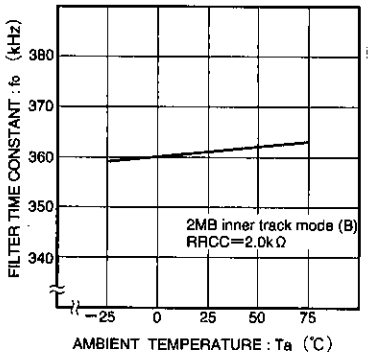



Fig. 6 Filter time constant ($f_0$) vs. ambient temperature

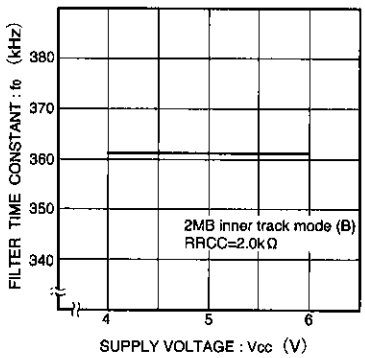



Fig. 7 Filter time constant ($f_0$) vs. supply voltage

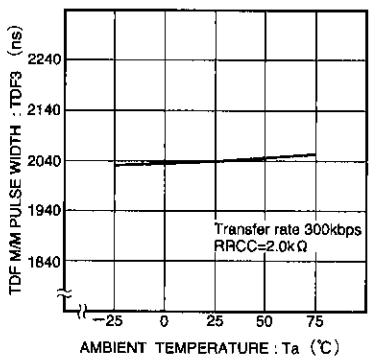



Fig. 8 TDF time constant vs. ambient temperature

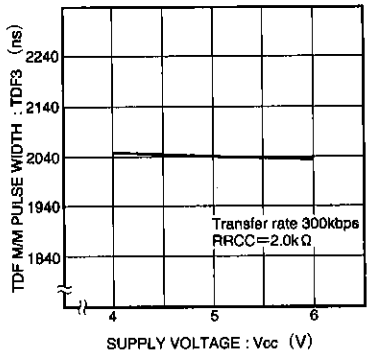



Fig. 9 TDF time constant vs. supply voltage

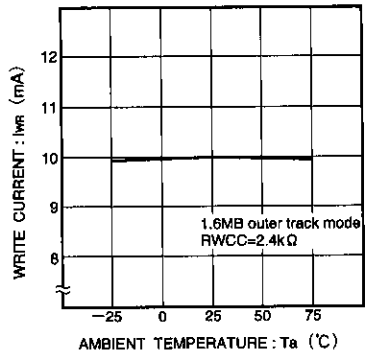



Fig. 10 Write current vs. ambient temperature

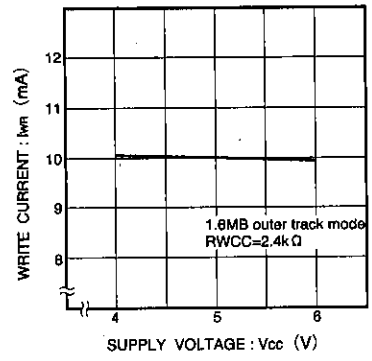



Fig. 11 Write current vs. supply voltage

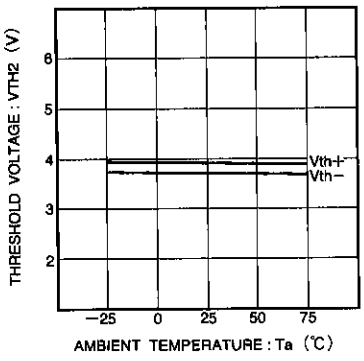



Fig. 12 Low level datection voltage vs. ambient temperature

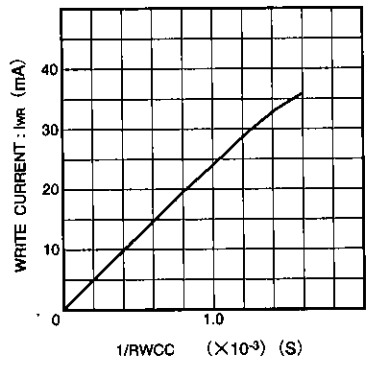
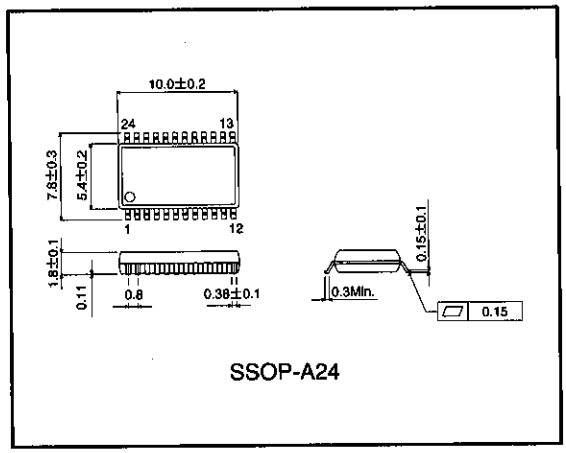



Fig. 13 Write current vs. write current adjustment resistance

●External dimensions (Units: mm)



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