Audio degital potentiometers
BH3532FS

The BH3532FS is a digital potentiometer designed for use in audio devices. Its built-in 22 Ω resistance systems can be used to set the data from the microcomputer in 256 steps.

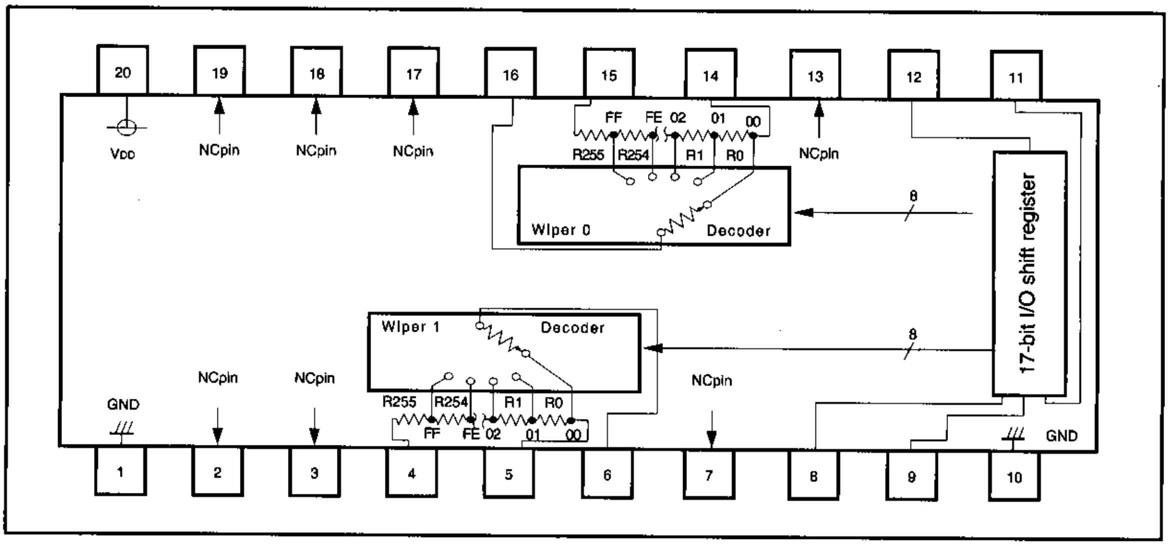
●Applications

Volume of recording and playing

●Features

1) Resistance can be set to any of 256 steps using digital codes (serial data).
2) Two built-in channels (Lch, Rch)
3) SSOP-A20 package

●Block diagram



●Absolute maximum ratings (Ta = 25℃)

Parameter	Symbol	Limits	Unit
Supply voltage	V_{CC}	7	V
Power dissipation	Pd	600*	mW
Operating temperature	Topr	−25～75	℃
Storage temperature	Tstg	−55～125	℃

* When used with Ta at greater than 25 ℃ moderate the power by 6 mW for every 1℃ above 25 ℃.

●Recommended operating conditions (Ta = 25℃)

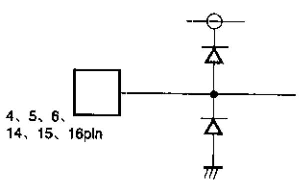
Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{DD}	3	−	5.5	V

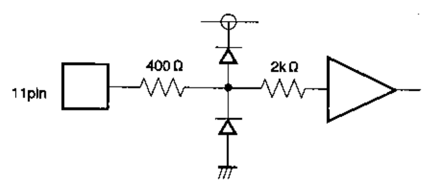
●Pin description

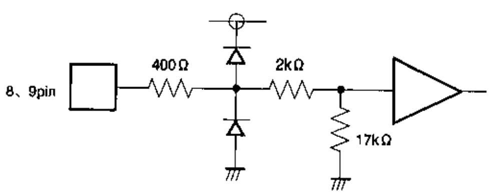
Pin No.	Pin Name	Function
1	GND	GND
2	NC	NCpin
3	NC	NCpin
4	H1	Ch 1 high position resistance pin
5	L1	Ch 1 low position resistance pin
6	W1	Pin for ch 1 wiper
7	NC	NCpin
8	EN	Overwrite authorization input pin
9	CLK	Clock input pin
10	GND	GND
11	DIN	Serial data input pin
12	DOUT	Serial data output pin
13	NC	NCpin
14	L0	Ch 0 low position resistance pin
15	H0	Ch 0 high position resistance pin
16	W0	Pin for Ch 0 wiper
17	NC	NCpin
18	NC	NCpin
19	NC	NCpin
20	V_{DD}	V_{DD}

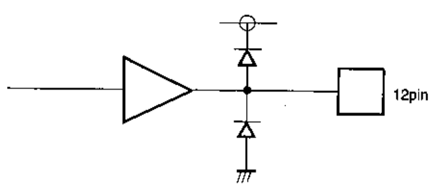
Note 1: Do not connect anything to the NC pin.

●Input/output circuit









●Electrical characteristics (Unless otherwise specified, Ta = 25℃, V_{CC} = 3.5V)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
<DC characteristics>						
Quiescent current	I_Q	50	100	150	μA	
Input leakage current	I_{LI}	−1.0	—	1.0	μA	*1
H input voltage	I_{IH}	3.0	—	—	V	
L input voltage	I_{IL}	—	—	0.5	V	
H output voltage	I_{OH}	3.0	—	—	V	I_{OH}=−100 μA
L output voltage	I_{OL}	—	—	0.5	V	I_{OL}=100 μA
Total resistance	R_T	17.6	22	26.4	kΩ	
Wiper resistance	R_W	0.4	0.8	1.6	kΩ	I_{OP}=500 μA
<AC characteristics>*2						
Clock frequency	F_{CLK}	—	—	1	MHz	
Clock pulse width	T_W	500	—	—	nS	
Data setup time	T_{SU}	300	—	—	nS	
Data hold time	T_H	100	—	—	nS	
Transmission lag time CLK→DOUT	T_{OLH} T_{OHL}	— —	— —	500 500	nS	
Transmission lag time EN→CLK	T_{CLH} T_{CHL}	500 500	— —	— —	nS	

◎Not designed for radiation resistence

*1 CLK input and EN input are pulled down when internal resistance is 17 kΩ.

*2 V_{DD}=3.5V

*3 Input capacity (reference value): 5 pF (max.) Output capacity (reference value): 7 pF (max.)

●Measurement circuit

The command during the Rw measurement is 00_H.

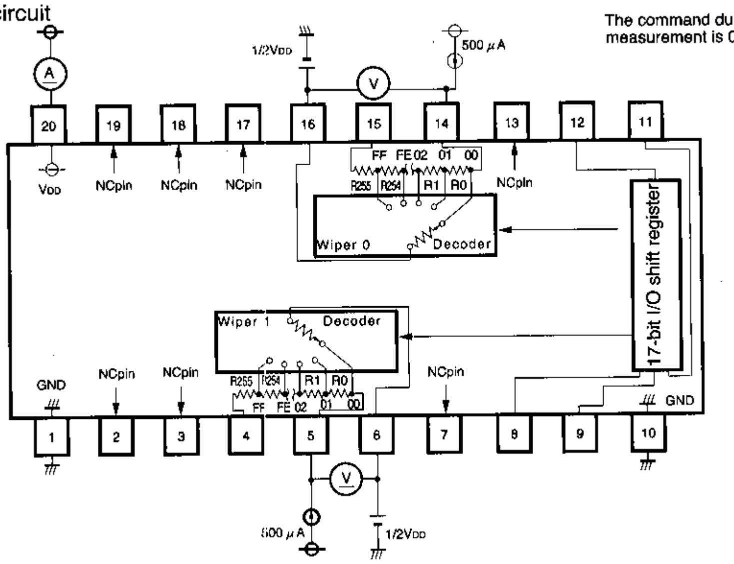


Fig. 1

●Circuit operation

The BH3532FS has two 22kΩ variable resistance systems which can be set in 256 steps (86Ω intervals). Resistance can be set in 256 steps using the MSB first 8-bit data.

Input data is 17-bit serial data. The first bit is always "L". The next eight bits set the resistance for wiper 1. The last eight bits set the resistance for wiper 0.

Input data is effective when the EN terminal is set to "H", and is put on hold when the EN terminal is set to "L". Also, the reading of the data is performed when CLK rises.

When input data is effective, the previous output data is output serially to the DOUT terminal.

See the figures below for more details.

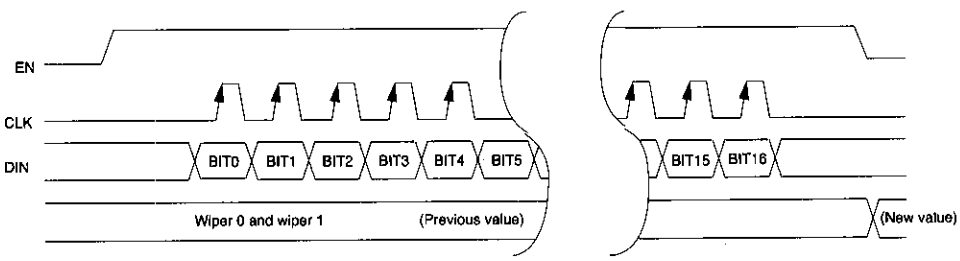


Fig. 2 Timing, figure 1

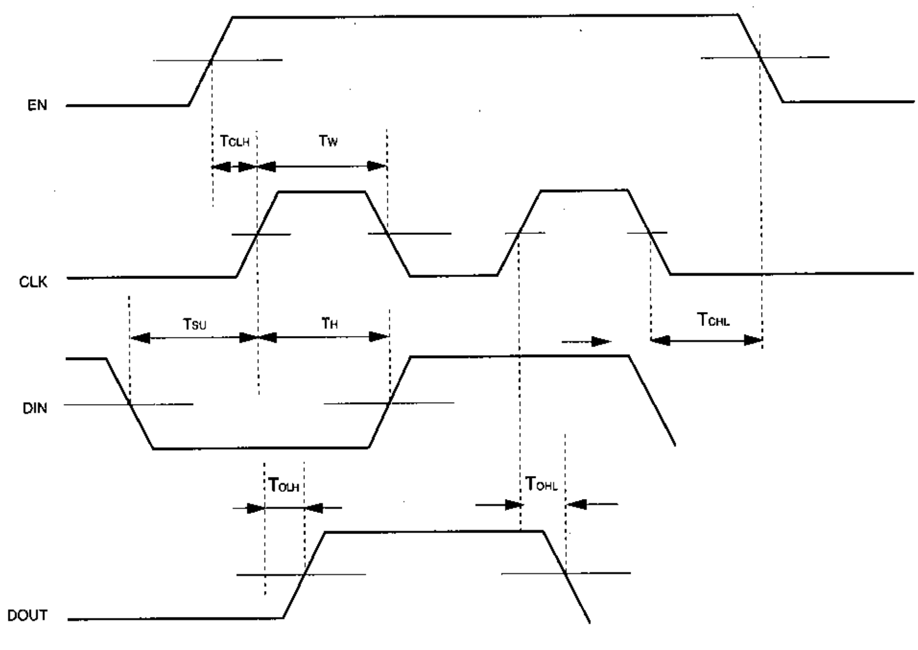


Fig. 3 Timing, figure 2

●Electrical characteristic curve

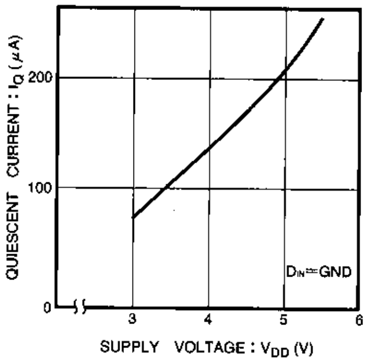


Fig. 4 Supply voltage vs .Quiescent curve

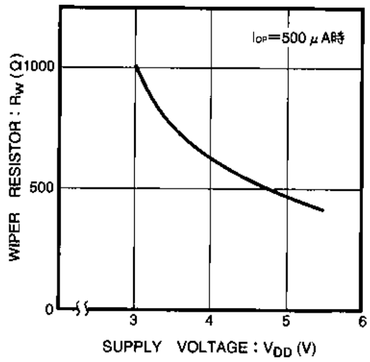
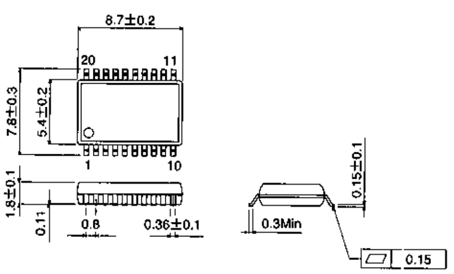


Fig. 5 Supply voltage vs. Wiper resistance

●External dimensions (Unit: mm)



SSOP-A20

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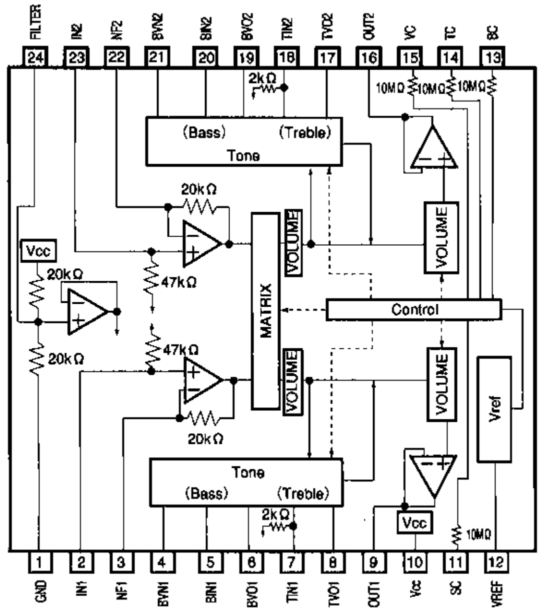
Sound control IC
BH3852S / BH3852FS

The BH3852S and BH3852FS are signal processing ICs designed for volume and tone control in CD radio cassettes and other audio products. They can be used without a microcomputer because they use DC current for control.

●Applications
CD radio cassettes, micro components, car stereos, televisions

●Features
1) Can control volume (main volume) and tone (bass, treble).
2) Volume is produced by a low-distortion, low-noise VCA, is controlled with DC current, and, due to an internal reference voltage with temperature compensation, can control two channels with a single variable resistor.
3) Input amp can be used for gain adjustment, and matrix surround yields powerful sound.

●Block diagram



●Absolute maximum ratings (Ta = 25℃)

Parameter		Symbol	Limits	Unit
Supply voltage		Vcc	10.0	V
Power dissipation	BH3852S	Pd	1050*1	mW
	BH3852FS		800 *2	
Operating temperature		Topr	−40~+85	℃
Storage temperature		Tstg	−55~+125	℃

*1 Reduced by 10.5mW for each increase in Ta of 1℃ over 25℃.
*2 Reduced by 8mW for each increase in Ta of 1℃ over 25℃.

●Recommended operating conditions

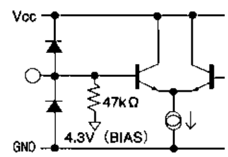
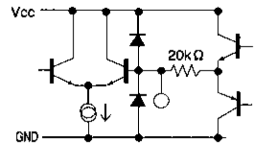
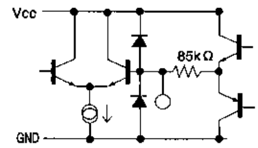
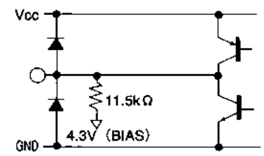
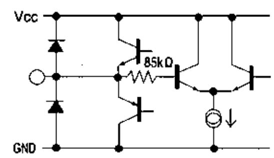
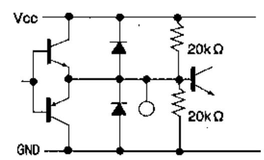
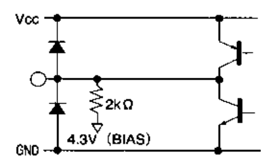
Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	Vcc	5.4	—	9.5	V

●Pin description

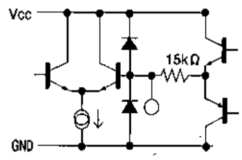
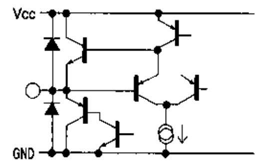
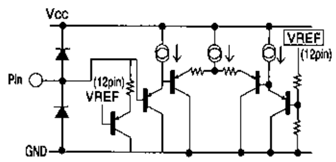
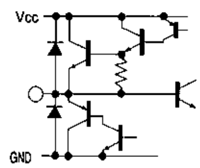
Pin No.	Pin Name	Function
1	GND	Ground
2	IN1	Ch1 volume input pin
3	NF1	Port for adjustment of input AMP gain
4	BVN1	Port for connection to ch 1 low-band filter
5	BIN1	Port for connection to ch 1 low-band filter
6	BVO1	Port for connection to ch 1 low-band filter
7	TIN1	Port for connection to ch 1 high-band filter
8	TVO1	Port for connection to ch 1 high-band filter
9	OUT1	Port for ch 1 volume output
10	Vcc	Power supply port
11	SC	Surround control pin
12	VREF	Standard voltage output pin

Pin No.	Pin Name	Function
13	BC	Bass control pin
14	TC	Treble control pin
15	VC	Volume control pin
16	OUT2	Port for ch 2 volume output
17	TVO2	Port for connection to ch 2 high-band filter
18	TIN2	Port for connection to ch 2 high-band filter
19	BVO2	Port for connection to ch 2 low-band filter
20	BIN2	Port for connection to ch 2 low-band filter
21	BVN2	Port for connection to ch 2 low-band filter
22	NF2	Port for adjustment of input AMP gain
23	IN2	Port for ch 2 volume input
24	FILTER	Filter pin

●Input / output circuit

Symbol	Pin no.	Pin voltage	Equivalent circuit	Description
IN1 IN2	2pin 23pin	4.3V 4.3V		Main volume input pin. Designed for input impedance of 47 kΩ (Typ).
NF1 NF2	3pin 22pin	4.3V 4.3V		Pin for adjustment of input amp gain. Approximately +6 dB with connection of 20 kΩ resistance.
BVN1 BVN2	4pin 21pin	4.3V 4.3V		Pin for low band filter connection.
BIN1 BIN2	5pin 20pin	4.3V 4.3V		Pin for low band filter connection.
BV01 BV02	6pin 19pin	4.3V 4.3V		Pin for low band filter connection.
FILTER	24pin	4.0V		Filter input pin.Filter input pin designed to operate at approximately 1/2 Vcc.Please install a capacitor of a bout 10 μF to the filter pin. Has built-in precharge and discharge circuits.
TIN1 TIN2	7pin 18pin	4.3V 4.3V		Pin for high band filter connection.

●Input / output circuit

Symbol	Pin no.	Pin voltage	Equivalent circuit	Description
TV01 TV02	8pin 17pin	4.3V 4.3V		Pin for high band filter connection.
OUT1 OUT2	9pin 16pin	4.0V 4.0V		Main volume output pin. OUT1 is the volume output for CH1. OUT2 is the volume output for CH2.
SC BC TC VC	11pin 13pin 14pin 15pin			VC: Volume pin TC: Treble pin BC: Bass pin SC: Surround pin
VREF	12pin	3.8V		Regulator output pin. Output requires capacitor for stopping oscillation.Output pin has built-in precharge and discharge circuits, so there is no problem when turned on or off, even with a large capacitor.
VCC	10pin	8V	Power supply voltage pin.	
GND	1pin	0V	GND pin. Connected to IC board.	

Note: All figures for pin voltage assume a power supply voltage (VCC) of 8V.

●Electrical characteristics (Unless otherwise specified, Ta = 25℃, V_{CC} = 8V, f = 1kHz, BW = 20 ~ 20kHz, VOL = Max., TONE = ALL FLAT, R_g = 600Ω, R_L = 10kΩ, INPUT_AMP_GAIN = 0dB)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Quiescent current	I_Q	8	17	25	mA	No signal
Max. input	Vim	1.8	2.0	–	Vrms	THD=1%, VOL=−20dB(ATT)
Max. output	Vom	1.8	2.0	–	Vrms	THD=1%
Voltage gain	G_V	−3.0	−1.0	1.0	dB	Vin=1Vrms
Max. attenuation	ATT	90	110	–	dB	V_O =1Vrms
Cross talk	V_{CT}	57	67	–	dB	V_O=1Vrms, BPF=400Hz~30kHz
Low-band control width	VBmax	12	15	18	dB	75Hz, Vin=100mVrms
	VBmin	−18	−15	−12	dB	75Hz, Vin=100mVrms
High-band control width	VTmax	12	15	18	dB	10kHz, Vin=100mVrms
	VTmin	−18	−15	−12	dB	10kHz, Vin=100mVrms
Mute attenuation	V_{MT}	90	110	–	dB	V_O=1Vrms *
Total Harmonic distortion	THD	–	0.03	0.1	%	V_O=0.3Vrms, BPF=400Hz~30kHz
Output noise voltage	$V_{NO}1$	–	25	35	μVrms	No signal VOL=MAX, Rg=0 *
Output noise voltage during full boost	$V_{NO}2$	–	73	113	μVrms	No signal TONE=ALL MAX, VOL=MAX, Rg=0 *
Residual output noise voltage	VM_{NO}	–	2	10	μVrms	No signal VOL=−∞, Rg=0 *
Standard power supply output voltage	V_{REF}	3.54	3.84	4.41	V	I_{REF}=3mA
Standard power supply output current power	I_{REF}	3.0	10	–	mA	VREF voltage drop of 0.1V or less
Channel balance	G_{CB}	−2.0	0	2.0	dB	CH1 taken as the standard for measurements.
Volume attenuation (-10 dB)	ATT10	−12.6	−10.6	−8.6	dB	V_{IN}=0dBV,VC=0.665XV_{REF}
VC port discharge current	IVC	–	0.2	0.4	μA	Pin 15 discharge current
TC port discharge current	ITC	–	0.2	0.4	μA	Pin 14th discharge current
BC port discharge current	IBC	–	0.2	0.4	μA	Pin 13th discharge current
SC port discharge current	ISC	–	0.2	0.4	μA	Pin 11th discharge current

* Items marked with an asterisk (*) were measured with the VP-9690A (displays mean detection and effective value), produced by Matsushita Communication Industrial.

◎Not designed for radiation resistence.

●Measurement circuit

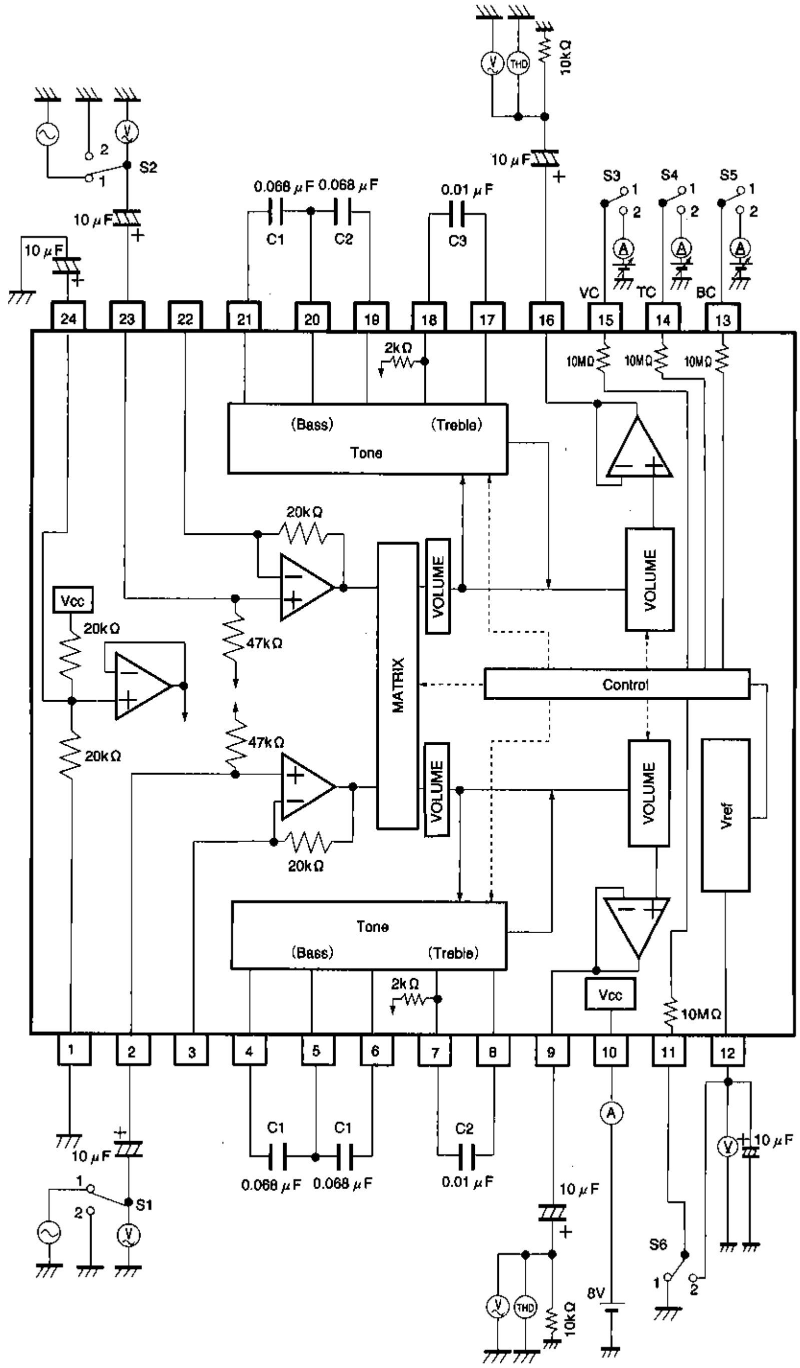
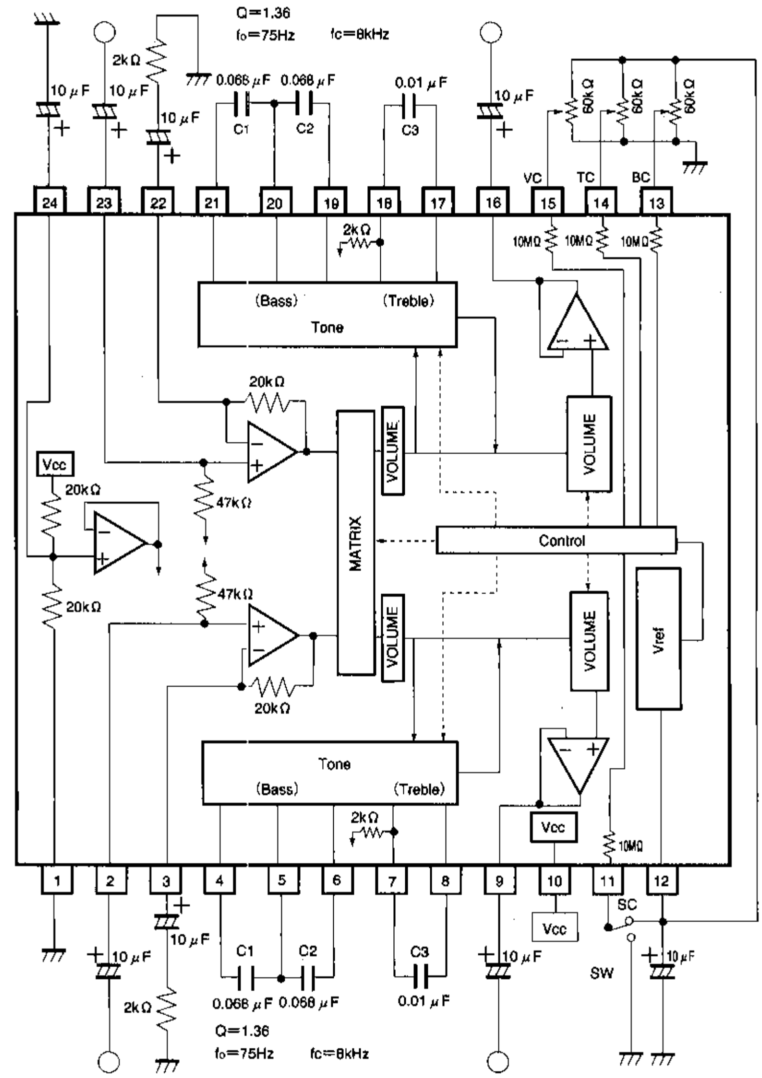


Fig. 1

●Application example



f0 adjustment (bass filter)

$f_o = (5.1 \times 10^{-6}) / C1$

fc adjustment (treble filter)

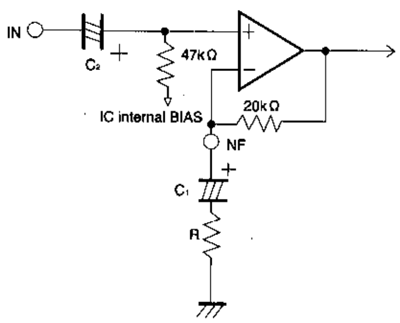
$f_c = (7.96 \times 10^{-6}) / C3$

Fig. 2

● Operation notes

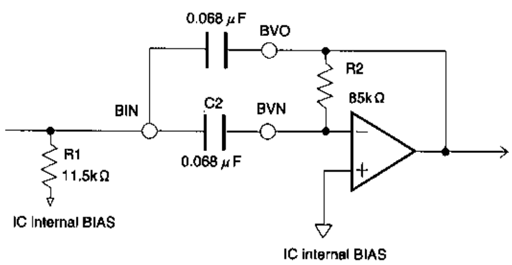
1. Operating power supply voltage range.
   As long as the operating power supply voltage and ambient temperature are kept within the specified range, the basic circuits are guaranteed to function, but be sure to check the constants as well as the element settings, voltage settings, and temperature settings. Also, volume curves sometimes depart from target values when there is a combination of low temperature and reduced power.

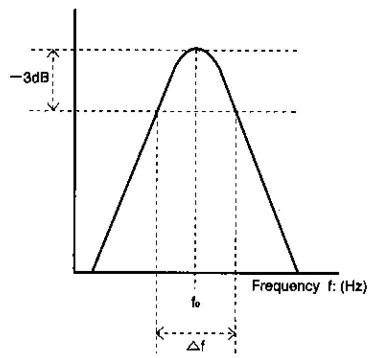
2. Primary amp



- The input impedance is 47kΩ.
- A buffer if R and C_1 are not present.
- The gain can be set by R and the 20kΩ.
  $G_{VC} = (R + 20k\Omega)/R$
  Note: Set C_2 (input coupling) and C_1 (used to set the gain) depending on the frequency band used.

3. Bass filter





- The BPF is composed of a multifeedback active filter.
  f_0 can be varied according to the value of C.
  (theoretical equation)

$$f_0 = \frac{1}{2\pi} \times \left(\frac{1}{R_1R_2C_1C_2} \right)^{\frac{1}{2}}$$

$$Q \fallingdotseq \left[\left(\frac{R_1}{R_2C_1C_2} \right)^{\frac{1}{2}} \times (C_1 + C_2) \right]^{-1}$$

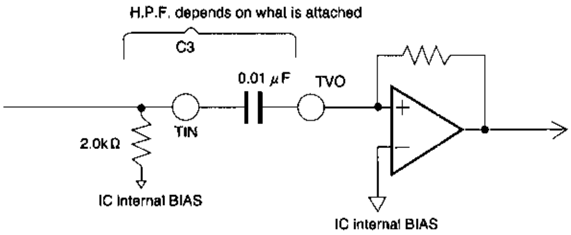
$$G = \frac{R_2}{5k\Omega} \times \left(1 + \frac{C_1}{C_2} \right)^{-1}$$

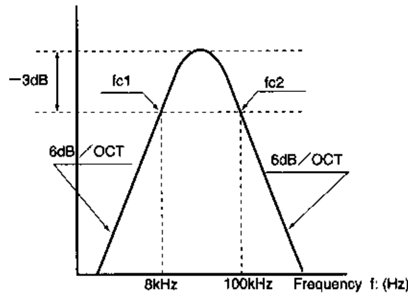
Note: Filter gain is calculated using the equation on the left. Total output gain is the sum of the gain for each of the internal circuits.

(When $R_1 = 11.5k\Omega$, $R_2 = 85k\Omega$, $C_1 = C_2 = C$)

$$f_0 = \frac{5.1 \times 10^{-6}}{C} \quad Q = 1.36 \quad G = 8.5$$

4. Treble filter





- Cutoff frequency (fc1) for the bypass filter can be changed using the attached C_3.

$$fc1 = \frac{1}{2\pi \times C_3 \times 2k\Omega}$$

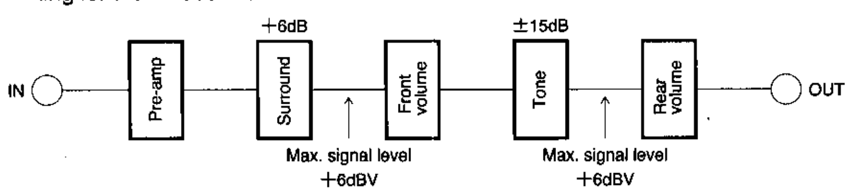
The fc1 for the recommended constant is approximately 8 kHz.

- fc2 is determined by the band of the built-in amp. fc2 is approximately 100 kHz.

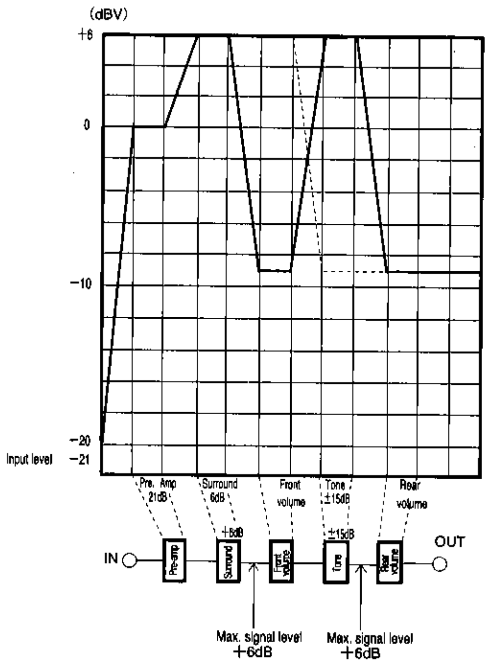
Tone control is designed to yield a variation of ±15dB (Typ.) when the frequency to be boosted or cut is at the peak or bottom of the filter frequency characteristic, so please take the frequency characteristic into consideration in designing the filter.

5. Signal level setting

The following figure represents the standard setting for the BH3852FS.

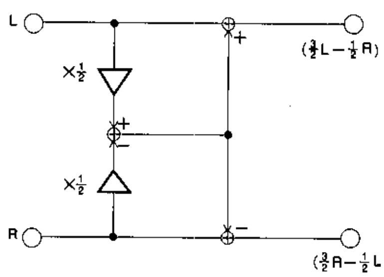


★As indicated above, if the front volume and rear volume input level are set so as not to exceed +6dBV (2Vrms), the pre-amp gain setting can be used to improve the S/N ratio.



The figure on the left is a level diagram.
Solid line: Input level during tone boost
Dotted line: Input level during tone cut

6. Matrix surround



◎The structure of the matrix surround is as shown in the figure above. Use the equations shown in the figure to calculate gain.

In-phase gain	0dB
Negative-phase gain	3.5dB

(Negative-phase gain only occurs when input is carried out at. a single Ch.)

7. DC control
It is recommended that DC control of the VC, TC, BC, and SC pins be performed by voltage delivered in variable volume from the VREF pin (12th pin). When using variable volume, take the discharge current of each pin into account in determining its settings.
Note:The voltage range for DC control is 0 (V) to V_{REF}(V). Be sure not to apply voltage greater than V_{REF}(V) to any pin.

8. GND
If several capacitors with good high-frequency characteristics are connected in parallel to the 12th-pin capacitor, the characteristics will be improved with respect to static electricity noise. (Recommended : ceramic capacitors of 0.001 μF to 0.1 μF)

●Electrical characteristic curves

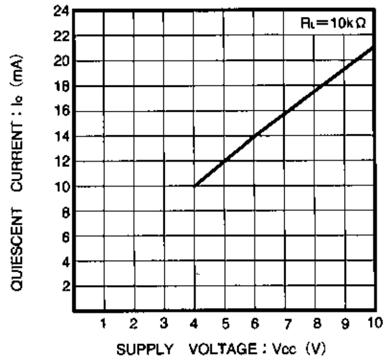


Fig. 3 Quiescent curve vs. supply voltage characteristics

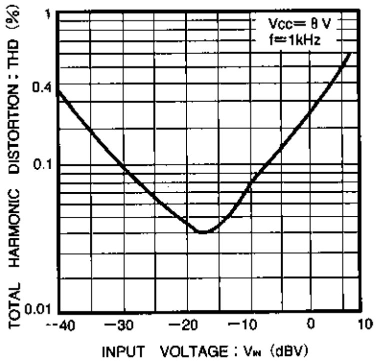


Fig.4 Harmonic distortion vs. Input voltage characteristics

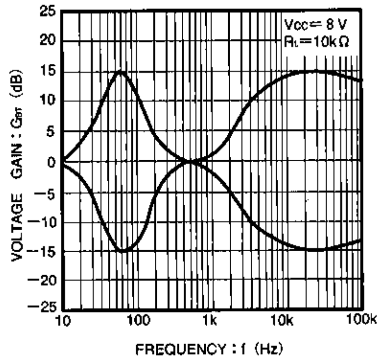
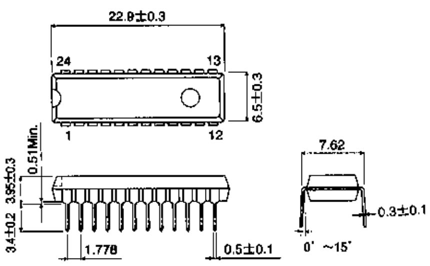


Fig. 5 Output gain vs. Frequency

●External dimensions (Unit: mm)

BH3852S



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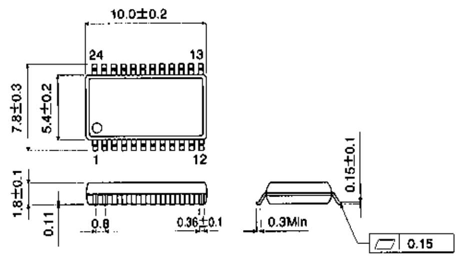
BH3852FS



SSOP-A24

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Sound control IC

BH3852S / BH3852FS

The BH3852S and BH3852FS are signal processing ICs designed for volume and tone control in CD radio cassettes and other audio products. They can be used without a microcomputer because they use DC current for control.

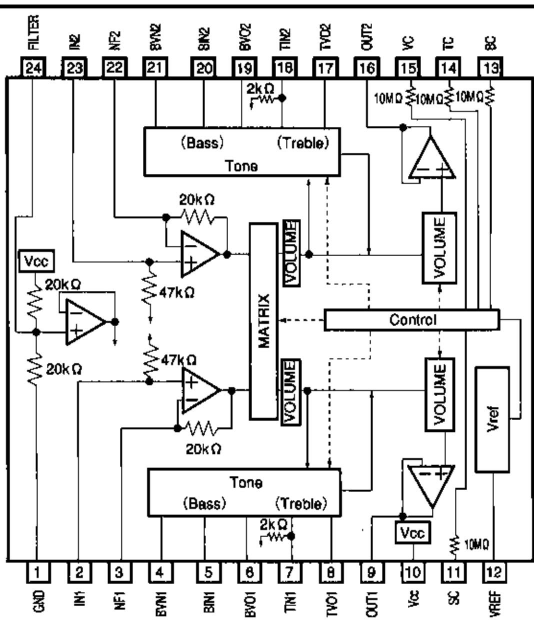
●Applications

CD radio cassettes, micro components, car stereos, televisions

●Features

1) Can control volume (main volume) and tone (bass, treble).
2) Volume is produced by a low-distortion, low-noise VCA, is controlled with DC current, and, due to an internal reference voltage with temperature compensation, can control two channels with a single variable resistor.
3) Input amp can be used for gain adjustment, and matrix surround yields powerful sound.

●Block diagram



●Absolute maximum ratings (Ta = 25℃)

Parameter		Symbol	Limits	Unit
Supply voltage		Vcc	10.0	V
Power dissipation	BH3852S	Pd	1050 *1	mW
	BH3852FS		800 *2	
Operating temperature		Topr	−40~+85	℃
Storage temperature		Tstg	−55~+125	℃

*1 Reduced by 10.5mW for each increase in Ta of 1℃ over 25℃.
*2 Reduced by 8mW for each increase in Ta of 1℃ over 25℃.

●Recommended operating conditions

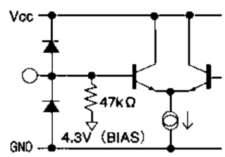
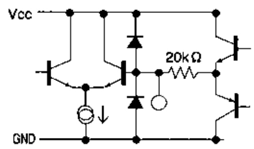
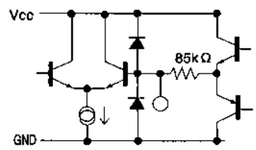
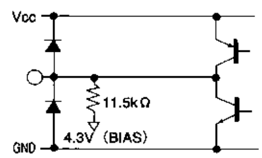
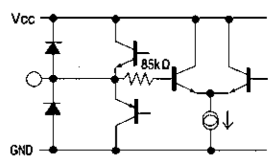
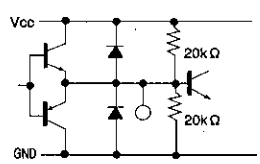
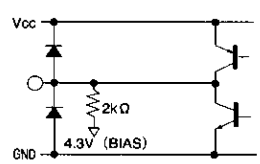
Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	Vcc	5.4	—	9.5	V

●Pin description

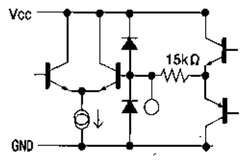
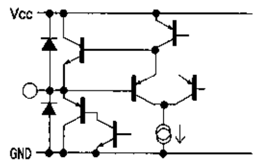
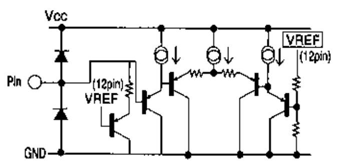
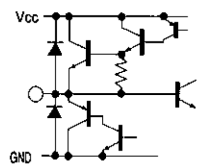
Pin No.	Pin Name	Function
1	GND	Ground
2	IN1	Ch1 volume input pin
3	NF1	Port for adjustment of input AMP gain
4	BVN1	Port for connection to ch 1 low-band filter
5	BIN1	Port for connection to ch 1 low-band filter
6	BVO1	Port for connection to ch 1 low-band filter
7	TIN1	Port for connection to ch 1 high-band filter
8	TVO1	Port for connection to ch 1 high-band filter
9	OUT1	Port for ch 1 volume output
10	Vcc	Power supply port
11	SC	Surround control pin
12	VREF	Standard voltage output pin

Pin No.	Pin Name	Function
13	BC	Bass control pin
14	TC	Treble control pin
15	VC	Volume control pin
16	OUT2	Port for ch 2 volume output
17	TVO2	Port for connection to ch 2 high-band filter
18	TIN2	Port for connection to ch 2 high-band filter
19	BVO2	Port for connection to ch 2 low-band filter
20	BIN2	Port for connection to ch 2 low-band filter
21	BVN2	Port for connection to ch 2 low-band filter
22	NF2	Port for adjustment of input AMP gain
23	IN2	Port for ch 2 volume input
24	FILTER	Filter pin

●Input / output circuit

Symbol	Pin no.	Pin voltage	Equivalent circuit	Description
IN1 IN2	2pin 23pin	4.3V 4.3V		Main volume input pin. Designed for input impedance of 47 kΩ (Typ).
NF1 NF2	3pin 22pin	4.3V 4.3V		Pin for adjustment of input amp gain. Approximately +6 dB with connection of 20 kΩ resistance.
BVN1 BVN2	4pin 21pin	4.3V 4.3V		Pin for low band filter connection.
BIN1 BIN2	5pin 20pin	4.3V 4.3V		Pin for low band filter connection.
BV01 BV02	6pin 19pin	4.3V 4.3V		Pin for low band filter connection.
FILTER	24pin	4.0V		Filter input pin.Filter input pin designed to operate at approximately 1/2 Vcc.Please install a capacitor of a bout 10 μF to the filter pin. Has built-in precharge and discharge circuits.
TIN1 TIN2	7pin 18pin	4.3V 4.3V		Pin for high band filter connection.

● Input / output circuit

Symbol	Pin no.	Pin voltage	Equivalent circuit	Description
TV01 TV02	8pin 17pin	4.3V 4.3V		Pin for high band filter connection.
OUT1 OUT2	9pin 16pin	4.0V 4.0V		Main volume output pin. OUT1 is the volume output for CH1. OUT2 is the volume output for CH2.
SC BC TC VC	11pin 13pin 14pin 15pin			VC: Volume pin TC: Treble pin BC: Bass pin SC: Surround pin
VREF	12pin	3.8V		Regulator output pin. Output requires capacitor for stopping oscillation.Output pin has built-in precharge and discharge circuits, so there is no problem when turned on or off, even with a large capacitor.
VCC	10pin	8V	Power supply voltage pin.	
GND	1pin	0V	GND pin. Connected to IC board.	

Note: All figures for pin voltage assume a power supply voltage (VCC) of 8V.

●Electrical characteristics (Unless otherwise specified, Ta = 25℃, V_{CC} = 8V, f = 1kHz, BW = 20 ~ 20kHz, VOL = Max., TONE = ALL FLAT, R_g = 600Ω, R_L = 10kΩ, INPUT_AMP_GAIN = 0dB)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Quiescent current	I_Q	8	17	25	mA	No signal
Max. input	Vim	1.8	2.0	–	Vrms	THD=1%, VOL=−20dB(ATT)
Max. output	Vom	1.8	2.0	–	Vrms	THD=1%
Voltage gain	G_V	−3.0	−1.0	1.0	dB	Vin=1Vrms
Max. attenuation	ATT	90	110	–	dB	V_O =1Vrms
Cross talk	V_{CT}	57	67	–	dB	V_O=1Vrms, BPF=400Hz~30kHz
Low-band control width	VBmax	12	15	18	dB	75Hz, Vin=100mVrms
	VBmin	−18	−15	−12	dB	75Hz, Vin=100mVrms
High-band control width	VTmax	12	15	18	dB	10kHz, Vin=100mVrms
	VTmin	−18	−15	−12	dB	10kHz, Vin=100mVrms
Mute attenuation	V_{MT}	90	110	–	dB	V_O=1Vrms *
Total Harmonic distortion	THD	–	0.03	0.1	%	V_O=0.3Vrms, BPF=400Hz~30kHz
Output noise voltage	$V_{NO}1$	–	25	35	μVrms	No signal VOL=MAX, Rg=0 *
Output noise voltage during full boost	$V_{NO}2$	–	73	113	μVrms	No signal TONE=ALL MAX, VOL=MAX, Rg=0 *
Residual output noise voltage	VM_{NO}	–	2	10	μVrms	No signal VOL=−∞, Rg=0 *
Standard power supply output voltage	V_{REF}	3.54	3.84	4.41	V	I_{REF}=3mA
Standard power supply output current power	I_{REF}	3.0	10	–	mA	VREF voltage drop of 0.1V or less
Channel balance	G_{CB}	−2.0	0	2.0	dB	CH1 taken as the standard for measurements.
Volume attenuation (-10 dB)	ATT10	−12.6	−10.6	−8.6	dB	V_{IN}=0dBV,VC=0.665XV_{REF}
VC port discharge current	IVC	–	0.2	0.4	μA	Pin 15 discharge current
TC port discharge current	ITC	–	0.2	0.4	μA	Pin 14th discharge current
BC port discharge current	IBC	–	0.2	0.4	μA	Pin 13th discharge current
SC port discharge current	ISC	–	0.2	0.4	μA	Pin 11th discharge current

* Items marked with an asterisk (*) were measured with the VP-9690A (displays mean detection and effective value), produced by Matsushita Communication Industrial.

◎Not designed for radiation resistence.

●Measurement circuit

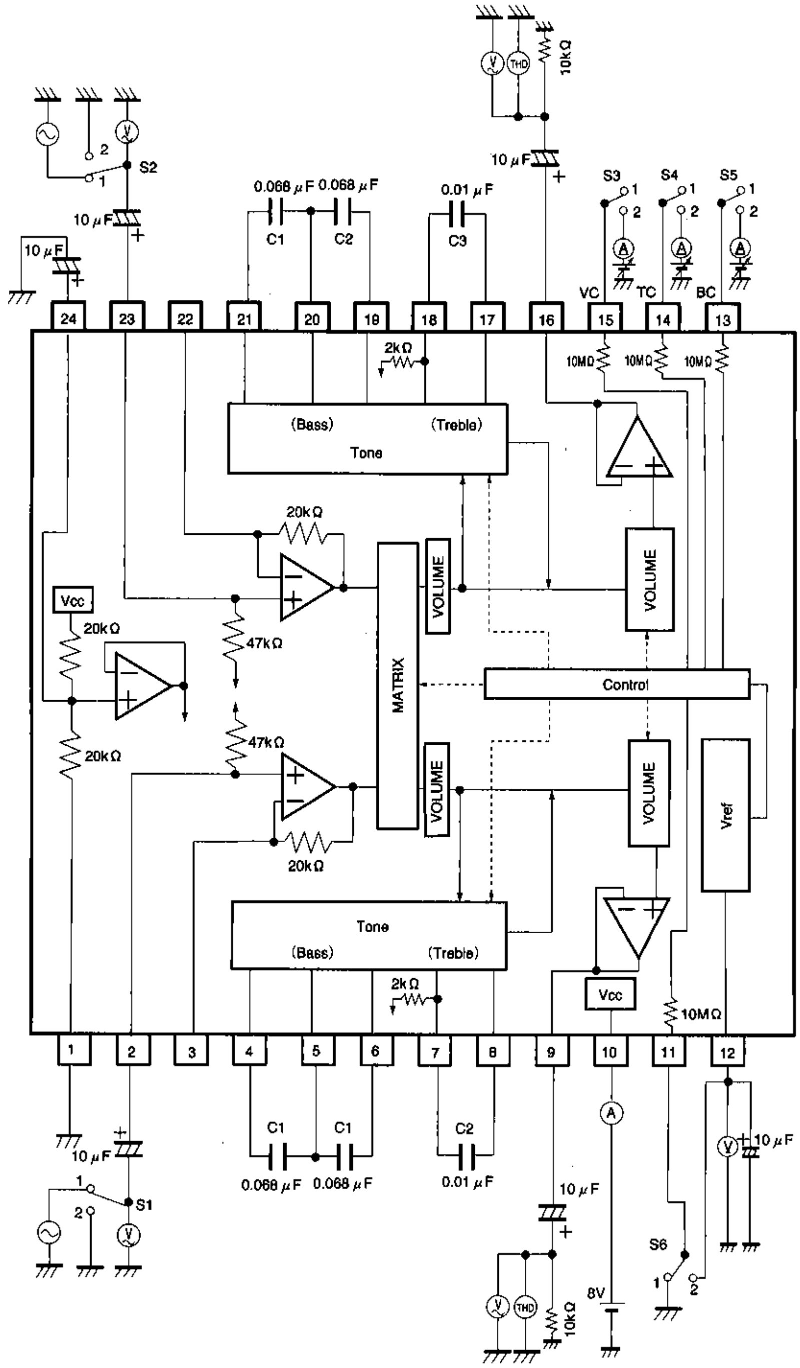
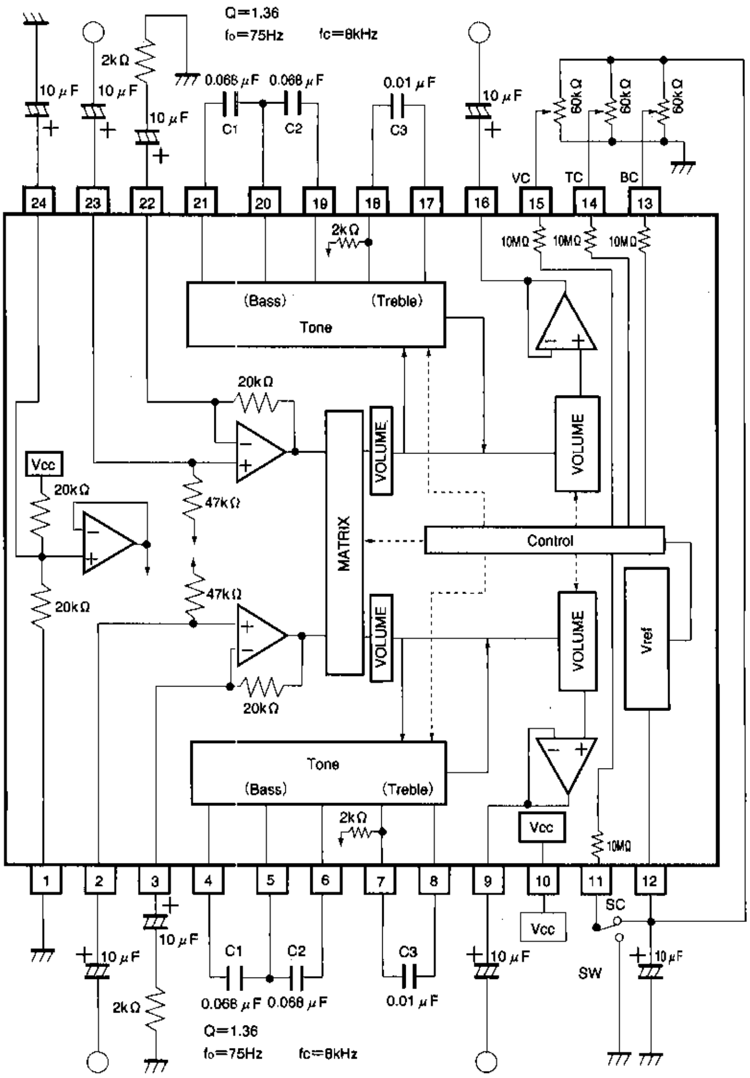


Fig. 1

●Application example



f0 adjustment (bass filter)

$f_o = (5.1 \times 10^{-6}) / C1$

fc adjustment (treble filter)

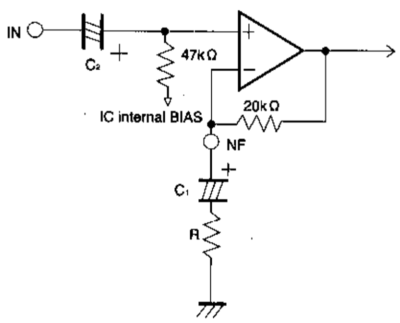
$fc = (7.96 \times 10^{-6}) / C3$

Fig. 2

●Operation notes

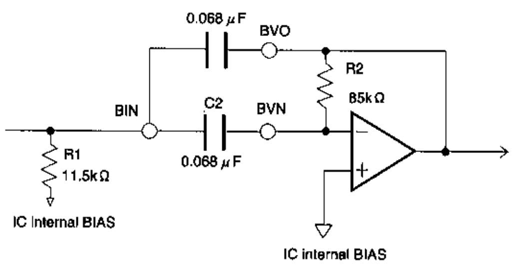
1. Operating power supply voltage range.
   As long as the operating power supply voltage and ambient temperature are kept within the specified range, the basic circuits are guaranteed to function, but be sure to check the constants as well as the element settings, voltage settings, and temperature settings. Also, volume curves sometimes depart from target values when there is a combination of low temperature and reduced power.

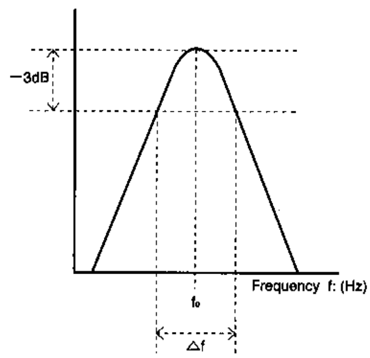
2. Primary amp



- The input impedance is 47kΩ.
- A buffer if R and C_1 are not present.
- The gain can be set by R and the 20kΩ.
  $G_{VC} = (R + 20k\Omega)/R$
  Note: Set C_2 (input coupling) and C_1 (used to set the gain) depending on the frequency band used.

3. Bass filter





- The BPF is composed of a multifeedback active filter.
  f_0 can be varied according to the value of C.
  (theoretical equation)

$$f_0 = \frac{1}{2\pi} \times \left(\frac{1}{R_1 R_2 C_1 C_2} \right)^{\frac{1}{2}}$$

$$G = \frac{R_2}{5k\Omega} \times \left(1 + \frac{C_1}{C_2} \right)^{-1}$$

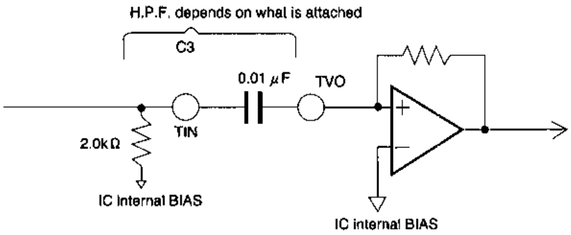
$$Q \fallingdotseq \left[\left(\frac{R_1}{R_2 C_1 C_2} \right)^{\frac{1}{2}} \times (C_1 + C_2) \right]^{-1}$$

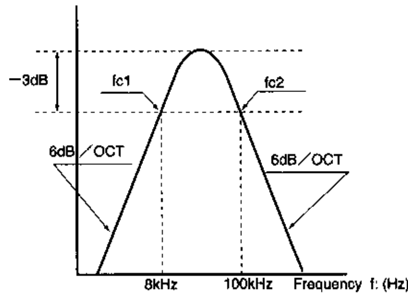
Note: Filter gain is calculated using the equation on the left. Total output gain is the sum of the gain for each of the internal circuits.

(When $R_1 = 11.5k\Omega$, $R_2 = 85k\Omega$, $C_1 = C_2 = C$)

$$f_0 = \frac{5.1 \times 10^{-6}}{C} \quad Q = 1.36 \quad G = 8.5$$

4. Treble filter





- Cutoff frequency (fc1) for the bypass filter can be changed using the attached C_3.

$$fc1 = \frac{1}{2\pi \times C_3 \times 2k\Omega}$$

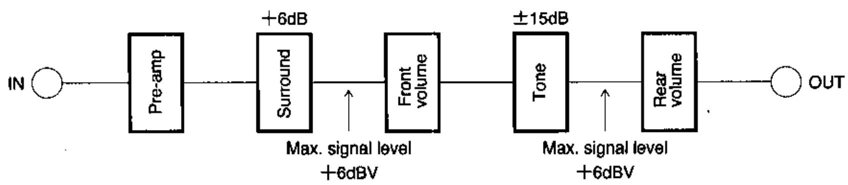
The fc1 for the recommended constant is approximately 8 kHz.

- fc2 is determined by the band of the built-in amp. fc2 is approximately 100 kHz.

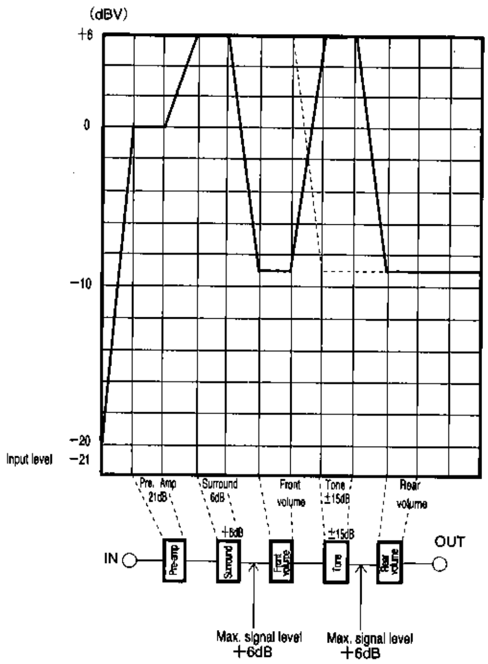
Tone control is designed to yield a variation of ±15dB (Typ.) when the frequency to be boosted or cut is at the peak or bottom of the filter frequency characteristic, so please take the frequency characteristic into consideration in designing the filter.

5. Signal level setting

The following figure represents the standard setting for the BH3852FS.

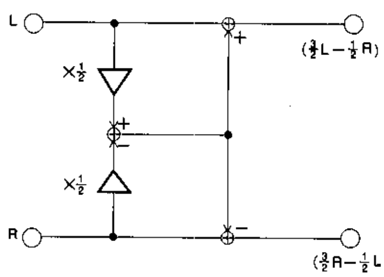


★As indicated above, if the front volume and rear volume input level are set so as not to exceed +6dBV (2Vrms), the pre-amp gain setting can be used to improve the S/N ratio.



The figure on the left is a level diagram.
Solid line: Input level during tone boost
Dotted line: Input level during tone cut

6. Matrix surround



◎The structure of the matrix surround is as shown in the figure above. Use the equations shown in the figure to calculate gain.

In-phase gain	0dB
Negative-phase gain	3.5dB

(Negative-phase gain only occurs when input is carried out at. a single Ch.)

7. DC control
It is recommended that DC control of the VC, TC, BC, and SC pins be performed by voltage delivered in variable volume from the VREF pin (12th pin). When using variable volume, take the discharge current of each pin into account in determining its settings.
Note:The voltage range for DC control is 0 (V) to V_{REF}(V). Be sure not to apply voltage greater than V_{REF}(V) to any pin.

8. GND
If several capacitors with good high-frequency characteristics are connected in parallel to the 12th-pin capacitor, the characteristics will be improved with respect to static electricity noise. (Recommended : ceramic capacitors of 0.001 μF to 0.1 μF)

●Electrical characteristic curves

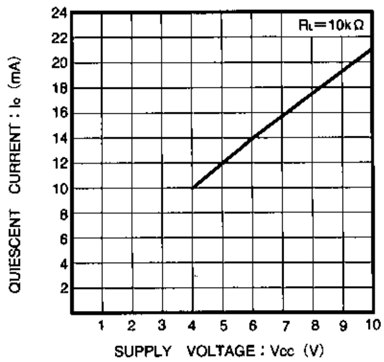


Fig. 3 Quiescent curve vs. supply voltage characteristics

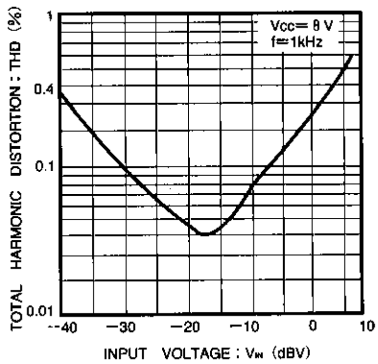


Fig.4 Harmonic distortion vs. Input voltage characteristics

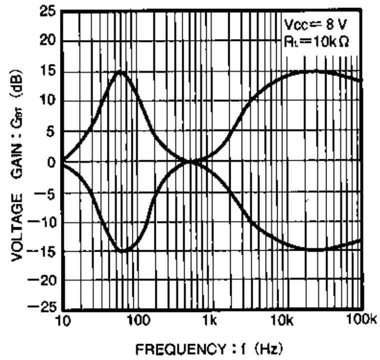
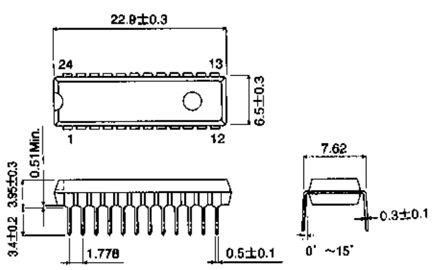


Fig. 5 Output gain vs. Frequency

●External dimensions (Unit: mm)

BH3852S



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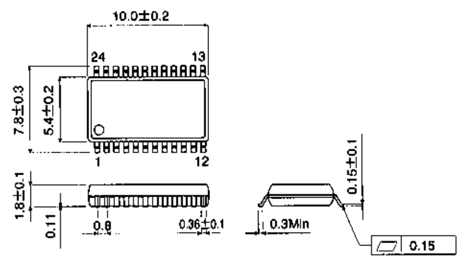

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Serial sound control IC

BH3854AS / BH3854AFS

The BH3854AS and BH3854AFS are signal processing ICs designed for volume and tone control in CD radio cassettes and other audio products. Their three-line serial control enables them to control volume and tone on the basis of signals from a microcomputer, etc.

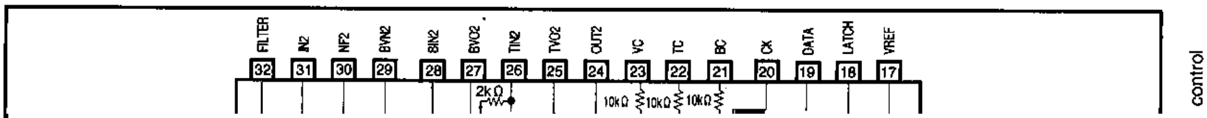
●Applications

CD radio cassettes, mini component stereo systems, car stereos

●Features

1) They facilitate direct serial control from a microcomputer of volume (main volume) and tone (bass, treble). DC control is also possible.
2) Volume is produced by a low-distortion, low-noise VCA. Designed to minimize step noise.
3) Input amp can be used for gain adjustment, and matrix surround yields powerful sound.
4) Stable standard voltage supply and built-in I / O buffer mean that few attachments are needed. SSOP32 package designed to save space.
5) Open collector has four outputs, which makes logic control possible.
6) Excellent for volume and tone control devices in CD radio cassettes, micro components, car stereos, televisions, etc.
7) Digital GND pin and analog GND pin are separated with an impedence of more than 1MΩ.

●Block diagram



●Absolute maximum ratings (Ta = 25℃)

Parameter	Symbol		Limits	Unit
Supply voltage	Vcc		8	V
Power dissipation	Pd	BH3854AS	1250*1	mW
		BH3854AFS	1000*2	
Operating temperature	Topr		−40~85	℃
Storage temperature	Tstg	BH3854AS	−55~125	℃
		BH3854AFS	−55~150	

*1 When used with a Ta greater than 25℃, reduce the power dissipation by 12.5 mW for every 1℃ over 25℃.
*2 When used with a Ta greater than 25℃, reduce the power dissipation by 8 mW for every 1℃ over 25℃.

●Recommended operating conditions (Ta = 25℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	Vcc	5.4	8.0	9.5	V

●Pin description

Pin No.	Pin Name	Function
1	A GND	Analog system ground
2	IN1	Pin for ch 1 volume input
3	NF1	Pin for adjustment of input amp gain
4	BVN1	Pin for connection to ch 1 low-band filter
5	BIN1	Pin for connection to ch 1 low-band filter
6	BVO1	Pin for connection to ch 1 low-band filter
7	TIN1	Pin for connection to ch 1 high-band filter
8	TVO1	Pin for connection to ch 1 high-band filter
9	OUT1	Pin for ch 1 volume output
10	Vcc	Power supply pin
11	SC	Time constant pin for prevention of switching shock
12	PORT1	Output pin
13	PORT2	Output pin
14	PORT3	Output pin
15	PORT4	Output pin
16	D GND	Digital system ground

Pin No.	Pin Name	Function
17	VREF	3.8V standard voltage output pin
18	LATCH	Pin for receiving LATCH data
19	DATA	Pin for receiving DATA
20	CK	Pin for receiving CLOCK data
21	BC	Time constant port for prevention of switching shock
22	TC	Time constant port for prevention of switching shock
23	VC	Time constant port for prevention of switching shock
24	OUT2	Pin for ch 2 volume output
25	TVO2	Pin for connection to ch 2 high-band filter
26	TIN2	Pin for connection to ch 2 high-band filter
27	BVO2	Pin for connection to ch 2 low-band filter
28	BIN2	Pin for connection to ch 2 low-band filter
29	BVN2	Pin for connection to ch 2 low-band filter
30	NF2	Pin for adjustment of input AMP gain
31	IN2	Pin for ch 2 volume input
32	FILTER	Filter pin

● Electrical characteristics (Unless otherwise specified, Ta = 25℃, V_{CC} = 8V, f = 1kHz, BW = 20 ~ 20kHz, VOL = Max, TONE = ALL FLAT, Rg = 600Ω, RL = 10kΩ, INPUT AMP GAIN = 0dB)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Quiescent current	I_Q	8	17	25	mA	No signal
Max. input	Vim	1.8	2.0	−	Vrms	THD=1%, VOL=−20dB(ATT)
Max. output	Vom	1.8	2.0	−	Vrms	THD=1%
Voltage gain	G_V	−3.0	−1.0	1.0	dB	Vin=1Vrms
Max. attenuation	ATT	90	110	−	dB	V_O =1Vrms
Cross talk	V_{CT}	64	70	−	dB	V_O=1Vrms, BPF=400Hz~30kHz
Low-band control width	VBmax	12	15	18	dB	75Hz, Vin=100mVrms
	VBmin	−18	−15	−12	dB	75Hz, Vin=100mVrms
High-band control width	VTmax	12	15	18	dB	10kHz, Vin=100mVrms
	VTmin	−18	−15	−12	dB	10kHz, Vin=100mVrms
Mute attenuation	V_{MT}	90	110	−	dB	V_O=1Vrms *
Harmonic distortion	THD	−	0.03	0.1	%	V_O=0.3Vrms, BPF=400Hz~30kHz
Output noise voltage	$V_{NO}1$	−	25	34	μVrms	No signal, VOL=MAX, Rg=0 *
Output noise voltage during full boost	$V_{NO}2$	−	80	120	μVrms	No signal, TONE=ALL MAX, VOL=MAX, Rg=0 *
Residual output noise voltage	VM_{NO}	−	2	10	μVrms	No signal, VOL=−∞, Rg=0 *
Standard power supply output voltage	V_{REF}	3.5	3.8	4.1	V	I_{REF}=3mA
Standard power supply output current power	I_{REF}	3.0	10	−	mA	V_{REF}>3.7V
Channel balance	G_{CB}	−2.0	0	2.0	dB	CH1 taken as the standard for measurements.
Port output current	I_{PMAX}	5.0	−	−	mA	
L output voltage	V_{OL}	−	0.4	0.5	V	I_{OL}=5mA
H output disable current	I_{OZH}	−	−	1.0	μA	V_O=5V
Volume attenuation (-10 dB)	ATT10	−12.0	−10.0	−8.0	dB	VIN = 0 dBV is the gain when the control data (10101010) is entered.

* Items marked with an asterisk (*) were measured with the VP-9690A (displays mean detection and effective value), produced by Matsushita Communication Industrial.

◎Not designed for radiation resistence.

● Timing chart constants

Parmater	Symbol	Min.	Typ.	Max.	Unit
H input voltage	V_{IH}	4.0	5.0	6.0	V
L input voltage	V_{IL}	−	0	1.0	V
Min. clock width	tw	2.0	−	−	μS
Min. data width	tw (DATA)	2.0	−	−	μS
Min. latch width	tw (LATCH)	2.0	−	−	μS
Setup time (DATA→CLK)	tsu	1.0	−	−	μS
Hold time (CLK→DATA)	th	1.0	−	−	μS
Setup time (CLK→LATCH)	ts	1.0	−	−	μS

Note: About the output pins...
- Pins 1 through 4 (pins 12 through 15) are reset when the power is turned ON.
- After the pins are reset, until the Vcc voltage setting for this IC (BH3854) is reached and the next data is input, the pins only operate while the CK, DATA, and LATCH lines are all maintained at LOW.
- Be sure that no more than 9V is applied to any of the output pins.

● Measurement circuit

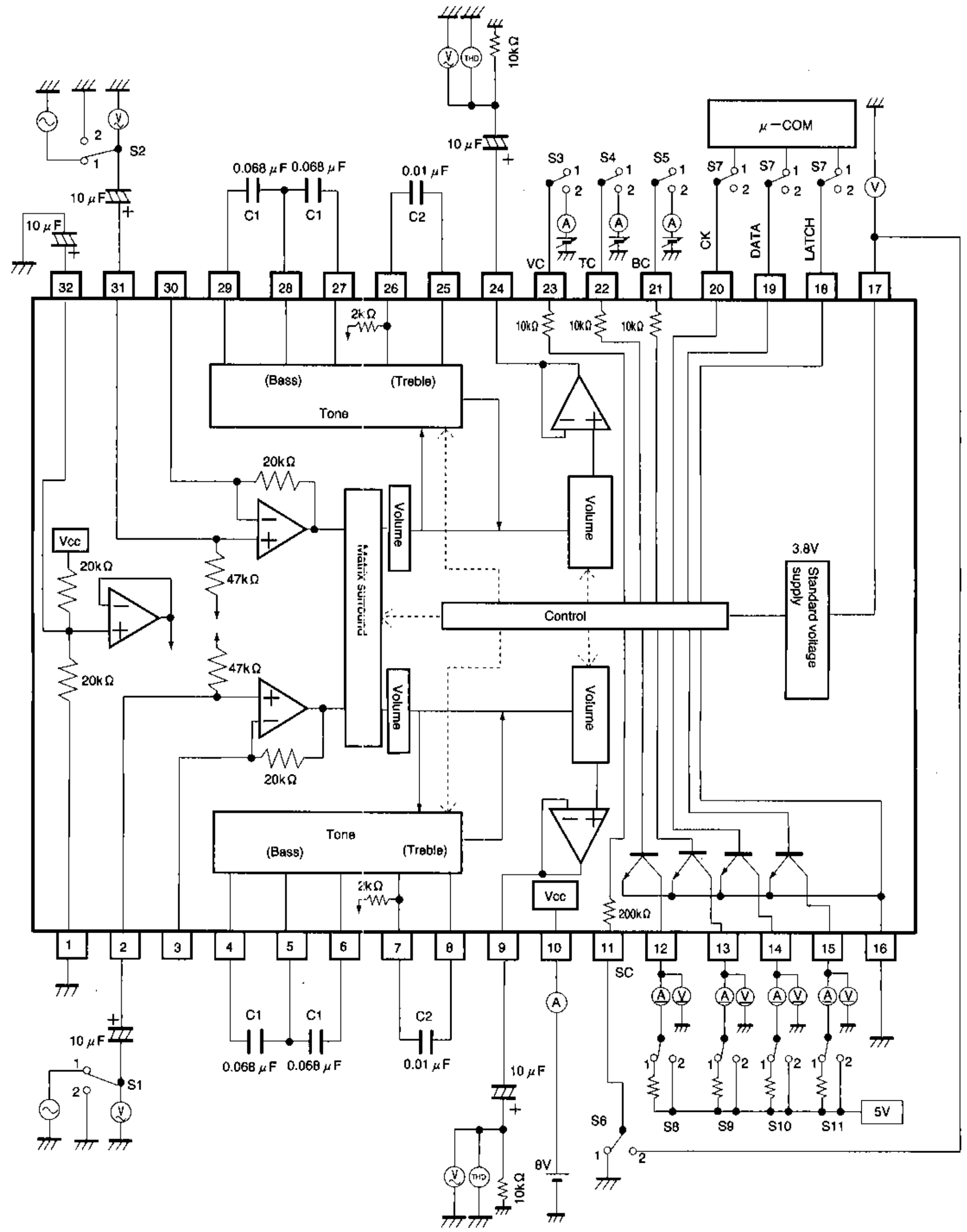


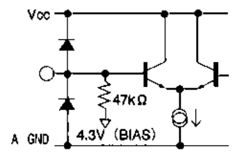
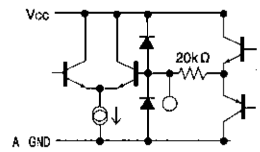
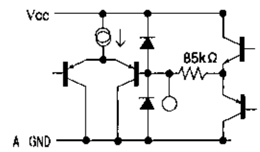
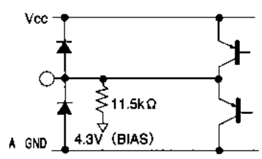
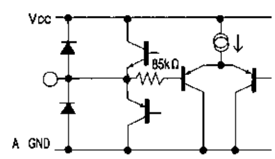
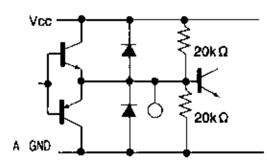
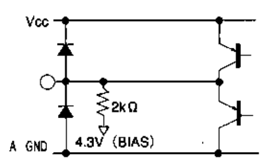
Fig. 1

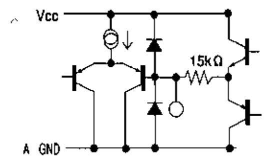
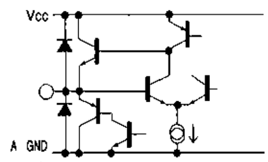
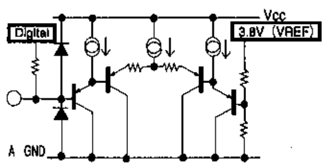
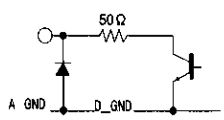
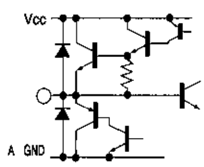
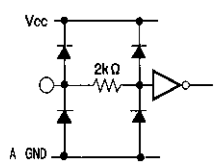
●Operation of measuring circuit switches

Parameter		S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11
Quiescent current		2	2	2A	2B	2B	2	2	1	1	1	1
Max. input		↓	↓	2B	↓	↓	↓	↓	↓	↓	↓	↓
Max. output		↓	↓	2A	↓	↓	↓	↓	↓	↓	↓	↓
Voltage gain		↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
Max. attenuation		↓	↓	A→C	↓	↓	↓	↓	↓	↓	↓	↓
Cross talk		1.2	2.1	2A	↓	↓	↓	↓	↓	↓	↓	↓
Low-band control width	Boost	1	1	↓	↓	2A	↓	↓	↓	↓	↓	↓
	Cut	↓	↓	↓	↓	2C	↓	↓	↓	↓	↓	↓
High-band control width	Boost	↓	↓	↓	2A	2B	↓	↓	↓	↓	↓	↓
	Cut	↓	↓	↓	2C	↓	↓	↓	↓	↓	↓	↓
Mute attenuation		↓	↓	A→C	2B	↓	↓	↓	↓	↓	↓	↓
Harmonic distortion		↓	↓	2A	↓	↓	↓	↓	↓	↓	↓	↓
Output noise voltage		2	2	↓	↓	↓	↓	↓	↓	↓	↓	↓
Output noise voltage during full boost		↓	↓	↓	2A	2A	↓	↓	↓	↓	↓	↓
Residual output noise voltage		↓	↓	2C	2B	2B	↓	↓	↓	↓	↓	↓
Standard power supply output voltage		↓	↓	2A	↓	↓	↓	↓	↓	↓	↓	↓
Standard power supply output current power		↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
Channel balance		1	1	↓	↓	↓	↓	↓	↓	↓	↓	↓
Port output current		2	2	↓	↓	↓	↓	1	↓	↓	↓	↓
L output voltage		↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
H output disable current		↓	↓	↓	↓	↓	↓	↓	2	2	2	2

*A, B, and C in the table represent the level of the variable voltage supply.
A = 3.8V
B = 1.9V
C = 0V

●Pin description

Symbol	Pin No	Pin voltage	Equivalent circuit	Description
IN1 IN2	2pin 31pin	4.3V 4.3V		Main volume input pin. Designed for input impedance of 47 kΩ (Typ).
NF1 NF2	3pin 30pin	4.3V 4.3V		Pin for adjustment of input amp gain. Approximately + 6 dB with connection of 20 kΩ resistance.
BVN1 BVN2	4pin 29pin	4.3V 4.3V		Pin for low band filter connection.
BIN1 BIN2	5pin 28pin	4.3V 4.3V		Pin for low band filter connection.
BV01 BV02	6pin 27pin	4.3V 4.3V		Pin for low band filter connection.
FILTER	32pin	4.0V		Filter input pin. Filter input pin designed to operate at approximately 1/2 Vcc. Please install a capacitor of about 10 μF to the filter pin. Has built-in precharge and discharge circuits.
TIN1 TIN2	7pin 26pin	4.3V 4.3V		Pin for high band filter connection.

Symbol	Pin No	Pin voltage	Equivalent circuit	Description
TV01 TV02	8pin 25pin	4.3V 4.3V		Pin for high band filter connection.
OUT1 OUT2	9pin 24pin	4.0V 4.0V		Main volume output pin. OUT1 is the volume output for CH1. OUT2 is the volume output for CH2.
SC BC TC VC	11pin 21pin 22pin 23pin			Time constant pin for prevention of switching shock noise SC : Surround pin BC : Bass pin TC : Treble pin VC : Volume pin
PORT1 PORT2 PORT3 PORT4	12pin 13pin 14pin 15pin			Output pin. Open collector output. Can pull a maximum of 5 mA.
V_{REF}	17pin	3.8V		3.8V regulator output pin. Output requires capacitor for stopping oscillation. Output pin has built-in precharge and discharge circuits, so there is no problem with start-up or shut-down even with a large capacitor.
LATCH DATA CK	18pin 19pin 20pin			Pin for receiving data from μcom. LATCH : latch line DATA : data line CK : clock line
VCC	10pin	8V	Power supply voltage pin.	
A_GND	1pin	0V	Analog GND pin. Connected to IC board.	
D_GND	16pin	0V	Digital GND pin. Separate from Analog GND pin.	

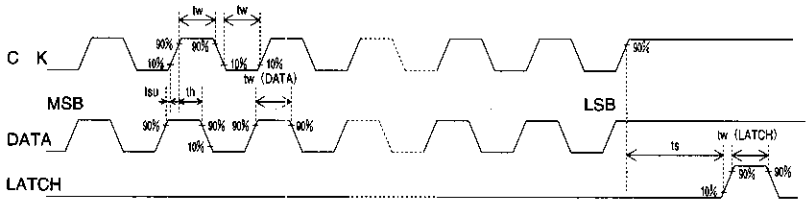
Note: All figures for pin voltage assume a power supply voltage (VCC) of 8V.

●Digital control specifications

●Data format : total of 23 bits

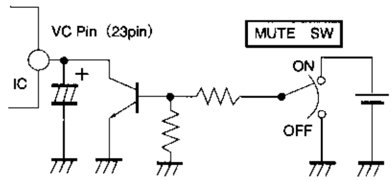
MSB							LSB
Volume	Treble	Bass	Surround	PORT1	PORT2	PORT3	PORT4
8bit	5bit	5bit	1bit	1bit	1bit	1bit	1bit

●Timing (recommended conditions)



★For timing chart constants, see the electrical characteristics.

- Surround is ON when the bit data is 0, and OFF when the bit data is 1.
- Pins 1 through 4 are set so that the output transistors will turn OFF if data is not input when the power is turned ON. They turn ON when the bit data is 1, and OFF when the bit data is 0.
- "H" level is 4V or greater. "L" level is 1V or less.
- Make the end of each control command LOW.



- The MUTE function can be controlled externally if the VC (volume control) pin is configured as shown in the diagram above. Attenuation is equal to the figure for attenuation when volume is at MIN.

●Volume data settings (reference values)

HEX Notation	Volume Gain	V_8 (MSB)	V_7	V_6	V_5	V_4	V_3	V_2	V_1 (LSB)
FF	0dB	1	1	1	1	1	1	1	1
E5	−1dB	1	1	1	0	0	1	0	1
DB	−2dB	1	1	0	1	1	0	1	1
D3	−3dB	1	1	0	1	0	0	1	1
CC	−4dB	1	1	0	0	1	1	0	0
C6	−5dB	1	1	0	0	0	1	1	0
C0	−6dB	1	1	0	0	0	0	0	0
BA	−7dB	1	0	1	1	1	0	1	0
B5	−8dB	1	0	1	1	0	1	0	1
B0	−9dB	1	0	1	1	0	0	0	0
AB	−10dB	1	0	1	0	1	0	1	1
A7	−11dB	1	0	1	0	0	1	1	1
A3	−12dB	1	0	1	0	0	0	1	1
9F	−13dB	1	0	0	1	1	1	1	1
9C	−14dB	1	0	0	1	1	1	0	0
98	−15dB	1	0	0	1	1	0	0	0
95	−16dB	1	0	0	1	0	1	0	1
91	−17dB	1	0	0	1	0	0	0	1
8E	−18dB	1	0	0	0	1	1	1	0
8A	−19dB	1	0	0	0	1	0	1	0

HEX Notation	Volume gain	V8 (MSB)	V7	V6	V5	V4	V3	V2	V1 (LSB)
87	−20dB	1	0	0	0	0	1	1	1
81	−22dB	1	0	0	0	0	0	0	1
7B	−24dB	0	1	1	1	1	0	1	1
75	−26dB	0	1	1	1	0	1	0	1
70	−28dB	0	1	1	1	0	0	0	0
6B	−30dB	0	1	1	0	1	0	1	1
66	−32dB	0	1	1	0	0	1	1	0
62	−34dB	0	1	1	0	0	0	1	0
5D	−36dB	0	1	0	1	1	1	0	1
59	−38dB	0	1	0	1	1	0	0	1
55	−40dB	0	1	0	1	0	1	0	1
51	−42dB	0	1	0	1	0	0	0	1
4D	−44dB	0	1	0	0	1	1	0	1
4A	−46dB	0	1	0	0	1	0	1	0
47	−48dB	0	1	0	0	0	1	1	1
43	−50dB	0	1	0	0	0	0	1	1
40	−52dB	0	1	0	0	0	0	0	0
3D	−54dB	0	0	1	1	1	1	0	1
3A	−56dB	0	0	1	1	1	0	1	0
37	−58dB	0	0	1	1	0	1	1	1
34	−60dB	0	0	1	1	0	1	0	0
32	−62dB	0	0	1	1	0	0	1	0
2F	−64dB	0	0	1	0	1	1	1	1
2D	−66dB	0	0	1	0	1	1	0	1
2B	−68dB	0	0	1	0	1	0	1	1
28	−70dB	0	0	1	0	1	0	0	0
26	−72dB	0	0	1	0	0	1	1	0
24	−74dB	0	0	1	0	0	1	0	0
23	−76dB	0	0	1	0	0	0	1	1
21	−78dB	0	0	1	0	0	0	0	1
1F	−80dB	0	0	0	1	1	1	1	1
1E	−82dB	0	0	0	1	1	1	1	0
1C	−84dB	0	0	0	1	1	1	0	0
00	−∞	0	0	0	0	0	0	0	0

Note: All figures in this table are reference values. When using this IC, check this table carefully and perform the appropriate setting.

●Treble settings (reference values)

Treble data

Settings MSB				LSB	Treble gain (dB)	HEX Notation
0	0	0	0	0	−15	00
0	0	1	0	0	−14	04
0	0	1	1	0	−12	06
0	1	0	0	0	−10	08
0	1	0	0	1	−8	09
0	1	0	1	0	−6	0A
0	1	0	1	1	−4	0B
0	1	1	0	0	−2	0C
0	1	1	1	1	±0	0F
1	0	1	0	0	+2	14
1	0	1	0	1	+4	15
1	0	1	1	0	+6	16
1	0	1	1	1	+8	17
1	1	0	0	0	+10	18
1	1	0	1	0	+12	1A
1	1	1	0	0	+14	1C
1	1	1	1	1	+15	1F

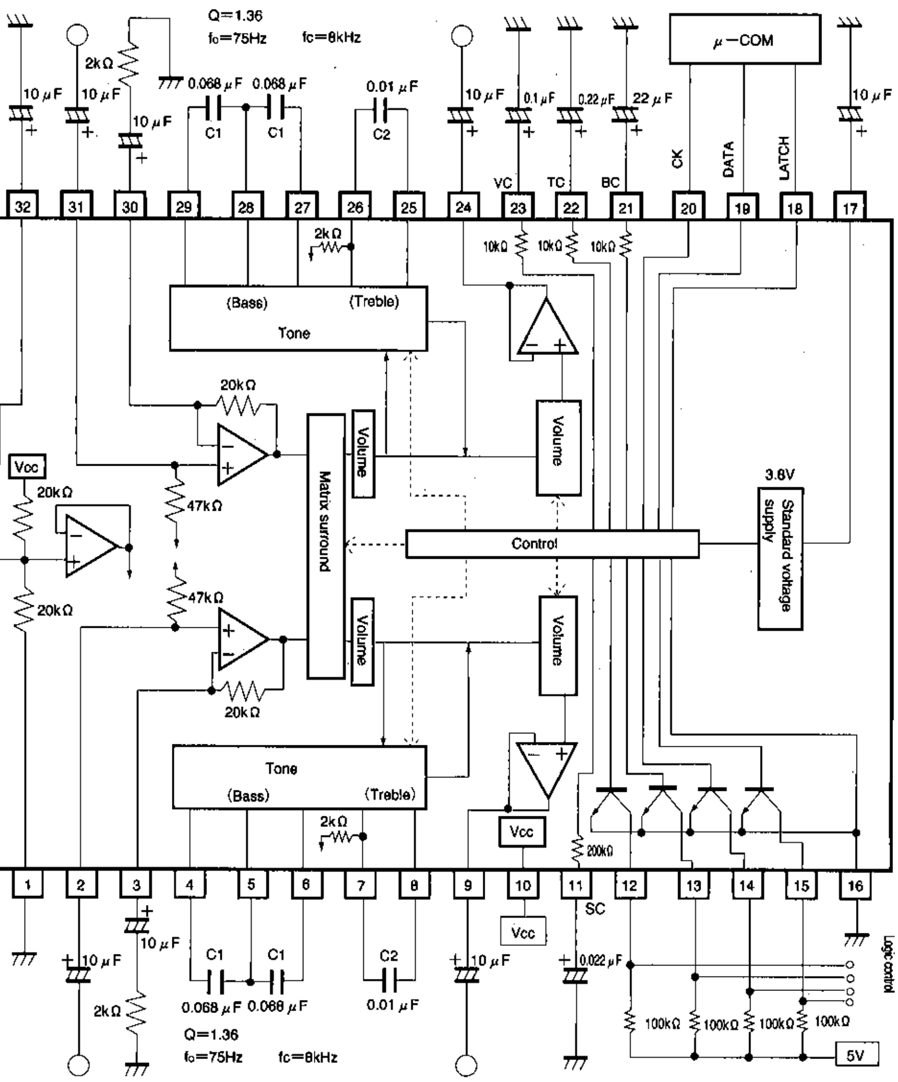
Bass data

Settings MSB				LSB	Bass Gain (dB)	HEX Notation
0	0	0	0	0	−15	00
0	0	1	0	1	−14	05
0	0	1	1	1	−12	07
0	1	0	0	1	−10	09
0	1	0	1	0	−8	0A
0	1	0	1	1	−6	0B
0	1	1	0	0	−4	0C
0	1	1	0	1	−2	0D
0	1	1	1	1	±0	0F
1	0	0	1	1	+2	13
1	0	1	0	0	+4	14
1	0	1	0	1	+6	15
1	0	1	1	0	+8	16
1	0	1	1	1	+10	17
1	1	0	0	1	+12	19
1	1	0	1	1	+14	1B
1	1	1	1	1	+15	1F

Notes:1. The gain values in the treble and bass data setting tables above are based on the assumption that the filter constants have been set so that maximum and minimum gain are equal to the peak and bottom values listed in the frequency characteristics drawings.

2. All figures in this table are reference values. When using this IC, check this table carefully and perform the appropriate setting.

●Application example



fo adjustment (bass filter)

$f_o = (5.1 \times 10^{-6}) / C1$

fc adjustment (treble filter)

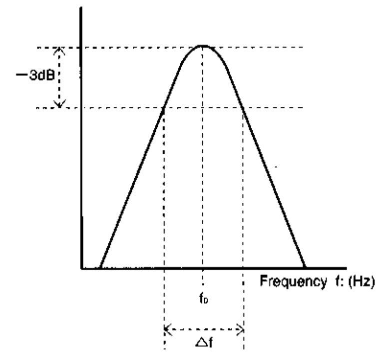
$f_c = (7.96 \times 10^{-5}) / C2$

Fig. 2

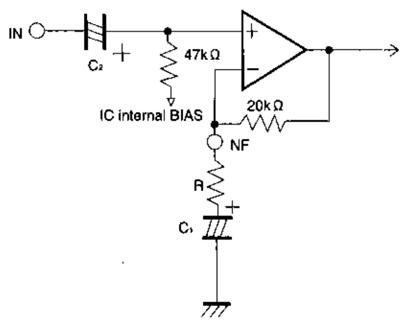
● Operation notes

1. Operating power supply voltage range

As long as the operating power supply voltage and ambient temperature are kept within the specified range, the basic circuits are guaranteed to function, but be sure to check the constants as well as the element settings, voltage settings, and temperature settings. Also, please take into consideration internal IC resistance dispersion (approx. ±20%) and temperature fluctuation when making settings for IC internal resistance, attachment resistance, capacitor gain, or frequency.



2. Primary amp

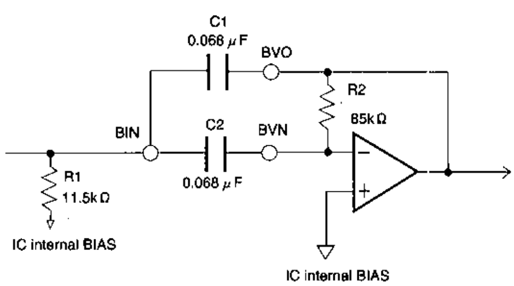


- The input impedance is 47kΩ.
- A buffer if R and C_1 are not present.
- The gain can be set by R and the 20kΩ.

G_{VC} = (R + 20kΩ)/R

Note: Set C_2 (input coupling) and C_1 (used to set the gain) depending on the frequency band used.

3. Bass filter



- The BPF is composed of a multifeedback active filter.

f_0 can be varied according to the value of C.
(theoretical equation)

$$f_0 = \frac{1}{2\pi} \times \left(\frac{1}{R_1 R_2 C_1 C_2} \right)^{\frac{1}{2}}$$

$$G = \frac{R_2}{5k\Omega} \times \left(1 + \frac{C_1}{C_2} \right)^{-1}$$

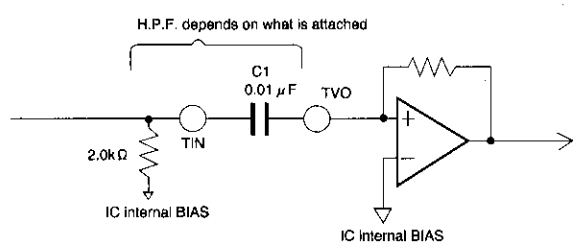
(When R_1 = 11.5kΩ, R_2 = 85kΩ, $C_1 = C_2 = C$)

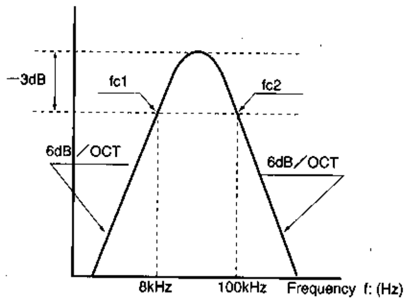
$$f_0 = \frac{5.1 \times 10^{-6}}{C} \quad Q \fallingdotseq 1.36 \quad G = 8.5$$

$$Q \fallingdotseq \left[\left(\frac{R_1}{R_2 C_1 C_2} \right)^{\frac{1}{2}} \times (C_1 + C_2) \right]^{-1}$$

Note: Filter gain is calculated using the equation above. Total output gain is the sum of the gain for each of the internal circuits.

4. Treble filter





- Cutoff frequency (f_{c1}) for the bypass filter can be changed using the attached C_1.

$$f_{c1} = \frac{1}{2\pi \times C_1 \times 2k\Omega}$$

The f_{c1} for the recommended constant is approximately 8kHz.

- f_{c2} is determined by the band of the built-in amp. f_{c2} is approximately 100kHz.

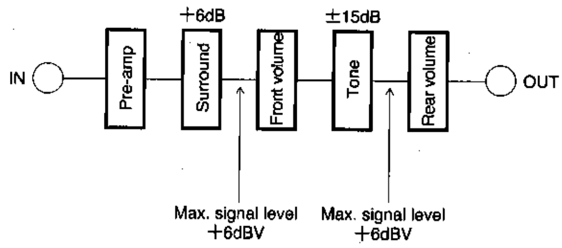
The tone control is designed for a fluctuation of ±15dB (Typ.) when the frequency that you want to boost or cut is a peak or valley of the frequency characteristics for the filter. So be sure to design the filter while taking into consideration its frequency characteristics.

5. Tone boost

When volume attenuation increases, tone control width will change. Reference values are listed below, but be aware that actual values vary for different products.
(Reference values)
At attenuation of 0dB, tone control width is ±15.0dB.
At attenuation of −40dB, tone control width is ±13.5dB.

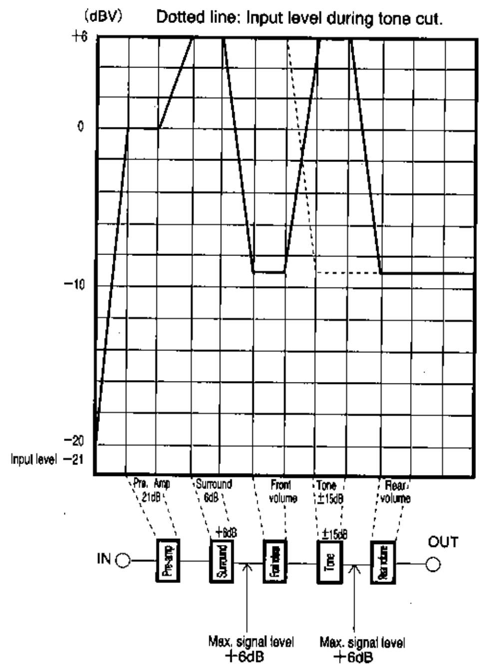
6. Signal level setting

The following figure represents the standard setting for the BH3854A.



As indicated above, if the front volume and rear volume input level are set so as not to exceed +6dBV (2 Vrms), the pre-amp gain setting can be used to improve the S/N ratio.

The figure on the left is a level diagram.
Solid line: Input level during tone boost.
Dotted line: Input level during tone cut.

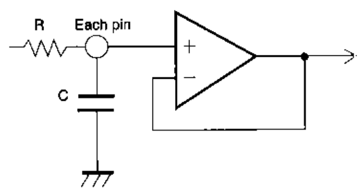


7. Serial control

High-frequency digital signals are input into the CK, DATA, and LATCH pins. Configure the wiring for these pins in such a manner that it does not create interference for lines carrying analog signals. When measuring for step switching noise caused by interference, connect in serial format resistance of approximately 2 kΩ right next to the microcomputer output pin (CK, DATA, LATCH) for each line.

8. Step switching noise

In the circuit of the sample application, a constant is given, as an example, to each of the VC (pin 23), TC (pin 22), BC (pin 21), and SC (pin 11) pins. These constants vary depending upon signal level settings, wiring patterns in the device to which they are mounted, etc. Consider each constant carefully. The following diagram depicts an internal equivalent circuit. (It is equipped with a primary integration circuit so that changes will occur slowly.)



	R value (kΩ)
VC, BC, TC	10
SC	200

9. Setting the volume and tone levels

These specifications include, as reference values, figures for attenuation or gain for control serial data. The internal D/A converter features an R-2R structure, thus when there is no change between consecutive data, data exists. This can be used when very fine settings must be made, provided that volume is 8 bits (256 steps) or fewer, and tone is 5 bits (32 steps) or fewer.

10. D/A separation

With this IC (BH3854), the analog and digital systems are completely separated in the power supply and GND. Within the digital system, there is a stable built-in standard voltage supply, all of which is supplied via the VREF (pin 17, 3.8V), so this IC can be used without any worry about timing being off or digital noise interference occurring.

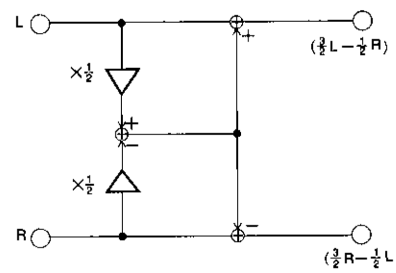
11. Output pins

PORT 1 through 4 (pins 12 through 15) are reset when the power is turned ON, and remain reset until the next serial data is input.

Note: From the time the power is turned ON until the next data is input, data in the CK, DATA, and LATCH lines are all maintained at LOW.

- Be sure that no more than 9V is applied to any of the output pins.

12. Matrix surround



◎The structure of the matrix surround is as shown in the figure above. Use the equations shown in the figure to calculate gain.

In-phase gain	0dB
Negative-phase gain	3.5dB

(Negative-phase gain only occurs when input is carried out on single Ch.)

13. DC control

There is internal impedance of 10kΩ at the VC (pin 23), TC (pin 22), and BC (pin 21) pins, and internal impedance of 200kΩ at the SC pin (pin 11). For this reason, it is recommended that DC control of these pins be performed by voltage delivered directly from the voltage source. When using variable volume, take the impedance into account in determining the settings.

Note: The voltage range for DC control is 0V to 3.8V. Be sure not to apply greater than 3.8V to any pin.

14. GND

- Connect the GND of the attached element, which is shown in the circuit of the sample application, to the analog GND.
- Connect the GND of the capacitor that is connected to pin 17 to the digital GND.
- If several capacitors with good high-frequency characteristics are connected in parallel to the 17th-pin capacitor, the characteristics will be improved with respect to static electricity noise. (Recommended : ceramic capacitors of 0.001 μF to 0.1 μF) If the wiring to the analog GND and digital GND is long, make sure that no potential difference arises between the two GNDs.

15. BH3854S → BH3854AS : Differences

- The bass filter R_2 constant changes from 100 kΩ → 85 kΩ. Accordingly, bass filter f_0 changes from 70Hz → 75Hz, which means bass filter Q changes from 1.47 → 1.36.
- The resistance at the treble filter's TIN pin changes from 20 kΩ → 2 kΩ. Accordingly, the value for the attached capacitor changes from 470pF → 0.01 μF, which means that cutoff frequency (f_{C1}) changes from 17kHz → 8kHz.

● Electrical characteristic curves

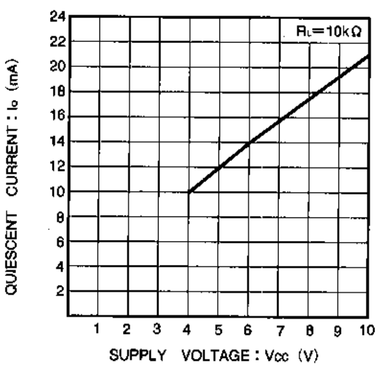


Fig. 3 Quiescent curve/Supply voltage characteristics

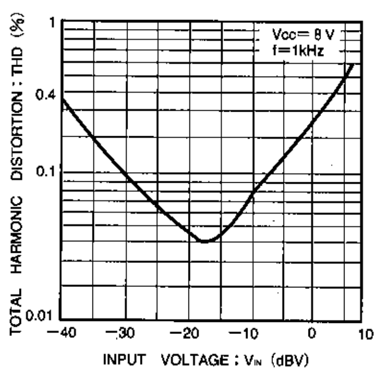


Fig. 4 Harmonic distortion/Input voltage characteristics

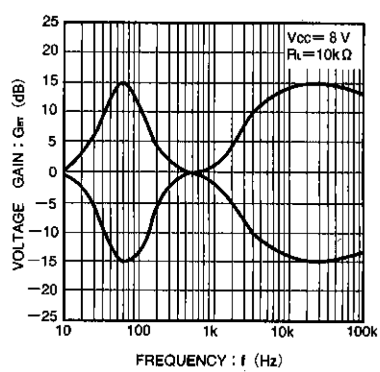
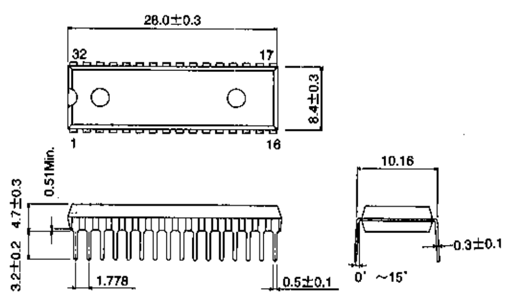
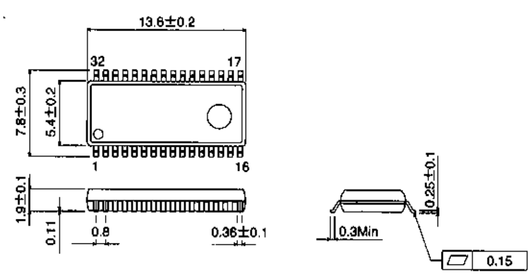


Fig. 5 Output gain/Frequency

● External dimensions (Unit: mm)



SDIP32



SSOP-A32

Sound control

Audio accessory components

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Serial sound control IC

BH3854AS / BH3854AFS

The BH3854AS and BH3854AFS are signal processing ICs designed for volume and tone control in CD radio cassettes and other audio products. Their three-line serial control enables them to control volume and tone on the basis of signals from a microcomputer, etc.

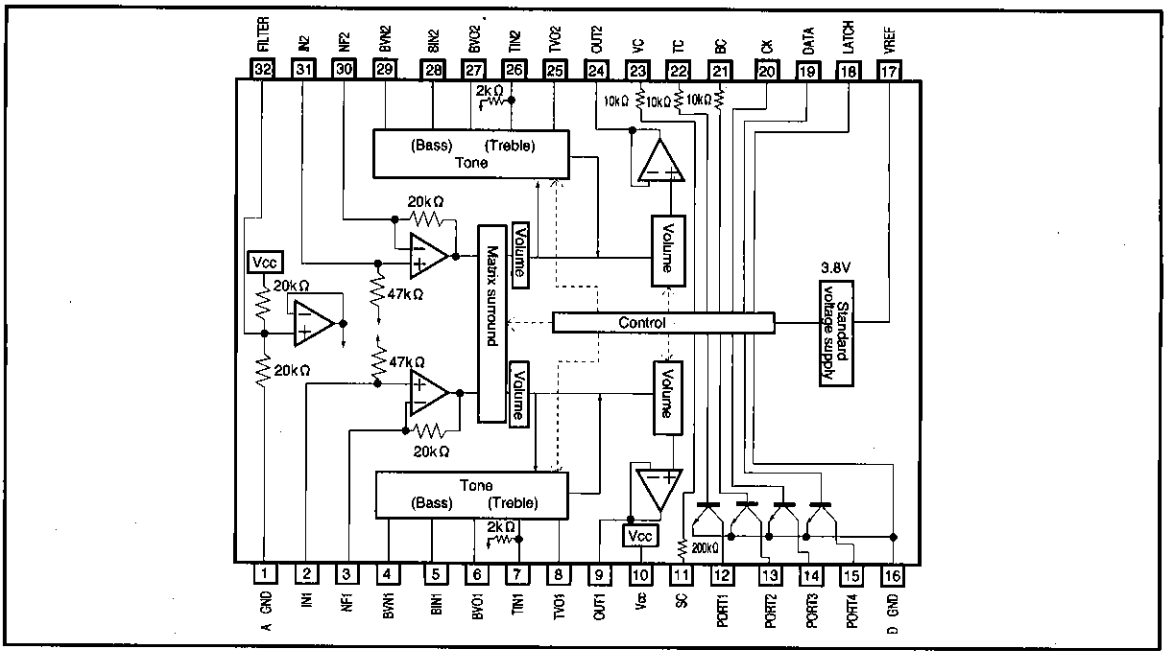
●Applications

CD radio cassettes, mini component stereo systems, car stereos

●Features

1) They facilitate direct serial control from a microcomputer of volume (main volume) and tone (bass, treble). DC control is also possible.
2) Volume is produced by a low-distortion, low-noise VCA. Designed to minimize step noise.
3) Input amp can be used for gain adjustment, and matrix surround yields powerful sound.
4) Stable standard voltage supply and built-in I / O buffer mean that few attachments are needed. SSOP32 package designed to save space.
5) Open collector has four outputs, which makes logic control possible.
6) Excellent for volume and tone control devices in CD radio cassettes, micro components, car stereos, televisions, etc.
7) Digital GND pin and analog GND pin are separated with an impedence of more than 1MΩ.

●Block diagram



* Supply of DC voltage from the VC (volume), BC (bass), TC (treble), and SC (surround) pinns facilitates external control of volume, bass, treble, and surround.
* Impedance at the VC, TC, and BC pins is 10 kΩ (Typ.).
* Impedance at the SC pin is 200 kΩ (Typ.).

●Absolute maximum ratings (Ta = 25℃)

Parameter	Symbol		Limits	Unit
Supply voltage	V_{CC}		8	V
Power dissipation	Pd	BH3854AS	1250*1	mW
		BH3854AFS	1000*2	
Operating temperature	Topr		−40~85	℃
Storage temperature	Tstg	BH3854AS	−55~125	℃
		BH3854AFS	−55~150	

*1 When used with a Ta greater than 25℃, reduce the power dissipation by 12.5 mW for every 1℃ over 25℃.
*2 When used with a Ta greater than 25℃, reduce the power dissipation by 8 mW for every 1℃ over 25℃.

●Recommended operating conditions (Ta = 25℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{CC}	5.4	8.0	9.5	V

●Pin description

Pin No.	Pin Name	Function
1	A GND	Analog system ground
2	IN1	Pin for ch 1 volume input
3	NF1	Pin for adjustment of input amp gain
4	BVN1	Pin for connection to ch 1 low-band filter
5	BIN1	Pin for connection to ch 1 low-band filter
6	BVO1	Pin for connection to ch 1 low-band filter
7	TIN1	Pin for connection to ch 1 high-band filter
8	TVO1	Pin for connection to ch 1 high-band filter
9	OUT1	Pin for ch 1 volume output
10	V_{CC}	Power supply pin
11	SC	Time constant pin for prevention of switching shock
12	PORT1	Output pin
13	PORT2	Output pin
14	PORT3	Output pin
15	PORT4	Output pin
16	D GND	Digital system ground
17	VREF	3.8V standard voltage output pin
18	LATCH	Pin for receiving LATCH data
19	DATA	Pin for receiving DATA
20	CK	Pin for receiving CLOCK data
21	BC	Time constant port for prevention of switching shock
22	TC	Time constant port for prevention of switching shock
23	VC	Time constant port for prevention of switching shock
24	OUT2	Pin for ch 2 volume output
25	TVO2	Pin for connection to ch 2 high-band filter
26	TIN2	Pin for connection to ch 2 high-band filter
27	BVO2	Pin for connection to ch 2 low-band filter
28	BIN2	Pin for connection to ch 2 low-band filter
29	BVN2	Pin for connection to ch 2 low-band filter
30	NF2	Pin for adjustment of input AMP gain
31	IN2	Pin for ch 2 volume input
32	FILTER	Filter pin

●Electrical characteristics (Unless otherwise specified, Ta = 25℃, V_{CC} = 8V, f = 1kHz, BW = 20 ~ 20kHz, VOL = Max, TONE = ALL FLAT, Rg = 600Ω, RL = 10kΩ, INPUT AMP GAIN = 0dB)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Quiescent current	I_Q	8	17	25	mA	No signal
Max. input	Vim	1.8	2.0	−	Vrms	THD=1%, VOL=−20dB(ATT)
Max. output	Vom	1.8	2.0	−	Vrms	THD=1%
Voltage gain	G_V	−3.0	−1.0	1.0	dB	Vin=1Vrms
Max. attenuation	ATT	90	110	−	dB	V_O =1Vrms
Cross talk	V_{CT}	64	70	−	dB	V_O=1Vrms, BPF=400Hz~30kHz
Low-band control width	VBmax	12	15	18	dB	75Hz, Vin=100mVrms
	VBmin	−18	−15	−12	dB	75Hz, Vin=100mVrms
High-band control width	VTmax	12	15	18	dB	10kHz, Vin=100mVrms
	VTmin	−18	−15	−12	dB	10kHz, Vin=100mVrms
Mute attenuation	V_{MT}	90	110	−	dB	V_O=1Vrms *
Harmonic distortion	THD	−	0.03	0.1	%	V_O=0.3Vrms, BPF=400Hz~30kHz
Output noise voltage	$V_{NO}1$	−	25	34	μVrms	No signal, VOL=MAX, Rg=0 *
Output noise voltage during full boost	$V_{NO}2$	−	80	120	μVrms	No signal, TONE=ALL MAX, VOL=MAX, Rg=0 *
Residual output noise voltage	VM_{NO}	−	2	10	μVrms	No signal, VOL=−∞, Rg=0 *
Standard power supply output voltage	V_{REF}	3.5	3.8	4.1	V	I_{REF}=3mA
Standard power supply output current power	I_{REF}	3.0	10	−	mA	V_{REF}>3.7V
Channel balance	G_{CB}	−2.0	0	2.0	dB	CH1 taken as the standard for measurements.
Port output current	I_{PMAX}	5.0	−	−	mA	
L output voltage	V_{OL}	−	0.4	0.5	V	I_{OL}=5mA
H output disable current	I_{OZH}	−	−	1.0	μA	V_O=5V
Volume attenuation (-10 dB)	ATT10	−12.0	−10.0	−8.0	dB	VIN = 0 dBV is the gain when the control data (10101010) is entered.

∗Items marked with an asterisk (∗) were measured with the VP-9690A (displays mean detection and effective value), produced by Matsushita Communication Industrial.
◎Not designed for radiation resistence.

●Timing chart constants

Parmater	Symbol	Min.	Typ.	Max.	Unit
H input voltage	V_{IH}	4.0	5.0	6.0	V
L input voltage	V_{IL}	−	0	1.0	V
Min. clock width	tw	2.0	−	−	μS
Min. data width	tw (DATA)	2.0	−	−	μS
Min. latch width	tw (LATCH)	2.0	−	−	μS
Setup time (DATA→CLK)	tsu	1.0	−	−	μS
Hold time (CLK→DATA)	th	1.0	−	−	μS
Setup time (CLK→LATCH)	ts	1.0	−	−	μS

Note: About the output pins...
- Pins 1 through 4 (pins 12 through 15) are reset when the power is turned ON.
- After the pins are reset, until the Vcc voltage setting for this IC (BH3854) is reached and the next data is input, the pins only operate while the CK, DATA, and LATCH lines are all maintained at LOW.
- Be sure that no more than 9V is applied to any of the output pins.

●Measurement circuit

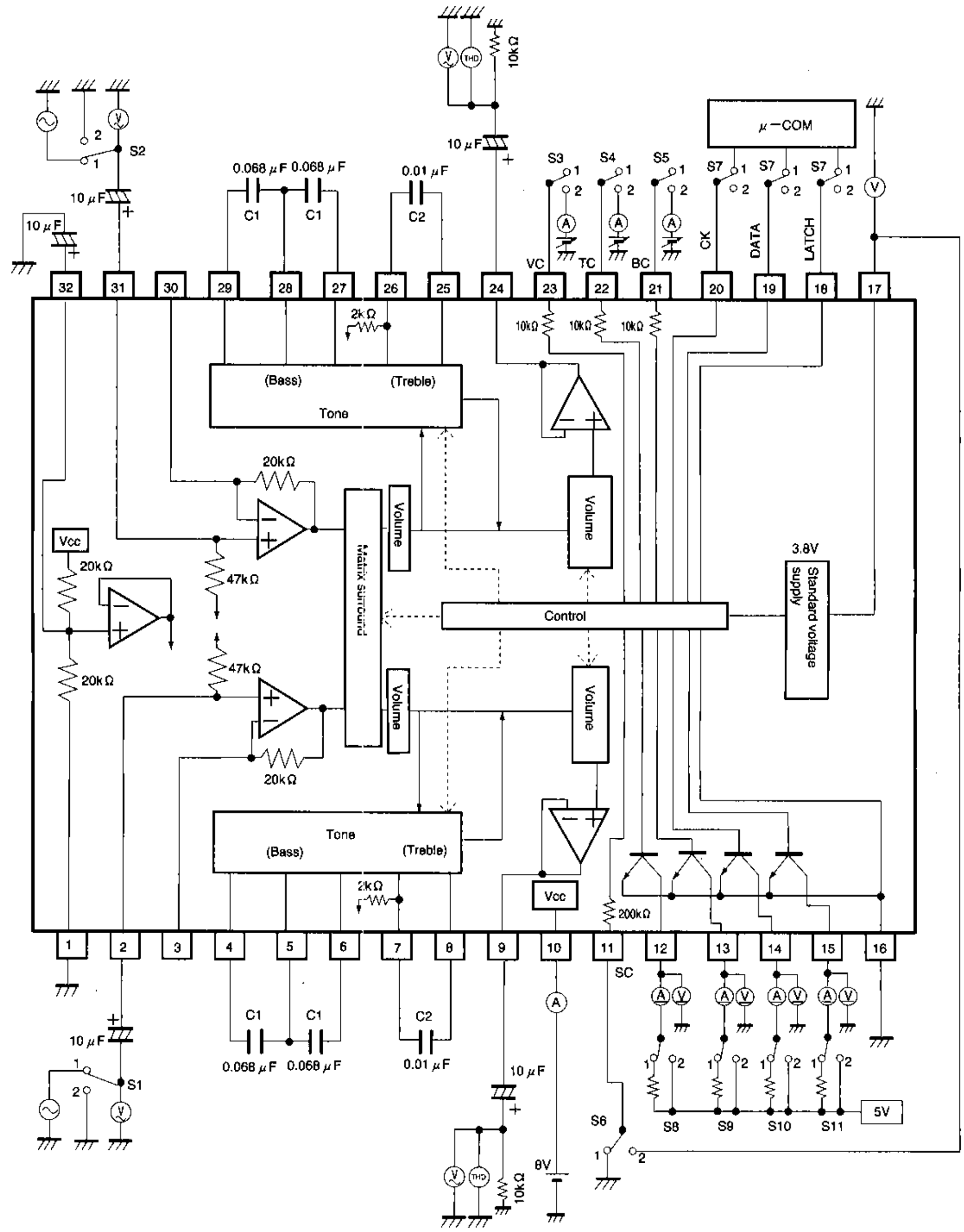


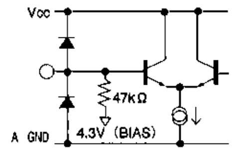
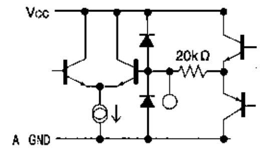
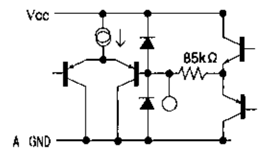
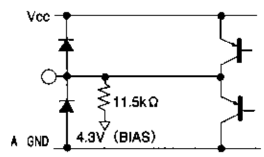
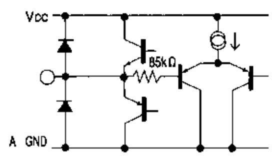
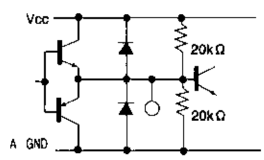
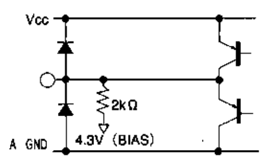
Fig. 1

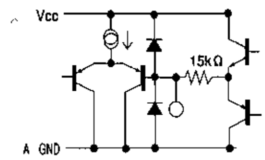
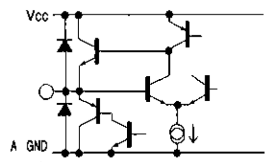
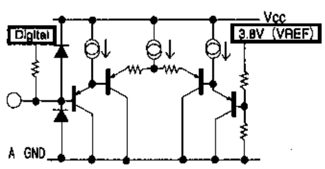
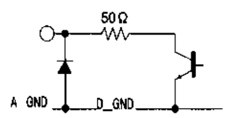
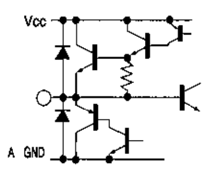
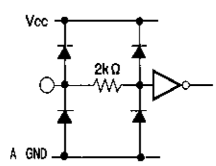
●Operation of measuring circuit switches

Parameter		S1	S2	S3	S4	S5	S6	S7	S8	S9	S10	S11
Quiescent current		2	2	2A	2B	2B	2	2	1	1	1	1
Max. input		↓	↓	2B	↓	↓	↓	↓	↓	↓	↓	↓
Max. output		↓	↓	2A	↓	↓	↓	↓	↓	↓	↓	↓
Voltage gain		↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
Max. attenuation		↓	↓	A→C	↓	↓	↓	↓	↓	↓	↓	↓
Cross talk		1.2	2.1	2A	↓	↓	↓	↓	↓	↓	↓	↓
Low-band control width	Boost	1	1	↓	↓	2A	↓	↓	↓	↓	↓	↓
	Cut	↓	↓	↓	↓	2C	↓	↓	↓	↓	↓	↓
High-band control width	Boost	↓	↓	↓	2A	2B	↓	↓	↓	↓	↓	↓
	Cut	↓	↓	↓	2C	↓	↓	↓	↓	↓	↓	↓
Mute attenuation		↓	↓	A→C	2B	↓	↓	↓	↓	↓	↓	↓
Harmonic distortion		↓	↓	2A	↓	↓	↓	↓	↓	↓	↓	↓
Output noise voltage		2	2	↓	↓	↓	↓	↓	↓	↓	↓	↓
Output noise voltage during full boost		↓	↓	↓	2A	2A	↓	↓	↓	↓	↓	↓
Residual output noise voltage		↓	↓	2C	2B	2B	↓	↓	↓	↓	↓	↓
Standard power supply output voltage		↓	↓	2A	↓	↓	↓	↓	↓	↓	↓	↓
Standard power supply output current power		↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
Channel balance		1	1	↓	↓	↓	↓	↓	↓	↓	↓	↓
Port output current		2	2	↓	↓	↓	↓	1	↓	↓	↓	↓
L output voltage		↓	↓	↓	↓	↓	↓	↓	↓	↓	↓	↓
H output disable current		↓	↓	↓	↓	↓	↓	↓	2	2	2	2

*A, B, and C in the table represent the level of the variable voltage supply.
A = 3.8V
B = 1.9V
C = 0V

●Pin description

Symbol	Pin No	Pin voltage	Equivalent circuit	Description
IN1 IN2	2pin 31pin	4.3V 4.3V		Main volume input pin. Designed for input impedance of 47 kΩ (Typ).
NF1 NF2	3pin 30pin	4.3V 4.3V		Pin for adjustment of input amp gain. Approximately + 6 dB with connection of 20 kΩ resistance.
BVN1 BVN2	4pin 29pin	4.3V 4.3V		Pin for low band filter connection.
BIN1 BIN2	5pin 28pin	4.3V 4.3V		Pin for low band filter connection.
BV01 BV02	6pin 27pin	4.3V 4.3V		Pin for low band filter connection.
FILTER	32pin	4.0V		Filter input pin. Filter input pin designed to operate at approximately 1/2 Vcc. Please install a capacitor of about 10 μF to the filter pin. Has built-in precharge and discharge circuits.
TIN1 TIN2	7pin 26pin	4.3V 4.3V		Pin for high band filter connection.

Symbol	Pin No	Pin voltage	Equivalent circuit	Description
TV01 TV02	8pin 25pin	4.3V 4.3V		Pin for high band filter connection.
OUT1 OUT2	9pin 24pin	4.0V 4.0V		Main volume output pin. OUT1 is the volume output for CH1. OUT2 is the volume output for CH2.
SC BC TC VC	11pin 21pin 22pin 23pin			Time constant pin for prevention of switching shock noise SC : Surround pin BC : Bass pin TC : Treble pin VC : Volume pin
PORT1 PORT2 PORT3 PORT4	12pin 13pin 14pin 15pin			Output pin. Open collector output. Can pull a maximum of 5 mA.
V_{REF}	17pin	3.8V		3.8V regulator output pin. Output requires capacitor for stopping oscillation. Output pin has built-in precharge and discharge circuits, so there is no problem with start-up or shut-down even with a large capacitor.
LATCH DATA CK	18pin 19pin 20pin			Pin for receiving data from μcom. LATCH : latch line DATA : data line CK : clock line
VCC	10pin	8V	Power supply voltage pin.	
A_GND	1pin	0V	Analog GND pin. Connected to IC board.	
D_GND	16pin	0V	Digital GND pin. Separate from Analog GND pin.	

Note: All figures for pin voltage assume a power supply voltage (VCC) of 8V.

Audio accessory components

Sound control

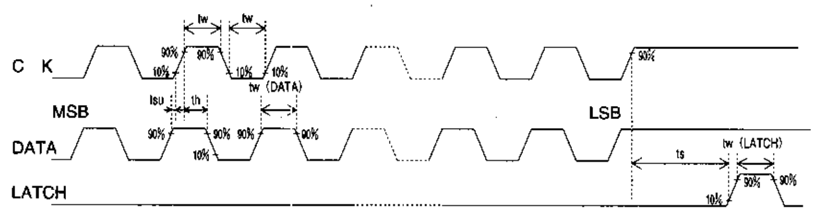
●Digital control specifications

●Data format : total of 23 bits

MSB LSB

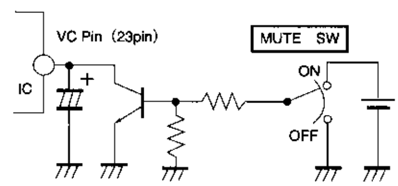
Volume	Treble	Bass	Surround	PORT1	PORT2	PORT3	PORT4
8bit	5bit	5bit	1bit	1bit	1bit	1bit	1bit

●Timing (recommended conditions)



★For timing chart constants, see the electrical characteristics.

- Surround is ON when the bit data is 0, and OFF when the bit data is 1.
- Pins 1 through 4 are set so that the output transistors will turn OFF if data is not input when the power is turned ON. They turn ON when the bit data is 1, and OFF when the bit data is 0.
- "H" level is 4V or greater. "L" level is 1V or less.
- Make the end of each control command LOW.



- The MUTE function can be controlled externally if the VC (volume control) pin is configured as shown in the diagram above. Attenuation is equal to the figure for attenuation when volume is at MIN.

●Volume data settings (reference values)

HEX Notation	Volume Gain	V_8 (MSB)	V_7	V_6	V_5	V_4	V_3	V_2	V_1 (LSB)
FF	0dB	1	1	1	1	1	1	1	1
E5	−1dB	1	1	1	0	0	1	0	1
DB	−2dB	1	1	0	1	1	0	1	1
D3	−3dB	1	1	0	1	0	0	1	1
CC	−4dB	1	1	0	0	1	1	0	0
C6	−5dB	1	1	0	0	0	1	1	0
C0	−6dB	1	1	0	0	0	0	0	0
BA	−7dB	1	0	1	1	1	0	1	0
B5	−8dB	1	0	1	1	0	1	0	1
B0	−9dB	1	0	1	1	0	0	0	0
AB	−10dB	1	0	1	0	1	0	1	1
A7	−11dB	1	0	1	0	0	1	1	1
A3	−12dB	1	0	1	0	0	0	1	1
9F	−13dB	1	0	0	1	1	1	1	1
9C	−14dB	1	0	0	1	1	1	0	0
98	−15dB	1	0	0	1	1	0	0	0
95	−16dB	1	0	0	1	0	1	0	1
91	−17dB	1	0	0	1	0	0	0	1
8E	−18dB	1	0	0	0	1	1	1	0
8A	−19dB	1	0	0	0	1	0	1	0

HEX Notation	Volume gain	V_8 (MSB)	V_7	V_6	V_5	V_4	V_3	V_2	V_1 (LSB)
87	−20dB	1	0	0	0	0	1	1	1
81	−22dB	1	0	0	0	0	0	0	1
7B	−24dB	0	1	1	1	1	0	1	1
75	−26dB	0	1	1	1	0	1	0	1
70	−28dB	0	1	1	1	0	0	0	0
6B	−30dB	0	1	1	0	1	0	1	1
66	−32dB	0	1	1	0	0	1	1	0
62	−34dB	0	1	1	0	0	0	1	0
5D	−36dB	0	1	0	1	1	1	0	1
59	−38dB	0	1	0	1	1	0	0	1
55	−40dB	0	1	0	1	0	1	0	1
51	−42dB	0	1	0	1	0	0	0	1
4D	−44dB	0	1	0	0	1	1	0	1
4A	−46dB	0	1	0	0	1	0	1	0
47	−48dB	0	1	0	0	0	1	1	1
43	−50dB	0	1	0	0	0	0	1	1
40	−52dB	0	1	0	0	0	0	0	0
3D	−54dB	0	0	1	1	1	1	0	1
3A	−56dB	0	0	1	1	1	0	1	0
37	−58dB	0	0	1	1	0	1	1	1
34	−60dB	0	0	1	1	0	1	0	0
32	−62dB	0	0	1	1	0	0	1	0
2F	−64dB	0	0	1	0	1	1	1	1
2D	−66dB	0	0	1	0	1	1	0	1
2B	−68dB	0	0	1	0	1	0	1	1
28	−70dB	0	0	1	0	1	0	0	0
26	−72dB	0	0	1	0	0	1	1	0
24	−74dB	0	0	1	0	0	1	0	0
23	−76dB	0	0	1	0	0	0	1	1
21	−78dB	0	0	1	0	0	0	0	1
1F	−80dB	0	0	0	1	1	1	1	1
1E	−82dB	0	0	0	1	1	1	1	0
1C	−84dB	0	0	0	1	1	1	0	0
00	−∞	0	0	0	0	0	0	0	0

Note: All figures in this table are reference values. When using this IC, check this table carefully and perform the appropriate setting.

● Treble settings (reference values)

Treble data

Settings MSB				LSB	Treble gain (dB)	HEX Notation
0	0	0	0	0	−15	00
0	0	1	0	0	−14	04
0	0	1	1	0	−12	06
0	1	0	0	0	−10	08
0	1	0	0	1	−8	09
0	1	0	1	0	−6	0A
0	1	0	1	1	−4	0B
0	1	1	0	0	−2	0C
0	1	1	1	1	±0	0F
1	0	1	0	0	+2	14
1	0	1	0	1	+4	15
1	0	1	1	0	+6	16
1	0	1	1	1	+8	17
1	1	0	0	0	+10	18
1	1	0	1	0	+12	1A
1	1	1	0	0	+14	1C
1	1	1	1	1	+15	1F

Bass data

Settings MSB				LSB	Bass Gain (dB)	HEX Notation
0	0	0	0	0	−15	00
0	0	1	0	1	−14	05
0	0	1	1	1	−12	07
0	1	0	0	1	−10	09
0	1	0	1	0	−8	0A
0	1	0	1	1	−6	0B
0	1	1	0	0	−4	0C
0	1	1	0	1	−2	0D
0	1	1	1	1	±0	0F
1	0	0	1	1	+2	13
1	0	1	0	0	+4	14
1	0	1	0	1	+6	15
1	0	1	1	0	+8	16
1	0	1	1	1	+10	17
1	1	0	0	1	+12	19
1	1	0	1	1	+14	1B
1	1	1	1	1	+15	1F

Notes:1. The gain values in the treble and bass data setting tables above are based on the assumption that the filter constants have been set so that maximum and minimum gain are equal to the peak and bottom values listed in the frequency characteristics drawings.

2. All figures in this table are reference values. When using this IC, check this table carefully and perform the appropriate setting.

●Application example

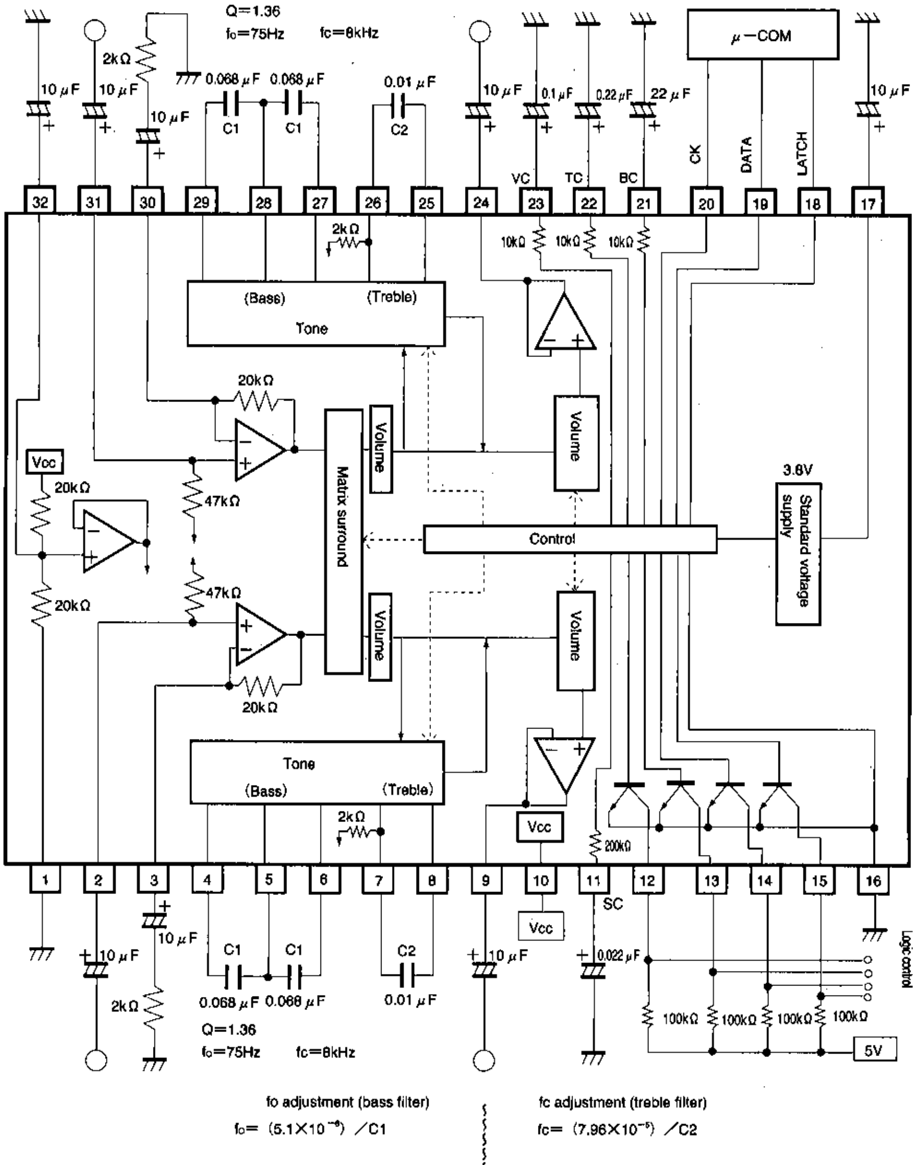
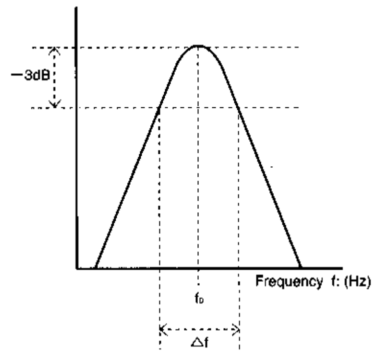


Fig. 2

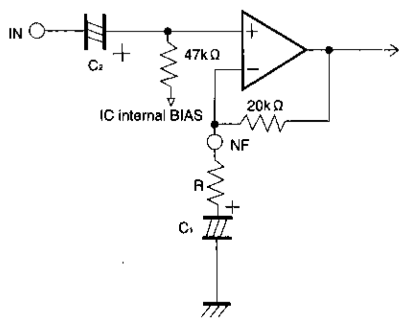
●Operation notes

1. Operating power supply voltage range

As long as the operating power supply voltage and ambient temperature are kept within the specified range, the basic circuits are guaranteed to function, but be sure to check the constants as well as the element settings, voltage settings, and temperature settings. Also, please take into consideration internal IC resistance dispersion (approx. ±20%) and temperature fluctuation when making settings for IC internal resistance, attachment resistance, capacitor gain, or frequency.



2. Primary amp

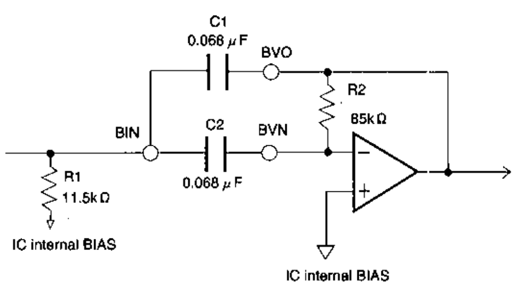


• The input impedance is 47kΩ.
• A buffer if R and C_1 are not present.
• The gain can be set by R and the 20kΩ.

G_{VC} = (R + 20kΩ)/R

Note: Set C_2 (input coupling) and C_1 (used to set the gain) depending on the frequency band used.

3. Bass filter



• The BPF is composed of a multifeedback active filter.

f_0 can be varied according to the value of C.

(theoretical equation)

$$f_0=\frac{1}{2\pi}\times\left(\frac{1}{R_1R_2C_1C_2}\right)^{\frac{1}{2}}$$

$$G=\frac{R_2}{5k\Omega}\times\left(1+\frac{C_1}{C_2}\right)^{-1}$$

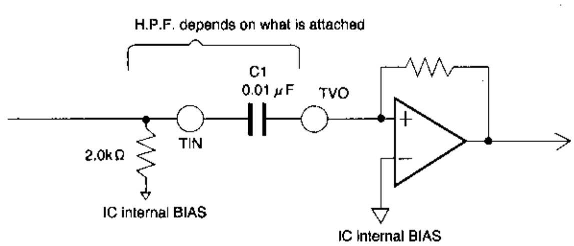
(When R_1 = 11.5kΩ, R_2 = 85kΩ, C_1 = C_2 = C)

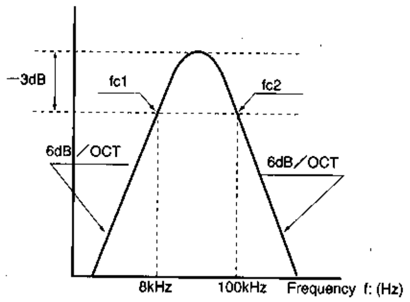
$$f_0=\frac{5.1\times10^{-6}}{C}\quad Q\fallingdotseq1.36\quad G=8.5$$

$$Q\fallingdotseq\left(\left(\frac{R_1}{R_2C_1C_2}\right)^{\frac{1}{2}}\times(C_1+C_2)\right)^{-1}$$

Note: Filter gain is calculated using the equation above. Total output gain is the sum of the gain for each of the internal circuits.

4. Treble filter





- Cutoff frequency (f_{c1}) for the bypass filter can be changed using the attached C_1.

$$f_{c1}=\frac{1}{2\pi \times C_1 \times 2k\Omega}$$

The f_{c1} for the recommended constant is approximately 8kHz.

- f_{c2} is determined by the band of the built-in amp. f_{c2} is approximately 100kHz.

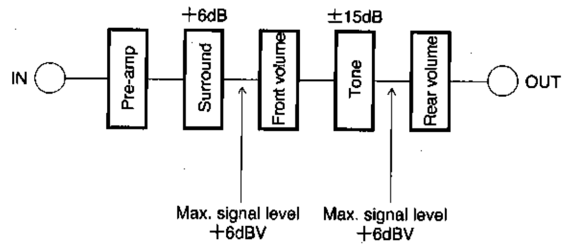
The tone control is designed for a fluctuation of ± 15dB (Typ.) when the frequency that you want to boost or cut is a peak or valley of the frequency characteristics for the filter. So be sure to design the filter while taking into consideration its frequency characteristics.

5. Tone boost

When volume attenuation increases, tone control width will change. Reference values are listed below, but be aware that actual values vary for different products.
(Reference values)
At attenuation of 0dB, tone control width is ±15.0dB.
At attenuation of −40dB, tone control width is ± 13.5dB.

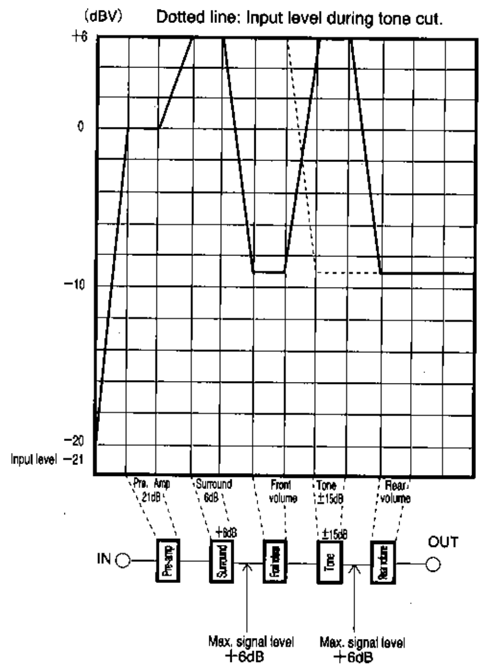
6. Signal level setting

The following figure represents the standard setting for the BH3854A.



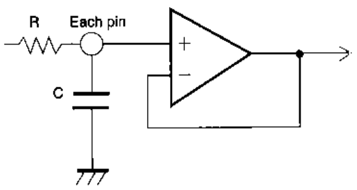
As indicated above, if the front volume and rear volume input level are set so as not to exceed +6dBV (2 Vrms), the pre-amp gain setting can be used to improve the S/N ratio.

The figure on the left is a level diagram.
Solid line: Input level during tone boost.
Dotted line: Input level during tone cut.



7. Serial control
High-frequency digital signals are input into the CK, DATA, and LATCH pins. Configure the wiring for these pins in such a manner that it does not create interference for lines carrying analog signals. When measuring for step switching noise caused by interference, connect in serial format resistance of approximately 2 kΩ right next to the microcomputer output pin (CK, DATA, LATCH) for each line.

8. Step switching noise
In the circuit of the sample application, a constant is given, as an example, to each of the VC (pin 23), TC (pin 22), BC (pin 21), and SC (pin 11) pins. These constants vary depending upon signal level settings, wiring patterns in the device to which they are mounted, etc. Consider each constant carefully. The following diagram depicts an internal equivalent circuit. (It is equipped with a primary integration circuit so that changes will occur slowly.)



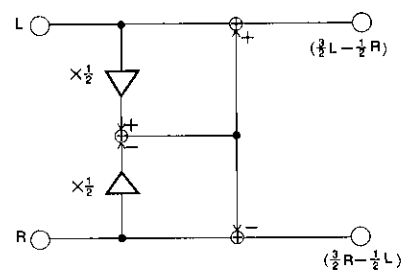
	R value (kΩ)
VC, BC, TC	10
SC	200

9. Setting the volume and tone levels
These specifications include, as reference values, figures for attenuation or gain for control serial data. The internal D/A converter features an R-2R structure, thus when there is no change between consecutive data, data exists. This can be used when very fine settings must be made, provided that volume is 8 bits (256 steps) or fewer, and tone is 5 bits (32 steps) or fewer.

10. D/A separation
With this IC (BH3854), the analog and digital systems are completely separated in the power supply and GND. Within the digital system, there is a stable built-in standard voltage supply, all of which is supplied via the VREF (pin 17, 3.8V), so this IC can be used without any worry about timing being off or digital noise interference occurring.

11. Output pins
PORT 1 through 4 (pins 12 through 15) are reset when the power is turned ON, and remain reset until the next serial data is input.
Note: From the time the power is turned ON until the next data is input, data in the CK, DATA, and LATCH lines are all maintained at LOW.
- Be sure that no more than 9V is applied to any of the output pins.

12. Matrix surround



◎The structure of the matrix surround is as shown in the figure above. Use the equations shown in the figure to calculate gain.

In-phase gain	0dB
Negative-phase gain	3.5dB

(Negative-phase gain only occurs when input is carried out on single Ch.)

13. DC control

There is internal impedance of 10kΩ at the VC (pin 23), TC (pin 22), and BC (pin 21) pins, and internal impedance of 200kΩ at the SC pin (pin 11). For this reason, it is recommended that DC control of these pins be performed by voltage delivered directly from the voltage source. When using variable volume, take the impedance into account in determining the settings.

Note: The voltage range for DC control is 0V to 3.8V. Be sure not to apply greater than 3.8V to any pin.

14. GND

- Connect the GND of the attached element, which is shown in the circuit of the sample application, to the analog GND.
- Connect the GND of the capacitor that is connected to pin 17 to the digital GND.
- If several capacitors with good high-frequency characteristics are connected in parallel to the 17th-pin capacitor, the characteristics will be improved with respect to static electricity noise. (Recommended : ceramic capacitors of 0.001 μF to 0.1 μF) If the wiring to the analog GND and digital GND is long, make sure that no potential difference arises between the two GNDs.

15. BH3854S → BH3854AS : Differences

- The bass filter R_2 constant changes from 100 kΩ → 85 kΩ. Accordingly, bass filter f_0 changes from 70Hz → 75Hz, which means bass filter Q changes from 1.47 → 1.36.
- The resistance at the treble filter's TIN pin changes from 20 kΩ → 2 kΩ. Accordingly, the value for the attached capacitor changes from 470pF → 0.01 μF, which means that cutoff frequency (f_{c1}) changes from 17kHz → 8kHz.

●Electrical characteristic curves

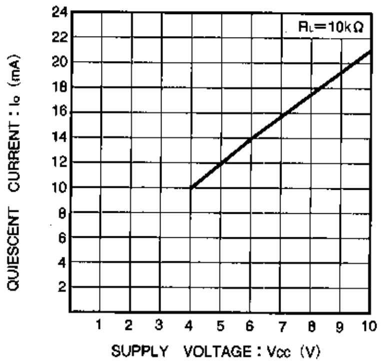


Fig. 3 Quiescent curve/Supply voltage characteristics

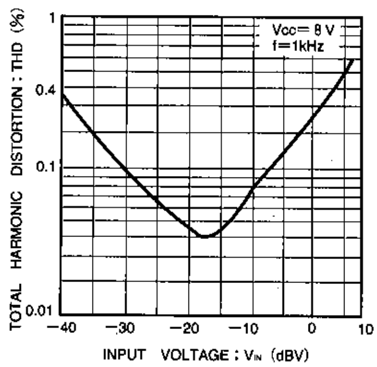


Fig. 4 Harmonic distortion/Input voltage characteristics

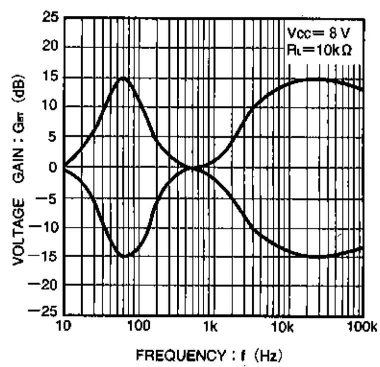
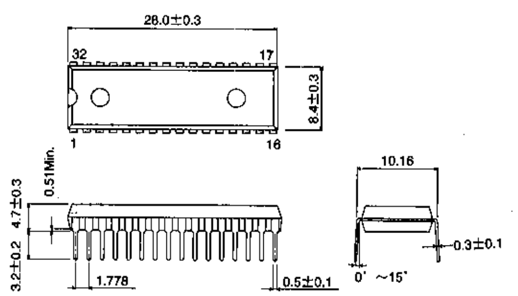


Fig. 5 Output gain/Frequency

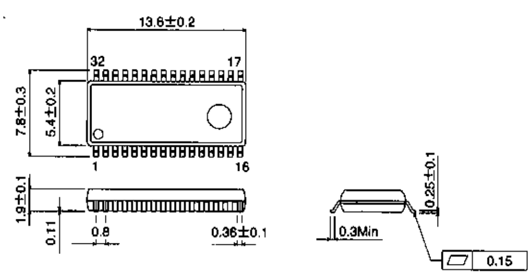
●External dimensions (Unit: mm)

BH3854AS



SDIP32

BH3854AFS



SSOP-A32

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2-wire serial sound control IC

BH3856S / BH3856FS

The BH3856S and BH3856FS are signal processing ICs designed for volume and tone control in televisions, mini component stereo systems, and other audio products. Their two-line serial control (I^2C-BUS) enables them to control volume and tone on the basis of signals from a microcomputer, etc.

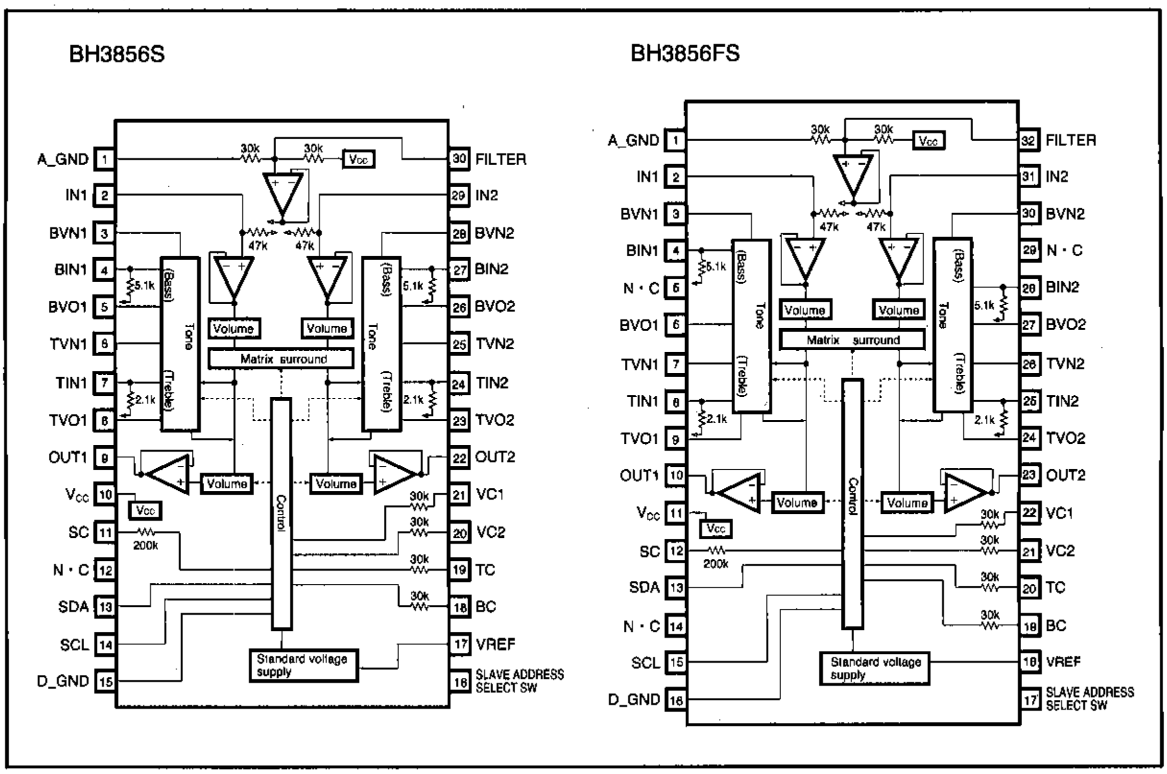
●Applications

Televisions, [VCRs] personal computer televisions, mini component stereo systems, car stereos

●Features

1) I^2C-BUS facilitates direct serial control from a microcomputer of volume (main volume), balance (left / right), and tone (bass, treble). DC control is also possible.
2) Volume is produced by a low-distortion, low-noise VCA. Designed to minimize step noise.
3) Stable standard voltage supply and built-in I / O buffer mean that few attachments are needed. SSOP32 package designed to save space.
4) Matrix surround yields powerful sound.

●Block diagram



●Absolute maximum ratings (Ta = 25℃)

Parameter		Symbol	Limits	Unit
Supply voltage		Vcc	10.0	V
Power dissipation	BH3856S	Pd	1200 *1	mW
	BH3856FS		850 *2	
Operating temperature		Topr	−40～+85	℃
Storage temperature		Tstg	−55～+150	℃

*1 Reduced by 12 mW for each increase in Ta of 1℃ over 25℃.
*2 Reduced by 6.8 mW for each increase in Ta of 1℃ over 25℃.

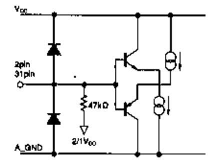
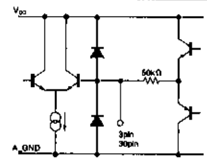
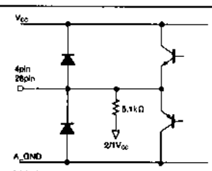
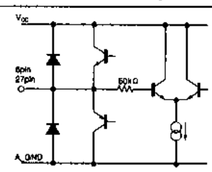
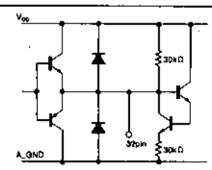
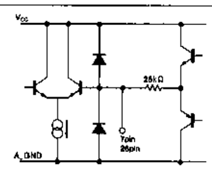
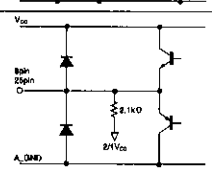
●Recommended operating conditions (Ta = 25℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	Vcc	6.0	9	9.5	V

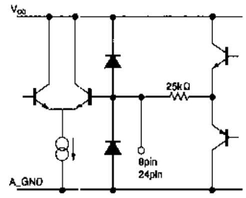
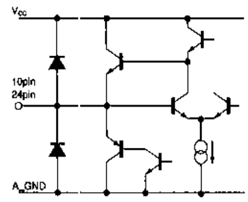
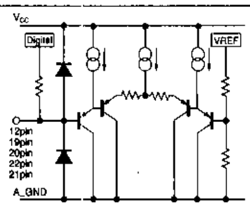
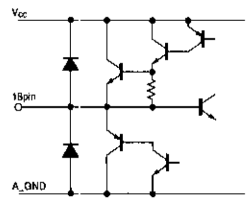
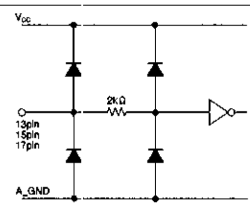
●Pin description

Pin No.		Symbol	Description
BH3856S	BH3856FS		
1	1	A_GND	Analog system ground
2	2	IN1	Pin for ch 1 volume input
3	3	BVN1	Pin for connection to ch 1 low-band filter
4	4	BIN1	Pin for connection to ch 1 low-band filter
5	6	BVO1	Pin for connection to ch 1 low-band filter
6	7	TVN1	Pin for connection to ch 1 high-band filter
7	8	TIN1	Pin for connection to ch 1 high-band filter
8	9	TVO1	Pin for connection to ch 1 high-band filter
9	10	OUT1	Pin for ch 1 volume output
10	11	Vcc	Power supply pin
11	12	SC	Time constant pin for prevention of switching shock
13	13	SDA	SDA data input pin
14	15	SCL	SCL data input pin
15	16	D_GND	Digital system ground
16	17	SASS	Slave address selection pin
17	18	VREF	Standard voltage output pin
18	19	BC	Time constant pin for prevention of switching shock
19	20	TC	Time constant pin for prevention of switching shock
20	21	VC2	Time constant pin for prevention of switching shock
21	22	VC1	Time constant pin for prevention of switching shock
22	23	OUT2	Pin for ch 2 volume output
23	24	TVO2	Pin for connection to ch 2 high-band filter
24	25	TIN2	Pin for connection to ch 2 high-band filter
25	26	TVN2	Pin for connection to ch 2 high-band filter
26	27	BVO2	Pin for connection to ch 2 low-band filter
27	29	BIN2	Pin for connection to ch 2 low-band filter
28	30	BVN2	Pin for connection to ch 2 low-band filter
29	31	IN2	Pin for ch 2 volume input
30	32	FILTER	Filter pin
12	5,14,28	NC	Not connected internally.

● Input / output circuit

Symbol	Pin Voltage	Equivalent circuit	Description
IN1 IN2	4.5V 4.5V		Main volume input pin. Designed for input impedance of 47 kΩ Typ).
BVN1 BVN2	4.5V 4.5V		Pin for low band filter connection.
BIN1 BIN2	4.5V 4.5V		Pin for low band filter connection.
BVO1 BVO1	4.5V 4.5V		Pin for low band filter connection.
FILTER	5.2V		Filter input pin. Please install a capacitor of about 10 μF to the filter pin. Has built-in precharge and discharge circuits.
TVN1 TVN2	4.5V 4.5V		Pin for high band filter connection.
TIN1 TIN2	4.5V 4.5V		Pin for high band filter connection.

※The pin numbers are for the BH3856S.

Symbol	Pin Voltage	Equivalent Circuit	Description
TVO1 TVO2	4.5V 4.5V		Pin for high band filter connection.
OUT1 OUT2	4.5V 4.5V		Main volume output pin. OUT1 is the volume output for CH1. OUT2 is the volume output for CH2.
SC BC TC VC1 VC2			For prevention of shock noise during step switching. SC: Surround pin BC: Bass pin TC: Treble pin VC1: Volume pin (CH1) VC2: Volume pin (CH2)
VREF	3.8V		3.8V regulator output pin. Output requires capacitor for stopping oscillation. Output pin has built-in precharge and discharge circuits, so there is no problem with start-up or shut-down even with a large capacitor. This pin is for connection to the high-band filter.
SDA SCL SASS			· I²C bass input pin SDA: serial data line SCL: serial clock line · Slave address selection pin SASS: slave address selection switch
VCC		Power supply voltage pin.	
A_GND		Analog GND pin. Connected to IC board.	
D_GND		Digital GND pin. Separate from Analog GND pin.	

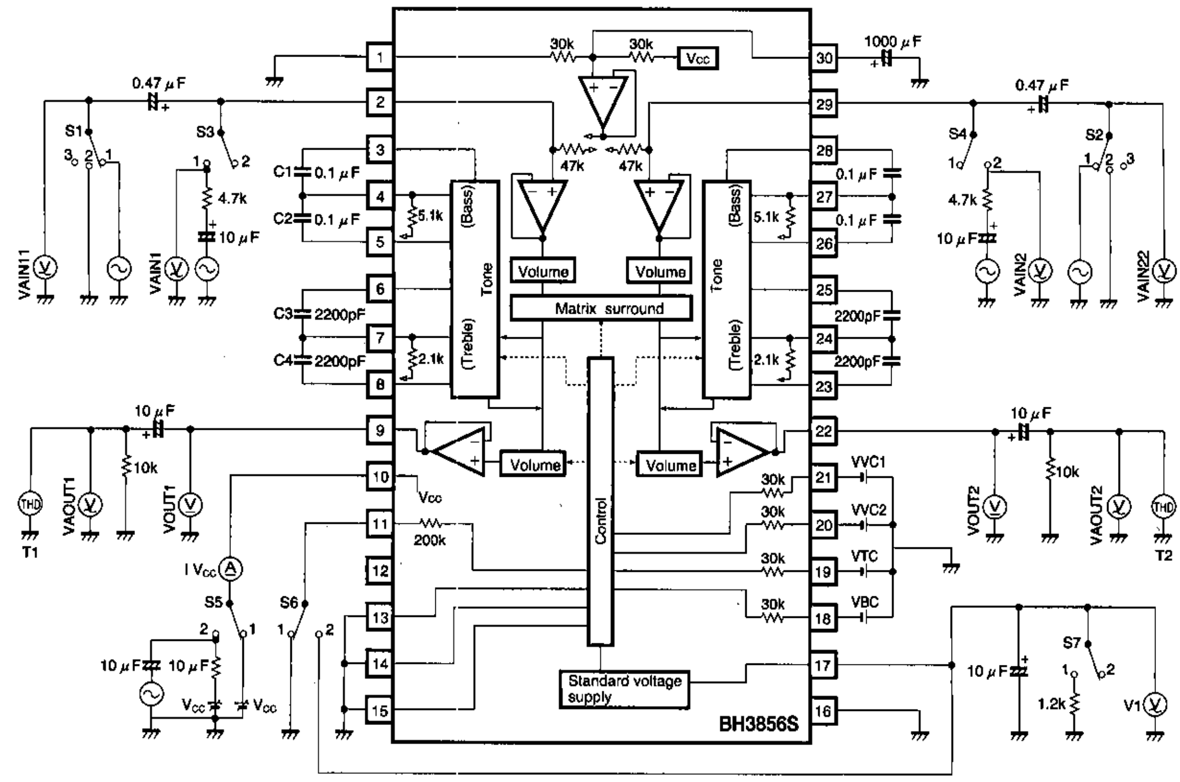
∗The pin numbers are for the BH3856S.

●Electrical characteristics (Unless otherwise specified, Ta = 25℃, V_{CC} = 9V, f = 1kHz, BW = 20 ~ 20kHz, VOL = Max., TONE = ALL FLAT, R_g = 600Ω, R_L = 10kΩ)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Quiescent current	I_Q	−	20	27	mA	No signal
Max. input	Vim	2.3	2.5	−	Vrms	THD=1%, VOL=−20dB (ATT)
Max. output	Vom	2.3	2.5	−	Vrms	THD=1%
Voltage gain	Gv	−1.5	0	+1.5	dB	Vin=1Vrms
Max. attenuation	ATT	90	110	−	dB	Vo=1Vrms
Cross talk	V_{CT}	70	80	−	dB	Vo=1Vrms
Low-band control width	VB Max.	+12	+15	+18	dB	100Hz, Vin=100mVrms
	VB Min.	−18	−15	−12	dB	100Hz, Vin=100mVrms
High-band control width	VT Max.	+12	+15	+18	dB	100kHz, Vin=100mVrms
	VT Min.	−18	−15	−12	dB	100kHz, Vin=100mVrms
Matrix surround single-channel gain	G_{SR}	4	6	8	dB	Vo=1Vrms *
Total Harmonic distortion	THD	−	0.01	0.1	%	Vo=0.5Vrms, BPF=400Hz~30kHz
Output noise voltage	$V_{NO}1$	−	45	65	μVrms	No signal, VOL=MAX, Rg=0 *
Residual output noise voltage	VM_{NO}	−	2	10	μVrms	No signal, VOL=−∞, Rg=0 *
Standard power supply output voltage	V_{REF}	3.5	3.8	4.1	V	I_{REF}=3mA
Standard power supply output current capability	I_{REF}	3.0	10	−	mA	V_{REF}>3.7V
Channel balance	G_{CB}	−1.5	0	+1.5	dB	CH1 taken as the standard for measurements.
Input impedance	R_{IN}	33	47	61	kΩ	f=1kHz
Output impedance	R_{OUT}	−	−	10	Ω	f=1kHz
Ripple rejection	RR	40	−	−	dB	f=100Hz, V_{RR}=1Vrms
Input voltage H	V_{IH}	4	−	−	V	SCL, SDA
Input voltage L	V_{IL}	−	−	1	V	SCL, SDA

Items marked with an asterisk (*) were measured with the VP-9690A (displays mean detection and effective value), produced by Matsushita Communication Industrial.
◎ Not designed for radiation resistance.
◎ Signal input occurs in equiphase.

● Measurement circuit



Unit : R [Ω]
C [F]

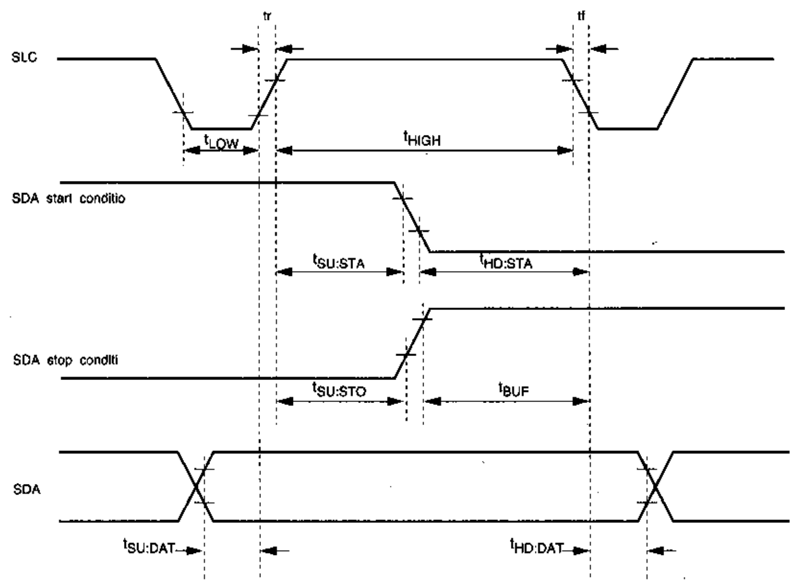
Fig. 1

Note: Diagram depicts the BH3856S.

●Performing data settings

(1) I²C BUS timing

Parameter	Symbol	Min.	Typ.	Max.	Unit
SCL clock frequency	f_{SCL}	0	—	100	kHz
SCL clock hold time, HIGH state	t_{HIGH}	4	—	—	μs
SCL clock hold time, LOW state	t_{LOW}	4.7	—	—	μs
SDA and SDL signal start-up time	tr	—	—	1	μs
SDA and SDL signal shut-down time	tf	—	—	0.3	μs
Set-up time for re-send [start] conditions	t_{SU};STA	4.7	—	—	μs
Hold time (re-send) [start] conditions (After hold time ends, initial clock pulse is generated.)	t_{HD};STA	4	—	—	μs
Set time for [stop] conditions.	t_{SU};STO	4.7	—	—	μs
Bus free time between [stop] condition and [start] condition	t_{BUF}	4.7	—	—	μs
Data set-up time	t_{SU};DAT	250	—	—	ns



t_{SU};STA=start code set-up time.
t_{HD};STA=start code hold time.
t_{SU};STO=stop code set-up time.
t_{BUF}=bus free time.
t_{SU};DAT=data set-up time.
t_{HD};DAT=data hold time.

I²C-BUS timing rules

(2) I²C BUS data format

S	Slave address	A	Select address	A	Data	A	P
	MSB … LSB		MSB … LSB		MSB LSB		
1bit	8bit	1bit	8bit	1bit	8bit	1bit	1bit

- S = start condition (start bit recognition)
- Slave address = IC recognition. Upper 7 bits are random. Bottom bit is "L" for the sake of overwrite.
- A = acknowledge bit (recognition of acknowledgment)
- Select address = selection between volume, bass, treble, and matrix surround
- Data = volume and tone data
- P = stop condition (stop bit recognition)

(3) BH3856S / BH3856FS slave addresses

MSB LSB

A6	A5	A4	A3	A2	A1	A0	R/W
1	0	0	0	0	0	A	0

- Slave address selection
  ①A = 1 (10000010) [SASS pin HI]
  ②A = 0 (10000000) [SASS pin LOW]

(4) Interface protocol

1) Basic protocol

S	Slave address	A	Select address	A	Data	A	P
	MSB … LSB		MSB … LSB		MSB LSB		

2) Auto increment (Select address increases (+1) by the value of the data.)

S	Slave address	A	Select address	A	Data 1, data 2,...data N	A	P
	MSB … LSB		MSB … LSB		MSB … LSB		

(Examples) ①The address data specified by select address is taken as data 1.
②The address data specified by select address +1 is taken as data 2.
③The address data specified by select address +N is taken as data N.

3) Structure with which transmission is not possible (In this case, only select address 1 is set.)

S	Slave address	A	Select address 1	A	Data	A	Select address 2	A	Data	A	P
	MSB … LSB		MSB … LSB		MSB LSB		MSB … LSB		MSB LSB		

Note: Following transmission of data, data transmitted as select address 2 will not be recognized as select address 2, but as data.

(5) Specification of select address and data

Function	Select address (MSB)							(LSB)	Data D7 (MSB)	D6	D5	D4	D3	D2	D1	D0 (LSB)
⓪ Volume CH1 (L)	0	0	0	0	0	0	0	0	VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0
① Volume CH2 (R)	0	0	0	0	0	0	0	1	VR7	VR6	VR5	VR4	VR3	VR2	VR1	VR0
② Bass	0	0	0	0	0	0	1	0	0	0	BA5	BA4	BA3	BA2	BA1	BA0
③Treble	0	0	0	0	0	0	1	1	0	0	TR5	TR4	TR3	TR2	TR1	TR0
④ Surround	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	SR0

- The auto increment function cycles the select address in the manner shown in Figure A.

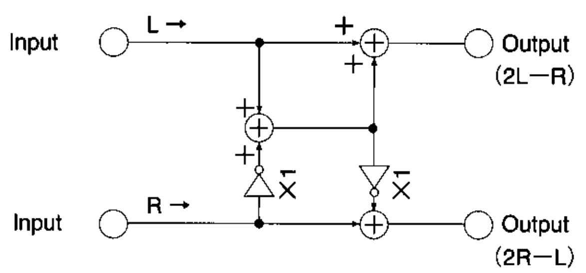
(Figure A) ⓪ → ① → ②
↑ ↓
④ ← ← ← ③

- The cycle commences from the initially specified select address.

(6) Surround data

Function	Data D7 (MSB)	D6	D5	D4	D3	D2	D1	D0 (LSB)
Matrix surround OFF	0	0	0	0	0	0	0	0
Matrix surround ON	0	0	0	0	0	0	0	1

(7) Matrix surround



Sound control
Audio accessory components

(8) Volume attenuation (reference values)

ATT (dB)	DATA (HEX)	ATT (dB)	DATA (HEX)	ATT (dB)	DATA (HEX)
0	FF	−19	85	−56	42
−1	E4	−20	82	−58	3F
−2	D8	−22	7C	−60	3C
−3	CF	−24	78	−62	39
−4	C8	−26	74	−64	36
−5	C2	−28	70	−66	34
−6	BD	−30	6D	−68	32
−7	B8	−32	6A	−70	2F
−8	B2	−34	68	−72	2D
−9	AD	−36	65	−74	2A
−10	A9	−38	61	−76	28
−11	A5	−40	5C	−78	26
−12	A0	−42	59	−80	24
−13	9C	−44	55	−82	22
−14	98	−46	52	−84	20
−15	94	−48	4E	−86	1E
−16	90	−50	4B	−90	1A
−17	8C	−52	48	−100	13
−18	89	−54	45	−112	00

Note: All figures in this table are reference values. When using this IC, check this table carefully and perform the appropriate setting.

(9) Bass/Treble gain settings (reference values)

ATT (dB)	DATA (HEX)	ATT (dB)	DATA (HEX)
15	3F	0	1F
14	38	−1	1C
13	35	−2	1B
12	33	−3	19
11	31	−4	18
10	2F	−5	17
9	2E	−6	16
8	2D	−7	15
7	2C	−8	13
6	2B	−9	12
5	2A	−10	11
4	29	−11	0F
3	27	−12	0D
2	26	−13	0B
1	25	−14	08
0	1F	−15	05

Notes: (1) The gain values in the treble and bass data setting tables above are based on the assumption that the filter constants have been set so that maximum and minimum gain are equal to the peak and bottom values listed in the frequency characteristics drawings.

(2) All figures in this table are reference values. When using this IC, check this table carefully and perform the appropriate setting.

● Application example

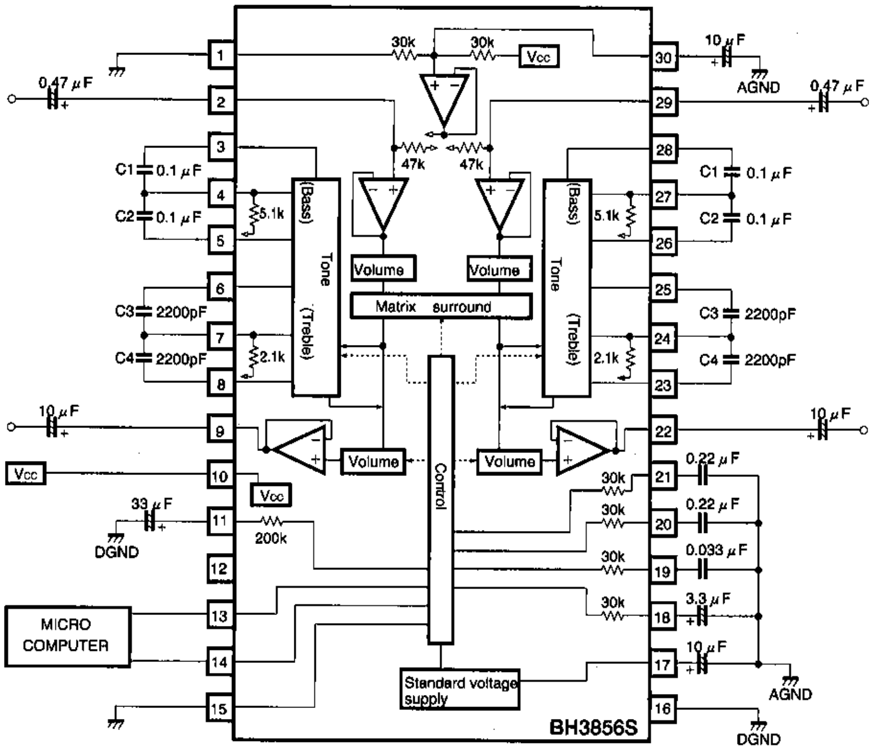


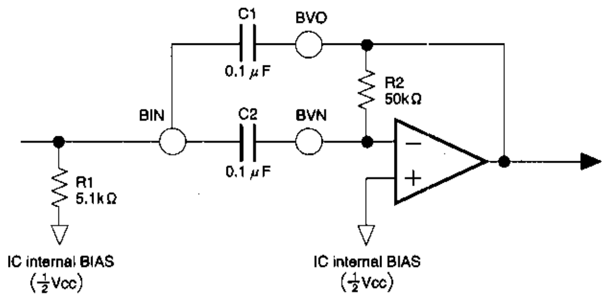
Fig. 2

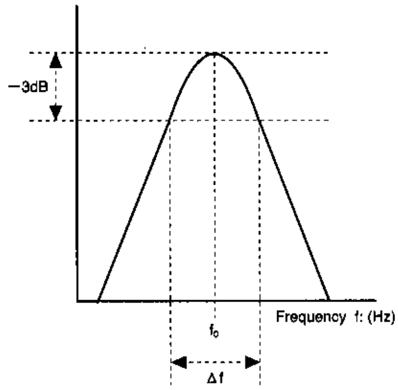
Note: Diagram depicts the BH3856S.

●Operation notes

1. Operating power supply voltage range
   As long as the operating power supply voltage and ambient temperature are kept within the specified range, the basic circuits are guaranteed to function, but be sure to check the constants as well as the element settings, voltage settings, and temperature settings.

2. Bass filter





・B.P.F. composed of multiple feedback active f_0 can be varied according to the value of C. (theoretical equation)

$$f_0 = \frac{1}{2\pi} \times \left(\frac{1}{R_1 R_2 C_1 C_2} \right)^{\frac{1}{2}} \qquad Q \fallingdotseq \left[\left(\frac{R_1}{R_2 C_1 C_2} \right)^{\frac{1}{2}} \times (C_1 + C_2) \right]^{-1}$$

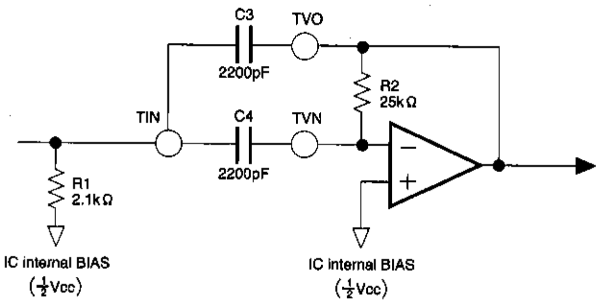
Note: Filter gain is calculated using the equation on the left. Total output gain is the sum of the gain for each of the internal circuits.

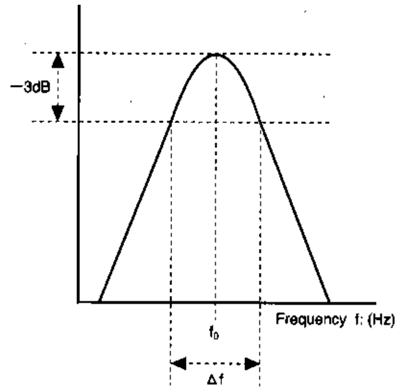
$$G = \frac{R_2}{5k\Omega} \times \left(1 + \frac{C_1}{C_2} \right)^{-1}$$

(When $R_1 = 5.1k\Omega$, $R_2 = 50k\Omega$, $C_1 = C_2 = C$)

$$f_0 = \frac{1.0 \times 10^{-5}}{C} \qquad Q \fallingdotseq 1.57 \quad G = 5.0$$

3. About the treble filter





- The band-pass filter is constructed using a multiple-feedback active filter.
  f_0 can be varied by changing the value of the capacitors.
  (Theoretical formulas)

$$f_0=\frac{1}{2\pi}\times\left(\frac{1}{R_1R_2C_3C_4}\right)^{\frac{1}{2}} \qquad Q\fallingdotseq\left(\left(\frac{R_1}{R_2C_3C_4}\right)^{\frac{1}{2}}\times(C_3+C_4)\right)^{-1}$$

$$G=\frac{R_2}{5k\Omega}\times\left(1+\frac{C_3}{C_4}\right)^{-1}$$

Note: The filter gain is given by the formula on the left, but the total output gain is determined by the this in combination with the internal circuit.

(When R_1 = 2.1kΩ, R_2 = 25kΩ, C_3 = C_4 = C)

$$f_0=\frac{2.2\times10^{-5}}{C} \qquad Q\fallingdotseq1.73 \quad G=2.5$$

4. I²CBUS control

High-frequency digital signals are input on the SCL and SDA terminals, so ensure that the wiring and PCB pattern is designed in such a way as to ensure that these signals do not interfere with the analog signal system.

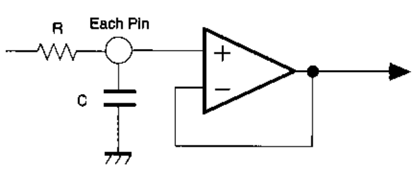
If you are not using I²CBUS control (i.e. you are using DC control), connect the SCL, SDA and SASS terminals to GND (do not leave them disconnected).

5. Step switching noise

The VC1, VC2, TC, BC and SC terminals have components connected to them the application example circuit. The values of these components may need to be changed depending on the signal level setting and PCB pattern.

Investigate carefully before deciding on the values of the various circuit constants.

The equivalent circuit for these terminals is given below (an integrator circuit is set at the first stage to slow the variation).

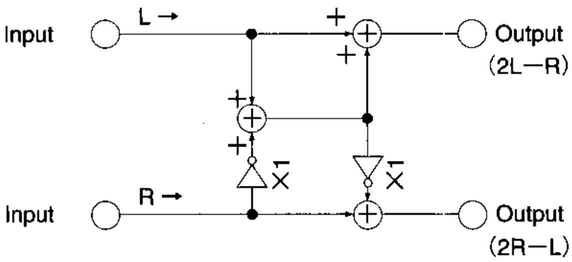


	R value (kΩ)
VC1, VC2, BC, TC	30
SC	200

6. Volume and tone level settings
This specification sheet gives reference values for the amount of attenuation and gain with respect to the serial control data. The internal D / A convertor is an R-2R circuit, and data exists for the places where continuous variation does not occur between data. Use this when fine setting is required. The setting limits are up to 8 bits for volume (256 steps) and 6 bits (64 steps) for tone.

7. Digital / analog separation
The digital and analog power supplies and grounds for this IC (BH3856) are completely separate. The digital circuits are supplied from a stable reference source that is on the chip (VREF (3.8V)). For this reason, there is no need to worry about timing shifts, or interference due to digital noise.

8. Matrix surround



◎The matrix surround circuit construction is as shown in the diagram above. The gain is obtained from the formulas in the diagram.

Phase Gain	0dB
Negative Phase Gain	6dB

(However, reverse-phase gain is for input to one Ch only)

9. DC control
An internal impedance of 30kΩ is seen from the VC1, VC2, TC, and BC terminals, and 200kΩ is seen from the SC (pin 11) terminal, so with regard to DC control, we recommend direct control with the voltage source. When using variable volume, take the impedance into consideration when making the setting.
Note: The DC control voltage range is 0V to VREF.
Do not apply voltages above VREF to the terminals.

10. GND
- As shown in the application example circuit, connect the external component GND to the analog GND.
- However, the GND for the capacitor connected to the VREF term inal should be connected to the digital GND.
- If a capacitor with goof high-frequency characteristics is connected in parallel with the capacitor connected to VREF, the performance of the circuit with respect to static noise will improve (we recommend a ceramic capacitor of between 0.001 μF and 0.1 μF)
- When using long digital and analog ground lines, take care to ensure that there is no potential difference between the two ground lines.

● Electrical characteristic curves

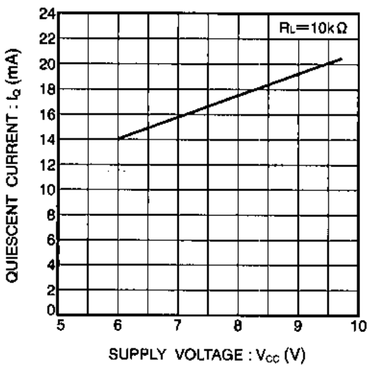


Fig. 3 Quiescent curve - Supply voltage characteristics

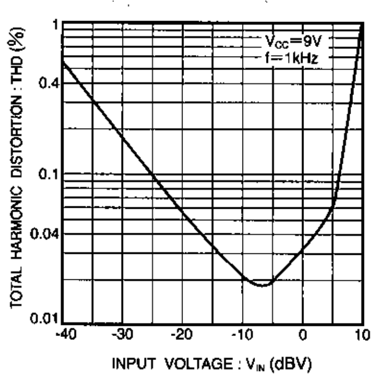


Fig.4 Total harmonic distortion - Input voltage characteristics

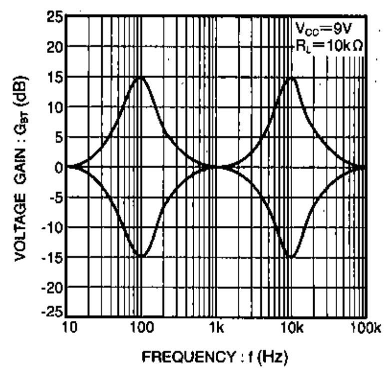
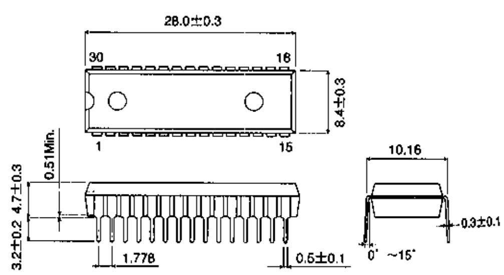


Fig. 5 Output gain - Frequency

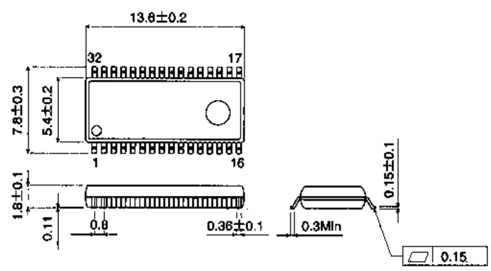
● External dimensions (Unit: mm)

BH3856S



SDIP30

BH3856FS



SSOP-A32

2-wire serial sound control IC

BH3856S / BH3856FS

The BH3856S and BH3856FS are signal processing ICs designed for volume and tone control in televisions, mini component stereo systems, and other audio products. Their two-line serial control (I^2C-BUS) enables them to control volume and tone on the basis of signals from a microcomputer, etc.

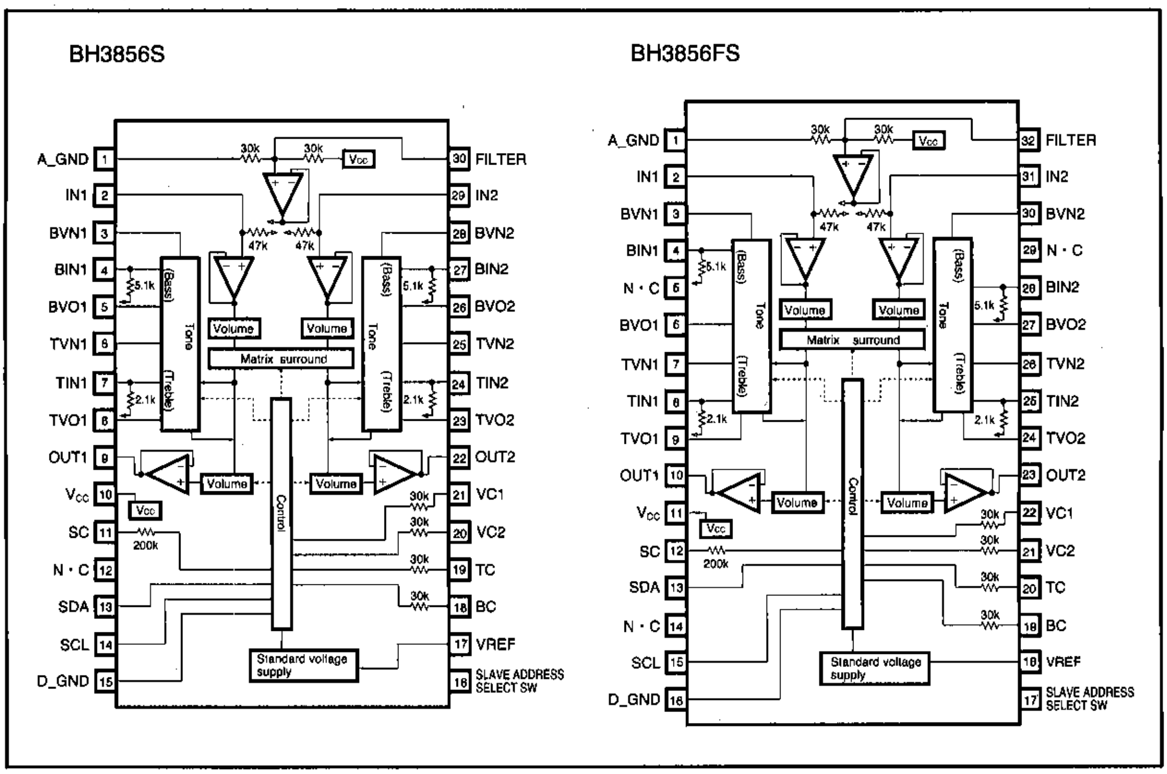
●Applications

Televisions, [VCRs] personal computer televisions, mini component stereo systems, car stereos

●Features

1) I^2C-BUS facilitates direct serial control from a microcomputer of volume (main volume), balance (left / right), and tone (bass, treble). DC control is also possible.
2) Volume is produced by a low-distortion, low-noise VCA. Designed to minimize step noise.
3) Stable standard voltage supply and built-in I / O buffer mean that few attachments are needed. SSOP32 package designed to save space.
4) Matrix surround yields powerful sound.

●Block diagram



ROHM

●Absolute maximum ratings (Ta = 25℃)

Parameter		Symbol	Limits	Unit
Supply voltage		Vcc	10.0	V
Power dissipation	BH3856S	Pd	1200 *1	mW
	BH3856FS		850 *2	
Operating temperature		Topr	−40～+85	℃
Storage temperature		Tstg	−55～+150	℃

*1 Reduced by 12 mW for each increase in Ta of 1℃ over 25℃.
*2 Reduced by 6.8 mW for each increase in Ta of 1℃ over 25℃.

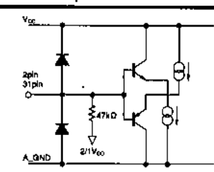
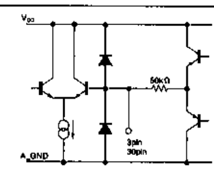
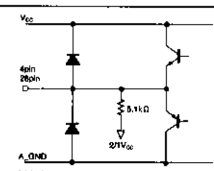
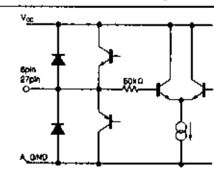
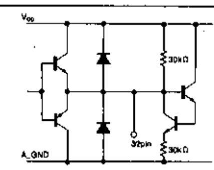
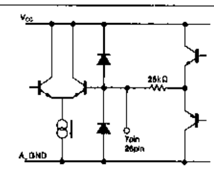
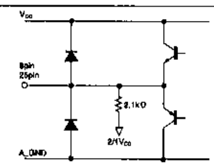
●Recommended operating conditions (Ta = 25℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	Vcc	6.0	9	9.5	V

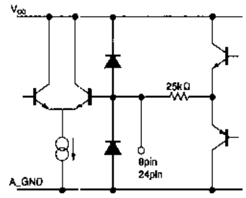
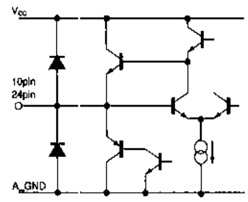
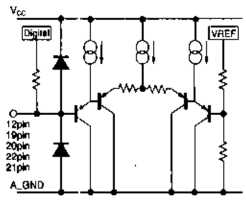
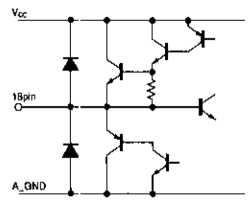
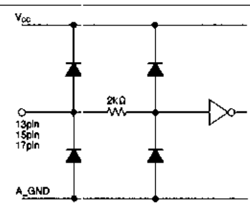
●Pin description

Pin No.		Symbol	Description
BH3856S	BH3856FS		
1	1	A_GND	Analog system ground
2	2	IN1	Pin for ch 1 volume input
3	3	BVN1	Pin for connection to ch 1 low-band filter
4	4	BIN1	Pin for connection to ch 1 low-band filter
5	6	BVO1	Pin for connection to ch 1 low-band filter
6	7	TVN1	Pin for connection to ch 1 high-band filter
7	8	TIN1	Pin for connection to ch 1 high-band filter
8	9	TVO1	Pin for connection to ch 1 high-band filter
9	10	OUT1	Pin for ch 1 volume output
10	11	Vcc	Power supply pin
11	12	SC	Time constant pin for prevention of switching shock
13	13	SDA	SDA data input pin
14	15	SCL	SCL data input pin
15	16	D_GND	Digital system ground
16	17	SASS	Slave address selection pin
17	18	VREF	Standard voltage output pin
18	19	BC	Time constant pin for prevention of switching shock
19	20	TC	Time constant pin for prevention of switching shock
20	21	VC2	Time constant pin for prevention of switching shock
21	22	VC1	Time constant pin for prevention of switching shock
22	23	OUT2	Pin for ch 2 volume output
23	24	TVO2	Pin for connection to ch 2 high-band filter
24	25	TIN2	Pin for connection to ch 2 high-band filter
25	26	TVN2	Pin for connection to ch 2 high-band filter
26	27	BVO2	Pin for connection to ch 2 low-band filter
27	29	BIN2	Pin for connection to ch 2 low-band filter
28	30	BVN2	Pin for connection to ch 2 low-band filter
29	31	IN2	Pin for ch 2 volume input
30	32	FILTER	Filter pin
12	5,14,28	NC	Not connected internally.

●Input / output circuit

Symbol	Pin Voltage	Equivalent circuit	Description
IN1 IN2	4.5V 4.5V		Main volume input pin. Designed for input impedance of 47 kΩ Typ).
BVN1 BVN2	4.5V 4.5V		Pin for low band filter connection.
BIN1 BIN2	4.5V 4.5V		Pin for low band filter connection.
BVO1 BVO1	4.5V 4.5V		Pin for low band filter connection.
FILTER	5.2V		Filter input pin. Please install a capacitor of about 10 μF to the filter pin. Has built-in precharge and discharge circuits.
TVN1 TVN2	4.5V 4.5V		Pin for high band filter connection.
TIN1 TIN2	4.5V 4.5V		Pin for high band filter connection.

※The pin numbers are for the BH3856S.

Symbol	Pin Voltage	Equivalent Circuit	Description
TVO1 TVO2	4.5V 4.5V		Pin for high band filter connection.
OUT1 OUT2	4.5V 4.5V		Main volume output pin. OUT1 is the volume output for CH1. OUT2 is the volume output for CH2.
SC BC TC VC1 VC2			For prevention of shock noise during step switching. SC: Surround pin BC: Bass pin TC: Treble pin VC1: Volume pin (CH1) VC2: Volume pin (CH2)
VREF	3.8V		3.8V regulator output pin. Output requires capacitor for stopping oscillation. Output pin has built-in precharge and discharge circuits, so there is no problem with start-up or shut-down even with a large capacitor. This pin is for connection to the high-band filter.
SDA SCL SASS			• I²C bass input pin SDA: serial data line SCL: serial clock line • Slave address selection pin SASS: slave address selection switch
VCC		Power supply voltage pin.	
A_GND		Analog GND pin. Connected to IC board.	
D_GND		Digital GND pin. Separate from Analog GND pin.	

*The pin numbers are for the BH3856S.

● Electrical characteristics (Unless otherwise specified, Ta = 25℃, V_{CC} = 9V, f = 1kHz, BW = 20 ~ 20kHz, VOL = Max., TONE = ALL FLAT, R_g = 600Ω, R_L = 10kΩ)

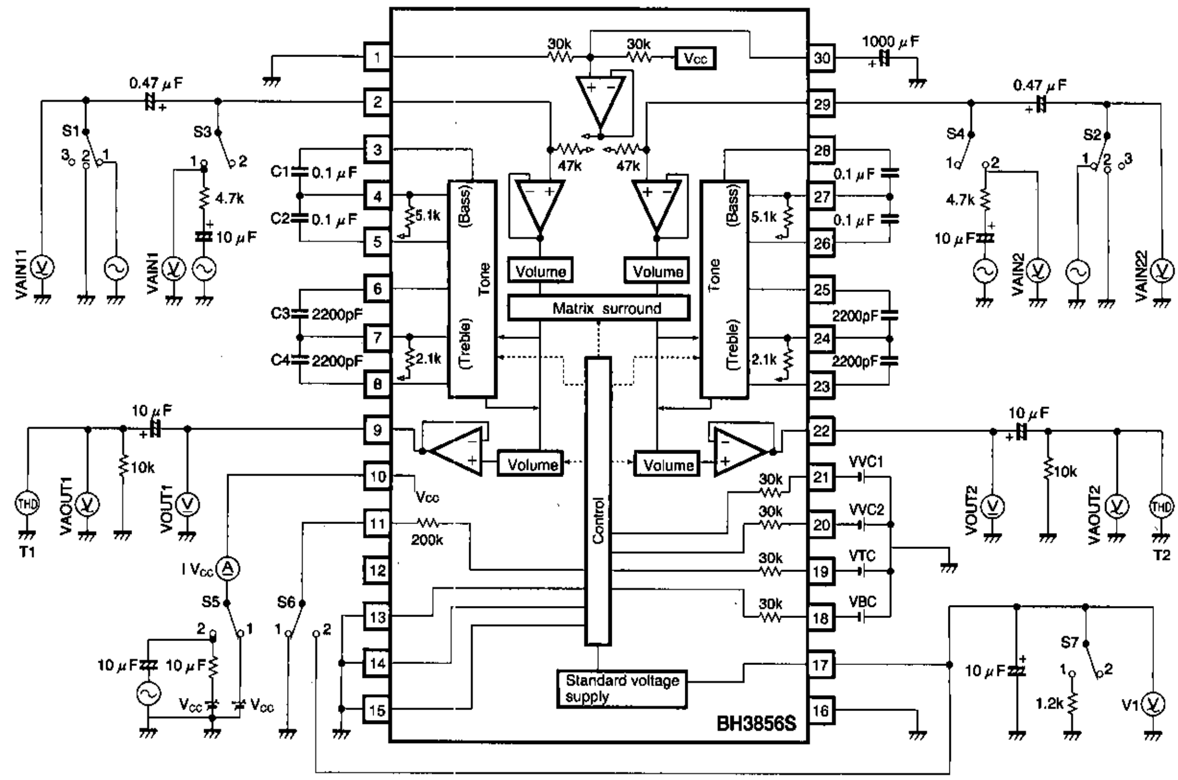
Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Quiescent current	I_Q	−	20	27	mA	No signal
Max. input	Vim	2.3	2.5	−	Vrms	THD=1%, VOL=−20dB (ATT)
Max. output	Vom	2.3	2.5	−	Vrms	THD=1%
Voltage gain	Gv	−1.5	0	+1.5	dB	Vin=1Vrms
Max. attenuation	ATT	90	110	−	dB	Vo=1Vrms
Cross talk	V_{CT}	70	80	−	dB	Vo=1Vrms
Low-band control width	VB Max.	+12	+15	+18	dB	100Hz, Vin=100mVrms
	VB Min.	−18	−15	−12	dB	100Hz, Vin=100mVrms
High-band control width	VT Max.	+12	+15	+18	dB	100kHz, Vin=100mVrms
	VT Min.	−18	−15	−12	dB	100kHz, Vin=100mVrms
Matrix surround single-channel gain	G_{SR}	4	6	8	dB	Vo=1Vrms *
Total Harmonic distortion	THD	−	0.01	0.1	%	Vo=0.5Vrms, BPF=400Hz~30kHz
Output noise voltage	$V_{NO}1$	−	45	65	μVrms	No signal, VOL=MAX, Rg=0 *
Residual output noise voltage	VM_{NO}	−	2	10	μVrms	No signal, VOL=−∞, Rg=0 *
Standard power supply output voltage	V_{REF}	3.5	3.8	4.1	V	I_{REF}=3mA
Standard power supply output current capability	I_{REF}	3.0	10	−	mA	V_{REF}>3.7V
Channel balance	G_{CB}	−1.5	0	+1.5	dB	CH1 taken as the standard for measurements.
Input impedance	R_{IN}	33	47	61	kΩ	f=1kHz
Output impedance	R_{OUT}	−	−	10	Ω	f=1kHz
Ripple rejection	RR	40	−	−	dB	f=100Hz, V_{RR}=1Vrms
Input voltage H	V_{IH}	4	−	−	V	SCL, SDA
Input voltage L	V_{IL}	−	−	1	V	SCL, SDA

Items marked with an asterisk (*) were measured with the VP-9690A (displays mean detection and effective value), produced by Matsushita Communication Industrial.
◎ Not designed for radiation resistance.
◎ Signal input occurs in equiphase.

Sound control

Audio accessory components

● Measurement circuit



Unit : R [Ω]
C [F]

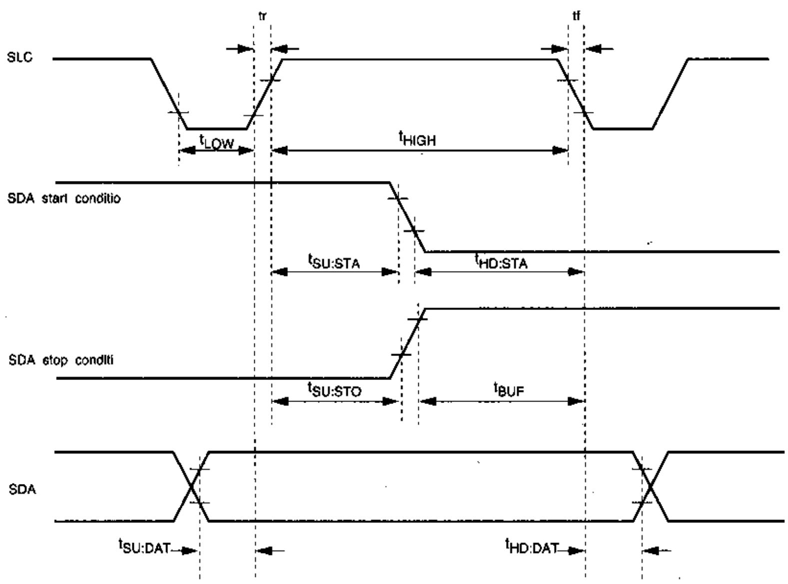
Fig. 1

Note: Diagram depicts the BH3856S.

●Performing data settings

(1) I^2C BUS timing

Parameter	Symbol	Min.	Typ.	Max.	Unit
SCL clock frequency	f_{SCL}	0	—	100	kHz
SCL clock hold time, HIGH state	t_{HIGH}	4	—	—	μs
SCL clock hold time, LOW state	t_{LOW}	4.7	—	—	μs
SDA and SDL signal start-up time	tr	—	—	1	μs
SDA and SDL signal shut-down time	tf	—	—	0.3	μs
Set-up time for re-send [start] conditions	t_{SU};STA	4.7	—	—	μs
Hold time (re-send) [start] conditions (After hold time ends, initial clock pulse is generated.)	t_{HD};STA	4	—	—	μs
Set time for [stop] conditions.	t_{SU};STO	4.7	—	—	μs
Bus free time between [stop] condition and [start] condition	t_{BUF}	4.7	—	—	μs
Data set-up time	t_{SU};DAT	250	—	—	ns



t_{SU};STA=start code set-up time.
t_{HD};STA=start code hold time.
t_{SU};STO=stop code set-up time.
t_{BUF}=bus free time.
t_{SU};DAT=data set-up time.
t_{HD};DAT=data hold time.

I^2C-BUS timing rules

(2) I²C BUS data format

	MSB LSB		MSB LSB		MSB LSB			
S	Slave address	A	Select address	A	Data	A	P
1bit	8bit	1bit	8bit	1bit	8bit	1bit	1bit

- S = start condition (start bit recognition)
- Slave address = IC recognition. Upper 7 bits are random. Bottom bit is "L" for the sake of overwrite.
- A = acknowledge bit (recognition of acknowledgment)
- Select address = selection between volume, bass, treble, and matrix surround
- Data = volume and tone data
- P = stop condition (stop bit recognition)

(3) BH3856S/BH3856FS slave addresses

MSB LSB

A6	A5	A4	A3	A2	A1	A0	R/W
1	0	0	0	0	0	A	0

- Slave address selection
  ①A = 1 (10000010) [SASS pin HI]
  ②A = 0 (10000000) [SASS pin LOW]

(4) Interface protocol

1) Basic protocol

S	Slave address	A	Select address	A	Data	A	P
	MSB LSB		MSB LSB		MSB LSB		

2) Auto increment (Select address increases (+1) by the value of the data.)

S	Slave address	A	Select address	A	Data 1, data 2,...data N	A	P
	MSB LSB		MSB LSB		MSB LSB		

(Examples) ①The address data specified by select address is taken as data 1.
②The address data specified by select address +1 is taken as data 2.
③The address data specified by select address +N is taken as data N.

3) Structure with which transmission is not possible (In this case, only select address 1 is set.)

S	Slave address	A	Select address 1	A	Data	A	Select address 2	A	Data	A	P
	MSB LSB		MSB LSB		MSB LSB		MSB LSB		MSB LSB		

> Note: Following transmission of data, data transmitted as select address 2 will not be recognized as select address 2, but as data.

(5) Specification of select address and data

Function	Select address (MSB)							(LSB)	Data (MSB) D7	D6	D5	D4	D3	D2	D1	(LSB) D0
⓪ Volume CH1 (L)	0	0	0	0	0	0	0	0	VL7	VL6	VL5	VL4	VL3	VL2	VL1	VL0
① Volume CH2 (R)	0	0	0	0	0	0	0	1	VR7	VR6	VR5	VR4	VR3	VR2	VR1	VR0
② Bass	0	0	0	0	0	0	1	0	0	0	BA5	BA4	BA3	BA2	BA1	BA0
③Treble	0	0	0	0	0	0	1	1	0	0	TR5	TR4	TR3	TR2	TR1	TR0
④ Surround	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	SR0

· The auto increment function cycles the select address in the manner shown in Figure A.

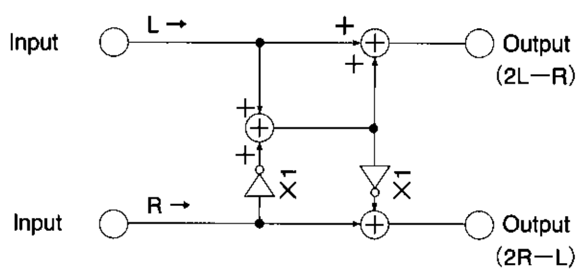
(Figure A) ⓪ → ① → ②
↑ ↓
④ ← ← ← ③

· The cycle commences from the initially specified select address.

(6) Surround data

Function	Data (MSB) D7	D6	D5	D4	D3	D2	D1	(LSB) D0
Matrix surround OFF	0	0	0	0	0	0	0	0
Matrix surround ON	0	0	0	0	0	0	0	1

(7) Matrix surround



(8) Volume attenuation (reference values)

ATT (dB)	DATA (HEX)	ATT (dB)	DATA (HEX)	ATT (dB)	DATA (HEX)
0	FF	−19	85	−56	42
−1	E4	−20	82	−58	3F
−2	D8	−22	7C	−60	3C
−3	CF	−24	78	−62	39
−4	C8	−26	74	−64	36
−5	C2	−28	70	−66	34
−6	BD	−30	6D	−68	32
−7	B8	−32	6A	−70	2F
−8	B2	−34	68	−72	2D
−9	AD	−36	65	−74	2A
−10	A9	−38	61	−76	28
−11	A5	−40	5C	−78	26
−12	A0	−42	59	−80	24
−13	9C	−44	55	−82	22
−14	98	−46	52	−84	20
−15	94	−48	4E	−86	1E
−16	90	−50	4B	−90	1A
−17	8C	−52	48	−100	13
−18	89	−54	45	−112	00

Note: All figures in this table are reference values. When using this IC, check this table carefully and perform the appropriate setting.

(9) Bass/Treble gain settings (reference values)

ATT (dB)	DATA (HEX)	ATT (dB)	DATA (HEX)
15	3F	0	1F
14	38	−1	1C
13	35	−2	1B
12	33	−3	19
11	31	−4	18
10	2F	−5	17
9	2E	−6	16
8	2D	−7	15
7	2C	−8	13
6	2B	−9	12
5	2A	−10	11
4	29	−11	0F
3	27	−12	0D
2	26	−13	0B
1	25	−14	08
0	1F	−15	05

Notes: (1) The gain values in the treble and bass data setting tables above are based on the assumption that the filter constants have been set so that maximum and minimum gain are equal to the peak and bottom values listed in the frequency characteristics drawings.

(2) All figures in this table are reference values. When using this IC, check this table carefully and perform the appropriate setting.

● Application example

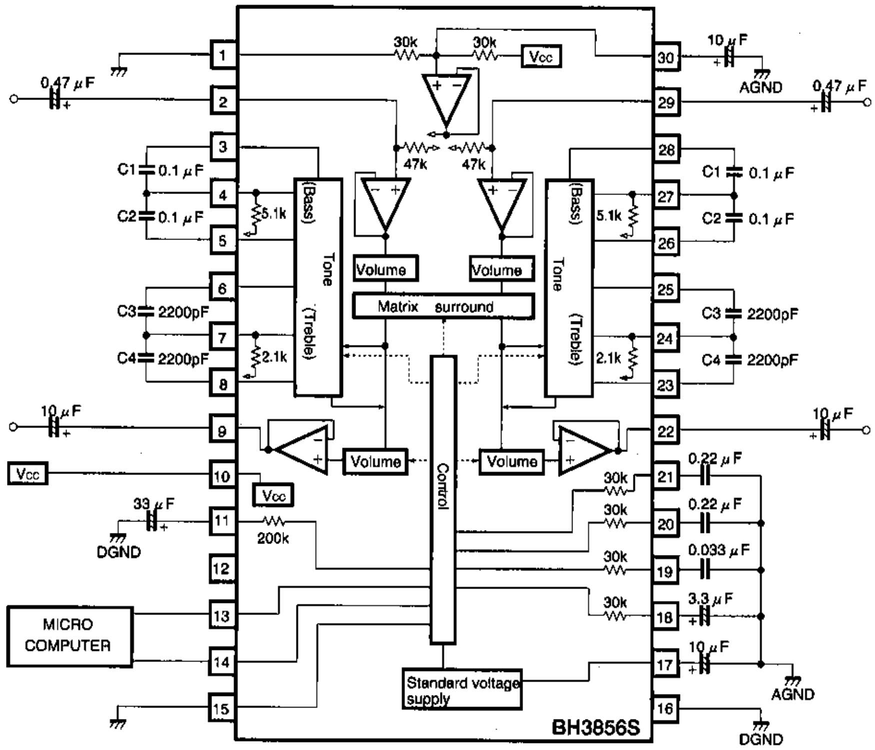


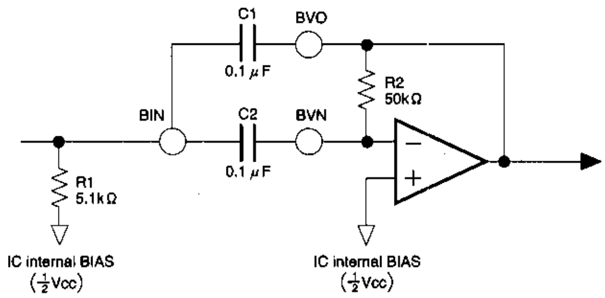
Fig. 2

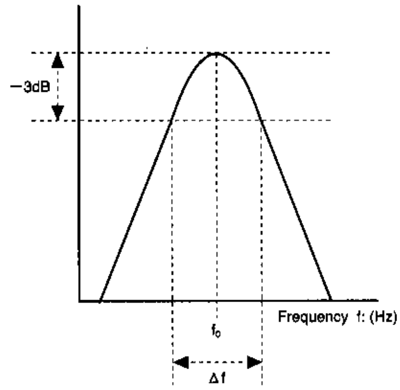
Note: Diagram depicts the BH3856S.

●Operation notes

1. Operating power supply voltage range
   As long as the operating power supply voltage and ambient temperature are kept within the specified range, the basic circuits are guaranteed to function, but be sure to check the constants as well as the element settings, voltage settings, and temperature settings.

2. Bass filter





• B.P.F. composed of multiple feedback active f_0 can be varied according to the value of C. (theoretical equation)

$$f_0 = \frac{1}{2\pi} \times \left(\frac{1}{R_1 R_2 C_1 C_2} \right)^{\frac{1}{2}} \qquad Q \fallingdotseq \left[\left(\frac{R_1}{R_2 C_1 C_2} \right)^{\frac{1}{2}} \times (C_1 + C_2) \right]^{-1}$$

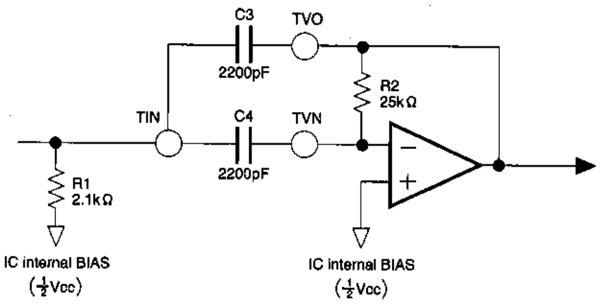
Note: Filter gain is calculated using the equation on the left. Total output gain is the sum of the gain for each of the internal circuits.

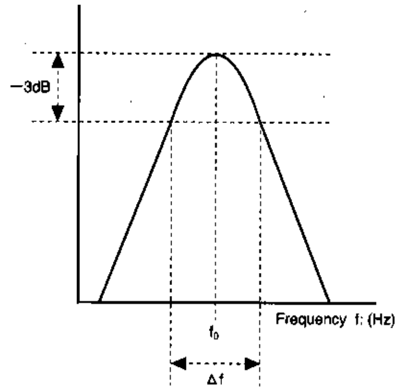
$$G = \frac{R_2}{5k\Omega} \times \left(1 + \frac{C_1}{C_2} \right)^{-1}$$

(When $R_1 = 5.1k\Omega$, $R_2 = 50k\Omega$, $C_1 = C_2 = C$)

$$f_0 = \frac{1.0 \times 10^{-5}}{C} \qquad Q \fallingdotseq 1.57 \quad G = 5.0$$

3. About the treble filter





- The band-pass filter is constructed using a multiple-feedback active filter.
  f_0 can be varied by changing the value of the capacitors.
  (Theoretical formulas)

$$f_0=\frac{1}{2\pi}\times\left(\frac{1}{R_1R_2C_3C_4}\right)^{\frac{1}{2}} \qquad Q\fallingdotseq\left(\left(\frac{R_1}{R_2C_3C_4}\right)^{\frac{1}{2}}\times(C_3+C_4)\right)^{-1}$$

Note: The filter gain is given by the formula on the left, but the total output gain is determined by the this in combination with the internal circuit.

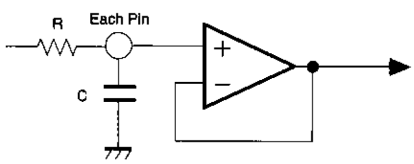
$$G=\frac{R_2}{5k\Omega}\times\left(1+\frac{C_3}{C_4}\right)^{-1}$$

(When $R_1 = 2.1k\Omega$, $R_2 = 25k\Omega$, $C_3 = C_4 = C$)

$$f_0=\frac{2.2\times10^{-5}}{C} \qquad Q\fallingdotseq1.73 \quad G=2.5$$

4. I²CBUS control
   High-frequency digital signals are input on the SCL and SDA terminals, so ensure that the wiring and PCB pattern is designed in such a way as to ensure that these signals do not interfere with the analog signal system.
   If you are not using I²CBUS control (i.e. you are using DC control), connect the SCL, SDA and SASS terminals to GND (do not leave them disconnected).

5. Step switching noise
   The VC1, VC2, TC, BC and SC terminals have components connected to them the application example circuit. The values of these components may need to be changed depending on the signal level setting and PCB pattern.
   Investigate carefully before deciding on the values of the various circuit constants.
   The equivalent circuit for these terminals is given below (an integrator circuit is set at the first stage to slow the variation).

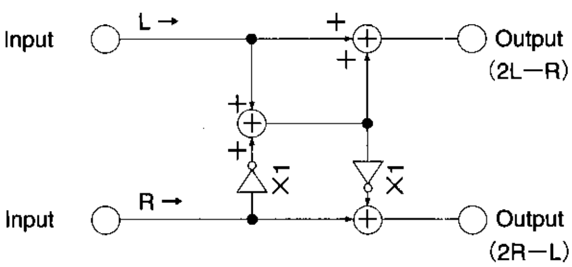


	R value (kΩ)
VC1, VC2, BC, TC	30
SC	200

6. Volume and tone level settings
This specification sheet gives reference values for the amount of attenuation and gain with respect to the serial control data. The internal D / A convertor is an R-2R circuit, and data exists for the places where continuous variation does not occur between data. Use this when fine setting is required. The setting limits are up to 8 bits for volume (256 steps) and 6 bits (64 steps) for tone.

7. Digital / analog separation
The digital and analog power supplies and grounds for this IC (BH3856) are completely separate. The digital circuits are supplied from a stable reference source that is on the chip (VREF (3.8V)). For this reason, there is no need to worry about timing shifts, or interference due to digital noise.

8. Matrix surround



◎The matrix surround circuit construction is as shown in the diagram above. The gain is obtained from the formulas in the diagram.

Phase Gain	0dB
Negative Phase Gain	6dB

(However, reverse-phase gain is for input to one Ch only)

9. DC control
An internal impedance of 30kΩ is seen from the VC1, VC2, TC, and BC terminals, and 200kΩ is seen from the SC (pin 11) terminal, so with regard to DC control, we recommend direct control with the voltage source. When using variable volume, take the impedance into consideration when making the setting.
Note: The DC control voltage range is 0V to VREF.
Do not apply voltages above VREF to the terminals.

10. GND
- As shown in the application example circuit, connect the external component GND to the analog GND.
- However, the GND for the capacitor connected to the VREF term inal should be connected to the digital GND.
- If a capacitor with goof high-frequency characteristics is connected in parallel with the capacitor connected to VREF, the performance of the circuit with respect to static noise will improve (we recommend a ceramic capacitor of between 0.001 μF and 0.1 μF)
- When using long digital and analog ground lines, take care to ensure that there is no potential difference between the two ground lines.

● Electrical characteristic curves

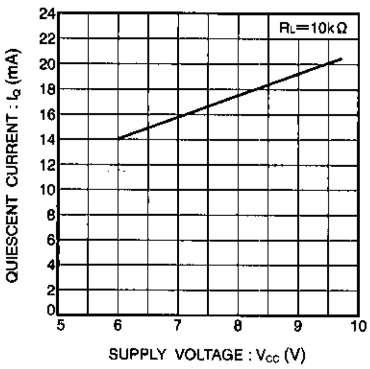


Fig. 3 Quiescent curve - Supply voltage characteristics

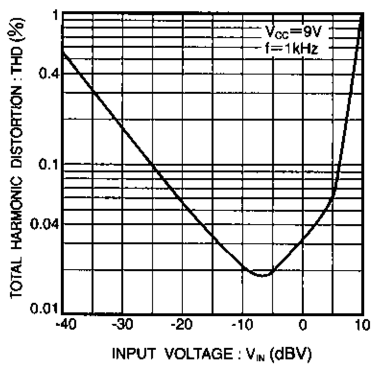


Fig.4 Total harmonic distortion - Input voltage characteristics

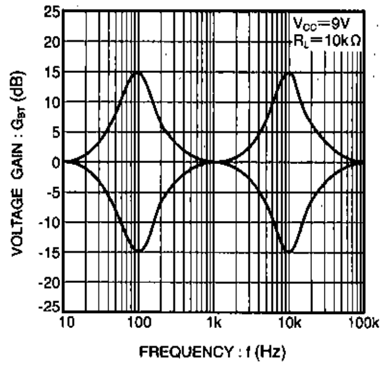
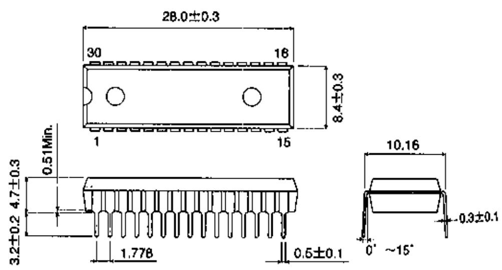


Fig. 5 Output gain - Frequency

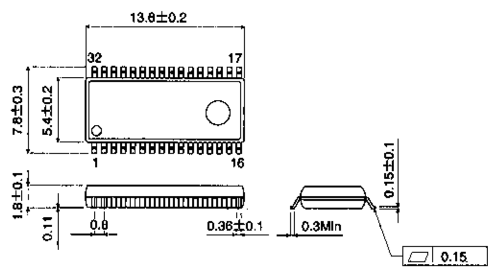
● External dimensions (Unit: mm)

BH3856S



SDIP30

BH3856FS



SSOP-A32

Sound control

Audio accessory components

Audio sound controller
BH3857FV

The BH3857FV is a signal-processing IC for controlling audio quality in CD radio-cassette players and mini-component stereo systems. Three-line serial control is available making it easy to adjust tone and volume using a microprocessor.

●Applications
Mini-component stereo systems, CD radio cassette players, car audio systems and TVs.

●Features
1) Volume (main volume) and tone (bass and treble) control possible by direct serial link to a microprocessor. DC control is also possible.
2) Volume control is done with a low-distortion, low-noise VCA, and step noise is suppressed.
3) The gain of the input amplifier can be adjusted, and two surround matrixes are available to expand the sound.
4) The IC includes a stable reference voltage source and input buffer to reduce external component requirements, and comes in a compact 40-pin SSOP package that is perfect for compact designs.
5) Four open-collector outputs are provided to make logic control possible.

●Absolute maximum ratings (Ta = 25℃)

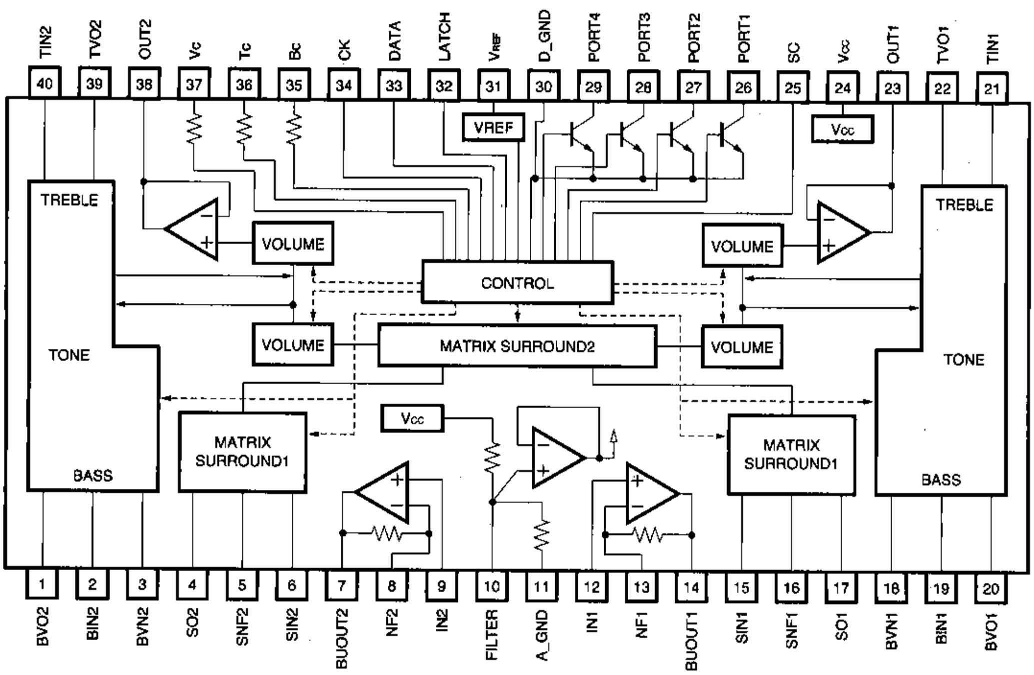
Parameter	Symbol	Limits	Unit
Applied voltage	V_{CC}	10.0	V
Power dissipation	Pd	1000	mW
Operating temperature	Topr	−40～+85	℃
Storage temperature	Tstg	−55～+150	℃
Port terminal voltage	PORT1～PORT4	15.0	V
Control terminal voltage	Vc, Tc Bc, Sc	V_{REF}	V

* Reduced by 8mW for each increase in Ta of 1°C over 25°C.

●Recommended operating conditions (Ta = 25℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{CC}	5.4	8.0	9.5	V

●Block diagram



◎Control of volume, bass, treble and surround 2 can also be done by external application of a DC voltage to the VC (volume), BC (bass), TC (treble) and SC (surround 2) terminals.
◎The impedance of the VC, TC, and BC terminals is 10kΩ (typ.).
◎The impedance of the SC terminal is 200kΩ (typ.).

●Pin descriptions

Pin No.	Symbol	Function
1	BVO2	Channel 2 bass filter
2	BIN2	Channel 2 bass filter
3	BVN2	Channel 2 bass filter
4	SO2	Channel 2 surround constant setting
5	SNF2	Channel 2 surround constant setting
6	SIN2	Channel 2 surround input
7	BUOUT2	Input-stage amplifier output
8	NF2	Input-stage amplifier gain setting
9	IN2	Channel 2 volume input
10	FILTER	Filter terminal
11	A_GND	Analog ground
12	IN1	Channel 1 volume input
13	NF1	Input-stage amplifier gain setting
14	BUOUT1	Input-stage amplifier output
15	SIN1	Channel 1 surround input
16	SNF1	Channel 1 surround constant setting
17	SO1	Channel 1 surround constant setting
18	BVN1	Channel 1 bass filter
19	BIN1	Channel 1 bass filter
20	BVO1	Channel 1 bass filter

Pin No.	Symbol	Function
21	TIN1	Channel 1 treble filter
22	TVO1	Channel 1 treble filter
23	OUT1	Channel 1 volume output
24	Vcc	Power supply
25	SC	Time constant setting terminal to prevent switching shock
26	PORT1	Port output
27	PORT2	Port output
28	PORT3	Port output
29	PORT4	Port output
30	D_GND	Digital ground
31	VREF	Reference voltage output
32	LATCH	Latch input
33	DATA	Data input
34	CK	Clock input
35	BC	Time constant setting terminal to prevent switching shock
36	TC	Time constant setting terminal to prevent switching shock
37	VC	Time constant setting terminal to prevent switching shock
38	OUT2	Channel 2 volume output
39	TVO2	Channel 2 treble filter
40	TIN2	Channel 2 treble filter

●Electrical characteristics (Unless otherwise specified, Ta = 25℃, V_{CC} = 8V, f = 1kHz, BW = 20Hz to 20kHz, VOL = MAX, Tone = ALL FLAT, R_g = 600Ω, R_L = 10kΩ, INPUT_AMP_GAIN = 0dB)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Quiescent current	I_Q	9	19	26	mA	No signal
Maximum input voltage	Vim	1.7	1.9	—	Vrms	THD=1%, V_{OL}=−20dB (ATT)
Maximum output voltage	Vom	1.8	2.0	—	Vrms	THD=1%
Voltage gain	G_V	−2.0	0.0	+2.0	dB	V_{IN}=1Vrms
Maximum attenuation	ATT	90	110	—	dB	V_O=1Vrms
Crosstalk	V_{CT}	64	70	—	dB	V_O=1Vrms, BPF=400Hz~30kHz
Bass control range	VBmax	+12	+15	+18	dB	75Hz, V_{IN}=100mVrms
	VBmin	−18	−15	−12	dB	75Hz, V_{IN}=100mVrms
Treble control range	VTmax	+12	+15	+18	dB	10kHz, V_{IN}=100mVrms
	VTmin	−18	−15	−12	dB	10kHz, V_{IN}=100mVrms
Mute attenuation	V_{MT}	90	110	—	dB	V_O=1Vrms *
Total harmonic distortion	THD	—	0.03	0.1	%	V_O=0.3Vrms, BPF=400Hz~30kHz
Residual output noise voltage	$V_{NO}1$	—	25	34	μVrms	No signal, V_{OL}=MAX, Rg=0 *
Output residual noise voltage at full boost	$V_{NO}2$	—	80	120	μVrms	No signal, TONE = ALL MAX, VOL = MAX, Rg = 0 *
Residual output noise voltage	VM_{NO}	—	2	10	μVrms	No signal, VOL = -infinity, Rg = 0 *
Reference voltage supply output	V_{REF}	3.5	3.8	4.1	V	I_{REF}=3mA
Reference voltage supply output current capacity	I_{REF}	3.0	10	—	mA	V_{REF}>3.7V
Channel balance	G_{CB}	−2.0	0	+2.0	dB	Measured with respect to CH1
Port output current	I_{PMAX}	5.0	—	—	mA	
L output voltage	V_{OL}	—	0.4	0.5	V	I_{OL}=5mA
H output disable current	I_{OZH}	—	—	1.0	μA	V_O=5V
Volume attenuation (-10dB)	ATT10	−12.0	−10.0	−8.0	dB	VIN = 0dBV, gain when control data 10101010 is input.
SC terminal (on voltage)	SC_{ON}	—	0	0.5	V	
VC terminal impedance	R_{VC}	8.0	10	12	kΩ	
BC terminal impedance	R_{BC}	8.0	10	12	kΩ	
TC terminal impedance	R_{TC}	8.0	10	12	kΩ	
SC terminal impedance	R_{SC}	160	200	240	kΩ	

* Measured using a Matsushita Communication Industrial VP-9690A (average value detector, effective value display).
Operating specifications: same phase for the input and output signals.
© Not designed for radiation resistance.

●Measurement circuit

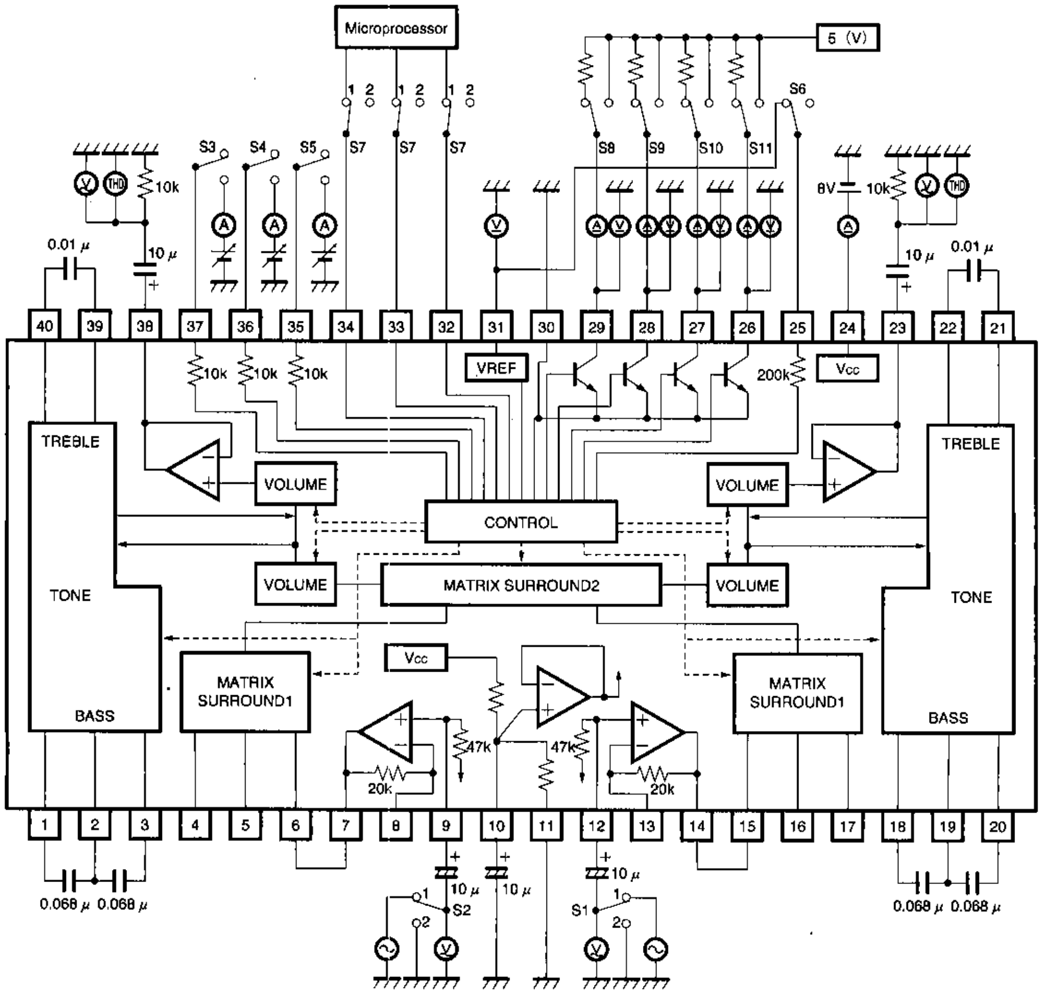


Fig. 1

●Circuit operation

(1) About the data format

As shown in Fig. 2, there are 32 bits of data. When the power is applied, a reset is applied to switch ports 1 to 4 off, but the reset is not applied to the other ports, so they are unstable. For this reason, it is necessary to input the data at least once while the set mute circuit is on.

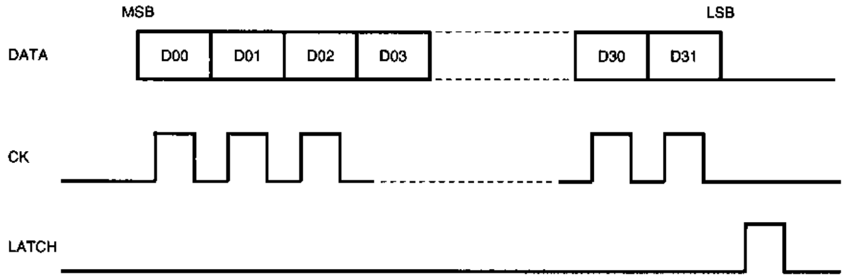


Fig. 2

Data	Function
D00~D07	Volume control
D08~D12	Treble control
D13~D17	Bass control
D18~D19	Surround control
D20~D23	Port control
D24~D31	Chip select + parity

※D18 : Surround matrix 1 control
D19 : Surround matrix 2 control

D20	D21	D22	D23
Port 1	Port 2	Port 3	Port 4

- Surround is on when the bit data is 0, and off when it is 1.
- With regard to the port 1 to 4 outputs, when the power is on, if no data is input the transistors for each output are set to off. The outputs are on when the bit data is 1, and off when it is 0.

※Apply the following data for chip select and parity.

D24 · · · · · · D31							
0	1	0	1	0	1	1	1

(2) Logic input terminals
Logic input terminals have a bipolar construction, so take care with regard to source current.

(3) Timing chart
The timing chart is shown in Fig. 3.

Timing (recommended conditions)

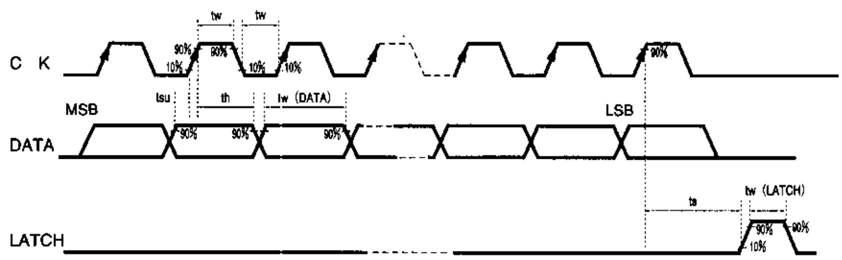


Fig.3

Timing chart constants

Parameter	Symbol	Min.	Typ.	Max.	Unit
H input voltage	V_{IH}	4.0	5.0	6.0	V
L input voltage	V_{IL}	—	0	1.0	V
Minimum clock width	tw	2.0	—	—	μS
Minimum data width	tw (DATA)	2.0	—	—	μS
Minimum latch width	tw (LATCH)	2.0	—	—	μS
Setup time (DATA to CLK)	tsu	1.0	—	—	μS
Hold time (CLK to DATA)	th	1.0	—	—	μS
Setup time (CLK to LATCH)	ts	1.0	—	—	μS

* Hold the logic terminal inputs at a "L" voltage until the voltage on the Vcc terminal reaches the minimum operating voltage (5.4V). The port terminals (pins 26 to 29) are off (open) at this time.

(4) Data table

The transmission data is given in the table below.

Volume data settings (reference values)

Hex display	Volume gain	MSB V_8	V_7	V_6	V_5	V_4	V_3	V_2	LSB V_1
FF	0dB	1	1	1	1	1	1	1	1
E5	−1dB	1	1	1	0	0	1	0	1
DB	−2dB	1	1	0	1	1	0	1	1
D3	−3dB	1	1	0	1	0	0	1	1
CC	−4dB	1	1	0	0	1	1	0	0
C6	−5dB	1	1	0	0	0	1	1	0
C0	−6dB	1	1	0	0	0	0	0	0
BA	−7dB	1	0	1	1	1	0	1	0
B5	−8dB	1	0	1	1	0	1	0	1
B0	−9dB	1	0	1	1	0	0	0	0
AB	−10dB	1	0	1	0	1	0	1	1
A7	−11dB	1	0	1	0	0	1	1	1
A3	−12dB	1	0	1	0	0	0	1	1
9F	−13dB	1	0	0	1	1	1	1	1
9C	−14dB	1	0	0	1	1	1	0	0
98	−15dB	1	0	0	1	1	0	0	0
95	−16dB	1	0	0	1	0	1	0	1
91	−17dB	1	0	0	1	0	0	0	1
8E	−18dB	1	0	0	0	1	1	1	0
8A	−19dB	1	0	0	0	1	0	1	0
87	−20dB	1	0	0	0	0	1	1	1
81	−22dB	1	0	0	0	0	0	0	1
7B	−24dB	0	1	1	1	1	0	1	1
75	−26dB	0	1	1	1	0	1	0	1
70	−28dB	0	1	1	1	0	0	0	0
6B	−30dB	0	1	1	0	1	0	1	1
66	−32dB	0	1	1	0	0	1	1	0
62	−34dB	0	1	1	0	0	0	1	0
5D	−36dB	0	1	0	1	1	1	0	1
59	−38dB	0	1	0	1	1	0	0	1
55	−40dB	0	1	0	1	0	1	0	1
51	−42dB	0	1	0	1	0	0	0	1
4D	−44dB	0	1	0	0	1	1	0	1
4A	−46dB	0	1	0	0	1	0	1	0
47	−48dB	0	1	0	0	0	1	1	1
43	−50dB	0	1	0	0	0	0	1	1
40	−52dB	0	1	0	0	0	0	0	0
3D	−54dB	0	0	1	1	1	1	0	1
3A	−56dB	0	0	1	1	1	0	1	0
37	−58dB	0	0	1	1	0	1	1	1
34	−60dB	0	0	1	1	0	1	0	0
32	−62dB	0	0	1	1	0	0	1	0

Hex display	Volume gain	V_8 (MSB)	V_7	V_6	V_5	V_4	V_3	V_2	V_1 (LSB)
2F	−64dB	0	0	1	0	1	1	1	1
2D	−66dB	0	0	1	0	1	1	0	1
2B	−68dB	0	0	1	0	1	0	1	1
28	−70dB	0	0	1	0	1	0	0	0
26	−72dB	0	0	1	0	0	1	1	0
24	−74dB	0	0	1	0	0	1	0	0
23	−76dB	0	0	1	0	0	0	1	1
21	−78dB	0	0	1	0	0	0	0	1
1F	−80dB	0	0	0	1	1	1	1	1
1E	−82dB	0	0	0	1	1	1	1	0
1C	−84dB	0	0	0	1	1	1	0	0
00	−∞	0	0	0	0	0	0	0	0

Note: The values given in this table are for reference only. Be sure to check them carefully in actual use.

Bass and treble settings (reference values)

Treble data

Setting data MSB				LSB	Treble gain (dB)	Hex display
0	0	0	0	0	−15	00
0	0	1	0	0	−14	04
0	0	1	1	0	−12	06
0	1	0	0	0	−10	08
0	1	0	0	1	−8	09
0	1	0	1	0	−6	0A
0	1	0	1	1	−4	0B
0	1	1	0	0	−2	0C
0	1	1	1	1	±0	0F
1	0	1	0	0	+2	14
1	0	1	0	1	+4	15
1	0	1	1	0	+6	16
1	0	1	1	1	+8	17
1	1	0	0	0	+10	18
1	1	0	1	0	+12	1A
1	1	1	0	0	+14	1C
1	1	1	1	1	+15	1F

Bass data

Setting data MSB				LSB	Treble gain (dB)	Hex display
0	0	0	0	0	−15	00
0	0	1	0	1	−14	05
0	0	1	1	1	−12	07
0	1	0	0	1	−10	09
0	1	0	1	0	−8	0A
0	1	0	1	1	−6	0B
0	1	1	0	0	−4	0C
0	1	1	0	1	−2	0D
0	1	1	1	1	±0	0F
1	0	0	1	1	+2	13
1	0	1	0	0	+4	14
1	0	1	0	1	+6	15
1	0	1	1	0	+8	16
1	0	1	1	1	+10	17
1	1	0	0	1	+12	19
1	1	0	1	1	+14	1B
1	1	1	1	1	+15	1F

Note: 1.The gain values given in the bass data setting table above are for when the filter constants are set so that the peak or bottom values in the frequency characteristic graph become the maximum or minimum gain values.
2.The values given in this table are for reference only. Be sure to check them carefully in actual use.

●Application example

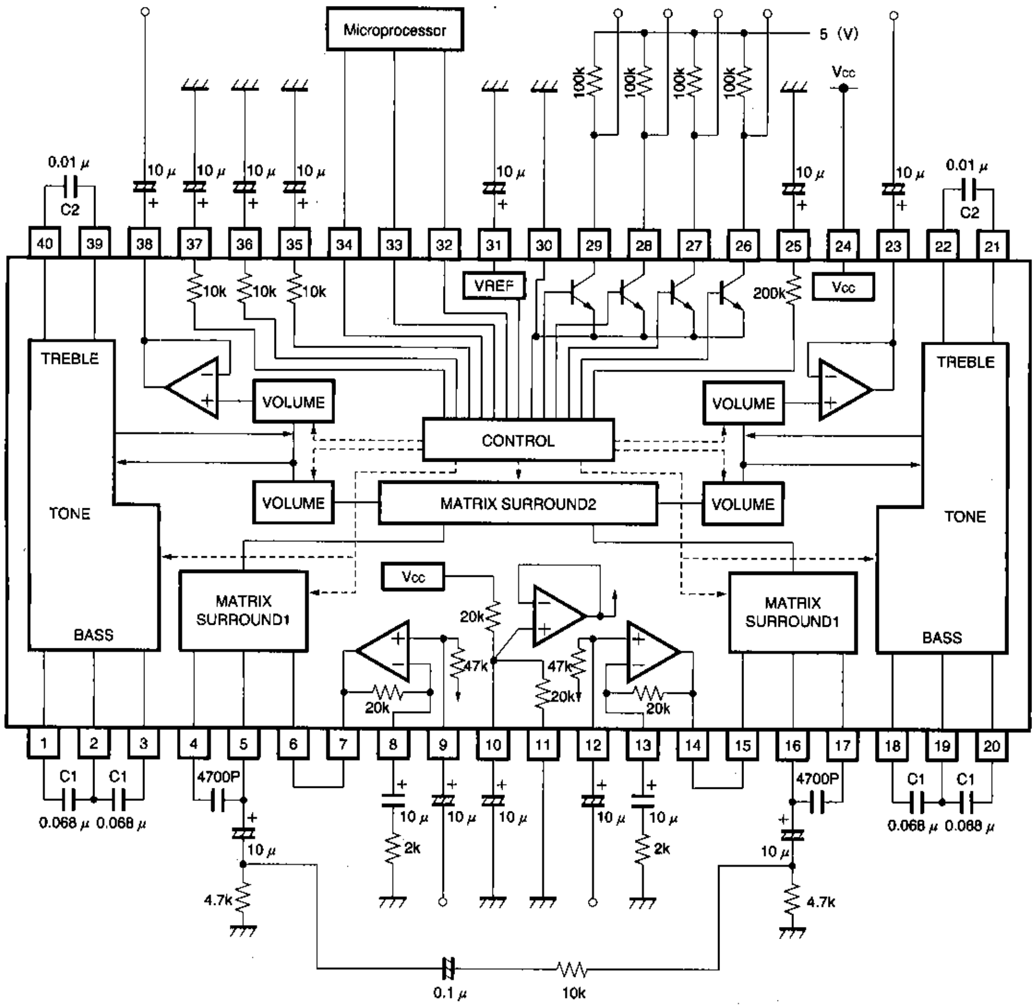
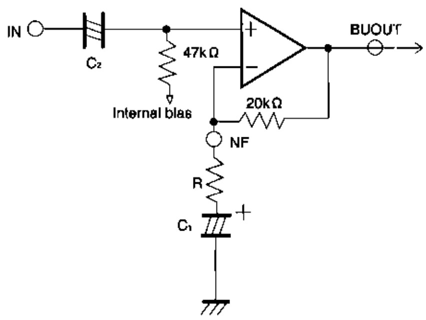


Fig. 4

● External components

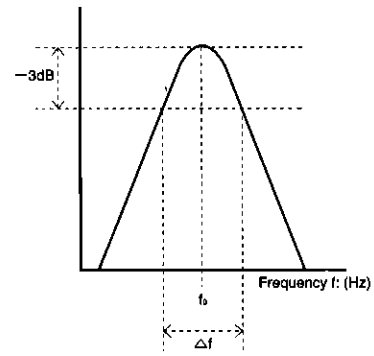
(1) Input buffer



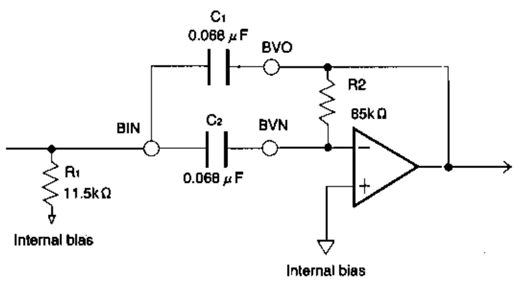
- The input impedance is 47kΩ.
- A buffer if R and C_1 are not present.
- The gain can be set by R and the 20kΩ.

$$G_{VC} = (R + 20k\Omega)/R$$

Note: Set C_2 (input coupling) and C_1 (used to set the gain) depending on the frequency band used.



(2) Bass filter



- A band-pass filter is constructed using a multiple-feedback type active filter.

F_0 can be changed using the C valve.

(Theoretical formula)

$$f_0 = \frac{1}{2\pi} \times \left(\frac{1}{R_1 R_2 C_1 C_2} \right)^{\frac{1}{2}} \qquad Q \fallingdotseq \left[\left(\frac{1}{R_2 C_1 C_2} \right)^{\frac{1}{2}} \times (C_1 + C_2) \right]^{-1}$$

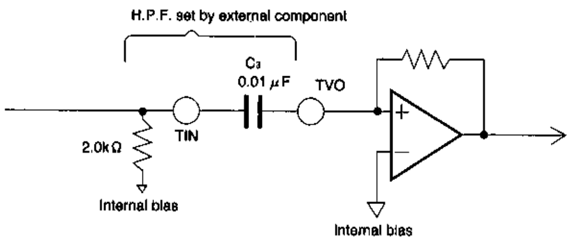
$$G = \frac{R_2}{5k} \times \left(1 + \frac{C_1}{C_2} \right)^{-1}$$

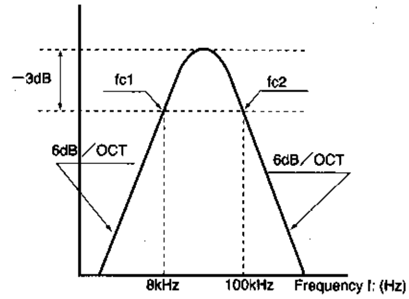
Note: The filter gain is calculated using these formulas, but the internal circuit must be added to give the total output gain.

(When $R_1 = 11.5k\Omega$, $R_2 = 85k\Omega$, and $C_1 = C_2 = C$)

$$f_0 = \frac{5.1 \times 10^{-6}}{C} \qquad Q \fallingdotseq 1.36 \quad G = 8.5$$

(3) Treble filter





- The bypass filter cutoff frequency (fc1) can be altered by changing the value of the external capacitor C_3.

$$fc1 = \frac{1}{2\pi \times C_3 \times 2k}$$

The recommended value for fc1 is about 8kHz.

- The bandwidth of the internal amplifier is determined by fc2 (about 100kHz).

The tone control provides gain boost or cut over a frequency range that you decide. At the peak and bottom of the frequency characteristic the boost is 15dB, and the cut is −15dB (Typ.). Take the frequency characteristic into consideration when designing the filter.

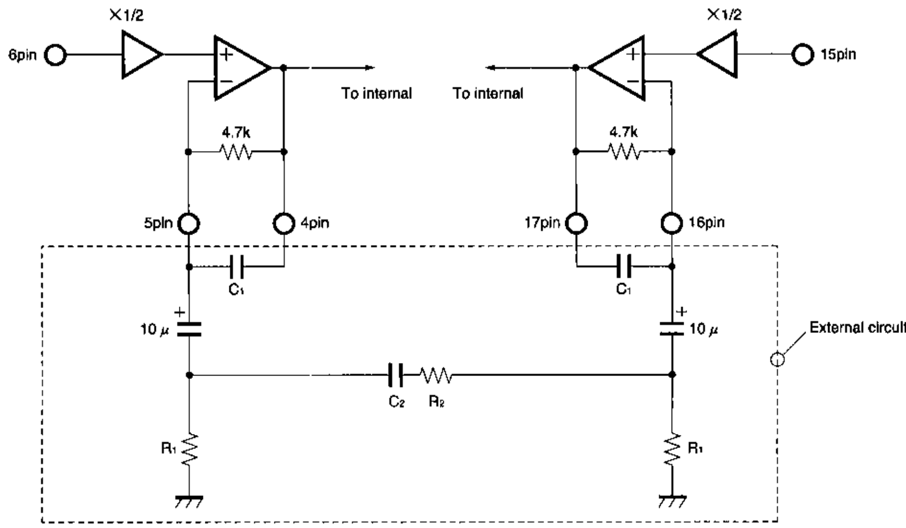
1) Amount of tone boost
When the amount of volume attenuation is large, the tone control width will change. Reference values are given below.
Note, however, that the actual values will vary due to differences in individual components.

Reference values :
Tone control width at 0dB volume attenuation : ±15.0dBTone control width at −40dB volume attenuation : ±13.5dBTone control width at −60dB volume attenuation : ±12.0dB

(4) Surround matrix

1) Surround 1

Circuit example



• Gain setting

Same-phase gain $\frac{1}{2} \times \frac{R_1 + 4.7k}{R_1}$ (1ch, 2ch)

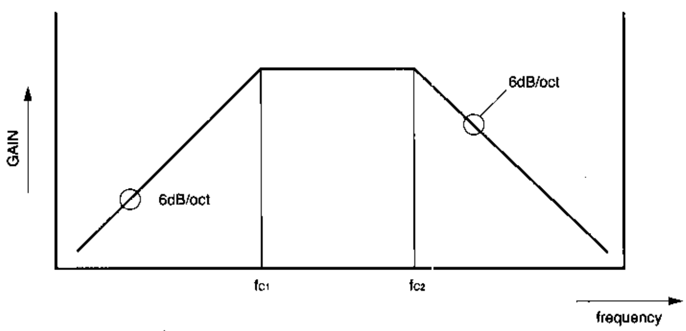
Single-phase gain $\frac{1}{2} \times \frac{(R_1 // R_2) + 4.7k}{R_1 // R_2}$ (1ch)

$\frac{1}{2} \times \frac{4.7k}{R_2}$ (2ch)

(* Channel 1 input, channel 2 AC ground)

Reverse-phase gain $\frac{1}{2} \times \frac{(R_1 // R_2)/2 + 4.7k}{(R_1 // R_2)/2}$ (1ch, 2ch)

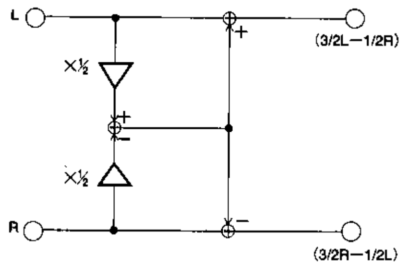
• Mixing signal frequency characteristic settings



$$f_{C1} = \frac{1}{2\pi C_2 R_2} \quad \text{(Hz)}$$

$$f_{C2} = \frac{1}{2\pi C_1 \times 4.7k} \quad \text{(Hz)}$$

2) Surround 2



◎The surround matrix construction is shown in the diagram on the left.
The gain calculations are given by the formulas in the diagram.

Same-phase gain	0dB
Reverse-phase gain	3.5dB

(However, the reverse-phase gain is input to one channel only)

●Operation notes

We guarantee the application circuit design, but recommend that you thoroughly check its characteristics and pay attention to the points of caution given below.If you change any of the external component values, check both the static and transient characteristics of the circuit, and allow sufficient margin in your selections to take into account variations in the components and ICs.

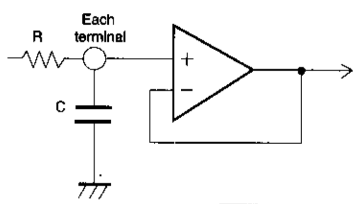
(1) Supply voltage range

The basic circuit functions are guaranteed to operate if the circuit is operated within the recommended temperature and supply voltage ranges. Please confirm the values of the circuit constants, voltage setting, and temperature in actual use.

(2) Step switching noise

The VC (pin 37), TC (pin 36), BC (pin 35), and SC (pin 25) terminals have components connected to them in the application example circuit. The values of these components may need to be changed depending on the signal level setting and PCB pattern. Investigate carefully before deciding on the values of the various circuit constants.

The equivalent circuit for these terminals is given below (an integrator circuit is set at the first stage to slow the variation).



	R value (kΩ)
VC, BC, TC	10
SC	200

(3) Volume and tone level settings

This specification sheet gives reference values for the amount of attenuation and gain with respect to the serial control data.

The internal D/A convertor is an R-2R circuit, and data exists for the places where continuous variation does not occur between data.

Use this when fine setting is required. The setting limits are up to 8 bits for volume (256 steps) and 5 bits (32 steps) for tone.

(4) Digital/analog separation

The digital and analog power supplies and grounds are completely separate. The digital circuits are supplied from a stable reference source that is on the chip (VREF (pin 31)). For this reason, there is no need to worry about timing shifts, or interference due to digital noise.

(5) Output ports

Ports 1 to 4 (pins 26 to 29), are reset when the power is applied. The reset state continues until the next serial data is input.

Note: The CK, DATA and LATCH line data must be held low up until the next data is input after power is applied.

• Do not apply more than 15V to the output ports.

(6) DC control

An internal impedance of 10kΩ is seen from the VC (pin 37), TC (pin 36), and BC (pin 35) terminals, and 200kΩ is seen from the SC (pin 25) terminal, so with regard to DC control, we recommend direct control with the voltage source.

When using variable volume, take the impedance into consideration when making the setting.

Note: The DC control voltage range is 0V to V_{REF}.
Do not apply voltages above V_{REF} to the terminals.

●Electrical characteristic curves

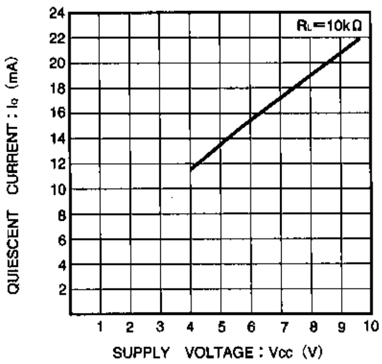


Fig. 5 Quiescent current vs. supply voltage

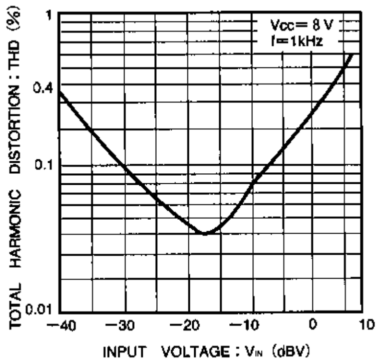


Fig. 6 Total harmonic distortion vs. input voltage

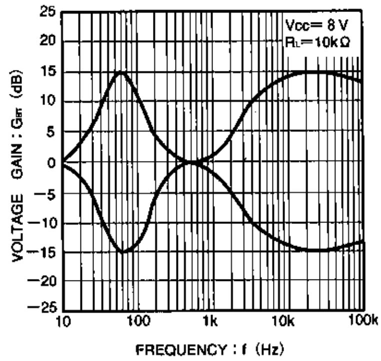
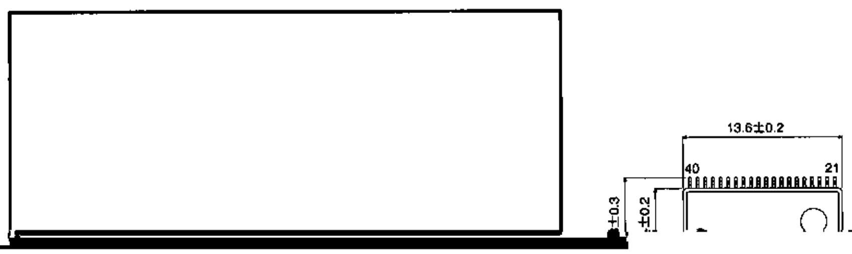


Fig. 7 Output gain vs. frequency

●External dimensions (Unit: mm)



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Audio sound controller
BH3864F

The BH3864F has been developed for use in mini-component stereo systems. Switching is done using a resistor ladder to suppress DC offset at switching. Two-line serial control is available, and external three-line serial control is also possible. The package is a compact 24-pin SOP.

●Applications

Mini- and micro-component stereo systems, CD radio cassette players and TVs.

●Features

1) Volume, tone, and dynamic bass boost control possible by a serial link to a microprocessor.
2) Left and right channel volume can be controlled independently.
3) Resistor-ladder type volume control uses BiCMOS process for low distortion and noise.
4) Dynamic bass and linked ALC are provided on chip.

●Absolute maximum ratings (Ta = 25℃)

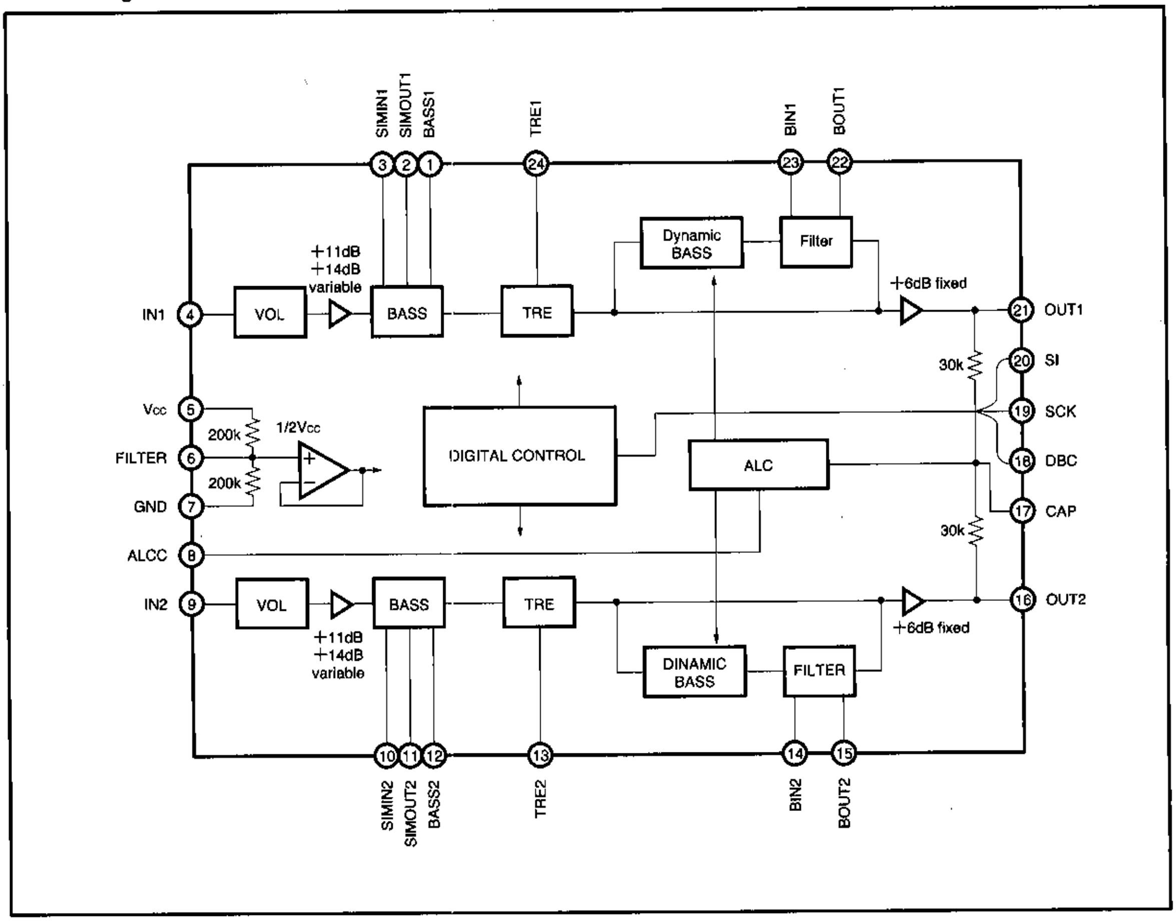
Parameter	Symbol	Limits	Unit
Applied voltage	V_{CC}	−0.3~10.0	V
Power dissipation	Pd	550 *	mW
Operating temperature	Topr	−40~+85	℃
Storage temperature	Tstg	−55~+125	℃

* Reduced by 5.5mW for each increase in Ta of 1°C over 25°C when mounted on a 50mm x 50mm x 1.6mm board.

●Recommended operating conditions (Ta = 25℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{CC}	7.0	9.0	9.5	V

●Block diagram



●Pin descriptions

Pin No.	Symbol	Function
1	BASS1	Channel 1 bass filter setting terminal
2	SIMOUT1	Channel 1 bass filter setting terminal
3	SIMIN1	Channel 1 bass filter setting terminal
4	IN1	Channel 1 signal input terminal
5	Vcc	Power supply terminal
6	FILTER	Filter terminal
7	GND	Ground terminal
8	ALCC	ALC attack and release time setting terminal
9	IN2	Channel 2 signal input terminal
10	SIMIN2	Channel 2 bass filter setting terminal
11	SIMOUT2	Channel 2 bass filter setting terminal
12	BASS2	Channel 2 bass filter setting terminal
13	TRE2	Channel 2 treble filter setting terminal
14	BIN2	Channel 2 dynamic bass filter setting terminal
15	BOUT2	Channel 2 dynamic bass filter setting terminal
16	OUT2	Channel 2 signal output terminal
17	CAP	ALC trap frequency setting terminal
18	DBC	Dynamic bass switch retiming setting terminal
19	SCK	Serial clock input terminal
20	SI	Serial data input terminal
21	OUT1	Channel 1 signal output terminal
22	BOUT1	Channel 1 dynamic bass filter setting terminal
23	BIN1	Channel 1 dynamic bass filter setting terminal
24	TRE1	Channel 1 treble filter setting terminal

●Electrical characteristics (Unless otherwise specified, Ta = 25℃, V_{CC} = 9V, f = 1kHz, Rg = 600Ω, R_L = 10kΩ, BW = 20Hz to 20kHz, VIN = 200mVrms, volume = 0dB, tone = 0dB, dynamic bass = 0dB, and gain select = 14dB)

Parameter	Symbol	Min.	Typ.	Max.	Unit	Conditions
Quiescent current	I_Q	—	11	22	mA	V_{IN}=0Vrms
Maximum input voltage	V_{IM}	2.2	2.5	—	Vrms	ATT = −30dB, output THD = 1%
Maximum output voltage	V_{OM}	2.2	2.5	—	Vrms	Output THD = 1%, BW = 400Hz to 30kHz
Voltage gain	G_V	18	20	22	dB	
Total harmonic distortion	THD	—	0.01	0.05	%	V_O=1Vrms
Output noise conversion voltage	V_{NO}	—	25	40	μVrms	Rg=0Ω *
Residual noise voltage	V_{MNO}	—	25	40	μVrms	Volume = −infinity *
Crosstalk	CT	—	94	60	dB	
Channel balance	CB	−1.5	0	1.5	dB	CH1 standard measuring
Input impedance	R_{IN1}	7.5	9.4	11.3	kΩ	
Input impedance	R_{IN2}	10.6	13.3	16.0	kΩ	ATT=−3dB (−45dB)
Ripple rejection	RR	—	−40	−35	dB	f_{RR}=100Hz, V_{RRIN}=100mVrms
Volume step resolution	AT_{STEP}	—	1	—	dB	
Maximum volume attenuation	AT_{MIN}	−80	−94	—	dB	
Volume step error	AT_{ERR}	—	0	—	dB	
Bass control range	VB	±8.5	±10.5	±12.5	dB	
Treble control range	VT	±8	±10	±12	dB	
Tone step resolution	V_{STEP}	—	2	—	dB	
Dynamic bass control range	VDB	18	20	22	dB	f=60Hz, V_{IN}=10mVrms
Dynamic bass step resolution	VD_{STEP}	—	5	—	dB	
Current from logic terminals when "L"	I_D	—	1	10	μA	

* Measured using a Matsushita Comminucation Industry VP-9690A (average value detector, effective value display) IHF-A filter.
Operating specifications: same phase for the input and output signals.
◎Circuit not designed for radiation resistance.

Sound control
Audio accessory components

● Measurement circuit

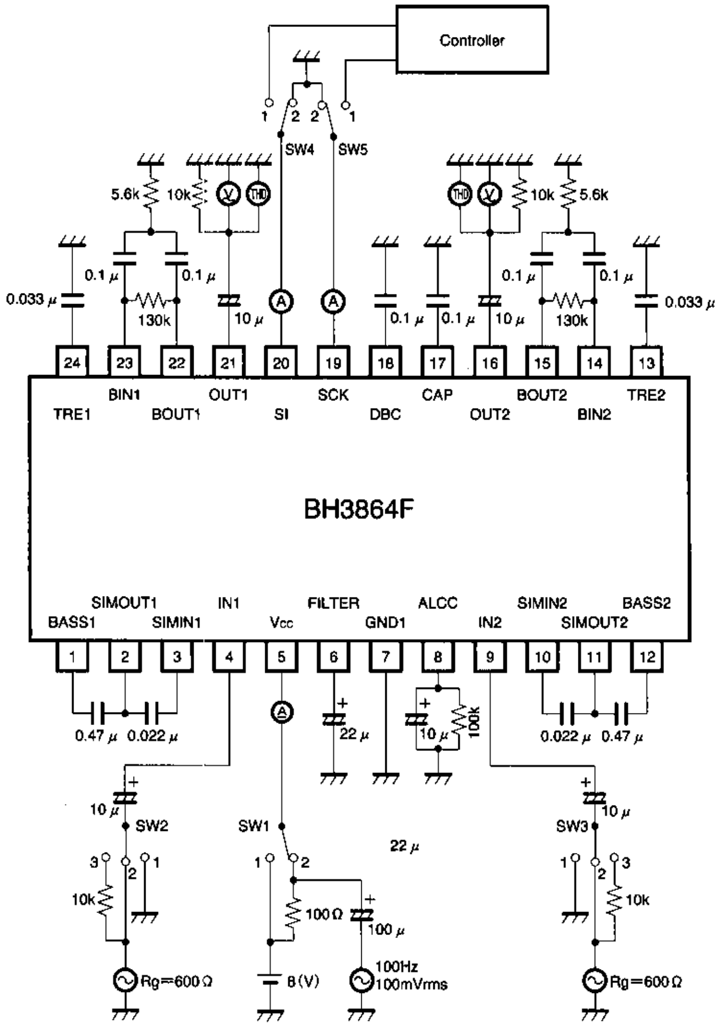


Fig. 1

●Circuit operation

(1) About the data format

As shown in Fig. 2, there are 28 bits of data. There are two chip select bits, but multiple units cannot be controlled by a single controller.

MSB D0 — 28bit total — D27 LSB

Gain	Dynamic bass	Treble	Bass	CH2 volume A	CH2 volume B	CH1 volume A	CH1 volume B	Chip select
1bit	3bit	4bit	4bit	5bit	2bit	5bit	2bit	2bit

(2) SCK and SI signal timing

The SCK and SI signal timing are shown in Fig. 3. The SI signal potential level decision is made internally. A Schmitt trigger circuit on the chip is used to provide noise margin. The internal circuits are bipolar, so take care with regard to source current.

The data is read in on the rising edge of the clock.

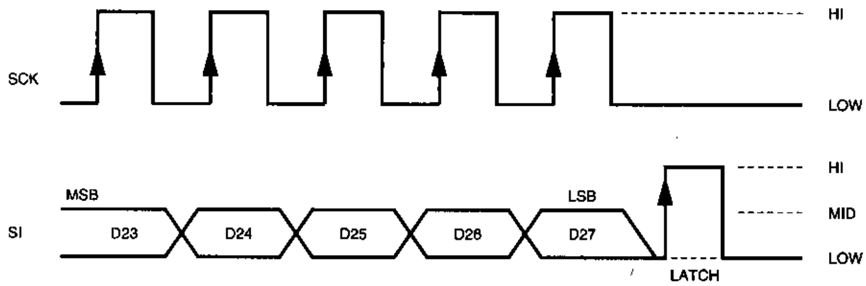
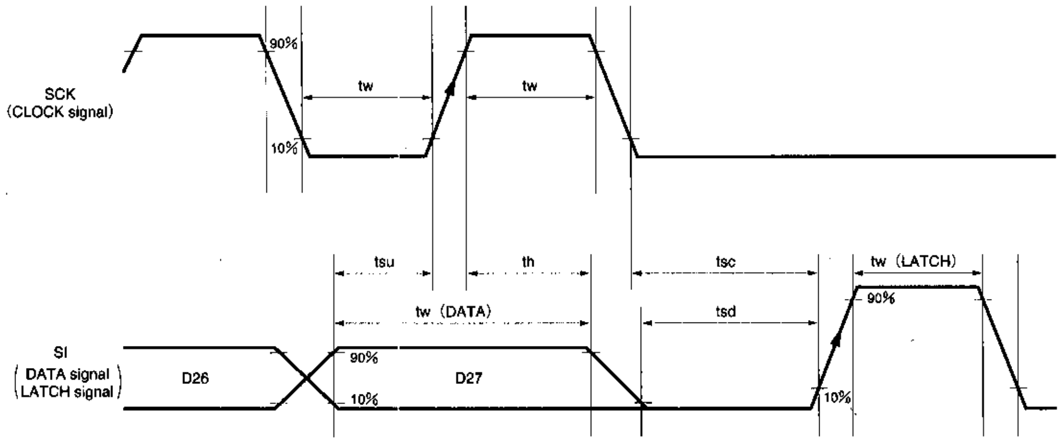


Fig. 3

(3) Timing chart
The timing chart is shown in Fig. 4.

Serial data timing



* When SI is "H", the DATA signal is forced "L" internally, and data is not accepted.

Fig. 4

Timing chart constants (Ta = 25℃, V_{CC} = 9V)

Parameter	Symbol	Min.	Typ.	Max.	Unit
H input voltage	V_{IH}	4.0	5.0	6.0	V
M input voltage	V_{IM}	2.0	2.5	3.0	V
L input voltage	V_{IL}	−0.3	0	1.0	V
Minimum clock width	tw	2.0	—	—	μS
Minimum data width	tw (DATA)	4.0	—	—	μS
Minimum latch width	tw (LATCH)	2.0	—	—	μS
Setup time (DATA to CLK)	tsu	1.0	—	—	μS
Hold time (CLK to DATA)	th	1.0	—	—	μS
Setup time (CLK to LATCH)	tsc	1.0	—	—	μS
Setup time (DATA to LATCH)	tsd	1.0	—	—	μS

(4) Data table
The transmission data is given in the table below.

VOLUME ATTENUATION
Volume A

GAIN	CH1	D19	D20	D21	D22	D23
	CH2	D12	D13	D14	D15	D16
0dB		0	0	0	0	0
−2dB		0	0	0	0	1
−4dB		0	0	0	1	0
−6dB		0	0	0	1	1
−8dB		0	0	1	0	0
−10dB		0	0	1	0	1
−12dB		0	0	1	1	0
−14dB		0	0	1	1	1
−16dB		0	1	0	0	0
−18dB		0	1	0	0	1
−20dB		0	1	0	1	0
−22dB		0	1	0	1	1
−24dB		0	1	1	0	0
−26dB		0	1	1	0	1
−28dB		0	1	1	1	0
−30dB		0	1	1	1	1
−32dB		1	0	0	0	0
−34dB		1	0	0	0	1
−36dB		1	0	0	1	0
−38dB		1	0	0	1	1
−40dB		1	0	1	0	0
−42dB		1	0	1	0	1
−46dB		1	0	1	1	0
−50dB		1	0	1	1	1
−54dB		1	1	0	0	0
−58dB		1	1	0	0	1
−62dB		1	1	0	1	0
−66dB		1	1	0	1	1
−70dB		1	1	1	0	0
−74dB		1	1	1	0	1
−78dB		1	1	1	1	0
−∞		1	1	1	1	1

Volume B

GAIN	CH1	D24	D25
	CH2	D17	D18
0dB		0	0
−1dB		0	1
−2dB		1	0
−3dB		1	1

(The −2dB and −3dB settings operate when the setting is −42dB or lower.)

By combining volume A and B, it is possible to provide control from 0dB to −81dB in 1dB steps.

BASS AND TREBLE (TONE CONTROL)

GAIN	BASS			
	D4	D5	D6	D7
+10.5dB	1	1	0	1
+8dB	1	1	0	0
+6dB	1	0	1	1
+4dB	1	0	1	0
+2dB	1	0	0	1
0dB	1	0	0	0
0dB	0	0	0	0
−2dB	0	0	0	1
−4dB	0	0	1	0
−6dB	0	0	1	1
−8dB	0	1	0	0
−10.5dB	0	1	0	1

GAIN	TREBLE			
	D8	D9	D10	D11
+10dB	1	1	0	1
+8dB	1	1	0	0
+6dB	1	0	1	1
+4dB	1	0	1	0
+2dB	1	0	0	1
0dB	1	0	0	0
0dB	0	0	0	0
−2dB	0	0	0	1
−4dB	0	0	1	0
−6dB	0	0	1	1
−8dB	0	1	0	0
−10dB	0	1	0	1

Note: Gain is the name given to the transfer data. Depending on the values of the external components, the specified gain may not be output.

DYNAMIC BASS BOOST

GAIN	D1	D2	D3
0dB	0	0	0
5dB	0	0	1
10dB	0	1	0
15dB	0	1	1
20dB	1	0	0

Note: Gain is the name given to the transfer data. Depending on the values of the external components, the specified gain may not be output.

CHIP SELECT

D26	D27
1	1

Note: For all other data, the previous data are maintained.

GAIN SELECT

INPUT AMP GAIN	D0
11dB	1
14dB	0

●Application example

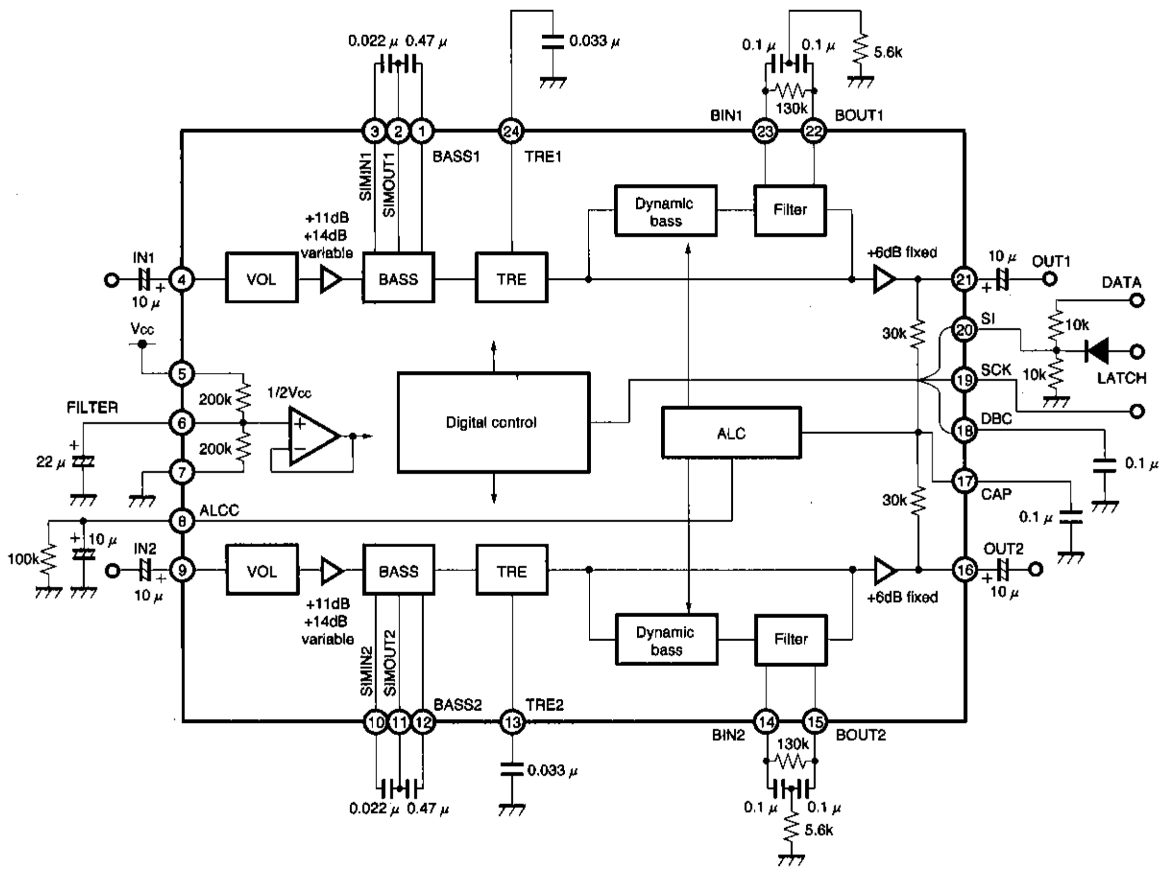


Fig. 5

Sound control

Audio accessory components

●External components

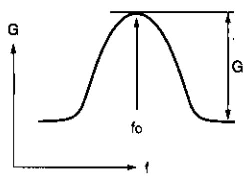
(1) Tone control filter constants

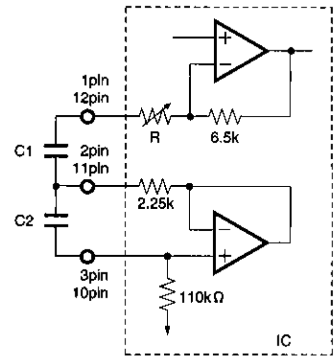
Bass region

$$f_o = \frac{1}{2\pi\sqrt{110k \times 2.25k \times C_1 \times C_2}} \quad (Hz)$$

$$Q = \sqrt{\frac{110k \times C_2}{2.25k \times C_1}}$$

$$G = 20\log\left(\frac{2.25k + R + 6.5k}{2.25k + R}\right) \quad (dB)$$





Equivalent circuit diagram

Note: The variables C_1, C_2 and R in the formulas are the components in the equivalent circuit.

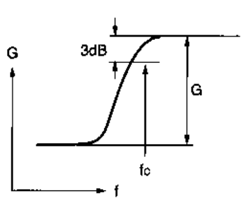
Bass control data	R(kΩ)
±10.5dB	0
±8dB	1.95
±6dB	4.5
±4dB	9.0
±2dB	23.0
±0dB	∞

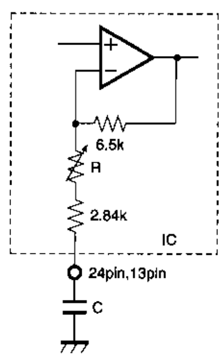
The actual gain may vary somewhat.

Treble

$$f_c = \frac{1}{2\pi \times 2.84k \times C} \quad (Hz)$$

$$G = 20\log\left(\frac{2.84k + R + 6.5k}{2.84k + R}\right) \quad (dB)$$





Equivalent circuit diagram

Note: The variables C and R in the formulas are the components in the equivalent circuit. The internally-fixed settings for R are as follows.

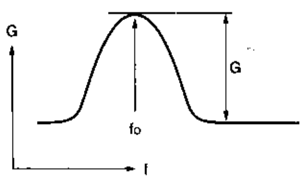
Treble control data	R(kΩ)
±10dB	0
±8dB	1.34
±6dB	3.6
±4dB	8.22
±2dB	22
±0dB	∞

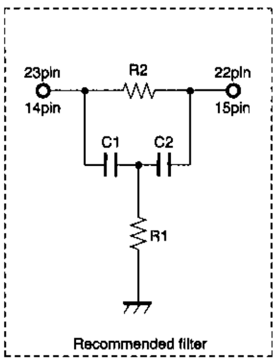
The actual gain may vary somewhat.

(2) Dynamic bass filter constants

$$fo = \frac{1}{2\pi\sqrt{R_1 \times R_2 \times C_1 \times C_2}} \quad \text{(Hz)}$$

$$G = 20\log\left(1 + \frac{55g}{1+54t}\right) \quad \text{(dB)}$$





Note: R_1, R_2, C_1 and C_2 are the recommended values for the filter. g is fixed internally (see the table below).

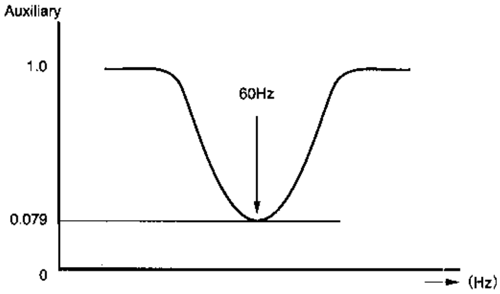
Dynamic bass control data	g
20dB	1
15dB	0.5
10dB	0.25
5dB	0.085
0dB	0

Constants in formulas

The variable "t" in the formula depends on the filter. For the recommended filter, the relationship is as follows.

$$t = 1 - \frac{1}{1+\frac{R_1}{R_2}\left(1+\frac{C_1}{C_2}\right)}$$

For the application circuit example, t = 0.079.



Recommended filter characteristics

The actual gain may vary slightly.

(3) ALC (automatic level control)

1) Trap frequency T_f

The trap frequency T_f is obtained from the following formula.

$$T_f = \frac{1}{2\pi \times 10k \times C} \quad (Hz)$$

Note: C is the value of the capacitance between pin 17 and GND.

2) Trap level

The signal level at which the ALC begins to operate depends on V_{CC}. The relationship is given below (T_L = trap level).

$$T_L = \frac{V_{CC}}{9} \quad (Vrms) \quad \text{(same phase input)}$$

Note: It is possible to switch ALC off permanently by connecting pin 8 to GND.

●Operation notes

We guarantee the application circuit design, but recommend that you thoroughly check its characteristics and pay attention to the points of caution given below. If you change any of the external component values, check both the static and transient characteristics of the circuit, and allow sufficient margin in your selections to take into account variations in the components and ICs.

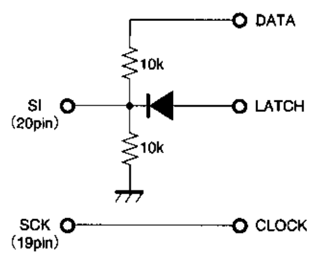
(1) Supply voltage range

The basic circuit functions are guaranteed to operate if the circuit is operated within the recommended temperature and supply voltage ranges. Please confirm the values of the circuit constants, voltage setting, and temperature in actual use.

(2) Serial control

High-frequency digital signals are input to the SI and SCK pins. Ensure that the wiring is done in such a way as to prevent interference with the analog signal lines. If noise is measured during step switching, connect resistors of about 2kΩ in series with and close to the microprocessor outputs.

If you plan to use the conventional three-line serial method, we recommend that you used the following circuit (as shown in the application example circuit).



The diode should have as low a V_F as possible.
Adjust the value of the resistors depending on the drive capacity of the microprocessor.

(3) Dynamic bass step switching noise
A capacitor is shown connected to DBC (pin 18) in the application circuit example. The value of this component varies with the signal level setting and PCB pattern. Investigate carefully before deciding on the values of the various circuit constants.

● Electrical characteristic curves

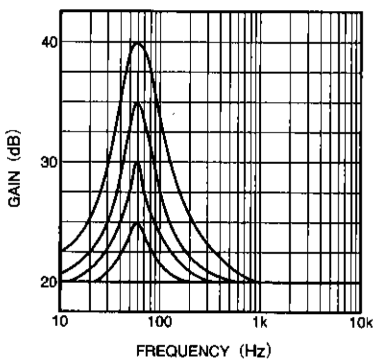


Fig. 6 Dynamic bass frequency characteristics

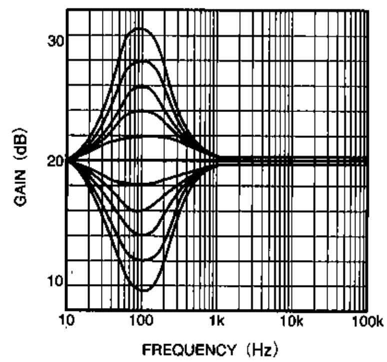


Fig. 7 Bass frequency characteristics

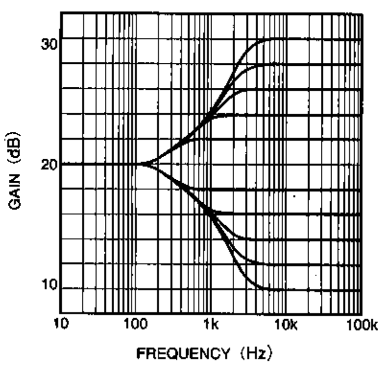
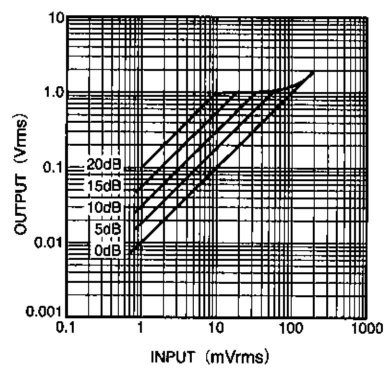


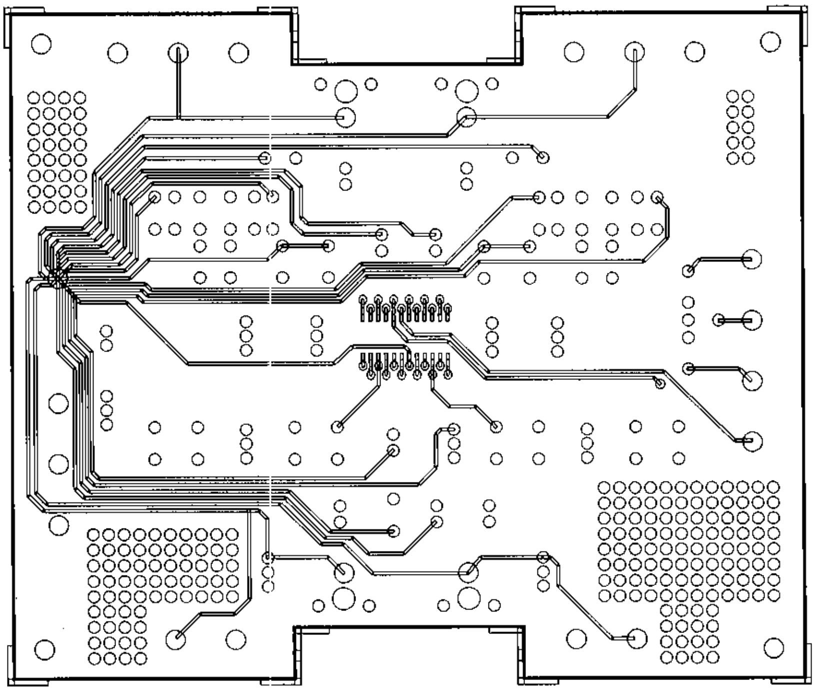
Fig. 8 Treble frequency characteristics

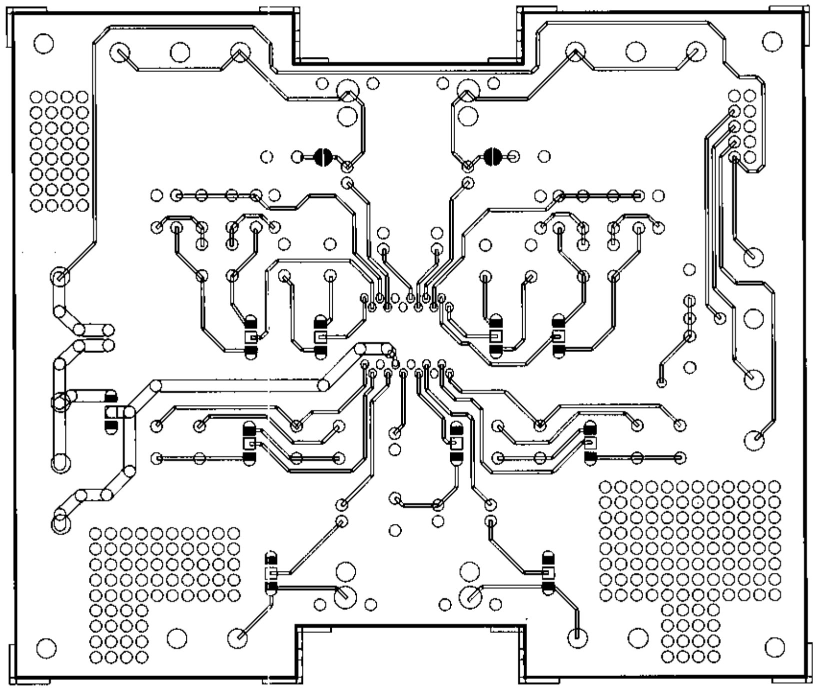


(the gain is the amount of dynamic bass boost)

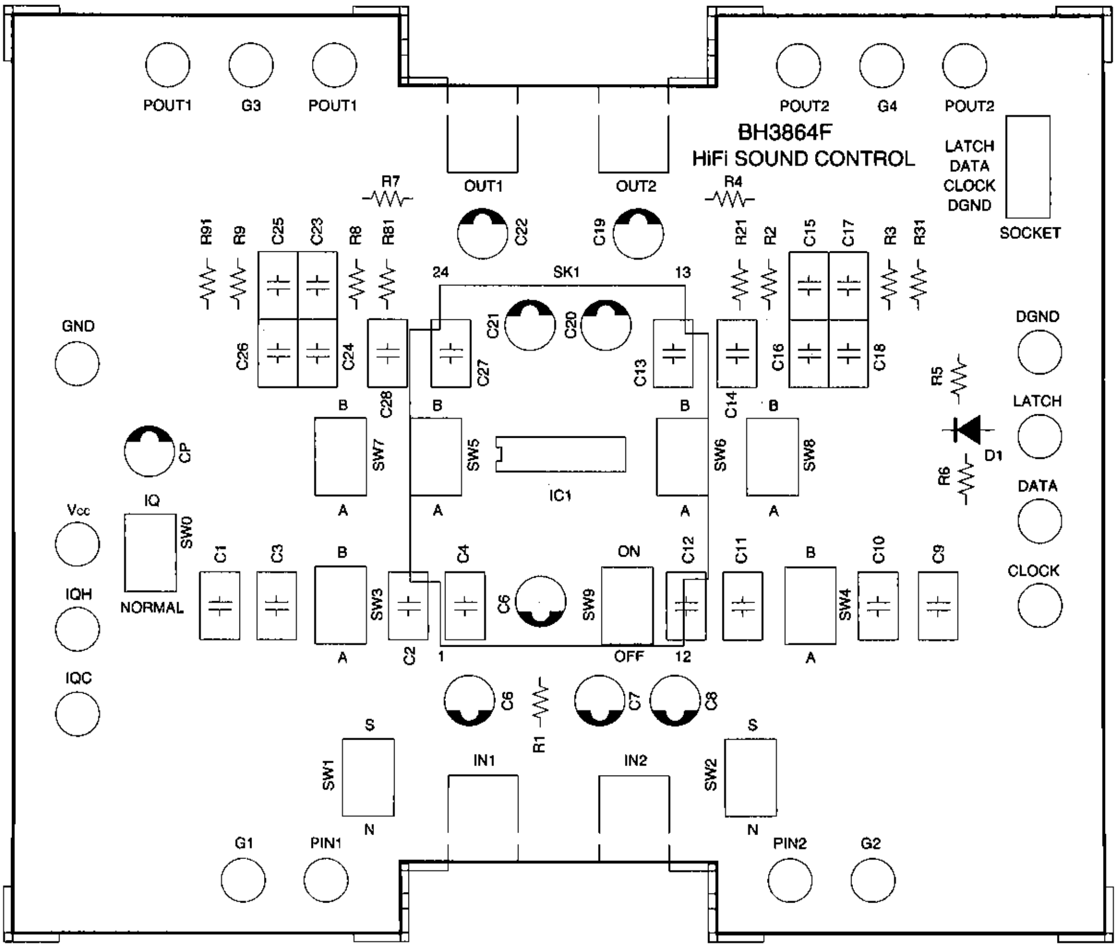
Fig. 9 ALC characteristics

●Application example circuit PCB

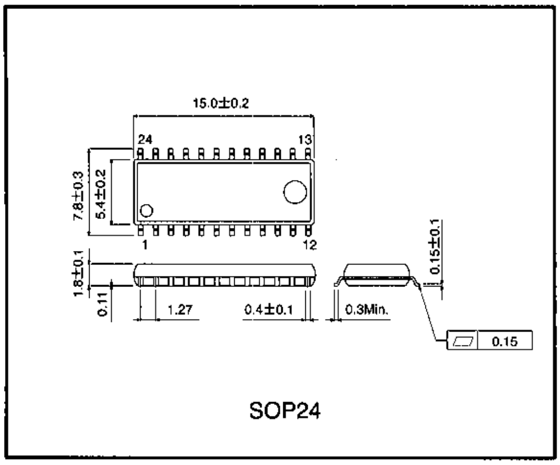




●Application example circuit component layout



●External dimensions (Unit: mm)



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