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<i>Yonemaru</i>	<i>17. JUN '97</i>		REPRESENTATIVE DIVISION ☐ ELECTRONIC COMPONENTS DIV. ☐ OPTICAL DEVICE DIV. ☐ PHOTO VOLTAICS DIV.

DEVICE SPECIFICATION FOR
 Single conversion tuner for DVB, PAL-G/B
 with Down converter

MODEL NO. CASD19E35

☐ CUSTOMER'S APPROVAL

DATE

BY

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TOYOMI YONEMARU

DEPARTMENT GENERAL MANAGER
 ENGINEERINGCOMPONENTS DIVISION3
 ELECTRONIC COMPONENTS DIVISION
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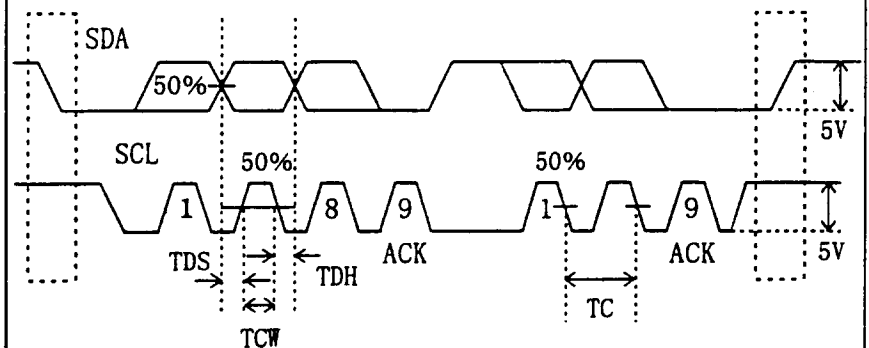
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1	General																														
1-1	Application	This tuner is intended to use in cable modem.																													
1-2	Receiving frequency range	VHF LOW 47to 145MHz, VHF HIGH 145 to 416MHz, UHF 416 to 866MHz																													
1-3	Input level	-13dBmV to 15dBmV																													
1-4	Nominal input impedance	75 Ω Unbalance																													
1-5	Nominal output impedance	Unbalance																													
1-6	Intermediate frequency	IF1 36.15MHz, IF2 6.875MHz																													
1-7	3dB Band width	8MHz (typ.)																													
1-8	Channel selection system	Frequency synthesizer (I2C-bus)																													
1-9	PLL step size	62.5kHz (PLL internal reference : 62.5kHz)																													
1-10	X'tal reference frequency	4.0MHz																													
1-11	Operating voltage	<table><tr><th>Terminal</th><th>Description</th><th>Voltage (V)</th><th>Condition</th></tr><tr><td>B1</td><td>Main supply</td><td>9.0$\pm$0.45</td><td></td></tr><tr><td>B2</td><td>Main supply</td><td>5.0$\pm$0.25</td><td></td></tr><tr><td>BT</td><td>Tuning supply</td><td>30.0$\pm$1.5</td><td></td></tr><tr><td>AGC</td><td>Gain control</td><td>0~5</td><td>5V to max gain</td></tr><tr><td rowspan="2">PLL control</td><td>VH(=1)</td><td>3~5.5</td><td rowspan="2">SCL, SDA</td></tr><tr><td>VL(=1)</td><td>1.5 max</td></tr></table>	Terminal	Description	Voltage (V)	Condition	B1	Main supply	9.0 $\pm$ 0.45		B2	Main supply	5.0 $\pm$ 0.25		BT	Tuning supply	30.0 $\pm$ 1.5		AGC	Gain control	0~5	5V to max gain	PLL control	VH(=1)	3~5.5	SCL, SDA	VL(=1)	1.5 max			
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1-12	Breakdown voltage	<table><tr><td>B1</td><td>Main supply</td><td>11.0</td><td></td></tr><tr><td>B2</td><td>Main supply</td><td>6.0</td><td></td></tr><tr><td>BT</td><td>Tuning supply</td><td>32.0</td><td></td></tr><tr><td>AGC</td><td>Gain control</td><td>6.0</td><td></td></tr><tr><td>PLL control</td><td></td><td>5.5</td><td>SCL, SDA</td></tr></table>	B1	Main supply	11.0		B2	Main supply	6.0		BT	Tuning supply	32.0		AGC	Gain control	6.0		PLL control		5.5	SCL, SDA									
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1-13	Temperature and humidity	<table><tr><th>Temperature</th><th>Humidity</th><th></th><th>Condition</th></tr><tr><td>-15°C~70°C</td><td>90%RH max.</td><td>Storage</td><td></td></tr><tr><td>-10°C~50°C</td><td>85%RH max.</td><td>Operating</td><td></td></tr></table>	Temperature	Humidity		Condition	-15 $^{\circ}$ C~70 $^{\circ}$ C	90%RH max.	Storage		-10 $^{\circ}$ C~50 $^{\circ}$ C	85%RH max.	Operating																		
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1-14	Circuit block diagram	Figure 1																													
2	Mechanical characteristics																														
2-1	Appearance	No appreciable defects in appearance																													
2-2	Shape and dimensions	As per attached outline drawing. (Figure 2)																													
2-3	Mounting on PC board	Must insert easily into PC board tuner holes as shown in the attached drawing. (Figure 2)																													

2-4 表 1	Terminal strength 1) IF output and Power supply terminal. 2) ANT terminal	Tensile strength Terminal No. 2~10 : 29.4N min. (3kgf) Forses required for insertion and extraction. 1. Force required for initial insertion :68.6N max. (Senter contact : ϕ 2.36mm $\pm$ 0.076mm) (Outer contact : ϕ 9.525mm $\pm$ 0.05) 2. Force required for initial extraction : 9.8N min. (Senter contact : ϕ 2.36mm $\pm$ 0.076mm) (Outer contact : ϕ 9.5257mm $\pm$ 0.05)				
3	Test condition					
3-1	Supply voltage	B1	:	9.0V $\pm$ 0.1V		
		B2	:	5.0V $\pm$ 0.1V		
		BT	:	30.0V $\pm$ 0.1V		
		AGC	:	5.0V $\pm$ 0.1V		
3-2	Ambient temperature	25 $^{\circ}$ C $\pm$ 2 $^{\circ}$ C				
3-3	Ambient humidity	55%RH $\pm$ 10%RH				
3-4	Receiving channel and input level (CM, IM, CTB)	Receiving channel		Input level	Modulation	
		STD103(47MHz~862MHz)		+15dBmV	CW or 15.75kHz, 100%AM	
		Set AGC voltage to keep IF(36.15MHz)output at +30dBmV				
4	Electrical characteristics	Electrical characteristics involve the spread of values guaranteed within the specified test condition. (Refer to 3-1~3-3)				
4-1	Current consumption	Min.	Typ.	Max.	Unit	Condition
	B1 (9.0V)		25		mA	
	B2 (5.0V)		145		mA	
	BT (30.0V)		1.5		mA	
	AGC (5V)			1	μ A	
4-2	Conversion gain	70			dB	
4-3	Noise figure			10	dB	
4-4	AGC range	25			dB	AGC=0.5V
4-5	Return loss	7			dB	From 47MHz to 862MHz
	Input terminal					
4-6	IF output bandpass response			3	dB	6.875MHz $\pm$ 2.75MHz
4-7	Group delay flatness			100	ns	6.875MHz $\pm$ 2.75MHz
4-8	Cross modulation			-50	dBc	Refer to 3-4

		MODEL	CASD19E35	P	3																																				
4-9	Intermodulation	Min.	Typ.	Max.	Unit	Condition																																			
	1) 2'nd/3rd order beat			-50	dBc	Refer to 3-4																																			
	2) Composite triple beat			-50	dBc	Refer to 3-4																																			
4-10	Spurious signals at input terminal			-35	dBmV	54 to (and including) 300																																			
	Local leakage			-35	dBmV	300 to (and including) 450																																			
				-20	dBmV	450 to (and including) 1000																																			
4-11	Image rejection			-40	dB																																				
4-12	IF rejection			-60	dB																																				
4-13	Local phase noise		-87	-85	dBc/Hz	10kHz offset																																			
			-105	-95	dBc/Hz	100kHz offset																																			
4-14	LO frequency accuracy			± 50	kHz	Over temperature of -10 to 50°C																																			
4-15	PLL setting time			100	msec	*																																			
* Setting time is measured after reference & local frequency set up data is transmitted. (f0±1kHz)																																									
5	Environmental tests	After the test(5-1~5-3) no mechanical looseness shall be present, the conversion gain and noise figure shall stay within ±3dB of the original.																																							
5-1	On-load test	1) In a high temperature, high humidity environment. (40°C, 90%RH for 500hours)																																							
5-2	Vibration test	2) In a high temperature environment. (60°C for 500hours) In 3 different directions, scanning time with 1min, for 2hours with peak to peak amplitude of 1.5min at a rate of 10Hz~55Hz.																																							
5-3	Impact test	In 686m/S2(70G) on 6 planes, 3 times each.																																							
6	Others																																								
6-1	Terminal affinity to solder	Sample terminals to be soldered shall be dipped in methanol (as per JIS-K-1501) into which rosin (as per JIS-K-5902) is dissolved to a concentration of 7~10% for about 5s, then dipped in a solder bath containing molten solder (JIS-Z-3282H, 63A) maintained at 230°C±5°C for 3±0.5s. After removal from the solder bath, each sample terminal tested shall show solder adhering over 90 % of the submerged portions along the entire circumference.																																							
6-2	PLL data format	<table><tr><td>Bus inputs SCL, SDA</td><td>Symbol</td><td>Min</td><td>Typ</td><td>Max</td><td>Units</td><td>Con.</td></tr><tr><td>HIGH input voltage</td><td>VH</td><td>3</td><td></td><td>5.5</td><td>V</td><td></td></tr><tr><td>LOW input voltage</td><td>VL</td><td></td><td></td><td>1.5</td><td>V</td><td></td></tr><tr><td>HIGH input current</td><td>IH</td><td></td><td></td><td>10</td><td>μA</td><td>VH=5 V</td></tr><tr><td>LOW input current</td><td>IL</td><td>-20</td><td></td><td></td><td>μA</td><td>VL=0 V</td></tr></table>					Bus inputs SCL, SDA	Symbol	Min	Typ	Max	Units	Con.	HIGH input voltage	VH	3		5.5	V		LOW input voltage	VL			1.5	V		HIGH input current	IH			10	μA	VH=5 V	LOW input current	IL	-20			μA	VL=0 V
Bus inputs SCL, SDA	Symbol	Min	Typ	Max	Units	Con.																																			
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HIGH input current	IH			10	μA	VH=5 V																																			
LOW input current	IL	-20			μA	VL=0 V																																			

	Symbol	Min	Typ	Max	Units	Conditions
S DATA set up time	TDS	0.1			μs	
S DATA hold time	TDH	0			μs	
S CLOCK pulse width	TCW	0.6			μs	
S CLOCK frequency	TC	2.5			μs	



	MSB	bit6	bit5	bit4	bit3	bit2	bit1	LSB	Ack
Address Byte	1	1	0	0	0	MA1	MA0	0	Ack
Prog.Divider Byte1	0	n14	n13	n12	n11	n10	n9	n8	Ack
Prog.Divider Byte2	n7	n6	n5	n4	n3	n2	n1	n0	Ack
Control Byte1	1	5I	0	0	1	1	1	0	Ack
Control Byte2	U/V	×	×	×	×	P2	P1	P0	Ack

Ports P0, P1, P2 :

High Open-collector output is active

Low Open-collector output is inactive

Bandswitch switch V/U :

High switch to OSC/MIX UHF

Low Switch to OSC/MIX VHF

Pump current 5I:

High switch to high current

Table 1 : Band Selection

	U/V	P2	P1	P0
UHF	1	0	0	1
VHF high	0	0	1	0
VHF low	0	1	0	0

6-3	Channel condition	Table2:Address Selection <table border="1"> <thead> <tr> <th>Voltage at CAS</th><th>MA1</th><th>MA0</th></tr> </thead> <tbody> <tr> <td>(0...0.1)*B2</td><td>0</td><td>0</td></tr> <tr> <td>open circuit</td><td>1</td><td>0</td></tr> <tr> <td>(0.4...0.6)*B2</td><td>0</td><td>1</td></tr> <tr> <td>(0.9...1)*B2</td><td>1</td><td>1</td></tr> </tbody> </table> Divider ratio: $fvco = N \times 62.5\text{kHz}$ $N = 16384 \times n14 + 8192 \times n13 + 4096 \times n12 + 2048 \times n11$ $+ 1024 \times n10 + 512 \times n9 + 256 \times n8 + 128 \times n7 + 64 \times n6$ $+ 32 \times n5 + 16 \times n4 + 8 \times n3 + 4 \times n2 + 2 \times n1 + n0$ $fvco$: Local frequency $fosc$: 4MHz (X' tal reference frequency) R : 64 (Reference divider) VHF low 83.15MHz~179.15MHz ($fvco$) VHF high 186.15MHz~446.15MHz UHF 454.15MHz~902.15MHz	Voltage at CAS	MA1	MA0	(0...0.1)*B2	0	0	open circuit	1	0	(0.4...0.6)*B2	0	1	(0.9...1)*B2	1	1
Voltage at CAS	MA1	MA0															
(0...0.1)*B2	0	0															
open circuit	1	0															
(0.4...0.6)*B2	0	1															
(0.9...1)*B2	1	1															

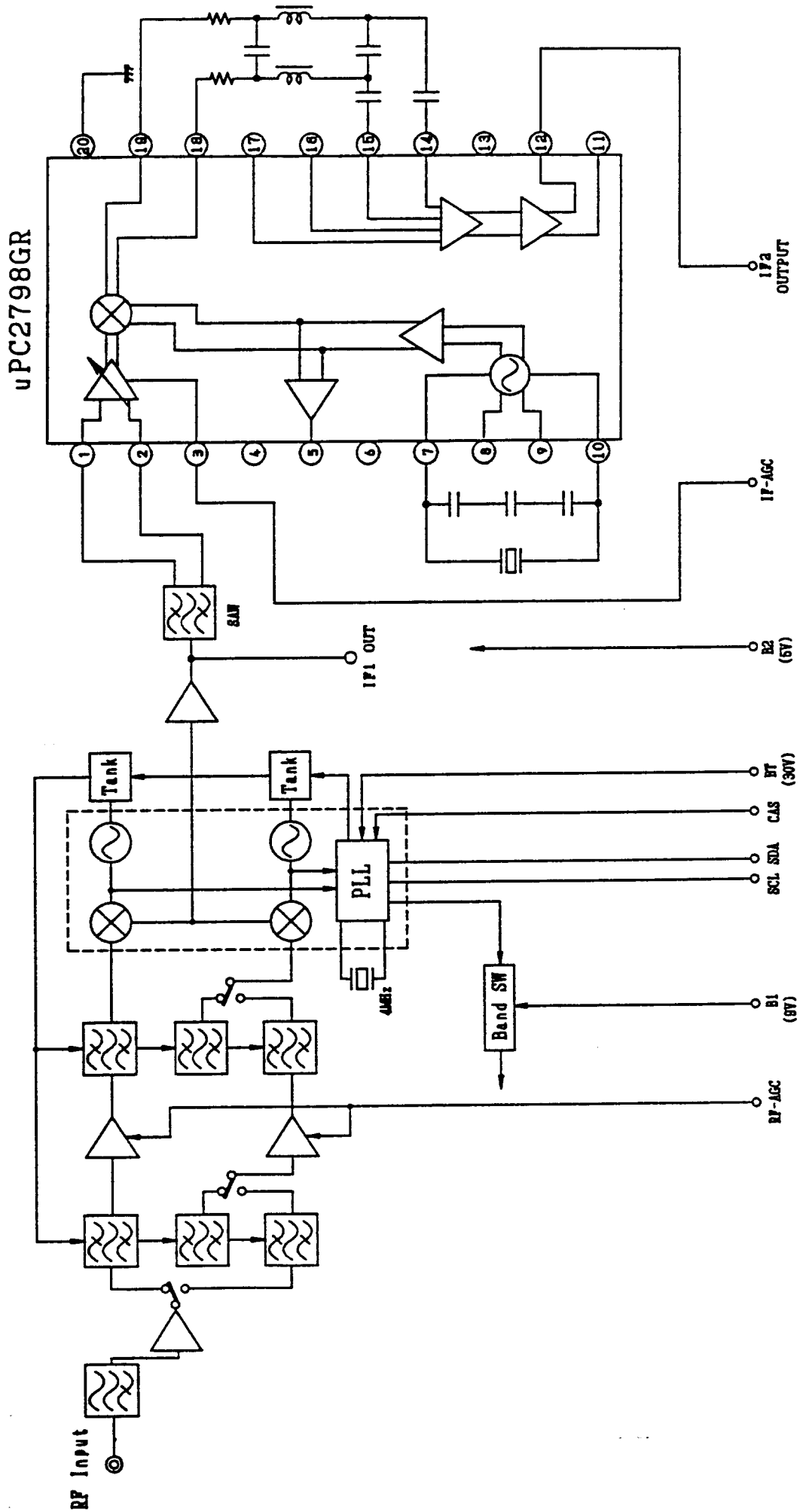


Figure 1 Block Diagram

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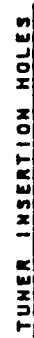


Figure 2. Outline drawing

No.	1	2	3	4	5	6	7	8	9	10	11
NAME	ANT IN	RF- AGC	B1 (9V)	B2 (5V)	SDA	SCL	CAS	BT (30V)	IF1	IF- AGC	IF2 OUT