CHAPTER 2

Switched Mode Power Supplies

2.1 Using Power Semiconductors in Switched Mode Topologies (including transistor selection guides)

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Using Power Semiconductors in Switched Mode Topologies

2.1.1 An Introduction to Switched Mode Power Supply Topologies

For many years the world of power supply design has seen a gradual movement away from the use of linear power supplies to the more practical switched mode power supply (S.M.P.S.). The linear power supply contains a mains transformer and a dissipative series regulator. This means the supply has extremely large and heavy 50/60 Hz transformers, and also very poor power conversion efficiencies, both serious drawbacks. Typical efficiencies of 30% are standard for a linear. This compares with efficiencies of between 70 and 80%, currently available using S.M.P.S. designs.

Furthermore, by employing high switching frequencies, the sizes of the power transformer and associated filtering components in the S.M.P.S. are dramatically reduced in comparison to the linear. For example, an S.M.P.S. operating at 20kHz produces a 4 times reduction in component size, and this increases to about 8 times at 100kHz and above. This means an S.M.P.S. design can produce very compact and lightweight supplies. This is now an essential requirement for the majority of electronic systems. The supply must slot into an ever shrinking space left for it by electronic system designers.

Outline

At the heart of the converter is the high frequency inverter section, where the input supply is chopped at very high frequencies (20 to 200kHz using present technologies) then filtered and smoothed to produce dc outputs. The circuit configuration which determines how the power is transferred is called the TOPOLOGY of the S.M.P.S., and is an extremely important part of the design process. The topology consists of an arrangement of transformer, inductors, capacitors and power semiconductors (bipolar or MOSFET power transistors and power rectifiers).

Presently, there is a very wide choice of topologies available, each one having its own particular advantages and disadvantages, making it suitable for specific power supply applications. Basic operation, advantages, drawbacks and most common areas of use for the most common topologies are discussed in the following sections. A selection guide to the Philips range of power semiconductors (including bipolars, MOSFETs and rectifiers) suitable for use in S.M.P.S. applications is given at the end of each section.

(1) Basic switched mode supply circuit.

An S.M.P.S. can be a fairly complicated circuit, as can be seen from the block diagram shown in Fig. 1. (This configuration assumes a 50/60Hz mains input supply is used.) The ac supply is first rectified, and then filtered by the input reservoir capacitor to produce a rough dc input supply. This level can fluctuate widely due to variations in the mains. In addition the capacitance on the input has to be fairly large to hold up the supply in case of a severe droop in the mains. (The S.M.P.S. can also be configured to operate from any suitable dc input, in this case the supply is called a dc to dc converter.)

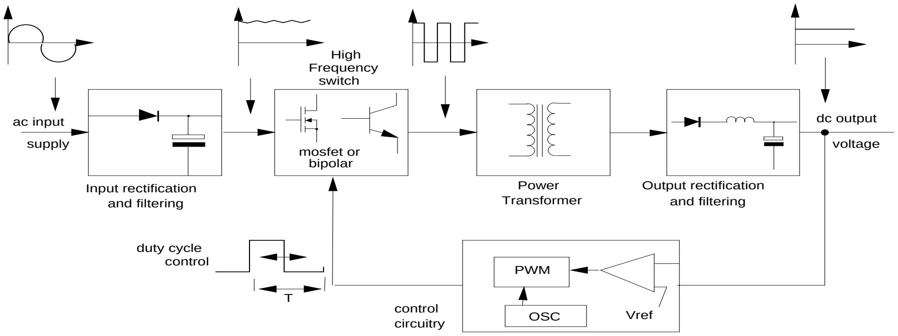


Fig. 1. Basic switched mode power supply block diagram.

The unregulated dc is fed directly to the central block of the supply, the high frequency power switching section. Fast switching power semiconductor devices such as MOSFETs and Bipolars are driven on and off, and switch the input voltage across the primary of the power transformer. The drive pulses are normally fixed frequency (20 to 200kHz) and variable duty cycle. Hence, a voltage pulse train of suitable magnitude and duty ratio appears on the transformer secondaries. This voltage pulse train is appropriately rectified, and then smoothed by the output filter, which is either a capacitor or capacitor / inductor arrangement, depending upon the topology used. This transfer of power has to be carried out with the lowest losses possible, to maintain efficiency. Thus, optimum design of the passive and magnetic components, and selection of the correct power semiconductors is critical.

Regulation of the output to provide a stabilised dc supply is carried out by the control / feedback block. Generally, most S.M.P.S. systems operate on a fixed frequency pulse width modulation basis, where the duration of the on time of the drive to the power switch is varied on a cycle by cycle basis. This compensates for changes in the input supply and output load. The output voltage is compared to an accurate reference supply, and the error voltage produced by the comparator is used by dedicated control logic to terminate the drive pulse to the main power switch/switches at the correct instance. Correctly designed, this will provide a very stable dc output supply.

It is essential that delays in the control loop are kept to a minimum, otherwise stability problems would occur. Hence, very high speed components must be selected for the loop. In transformer-coupled supplies, in order to keep the isolation barrier intact, some type of electronic isolation is required in the feedback. This is usually achieved by using a small pulse transformer or an opto-isolator, hence adding to the component count.

In most applications, the S.M.P.S. topology contains a power transformer. This provides isolation, voltage scaling through the turns ratio, and the ability to provide multiple outputs. However, there are non-isolated topologies (without transformers) such as the buck and the boost converters, where the power processing is achieved by inductive energy transfer alone. All of the more complex arrangements are based on these non-isolated types.

(2) Non-Isolated converters.

The majority of the topologies used in today's converters are all derived from the following three non-isolated versions called the buck, the boost and the buck-boost. These are the simplest configurations possible, and have the lowest component count, requiring only one inductor, capacitor, transistor and diode to generate their single output. If isolation between the input and output is required, a transformer must be included before the converter.

(a) The Buck converter.

The forward converter family which includes the push-pull and bridge types, are all based on the buck converter, shown in Fig. 2. Its operation is straightforward. When switch TR1 is turned on, the input voltage is applied to inductor L1 and power is delivered to the output. Inductor current also builds up according to Faraday's law shown below:-

$$V = L\frac{dI}{dt}$$

When the switch is turned off, the voltage across the inductor reverses and freewheel diode D1 becomes forward biased. This allows the energy stored in the inductor to be delivered to the output. This continuous current is then smoothed by output capacitor Co. Typical buck waveforms are also shown in Fig. 2.

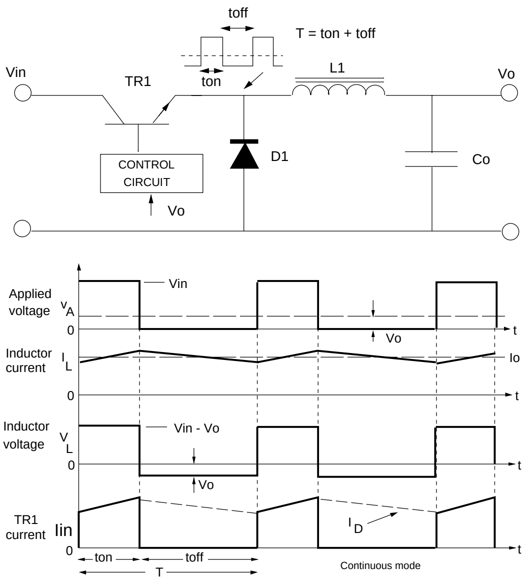


Fig. 2 Buck Regulator (step-down).

The LC filter has an averaging effect on the applied pulsating input, producing a smooth dc output voltage and current, with very small ripple components superimposed. The average voltage/sec across the inductor over a complete switching cycle must equal zero in the steady state. (The same applies to all of the regulators that will be discussed.)

Neglecting circuit losses, the average voltage at the input side of the inductor is $V_{in}D$, while V_o is the output side voltage. Thus, in the steady state, for the average voltage across the inductor to be zero, the basic dc equation of the buck is simply:-

$$\frac{V_o}{V_i} = D$$

D is the transistor switch duty cycle, defined as the conduction time divided by one switching period, usually expressed in the form shown below:-

$$D = \frac{t_{on}}{T}; \quad where \quad T = t_{on} + t_{off}$$

Thus, the buck is a stepdown type, where the output voltage is always lower than the input. (Since D never reaches one.) Output voltage regulation is provided by varying the duty cycle of the switch. The LC arrangement provides very effective filtering of the inductor current. Hence, the buck and its derivatives all have very low output ripple characteristics. The buck is normally always operated in continuous mode (inductor current never falls to zero) where peak currents are lower, and the smoothing capacitor requirements are smaller. There are no major control problems with the continuous mode buck.

(b) The Boost Converter.

Operation of another fundamental regulator, the boost, shown in Fig. 3 is more complex than the buck. When the switch is on, diode D1 is reverse biased, and V_{in} is applied across inductor, L1. Current builds up in the inductor to a peak value, either from zero current in a discontinuous mode, or an initial value in the continuous mode. When the switch turns off, the voltage across L1 reverses, causing the voltage at the diode to rise above the input voltage. The diode then conducts the energy stored in the inductor, plus energy direct from the supply to the smoothing capacitor and load. Hence, V_o is always greater than V_{in}, making this a stepup converter. For continuous mode operation, the boost dc equation is obtained by a similar process as for the buck, and is given below:-

$$\frac{V_o}{V_i} = \frac{1}{1-D}$$

Again, the output only depends upon the input and duty cycle. Thus, by controlling the duty cycle, output regulation is achieved.

From the boost waveforms shown in Fig. 3, it is clear that the current supplied to the output smoothing capacitor from the converter is the diode current, which will always be discontinuous. This means that the output capacitor must be large, with a low equivalent series resistance (e.s.r) to produce a relatively acceptable output ripple. This is in contrast to the buck output capacitor requirements described earlier. On the other hand, the boost input current is the continuous inductor current, and this provides low input ripple characteristics. The boost is very popular for capacitive load applications such as photo-flashers and battery chargers. Furthermore, the continuous input current makes the boost a popular choice as a pre-regulator, placed before the main converter. The main functions being to regulate the input supply, and to greatly improve the line power factor. This requirement has become very important in recent years, in a concerted effort to improve the power factor of the mains supplies.

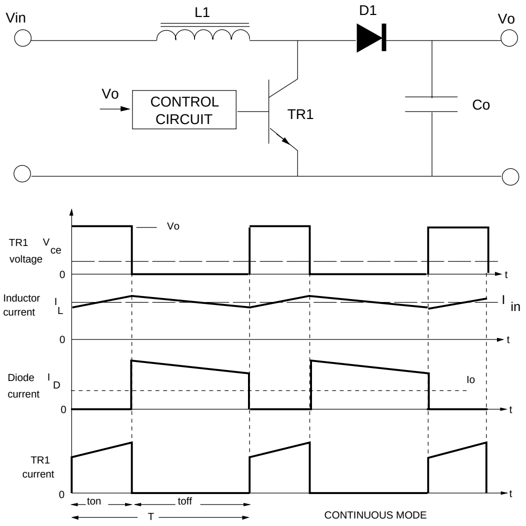


Fig. 3 Boost Regulator (step-up).

If the boost is used in discontinuous mode, the peak transistor and diode currents will be higher, and the output capacitor will need to be doubled in size to achieve the same output ripple as in continuous mode. Furthermore, in discontinuous operation, the output voltage also becomes dependent on the load, resulting in poorer load regulation.

Unfortunately, there are major control and regulation problems with the boost when operated in continuous mode. The pseudo LC filter effectively causes a complex second order characteristic in the small signal (control) response. In the discontinuous mode, the energy in the inductor at the start of each cycle is zero. This removes the inductance from the small signal response, leaving only the output capacitance effect. This produces a much simpler response, which is far easier to compensate and control.

(c) The Buck-Boost Regulator (Non-isolated Flyback).

The very popular flyback converter (see section 5(a)) is not actually derived solely from the boost. The flyback only delivers stored inductor energy during the switch off-time. The boost, however, also delivers energy from the input. The flyback is actually based on a combined topology of the previous two, called the buck-boost or non isolated flyback regulator. This topology is shown in Fig. 4.

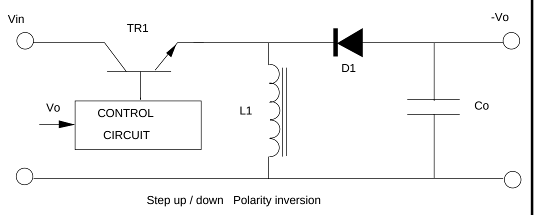


Fig. 4 Buck-Boost (Flyback) Regulator.

When the switch is on, the diode is reverse biased and the input is connected across the inductor, which stores energy as previously explained. At turn-off, the inductor voltage reverses and the stored energy is then passed to the capacitor and load through the forward biased rectifier diode.

The waveforms are similar to the boost except that the transistor switch now has to support the sum of Vin and Vo across it. Clearly, both the input and output currents must be discontinuous. There is also a polarity inversion, the output voltage generated is negative with respect to the input. Close inspection reveals that the continuous mode dc transfer function is as shown below:-

$$\frac{V_o}{V_i} = \frac{D}{1-D}$$

Observation shows that the value of the switch duty ratio, D can be selected such that the output voltage can either be higher or lower than the input voltage. This gives the converter the flexibility to either step up or step down the supply.

This regulator also suffers from the same continuous mode control problems as the boost, and discontinuous mode is usually favoured.

Since both input and output currents are pulsating, low ripple levels are very difficult to achieve using the buck-boost. Very large output filter capacitors are needed, typically up to 8 times that of a buck regulator.
The transistor switch also needs to be able to conduct the high peak current, as well as supporting the higher summed voltage. The flyback regulator (buck-boost) topology places the most stress on the transistor. The rectifier diode also has to carry high peak currents and so the r.m.s conduction losses will be higher than those of the buck.

(3) Transformers in S.M.P.S. converters.

The non-isolated versions have very limited use, such as dc-dc regulators only capable of producing a single output. The output range is also limited by the input and duty cycle. The addition of a transformer removes most of these constraints and provides a converter with the following advantages:-

1) Input to output isolation is provided. This is normally always necessary for 220 / 110 V mains applications, where a degree of safety is provided for the outputs.

2) The transformer turns ratio can be selected to provide outputs widely different from the input; non-isolated versions are limited to a range of approximately 5 times. By selecting the correct turns ratio, the duty cycle of the converter can also be optimised and the peak currents flowing minimised. The polarity of each output is also selectable, dependent upon the polarity of the secondary w.r.t the primary.

3) Multiple outputs are very easily obtained, simply by adding more secondary windings to the transformer.

There are some disadvantages with transformers, such as their additional size, weight and power loss. The generation of voltage spikes due to leakage inductance may also be a problem.

The isolated converters to be covered are split into two main categories, called asymmetrical and symmetrical converters, depending upon how the transformer is operated.

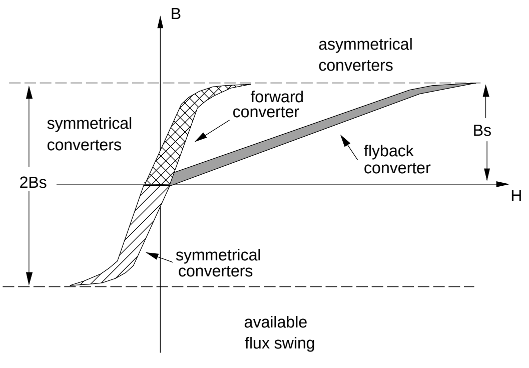


Fig. 5 Comparative core usage of asymmetrical and symmetrical converters.

In asymmetrical converters the magnetic operating point of the transformer is always in one quadrant i.e the flux and the magnetic field never changes sign. The core has to be reset each cycle to avoid saturation, meaning that only half of the usable flux is ever exploited. This can be seen in Fig. 5, which shows the operating mode of each converter. The flyback and forward converter are both asymmetrical types. The diagram also indicates that the flyback converter is operated at a lower permeability (B/H) and lower inductance than the others. This is because the flyback transformer actually stores all of the energy before dumping into the load, hence an air gap is required to store this energy and avoid core saturation. The air gap has the effect of reducing the overall permeability of the core. All of the other converters have true transformer action and ideally store no energy, hence, no air gap is needed.

In the symmetrical converters which always require an even number of transistor switches, the full available flux swing in both quadrants of the B / H loop is used, thus utilising the core much more effectively. Symmetrical converters can therefore produce more power than their asymmetrical cousins. The 3 major symmetrical topologies used in practice are the push-pull, the half-bridge and the full bridge types.

Table 1 outlines the typical maximum output power available from each topology using present day technologies:-

Converter Topology	Typical max output power
Flyback	200W
Forward	300W
Two transistor forward / flyback	400W
Push-pull	500W
Half-Bridge	1000W
Full-Bridge	>1000W

Table 1. Converter output power range.

Many other topologies exist, but the types outlined in Table 1 are by far the most commonly used in present S.M.P.S. designs. Each is now looked at in more detail, with a selection guide for the most suitable Philips power semiconductors included.

(4) Selection of the power semiconductors.

The Power Transistor.

The two most common power semiconductors used in the S.M.P.S. are the Bipolar transistor and the power MOSFET. The Bipolar transistor is normally limited to use at frequencies up to 30kHz, due to switching loss. However, it has very low on-state losses and is a relatively cheap device, making it the most suitable for lower frequency applications. The MOSFET is selected for higher frequency operation because of its very fast switching speeds, resulting in low (frequency dependent) switching losses. The driving of the MOSFET is also far simpler and less expensive than that required for the Bipolar. However, the on-state losses of the MOSFET are far higher than the Bipolar, and they are also usually more expensive. The selection of which particular device to use is normally a compromise between the cost, and the performance required.

(i) Voltage limiting value:-

After deciding upon whether to use a Bipolar or MOSFET, the next step in deciding upon a suitable type is by the correct selection of the transistor voltage. For transformer coupled topologies, the maximum voltage developed across the device is normally at turn-off. This will be either half, full or double the magnitude of the input supply voltage, dependent upon the topology used. There may also be a significant voltage spike due to transformer leakage inductance that must be included. The transistor must safely withstand these worst case values without breaking down. Hence, for a bipolar device, a suitably high $V_{ces(max)}$ must be selected, and for a MOSFET, a suitably high $V_{BR(DSS)}$. At present 1750V is the maximum blocking voltage available for power Bipolars, and a maximum of 1000V for power MOSFETs.

The selection guides assume that a rectified 220V or 110V mains input is used. The maximum dc link voltages that will be produced for these conditions are 385V and 190V respectively. These values are the input voltage levels used to select the correct device voltage rating.

(ii) Current limiting value:-

The Bipolar device has a very low voltage drop across it during conduction, which is relatively constant within the rated current range. Hence, for maximum utilisation of a bipolar transistor, it should be run close to its I_{Csat} value. This gives a good compromise between cost, drive requirements and switching. The maximum current for a particular throughput power is calculated for each topology using simple equations. These equations are listed in the appropriate sections, and the levels obtained used to select a suitable Bipolar device.

The MOSFET device operates differently from the bipolar in that the voltage developed across it (hence, transistor dissipation) is dependent upon the current flowing and the device "on-resistance" which is variable with temperature. Hence, the optimum MOSFET for a given converter can only be chosen on the basis that the device must not exceed a certain percentage of throughput (output) power. (In this selection a 5% loss in the MOSFET was assumed). A set of equations used to estimate the correct MOSFET $R_{DS(on)}$ value for a particular power level has been derived for each topology. These equations are included in Appendix A at the end of the paper. The value of RDS(on) obtained was then used to select a suitable MOSFET device for each requirement.

NOTE! This method assumes negligible switching losses in the MOSFET. However for frequencies above 50kHz, switching losses become increasingly significant.

Rectifiers

Two types of output rectifier are specified from the Philips range. For very low output voltages below 10V it is necessary to have an extremely low rectifier forward voltage drop, V_F, in order to keep converter efficiency high. Schottky types are specified here, since they have very low V_F values (typically 0.5V). The Schottky also has negligible switching losses and can be used at very high frequencies. Unfortunately, the very low V_F of the Schottky is lost at higher reverse blocking voltages (typically above 100V) and other diode types become more suitable. This means that the Schottky is normally reserved for use on outputs up to 20V or so.

Note. A suitable guideline in selecting the correct rectifier reverse voltage is to ensure the device will block 4 to 6 times the output voltage it is used to provide (depends on topology and whether rugged devices are being used).

For higher voltage outputs the most suitable rectifier is the fast recovery epitaxial diode (FRED). This device has been optimised for use in high frequency rectification. Its characteristics include low V_F (approx. 1V) with very fast and efficient switching characteristics. The FRED has reverse voltage blocking capabilities up to 800V. They are therefore suitable for use in outputs from 10 to 200V.

The rectifier devices specified in each selection guide were chosen as having the correct voltage limiting value and high enough current handling capability for the particular output power specified. (A single output is assumed).

(5) Standard isolated topologies.

(a) The Flyback converter.

Operation

Of all the isolated converters, by far the simplest is the single-ended flyback converter shown in Fig. 6. The use of a single transistor switch means that the transformer can only be driven unipolar (asymmetrical). This results in a large core size. The flyback, which is an isolated version of the buck-boost, does not in truth contain a transformer but a coupled inductor arrangement. When the transistor is turned on, current builds up in the primary and energy is stored in the core, this energy is then released to the output circuit through the secondary when the switch is turned off. (A normal transformer such as the types used in the buck derived topologies couples the energy directly during transistor on-time, ideally storing no energy).

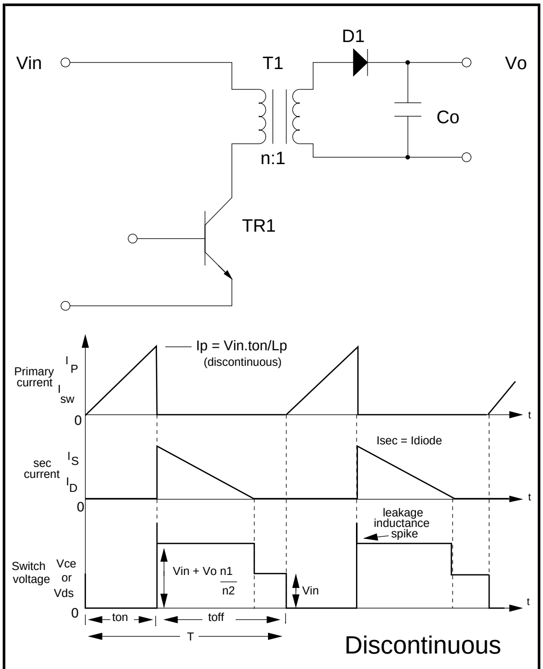


Fig. 6 Flyback converter circuit and waveforms.

The polarity of the windings is such that the output diode blocks during the transistor on time. When the transistor turns off, the secondary voltage reverses, maintaining a constant flux in the core and forcing secondary current to flow through the diode to the output load. The magnitude of the peak secondary current is the peak primary current reached at transistor turn-off reflected through the turns ratio, thus maintaining a constant Ampere-turn balance.

The fact that all of the output power of the flyback has to be stored in the core as $1/2LI^2$ energy means that the core size and cost will be much greater than in the other topologies, where only the core excitation (magnetisation) energy, which is normally small, is stored. This, in addition to the initial poor unipolar core utilisation, means that the transformer bulk is one of the major drawbacks of the flyback converter.

In order to obtain sufficiently high stored energy, the flyback primary inductance has to be significantly lower than required for a true transformer, since high peak currents are needed. This is normally achieved by gapping the core. The gap reduces the inductance, and most of the high peak energy is then stored in the gap, thus avoiding transformer saturation.

When the transistor turns off, the output voltage is back reflected through the transformer to the primary and in many cases this can be nearly as high as the supply voltage. There is also a voltage spike at turn-off due to the stored energy in the transformer leakage inductance. This means that the transistor must be capable of blocking approximately twice the supply voltage plus the leakage spike. Hence, for a 220V ac application where the dc link can be up to 385V, the transistor voltage limiting value must lie between 800 and 1000V.

Using a 1000V Bipolar transistor such as the BUT11A or BUW13A allows a switching frequency of 30kHz to be used at output powers up to 200Watts.

MOSFETs with 800V and 1000V limiting values can also be used, such as the BUK456-800A which can supply 100W at switching frequencies anywhere up to 300kHz. Although the MOSFET can be switched much faster and has lower switching losses , it does suffer from significant on-state losses, especially in the higher voltage devices when compared to the bipolars. An outline of suitable transistors and output rectifiers for different input and power levels using the flyback is given in Table 2.

One way of removing the transformer leakage voltage spike is to add a clamp winding as shown in Fig. 8. This allows the leakage energy to be returned to the input instead of stressing the transistor. The diode is always placed at the high voltage end so that the clamp winding capacitance does not interfere with the transistor turn-on current spike, which would happen if the diode was connected to ground. This clamp is optional and depends on the designer's particular requirements.

Advantages.

The action of the flyback means that the secondary inductance is in series with the output diode when current is delivered to the load; i.e driven from a current source. This means that no filter inductor is needed in the output circuit. Hence, each output requires only one diode and output filter capacitor. This means the flyback is the ideal choice for generating low cost, multiple output supplies. The cross regulation obtained using multiple outputs is also very good (load changes on one output have little effect on the others) because of the absence of the output choke, which degrades this dynamic performance.

The flyback is also ideally suited for generating high voltage outputs. If a buck type LC filter was used to generate a high voltage, a very large inductance value would be needed to reduce the ripple current levels sufficiently to achieve the continuous mode operation required. This restriction does not apply to the flyback, since it does not require an output inductance for successful operation.

Disadvantages.

From the flyback waveforms in Fig. 6 it is clear that the output capacitor is only supplied during the transistor off time. This means that the capacitor has to smooth a pulsating output current which has higher peak values than the continuous output current that would be produced in a forward converter, for example. In order to achieve low output ripple, very large output capacitors are needed, with very low equivalent series resistance (e.s.r). It can be shown that at the same frequency, an LC filter is approximately 8 times more effective at ripple reduction than a capacitor alone. Hence, flybacks have inherently much higher output ripples than other topologies. This, together with the higher peak currents, large capacitors and transformers, limits the flyback to lower output power applications in the 20 to 200W range. (It should be noted that at higher voltages, the required output voltage ripple magnitudes are not normally as stringent, and this means that the e.s.r requirement and hence capacitor size will not be as large as expected.)

Two transistor flyback.

One possible solution to the 1000V transistor requirement is the two transistor flyback version shown in Fig. 7. Both transistors are switched simultaneously, and all waveforms are exactly the same, except that the voltage across each transistor never exceeds the input voltage. The clamp winding is now redundant, since the two clamp diodes act to return leakage energy to the input. Two 400 or 500V devices can now be selected, which will have faster switching and lower conduction losses. The output power and switching frequencies can thus be significantly increased. The drawbacks of the two transistor version are the extra cost and more complex isolated base drive needed for the top floating transistor.

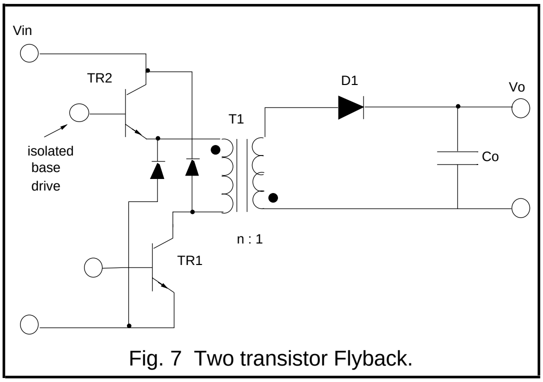


Fig. 7 Two transistor Flyback.

Continuous Vs Discontinuous operation.

As with the buck-boost, the flyback can operate in both continuous and discontinuous modes. The waveforms in Fig. 6 show discontinuous mode operation. In discontinuous mode, the secondary current falls to zero in each switching period, and all of the energy is removed from the transformer. In continuous mode there is current flowing in the coupled inductor at all times, resulting in trapezoidal current waveforms.

The main plus of continuous mode is that the peak currents flowing are only half that of the discontinuous for the same output power, hence, lower output ripple is possible. However, the core size is about 2 to 4 times larger in continuous mode to achieve the increased inductance needed to reduce the peak currents to achieve continuity.

A further disadvantage of continuous mode is that the closed loop is far more difficult to control than the discontinuous mode flyback. (Continuous mode contains a right hand plane zero in its open loop frequency response, the discontinuous flyback does not. See Ref[2] for further explanation.) This means that much more time and effort is required for continuous mode to design the much more complicated compensation components needed to achieve stability.

There is negligible turn-on dissipation in the transistor in discontinuous mode, whereas this dissipation can be fairly high in continuous mode, especially when the additional effects of the output diode reverse recovery current, which only occurs in the continuous case, is included. This normally means that a snubber must be added to protect the transistor against switch-on stresses.

One advantage of the continuous mode is that its open loop gain is independent of the output load i.e V_o only depends upon D and V_{in} as shown in the dc gain equation at the end of the section. Continuous mode has excellent open loop load regulation, i.e varying the output load will not affect V_o. Discontinuous mode, on the other-hand, does have a dependency on the output, expressed as R_L in the dc gain equation. Hence, discontinuous mode has a much poorer open loop load regulation, i.e changing the output will affect V_o. This problem disappears, however, when the control loop is closed, and the load regulation problem is usually completely overcome.

The use of current mode control with discontinuous flyback (where both the primary current and output voltage are sensed and combined to control the duty cycle) produces a much improved overall loop regulation, requiring less closed loop gain.

Although the discontinuous mode has the major disadvantage of very high peak currents and a large output capacitor requirement, it is much easier to implement, and is by far the more common of the two methods used in present day designs.

Output power	50W		100W		200W	
Line voltage, Vin	110V ac	220V ac	110V ac	220V ac	110V ac	220V ac
Transistor requirements Max current Max voltage	 2.25A 400V	 1.2A 800V	 4A 400V	 2.5A 800V	 8A 400V	 4.4A 800V
Bipolar transistors. TO-220 Isolated SOT-186 SOT-93 Isolated SOT-199	 BUT11 BUT11F --- ---	 BUX85 BUX85F --- ---	 BUT12 BUT12F --- ---	 BUT11A BUT11AF --- ---	 --- --- BUW13 BUW13F	 BUT12A BUT12AF --- ---
Power MOSFET TO-220 Isolated SOT-186 SOT-93	 BUK454-400B BUK444-400B ---	 BUK454-800A BUK444-800A ---	 BUK455-400B BUK445-400B ---	 BUK456-800A BUK446-800A ---	 --- --- BUK437-400B	 --- --- BUK438-800A
Output Rectifiers O/P voltage 5V 10V 20V 50V 100V	 PBYR1635 PBYR10100 BYW29E-100/150/200 PBYR10100 BYW29E-100/150/200 BYV29-300 BYV29-500		 PBYR2535CT PBYR20100CT BYV79E-100/150/200 PBYR10100 BYW29E-100/150/200 BYV29-300 BYV29-500		 --- PBYR30100PT BYV42E-100/150/200 BYV72E-100/150/200 PBYR20100CT BYV32E-100/150/200 BYV29-300 BYV29-500	

Table 2. Recommended Power Semiconductors for single-ended flyback.

Note! The above values are for discontinuous mode. In continuous mode the peak transistor currents are approximately halved and the output power available is thus increased.

Flyback

Converter efficiency, η = 80%; Max duty cycle, $D_{max} = 0.45$

Max transistor voltage, V_{ce} or $V_{ds} = 2V_{in(max)}$ + leakage spike

$$\mathrm{Max}\, transistor\, current, I_C \quad ; \quad I_D = 2\frac{P_{out}}{\eta \; D_{\max} \; V_{\min}}$$

dc voltage gain:- (a) continuous $\frac{Vo}{Vin} = n\frac{D}{1-D}$ (b) Discontinuous $\frac{Vo}{Vin} = D\sqrt{\frac{R_L}{2}\frac{T}{L_P}}$

Applications:- Lowest cost, multiple output supplies in the 20 to 200W range. E.g. mains input T.V. supplies, small computer supplies, E.H.T. supplies.

(b) The Forward converter.

Operation.

The forward converter is also a single switch isolated topology, and is shown in Fig. 8. This is based on the buck converter described earlier, with the addition of a transformer and another diode in the output circuit. The characteristic LC output filter is clearly present.

In contrast to the flyback, the forward converter has a true transformer action, where energy is transferred directly to the output through the inductor during the transistor on-time. It can be seen that the polarity of the secondary winding is opposite to that of the flyback, hence allowing direct current flow through blocking diode D1. During the on-time, the current flowing causes energy to be built up in the output inductor L1. When the transistor turns off, the secondary voltage reverses, D1 goes from conducting to blocking mode and the freewheel diode D2 then becomes forward biased and provides a path for the inductor current to continue to flow. This allows the energy stored in L1 to be released into the load during the transistor off time.

The forward converter is always operated in continuous mode (in this case the output inductor current), since this produces very low peak input and output currents and small ripple components. Going into discontinuous mode would greatly increase these values, as well as increasing the amount of switching noise generated. No destabilising right hand plane zero occurs in the frequency response of the forward in continuous mode (as with the buck). See Ref[2]. This means that the control problems that existed with the continuous flyback are not present here. So there are no real advantages to be gained by using discontinuous mode operation for the forward converter.

Advantages.

As can be seen from the waveforms in Fig. 8, the inductor current I_L, which is also the output current, is always continuous. The magnitude of the ripple component, and hence the peak secondary current, depends upon the size of the output inductor. Therefore, the ripple can be made relatively small compared to the output current, with the peak current minimised. This low ripple, continuous output current is very easy to smooth, and so the requirements for the output capacitor size, e.s.r and peak current handling are far smaller than they are for the flyback.

Since the transformer in this topology transfers energy directly there is negligible stored energy in the core compared to the flyback. However, there is a small magnetisation energy required to excite the core, allowing it to become an energy transfer medium. This energy is very small and only a very small primary magnetisation current is needed. This means that a high primary inductance is usually suitable, with no need for the core air gap required in the flyback. Standard un-gapped ferrite cores with high permeabilities (2000-3000) are ideal for providing the high inductance required. Negligible energy storage means that the forward converter transformer is considerably smaller than the flyback, and core loss is also much smaller for the same throughput power. However, the transformer is still operated asymmetrically, which means that power is only transferred during the switch on-time, and this poor utilisation means the transformer is still far bigger than in the symmetrical types.

The transistors have the same voltage rating as the discontinuous flyback (see disadvantages), but the peak current required for the same output power is halved, and this can be seen in the equations given for the forward converter. This, coupled with the smaller transformer and output filter capacitor requirements means that the forward converter is suitable for use at higher output powers than the flyback can attain, and is normally designed to operate in the 100 to 400W range. Suitable bipolars and MOSFETs for the forward converter are listed in Table 3.

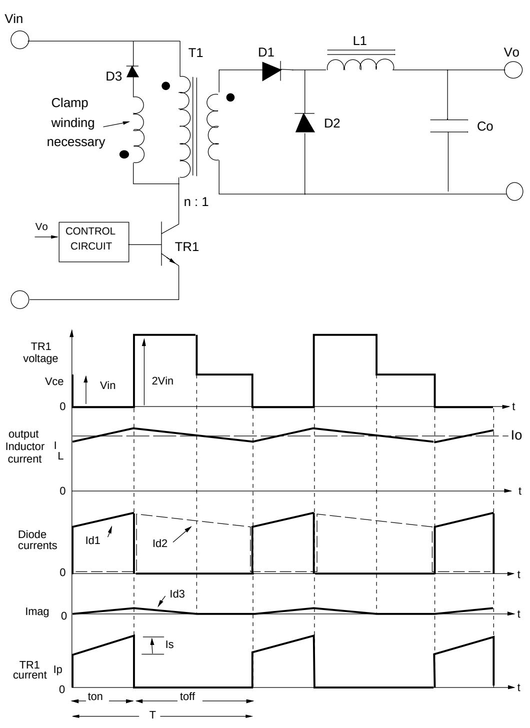


Fig. 8 The Forward converter and waveforms.

Disadvantages.

Because of the unipolar switching action of the forward converter, there is a major problem in how to remove the core magnetisation energy by the end of each switching cycle. If this did not happen, there would be a net dc flux build-up, leading to core saturation, and possible transistor destruction. This magnetisation energy is removed automatically by the push-pull action of the symmetrical types. In the flyback this energy is dumped into the load at transistor turn-off. However, there is no such path in the forward circuit.

This path is provided by adding an additional reset winding of opposite polarity to the primary. A clamp diode is added, such that the magnetisation energy is returned to the input supply during the transistor off time. The reset winding is wound bifilar with the primary to ensure good coupling, and is normally made to have the same number of turns as the primary. (The reset winding wire gauge can be very small, since it only has to conduct the small magnetisation current.) The time for the magnetisation energy to fall to zero is thus the same duration as the transistor on-time. This means that the maximum theoretical duty ratio of the forward converter is 0.5 and after taking into account switching delays, this falls to 0.45. This limited control range is one of the drawbacks of using the forward converter. The waveform of the magnetisation current is also shown in Fig. 8. The clamp winding in the flyback is optional, but is always needed in the forward for correct operation.

Due to the presence of the reset winding, in order to maintain volt-sec balance within the transformer, the input voltage is back reflected to the primary from the clamp winding at transistor turn-off for the duration of the flow of the magnetisation reset current through D3. (There is also a voltage reversal across the secondary winding, and this is why diode D1 is added to block this voltage from the output circuit.) This means that the transistor must block two times Vin during switch-off. The voltage returns to Vin after reset has finished, which means transistor turn-on losses will be smaller. The transistors must have the same added burden of the voltage rating of the flyback, i.e 400V for 110V mains and 800V for 220V mains applications.

Output diode selection.

The diodes in the output circuit both have to conduct the full magnitude of the output current. They are also subject to abrupt changes in current, causing a reverse recovery spike, particularly in the freewheel diode, D2. This spike can cause additional turn-on switching loss in the transistor, possibly causing device failure in the absence of snubbing. Thus, very high efficiency, fast trr diodes are required to minimise conduction losses and to reduce the reverse recovery spike. These requirements are met with Schottky diodes for outputs up to 20V, and fast recovery epitaxial diodes for higher voltage outputs. It is not normal for forward converter outputs to exceed 100V because of the need for a very large output choke, and flybacks are normally used. Usually, both rectifiers are included in a single package i.e a dual centre-tap arrangement. The Philips range of Schottkies and FREDs which meet these requirements are also included in Table 3.

Two transistor forward.

In order to avoid the use of higher voltage transistors, the two transistor version of the forward can be used. This circuit, shown in Fig. 9, is very similar to the two transistor flyback and has the same advantages. The voltage across the transistor is again clamped to V_{in}, allowing the use of faster more efficient 400 or 500V devices for 220V mains applications. The magnetisation reset is achieved through the two clamp diodes, permitting the removal of the clamp winding.

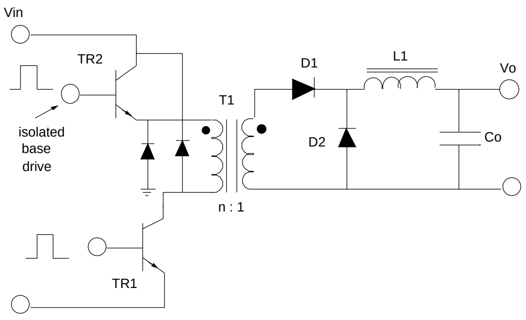


Fig. 9 Two transistor Forward.

The two transistor version is popular for off-line applications. It provides higher output powers and faster switching frequencies. The disadvantages are again the extra cost of the higher component count, and the need for an isolated drive for the top transistor.

Although this converter has some drawbacks, and utilises the transformer poorly, it is a very popular selection for the power range mentioned above, and offers simple drive for the single switch and cheap component costs. Multiple output types are very common. The output inductors are normally wound on a single core, which has the effect of improving dynamic cross regulation, and if designed correctly also reduces the output ripple magnitudes even further. The major advantage of the forward converter is the very low output ripple that can be achieved for relatively small sized LC components. This means that forward converters are normally used to generate lower voltage, high current multiple outputs such as 5, 12, 15, 28V from mains off-line applications, where lower ripple specifications are normally specified for the outputs. The high peak currents that would occur if a flyback was used would place an impossible burden on the smoothing capacitor.

Output power	100W		200W		300W	
Line voltage, Vin	110V ac	220V ac	110V ac	220V ac	110V ac	220V ac
Transistor requirements						
Max current	2.25A	1.2A	4A	2.5A	6A	3.3A
Max voltage	400V	800V	400V	800V	400V	800V
Bipolar transistors.						
TO-220	BUT11	BUX85	BUT12	BUT11A	---	BUT12A
Isolated SOT-186	BUT11F	BUX85F	BUT12F	BUT11AF	---	BUT12AF
SOT-93	---	---	---	---	BUW13	---
Isolated SOT-199	---	---	---	---	BUW13F	---
Power MOSFET						
TO-220	BUK454-400B	BUK454-800A	BUK455-400B	BUK456-800A	---	---
Isolated SOT-186	BUK444-400B	BUK444-800A	BUK445-400B	BUK446-800A	---	---
SOT-93	---	---	---	---	BUK437-400B	BUK438-800A
Output Rectifiers (dual)						
O/P voltage						
5V	PBYR2535CT		---		---	
10V	PBYR20100CT BYV32E-100/150/200		PBYR30100PT BYV42E-100/150/200 BYV72E100/150/200		PBYR30100PT BYV72E-100/150/200	
20V	PBYR20100CT BYQ28E-100/150/200		PBYR20100CT BYV32E-100/150/200		PBYR20100CT BYV32E-100/150/200	
50V	BYT28-300		BYT28-300		BYT28-300	

Table 3. Recommended Power Semiconductors for single-ended forward.

Forward

Converter efficiency, η = 80%; Max duty cycle, $D_{max} = 0.45$

Max transistor voltage, V_{ce} or $V_{ds} = 2V_{in(max)}$

$$\text{Max}\,transistor\,current, I_C \quad ; \quad I_D = \frac{P_{out}}{\eta \quad D_{\max} \quad V_{\min}}$$

dc voltage gain:- $\frac{Vo}{Vin} = n \quad D$

Applications:- Low cost, low output ripple, multiple output supplies in the 50 to 400W range. E.g. small computer supplies, DC/DC converters.

(c) The Push-pull converter.

Operation.

To utilise the transformer flux swing fully, it is necessary to operate the core symmetrically as described earlier. This permits much smaller transformer sizes and provides higher output powers than possible with the single ended types. The symmetrical types always require an even number of transistor switches. One of the best known of the symmetrical types is the push-pull converter shown in Fig. 10.

The primary is a centre-tapped arrangement and each transistor switch is driven alternately, driving the transformer in both directions. The push-pull transformer is typically half the size of that for the single ended types, resulting in a more compact design. This push-pull action produces natural core resetting during each half cycle, hence no clamp winding is required. Power is transferred to the buck type output circuit during each transistor conduction period. The duty ratio of each switch is usually less than 0.45. This provides enough dead time to avoid transistor cross conduction. The power can now be transferred to the output for up to 90% of the switching period, hence allowing greater throughput power than with the single-ended types. The push-pull configuration is normally used for output powers in the 100 to 500W range.

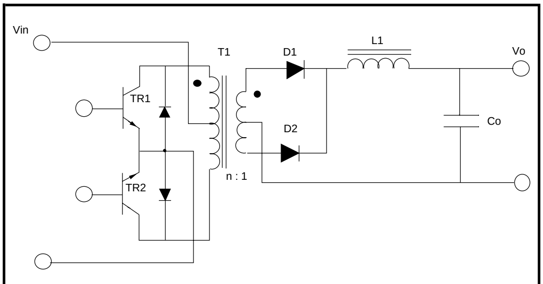


Fig. 10 Push-pull converter.

The bipolar switching action also means that the output circuit is actually operated at twice the switching frequency of the power transistors, as can be seen from the waveforms in Fig. 11. Therefore, the output inductor and capacitor can be even smaller for similar output ripple levels. Push-pull converters are thus excellent for high power density, low ripple outputs.

Advantages.

As stated, the push-pull offers very compact design of the transformer and output filter, while producing very low output ripple. So if space is a premium issue, the push-pull could be suitable. The control of the push-pull is similar to the forward, in that it is again based on the continuous mode buck. When closing the feedback control loop, compensation is relatively easy. For multiple outputs, the same recommendations given for the forward converter apply.

Clamp diodes are fitted across the transistors, as shown. This allows leakage and magnetisation energy to be simply channelled back to the supply, reducing stress on the switches and slightly improving efficiency.

The emitter or source of the power transistors are both at the same potential in the push-pull configuration, and are normally referenced to ground. This means that simple base drive can be used for both, and no costly isolating drive transformer is required. (This is not so for the bridge types which are discussed latter.)

Disadvantages.

One of the main drawbacks of the push-pull converter is the fact that each transistor must block twice the input voltage due to the doubling effect of the centre-tapped primary, even though two transistors are used. This occurs when one transistor is off and the other is conducting. When both are off, each then blocks the supply voltage, this is shown in the waveforms in Fig. 11. This means that TWO expensive, less efficient 800 to 1000V transistors would be required for a 220V off-line application. A selection of transistors and rectifiers suitable for the push-pull used in off-line applications is given in Table 4.

A further major problem with the push-pull is that it is prone to flux symmetry imbalance. If the flux swing in each half cycle is not exactly symmetrical, the volt-sec will not balance and this will result in transformer saturation, particularly for high input voltages. Symmetry imbalance can be caused by different characteristics in the two transistors such as storage time in a bipolar and different on-state losses.

The centre-tap arrangement also means that extra copper is needed for the primary, and very good coupling between the two halves is necessary to minimise possible leakage spikes. It should also be noted that if snubbers are used to protect the transistors, the design must be very precise since each tends to interact with the other. This is true for all symmetrically driven converters.

These disadvantages usually dictate that the push-pull is normally operated at lower voltage inputs such as 12, 28 or 48V. DC-DC converters found in the automotive and telecommunication industries are often push-pull designs. At these voltage levels, transformer saturation is easier to avoid.

Since the push-pull is commonly operated with low dc voltages, a selection guide for suitable power MOSFETs is also included for 48 and 96V applications, seen in Table 5.

Current mode control.

The introduction of current mode control circuits has also benefited the push-pull type. In this type of control, the primary current is monitored, and any imbalance which occurs is corrected on a cycle by cycle basis by varying the duty cycle immediately. Current mode control completely removes the symmetry imbalance problem, and the possibilities of saturation are minimised. This has meant that push-pull designs have become more popular in recent years, with some designers even using them in off-line applications.

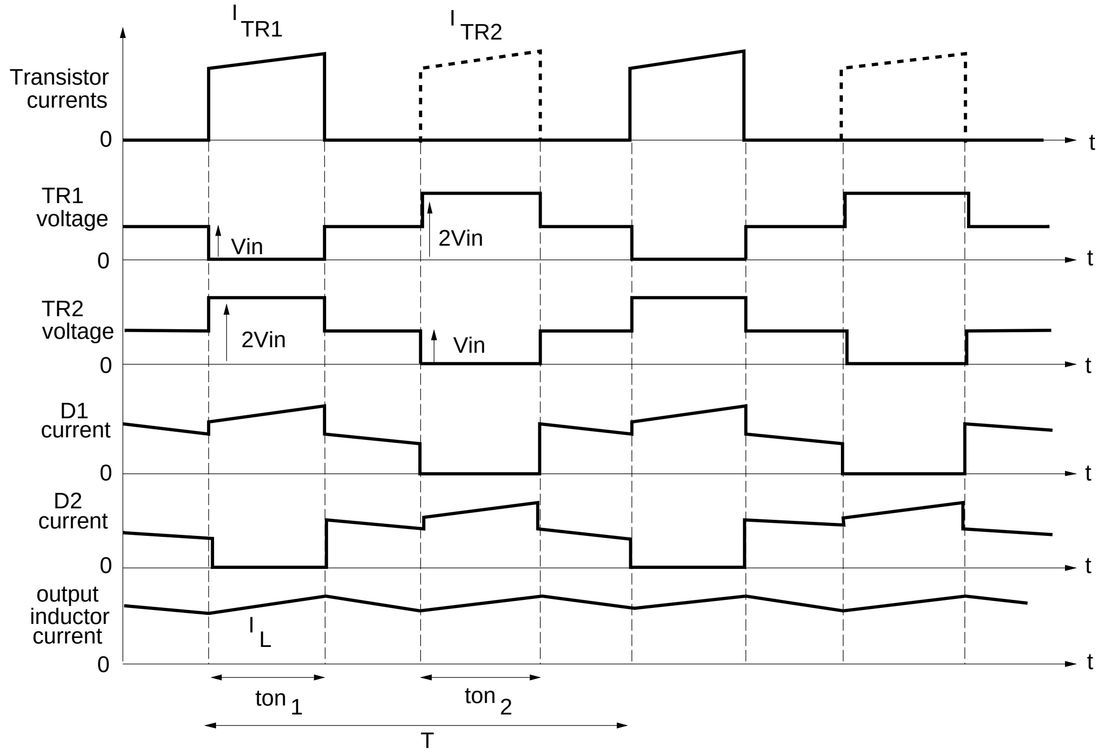

I TR1
I TR2
Transistor currents
0
t
TR1 voltage
Vin
2Vin
0
t
TR2 voltage
2Vin
Vin
0
t
D1 current
0
t
D2 current
0
t
output inductor current
I L
0
t
ton 1
ton 2
T

Fig. 11 Push Pull waveforms.

Output power	100W		300W		500W	
Line voltage, Vin	110V ac	220V ac	110V ac	220V ac	110V ac	220V ac
Transistor requirements						
Max current	1.2A	0.6A	4.8A	3.0A	5.8A	3.1A
Max voltage	400V	800V	400V	800V	400V	800V
Bipolar transistors.						
TO-220	BUT11	BUX85	BUT12	BUT11A	---	BUT12A
Isolated SOT-186	BUT11F	BUX85F	BUT12F	BUT11AF	---	BUT12AF
SOT-93	---	---	---	---	BUW13	---
Isolated SOT-199	---	---	---	---	BUW13F	---
Power MOSFET						
TO-220	BUK454-400B	BUK454-800A	BUK455-400B	BUK456-800A	---	---
Isolated SOT-186	BUK444-400B	BUK444-800A	BUK445-400B	BUK446-800A	---	---
SOT-93	---	---	---	---	BUK437-400B	BUK438-800A
Output Rectifiers (dual)						
O/P voltage						
5V	PBYR2535CT		---		---	
10V	PBYR20100CT		PBYR30100PT		---	
	BYV32E-100/150/200		BYV72E-100/150/200		BYT230PI-200	
20V	PBYR20100CT		PBYR20100CT		PBYR30100PT	
	BYQ28E-100/150/200		BYV32E-100/150/200		BYV42E-100/150/200	
					BYV72E-100/150/200	
50V	BYT28-300		BYT28-300		BYV34-300	

Table 4. Recommended Power Semiconductors for off-line Push-pull converter.

Output power	100W		200W		300W	
Line voltage, Vin	96V dc	48V dc	96V dc	48V dc	96V dc	48V dc
Power MOSFET						
TO-220	BUK455-400B	BUK454-200A	BUK457-400B	BUK456-200B	---	---
Isolated SOT-186	BUK445-400B	BUK444-200A	BUK437-400B	BUK436-200B	---	---
SOT-93	---	---	---	---	BUK437-400B	---

Table 5. Recommended power MOSFETs for lower input voltage push-pull.

Push-Pull converter.

Converter efficiency, $\eta = 80\%$; Max duty cycle, $D_{max} = 0.9$

Max transistor voltage, V_{ce} or $V_{ds} = 2V_{in(max)}$ + leakage spike.

$$\text{Max transistor current}, I_C \quad ; \quad I_D = \frac{P_{out}}{\eta \quad D_{max} \quad V_{min}}$$

dc voltage gain:- $\frac{Vo}{Vin} = 2 \quad n \quad D$

Applications:- Compact design, very low output ripple supplies in the 100 to 500W range. More suited to low input applications. E.g. battery, 28, 40V inputs, high current outputs. Telecommunication supplies.

(d) The Half-Bridge.

Of all the symmetrical high power converters, the half-bridge converter shown in Fig. 12 is the most popular. It is also referred to as the single ended push-pull, and in principle is a balanced version of the forward converter. Again it is a derivative of the buck. The Half-Bridge has some key advantages over the push-pull, which usually makes it first choice for higher power applications in the 500 to 1000W range.

Operation.

The two mains bulk capacitors C1 and C2 are connected in series, and an artificial input voltage mid-point is provided, shown as point A in the diagram. The two transistor switches are driven alternately, and this connects each capacitor across the single primary winding each half cycle. $V_{in}/2$ is superimposed symmetrically across the primary in a push-pull manner. Power is transferred directly to the output on each transistor conduction time and a maximum duty cycle of 90% is available (Some dead time is required to prevent transistor cross-conduction.) Since the primary is driven in both directions, (natural reset) a full wave buck output filter (operating at twice the switching frequency) rather than a half wave filter is implemented. This again results in very efficient core utilisation. As can be seen in Fig. 13, the waveforms are identical to the push-pull, except that the voltage across the transistors is halved. (The device current would be higher for the same output power.)

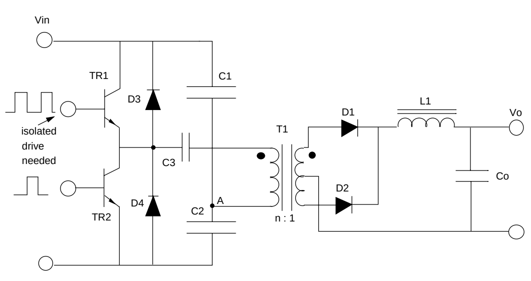


Fig. 12 Half-Bridge converter.

Advantages.

Since both transistors are effectively in series, they never see greater than the supply voltage, V_{in}. When both are off, their voltages reach an equilibrium point of $V_{in}/2$. This is half the voltage rating of the push-pull (although double the current). This means that the half-bridge is particularly suited to high voltage inputs, such as off-line applications. For example, a 220V mains application can use two higher speed, higher efficiency 450V transistors instead of the 800V types needed for a push-pull. This allows higher frequency operation.

Another major advantage over the push-pull is that the transformer saturation problems due to flux symmetry imbalance are not a problem. By using a small capacitor (less than 10µF) any dc build-up of flux in the transformer is blocked, and only symmetrical ac is drawn from the input.

The configuration of the half-bridge allows clamp diodes to be added across the transistors, shown as D3 and D4 in Fig. 12. The leakage inductance and magnetisation energies are dumped straight back into the two input capacitors, protecting the transistors from dangerous transients and improving overall efficiency.

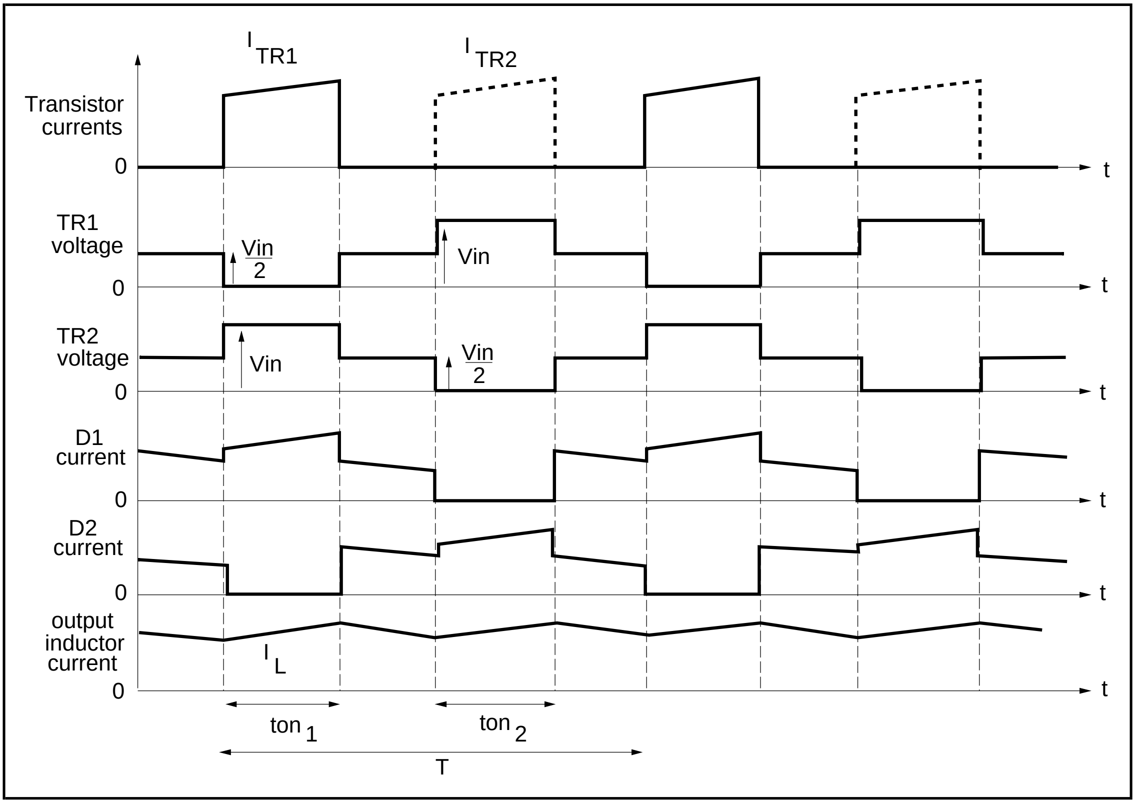
A less obvious exclusive advantage of the half-bridge is that the two series reservoir capacitors already exist, and this makes it ideal for implementing a voltage doubling circuit. This permits the use of either 110V /220V mains as selectable inputs to the supply.

The bridge circuits also have the same advantages over the single-ended types that the push-pull possesses, including excellent transformer utilisation, very low output ripple, and high output power capabilities. The limiting factor in the maximum output power available from the half-bridge is the peak current handling capabilities of present day transistors. 1000W is typically the upper power limit. For higher output powers the four switch full bridge is normally used.

Disadvantages.

The need for two 50/60 Hz input capacitors is a drawback because of their large size. The top transistor must also have isolated drive, since the gate / base is at a floating potential. Furthermore, if snubbers are used across the power transistors, great care must be taken in their design, since the symmetrical action means that they will interact with one another. The circuit cost and complexity have clearly increased, and this must be weighed up against the advantages gained. In many cases, this normally excludes the use of the half-bridge at output power levels below 500W.

Suitable transistors and rectifiers for the half-bridge are given in Table 6.


I TR1
I TR2
Transistor currents
0
t
TR1 voltage
Vin/2
Vin
0
t
TR2 voltage
Vin
Vin/2
0
t
D1 current
0
t
D2 current
0
t
output inductor current
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0
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Fig. 13 Half-Bridge waveforms.

Output power	300W		500W		750W	
Line voltage, Vin	110V ac	220V ac	110V ac	220V ac	110V ac	220V ac
Transistor requirements						
Max current	4.9A	2.66A	11.7A	6.25A	17.5A	9.4A
Max voltage	250V	450V	250V	450V	250V	450V
Bipolar transistors.						
TO-220	BUT12	BUT11	---	---	---	---
Isolated SOT-186	BUT12F	BUT11F	---	---	---	---
SOT-93	---	---	BUW13	BUW13	---	BUW13
Isolated SOT-199	---	---	BUW13F	BUW13F	---	BUW13F
Power MOSFET SOT-93	---	BUK437-500B	---	---	---	---
Output Rectifiers (dual) O/P voltage						
5V	---		---		---	
10V	PBYR30100PT BYV72E-100/150/200		---		---	
20V	PBYR20100CT BYV32E-100/150/200		PBYR30100PT BYV42E-100/150/200 BYV72E-100/150/200		---	
50V	BYT28-300		BYV34-300		BYV34-300	

Table 6. Recommended Power Semiconductors for off-line Half-Bridge converter.

Half-Bridge converter.

Converter efficiency, η = 80%; Max duty cycle, D_{max} = 0.9

Max transistor voltage, V_{ce} or V_{ds} = $V_{in(max)}$ + leakage spike.

$$\text{Max}\, transistor\, current, I_C \quad ; \quad I_D = 2\frac{P_{out}}{\eta \quad D_{\max} \quad V_{\min}}$$

dc voltage gain:- $\frac{Vo}{Vin} = n \quad D$

Applications:- High power, up to 1000W. High current, very low output ripple outputs. Well suited for high input voltage applications. E.g. 110, 220, 440V mains. E.g. Large computer supplies, Lab equipment supplies.

(e) The Full-Bridge.

Outline.

The Full-Bridge converter shown in Fig. 14 is a higher power version of the Half-Bridge, and provides the highest output power level of any of the converters discussed. The maximum current ratings of the power transistors will eventually determine the upper limit of the output power of the half-bridge. These levels can be doubled by using the Full-Bridge, which is obtained by adding another two transistors and clamp diodes to the Half-Bridge arrangement. The transistors are driven alternately in pairs, T1 and T3, then T2 and T4. The transformer primary is now subjected to the full input voltage. The current levels flowing are halved compared to the half-bridge for a given power level. Hence, the Full-Bridge will double the output power of the Half-Bridge using the same transistor types.

The secondary circuit operates in exactly the same manner as the push-pull and half-bridge, also producing very low ripple outputs at very high current levels. Therefore, the waveforms for the Full-Bridge are identical to the Half-Bridge waveforms shown in Fig. 13, except for the voltage across the primary, which is effectively doubled (and switch currents halved). This is expressed in the dc gain and peak current equations, where the factor of two comes in, compared with the Half-Bridge.

Advantages.

As stated, the Full-Bridge is ideal for the generation of very high output power levels. The increased circuit complexity normally means that the Full-Bridge is reserved for applications with power output levels of 1kW and above. For such high power requirements, designers often select power Darlingtons, since their superior current ratings and switching characteristics provide additional performance and in many cases a more cost effective design.

The Full-Bridge also has the advantage of only requiring one mains smoothing capacitor compared to two for the Half-Bridge, hence, saving space. Its other major advantages are the same as for the Half-Bridge.

Disadvantages.

Four transistors and clamp diodes are needed instead of two for the other symmetrical types. Isolated drive for two floating potential transistors is now required. The Full-Bridge has the most complex and costly design of any of the converters discussed, and should only be used where other types do not meet the requirements. Again, the four transistor snubbers (if required) must be implemented carefully to prevent interactions occurring between them.

Table 7 gives an outline of the Philips power semiconductors suitable for use with the Full-Bridge.

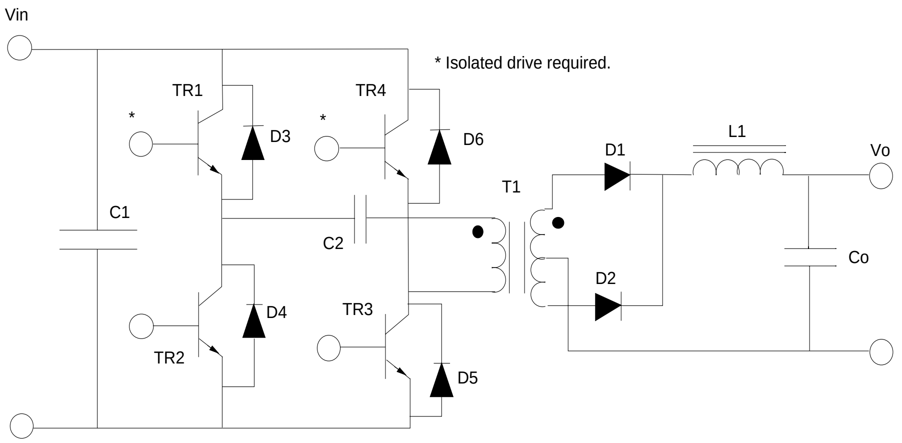


Fig. 14 The Full-Bridge converter.

Output power	500W		1000W		2000W	
Line voltage, Vin	110V ac	220V ac	110V ac	220V ac	110V ac	220V ac
Transistor requirements						
Max current	5.7A	3.1A	11.5A	6.25A	23.0A	12.5A
Max voltage	250V	450V	250V	450V	250V	450V
Bipolar transistors.						
TO-220	BUT12	BUT18	---	---	---	---
Isolated SOT-186	BUT12F	BUT18F	---	---	---	---
SOT-93	---	---	BUW13	BUW13	---	BUW13
Isolated SOT-199	---	---	BUW13F	BUW13F	---	BUW13F
Power MOSFET						
SOT-93	---	BUK438-500B	---	---	---	---
Output Rectifiers (dual)						
O/P voltage						
5V	---		---		---	
10V	---		---		---	
20V	PBYR30100PT BYV42E-100/150/200 BYV72E-100/150/200		---		---	
50V	BYV34-300		BYV44-300		---	

Table 7. Recommended Power Semiconductors for the Full-Bridge converter.

Full-Bridge converter.

Converter efficiency, η = 80%; Max duty cycle, D_{max} = 0.9

Max transistor voltage, V_{ce} or $V_{ds} = V_{in(max)}$ + leakage spike.

$$\text{Max}\,transistor\,current, I_C \quad ; \quad I_D = \frac{P_{out}}{\eta \quad D_{\max} \quad V_{\min}}$$

dc voltage gain:- $\frac{Vo}{Vin} = 2 \quad n \quad D$

Applications:- Very high power, normally above 1000W. Very high current, very low ripple outputs. Well suited for high input voltage applications. E.g. 110, 220, 440V mains. E.g. Computer Mainframe supplies, Large lab equipment supplies, Telecomm systems.

Conclusion.

The 5 most common S.M.P.S. converter topologies, the flyback, forward, push-pull, half-bridge and full-bridge types have been outlined. Each has its own particular operating characteristics and advantages, which makes it suited to particular applications.

The converter topology also defines the voltage and current requirements of the power transistors (either MOSFET or Bipolar). Simple equations and calculations used to outline the requirements of the transistors for each topology have been presented.

The selection guide for transistors and rectifiers at the end of each topology section shows some of the Philips devices which are ideal for use in S.M.P.S. applications.

References.

(1) Philips MOSFET Selection Guide For S.M.P.S. by M.J.Humphreys. Philips Power Semiconductor Applications group, Hazel Grove.

(2) Switch Mode Power Conversion - Basic theory and design by K.Kit.Sum. (Published by Marcel Dekker inc.1984)

Appendix A.

MOSFET throughput power calculations.

Assumptions made:-

The power loss (Watts) in the transistor due to on-state losses is 5% of the total throughput (output) power.

Switching losses in the transistor are negligible. N.B. At frequencies significantly higher than 50kHz the switching losses may become important.

The device junction temperature, T_j is taken to be 125˚C. The ratio $R_{ds(125C˚)}/R_{ds(25˚C)}$ is dependent on the voltage of the MOSFET device. Table A1 gives the ratio for the relevant voltage limiting values.

The value of $V_{s(min)}$ for each input value is given in Table A2.

Device voltage limiting value.	$R_{ds(125C)}$ -------- $R_{ds(25C)}$
100	1.74
200	1.91
400	1.98
500	2.01
800	2.11
1000	2.15

Table A1. On resistance ratio.

Main input voltage	Maximum dc link voltage	Minimum dc link voltage
220 / 240V ac	385V	200V
110 / 120V ac	190V	110V

Table A2. Max and Min dc link voltages for mains inputs.

Using the following equations, for a given device with a known $R_{ds(125˚C)}$, the maximum throughput power in each topology can be calculated.

Where:-

$P_{th(max)}$ = Maximum throughput power.
D_{max} = maximum duty cycle.
τ = required transistor efficiency (0.05 ± 0.005)
$Rds_{(125˚C)} = R_{ds(25˚C)}$ x ratio.
$V_{s(min)}$ = minimum dc link voltage.

Forward converter.

$$P_{th(\max)} = \frac{\tau \times V_{s(\min)}^2 \times D_{\max}}{R_{ds(125c)}}$$

$D_{max} = 0.45$

Flyback Converter.

$$P_{th(\max)} = \frac{3 \times \tau \times V_{s(\min)}^2 \times D_{\max}}{4 \times R_{ds(125c)}}$$

$D_{max} = 0.45$

Push Pull Converter.

$$P_{th(\max)} = \frac{\tau \times V_{s(\min)}^2 \times D_{\max}}{R_{ds(125c)}}$$

$D_{max} = 0.9$

Half Bridge Converter.

$$P_{th(\max)} = \frac{\tau \times V_{s(\min)}^2 \times D_{\max}}{4 \times R_{ds(125c)}}$$

$D_{max} = 0.9$

Full Bridge Converter.

$$P_{th(\max)} = \frac{\tau \times V_{s(\min)}^2 \times D_{\max}}{2 \times R_{ds(125c)}}$$

$D_{max} = 0.9$

2.1.2 The Power Supply Designer's Guide to High Voltage Transistors

One of the most critical components in power switching converters is the high voltage transistor. Despite its wide usage, feedback from power supply designers suggests that there are several features of high voltage transistors which are generally not well understood.

This section begins with a straightforward explanation of the key properties of high voltage transistors. This is done by showing how the basic technology of the transistor leads to its voltage, current, power and second breakdown limits. It is also made clear how deviations from conditions specified in the data book will affect the performance of the transistor. The final section of the paper gives practical advice for designers on how circuits might be optimised and transistor failures avoided.

Introduction

A large amount of useful information about the characteristics of a given component is provided in the relevant data book. By using this information, a designer can usually be sure of choosing the optimum component for a particular application.

However, if a problem arises with the completed circuit, and a more detailed analysis of the most critical components becomes necessary, the data book can become a source of frustration rather than practical assistance. In the data book, a component is often measured under a very specific set of conditions. Very little is said about how the component performance is affected if these conditions are not reproduced exactly when the component is used in a circuit.

There are as many different sets of requirements for high voltage transistors as there are circuits which make use of them. Covering every possible drive and load condition in the device specification is an impossible task. There is therefore a real need for any designer using high voltage transistors to have an understanding of how deviations from the conditions specified in the transistor data book will affect the electrical performance of the device, in particular its limiting values.

Feedback from designers implies that this information is not readily available. The intention of this report is therefore to provide designers with the information they need in order to optimise the reliability of their circuits. The characteristics of high voltage transistors stem from their basic technology and so it is important to begin with an overview of this.

HVT technology

Stripping away the encapsulation of the transistor reveals how the electrical connections are made (see Fig. 1). The collector is contacted through the back surface of the transistor chip, which is soldered to the nickel-plated copper lead frame. For Philips power transistors the lead frame and the centre leg are formed from a single piece of copper, and so the collector can be accessed through either the centre leg or any exposed part of the lead frame (eg the mounting base for TO-220 and SOT-93).

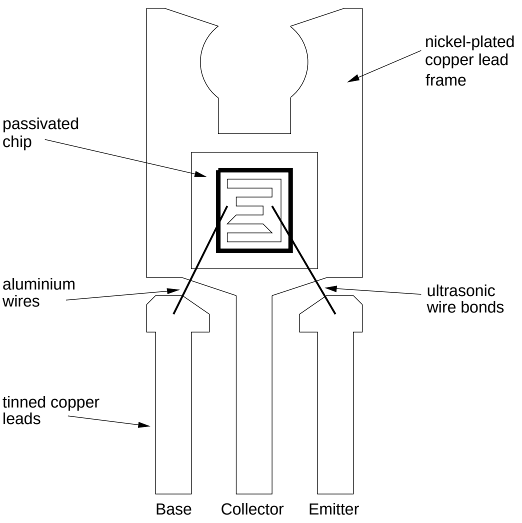


Fig. 1 High voltage transistor without the plastic case.

The emitter area of the transistor is contacted from the top surface of the chip. A thin layer of aluminium joins all of the emitter area to a large bond pad. This bond pad is aluminium wire bonded to the emitter leg of the transistor when the transistor is assembled. The same method is used to contact the base area of the chip. Fig. 2 shows the top view of a high voltage transistor chip in more detail.

Viewing the top surface of the transistor chip, the base and emitter fingers are clearly visible. Around the periphery of the chip is the high voltage glass passivation. The purpose of this is explained later.

Taking a cross section through the transistor chip reveals its npn structure. A cross section which cuts one of the emitter fingers and two of the base fingers is shown in Fig. 3.

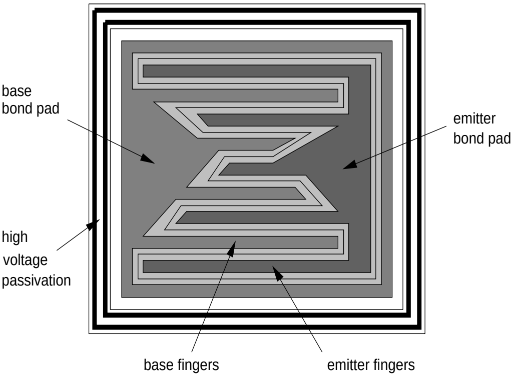

base
bond pad
emitter
bond pad
high
voltage
passivation
base fingers
emitter fingers

Fig. 2 High voltage transistor chip.

On the top surface of the transistor are the aluminium tracks which contact the base and emitter areas. The emitter finger is shown connected to an n+ region. This is the emitter area. The n+ denotes that this is very highly doped n type silicon. Surrounding the n+ emitter is the base, and as shown in Fig. 3 this is contacted by the base fingers, one on either side of the emitter. The p denotes that this is highly doped p type silicon.

On the other side of the base is the thick collector n- region. The n- denotes that this is lightly doped n type silicon. The collector region supports the transistor blocking voltage, and its thickness and resistivity must increase with the voltage rating of the device.

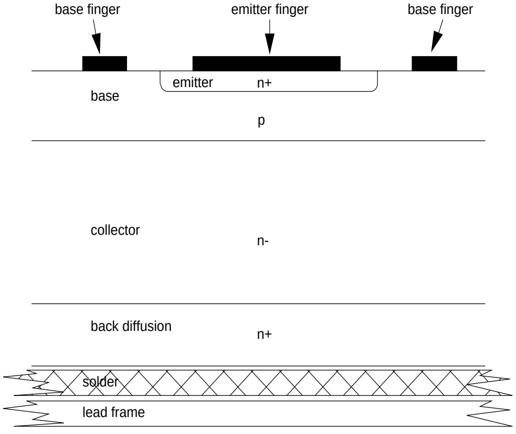

base finger
emitter finger
base finger
emitter
n+
base
p
collector
n-
back diffusion
n+
solder
lead frame

Fig. 3 Cross section of HVT.

Following the collector region is the n+ back diffusion. The n+ back diffusion ensures a good electrical contact is made between the collector region and the lead frame/collector leg, whilst also allowing the crystal to be thick enough to prevent it from cracking during processing and assembly. The bottom surface of the chip is soldered to the lead frame.

Voltage limiting values

Part 1: Base shorted to emitter.

When the transistor is in its off state with a high voltage applied to the collector, the base collector junction is reverse biased by a very high voltage. The voltage supporting *depletion region* extends deep into the collector, right up to the back diffusion, as shown in Fig. 4.

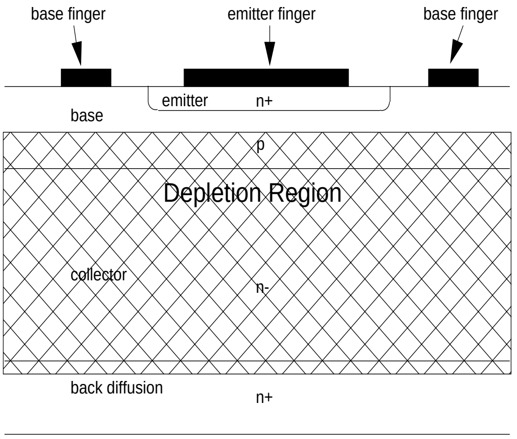

base finger
emitter finger
base finger
emitter
n+
base
p
Depletion Region
collector
n-
back diffusion
n+

Fig. 4 Depletion region extends deep into the collector during the off state.

With the base of the transistor short circuited to the emitter, or at a lower potential than the emitter, the voltage rating is governed by the voltage supporting capability of the reverse biased base collector junction. This is the transistor $V_{CESMmax}$. The breakdown voltage of the reverse biased base collector junction is determined mainly by the collector width and resistivity as follows:

Figure 5 shows the doping profile of the transistor. Note the very high doping of the emitter and the back diffusion, the high doping of the base and the low doping of the collector. Also shown in Fig. 5 is the electric field concentration throughout the depletion region for the case where the transistor is supporting its off state voltage. The electric field, E, is given by the equation, E = -dV/dx, where -dV is the voltage drop in a distance dx. Rewriting this equation gives the voltage supported by the depletion region:

$$V = -\int E dx$$

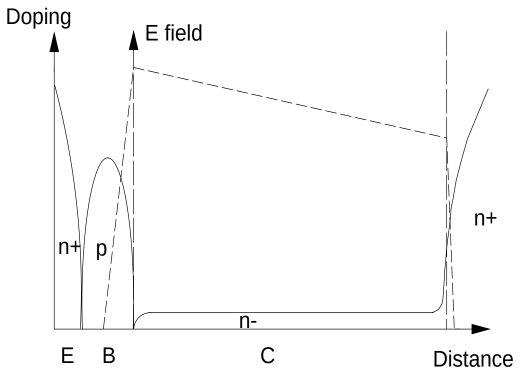


Fig. 5 Doping profile and E field distribution.

This is the area under the dotted line in Fig.5.

During the off state, the peak electric field occurs at the base collector junction as shown in Fig. 5. If the electric field anywhere in the transistor exceeds 200 kVolts per cm then avalanche breakdown occurs and the current which flows in the transistor is limited only by the surrounding circuitry. If the avalanche current is not limited to a very low value then the power rating of the transistor can easily be exceeded and the transistor destroyed as a result of thermal breakdown. Thus the maximum allowable value of electric field is 200 kV/cm.

The gradient of the electric field, dE/dx, is proportional to charge density which is in turn proportional to the level of doping. In the base, the gradient of the electric field is high because of the high level of doping, and positive because the base is p type silicon. In the collector, the gradient of the electric field is low because of the low level of doping, and negative because the collector is n type silicon. In the back diffused region, the gradient of the electric field is very highly negative because this is very highly doped n type silicon.

Increasing the voltage capability of the transistor can therefore be done by either increasing the resistivity (lowering the level of doping) of the collector region in order to maintain a high electric field for the entire collector width, or increasing the collector width itself. Both of these measures can be seen to work in principle because they increase the area under the dotted line in Fig. 5.

The breakdown voltage of the transistor, $V_{CESMmax}$, is limited by the need to keep the peak electric field, E, below 200 kV/cm. Without special measures, the electric field would crowd at the edges of the transistor chip because of the surface irregularities. This would limit breakdown voltages to considerably less than the full capability of the silicon. Crowding of the equipotential lines at the chip edges is avoided by the use of a glass passivation (see Fig. 6). The glass passivation therefore allows the full voltage capability of the transistor to be realised.

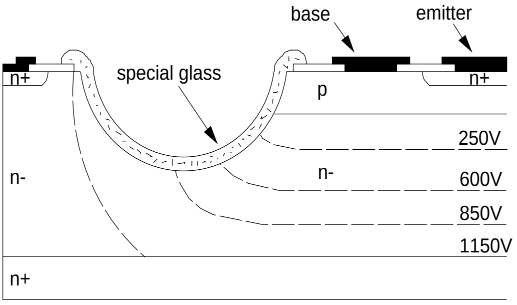


Fig. 6 High voltage passivation.

The glass used is negatively charged to induce a p- channel underneath it. This ensures that the applied voltage is supported evenly over the width of the glass and does not crowd at any one point. High voltage breakdown therefore occurs in the bulk of the transistor, at the base collector junction, and not at the edges of the crystal.

Exceeding the voltage rating of the transistor, even for a fraction of a second, must be avoided. High voltage breakdown effects can be concentrated in a very small area of the transistor, and only a small amount of energy may damage the device. However, there is no danger in using the full voltage capability of the transistor as the limit under worst case conditions because the high voltage passivation is extremely stable.

Part 2: Open circuit base.

With the base of the transistor open circuit the voltage capability is much lower. This is the V_{CEOmax} of the device and it is typically just less than half of the $V_{CESMmax}$ rating. The reason for the lower voltage capability under open circuit base conditions is as follows:

As the collector emitter voltage of the transistor rises, the peak electric field located at the base collector junction rises too. Above a peak E field value of 100 kV/cm there is an appreciable leakage current being generated.

In the previous case, with the base contact short circuited to the emitter, or held at a lower potential than the emitter, any holes which are generated drift from the edge of the depletion region towards the base contact where they are extracted. However, with the base contact open circuit, the holes generated diffuse from the edge of the depletion region towards the emitter where they effectively act as base current. This causes the emitter to inject electrons into the base, which diffuse towards the collector. Thus there is a flow of electrons from the emitter to the collector.

The high electric field in the collector accelerates the electrons to the level where some have sufficient energy to produce more hole electron pairs through their collisions with the lattice. The current generated in this way adds to the leakage current. Thus with the base contact open circuit the emitter becomes active and provides the system with *gain*, multiplying the leakage current and consequently reducing the breakdown voltage.

For a given transistor the gain of the system is dependant on two things. Firstly it is dependant on the probability that a hole leaving the depletion region will reach the emitter. If the base is open circuit and no recombination occurs then this probability is 1. If the base is not open circuit, and instead a potential below V_{BEon} is applied, then there is a chance that a hole leaving the depletion region will be extracted at the base contact. As the voltage on the base contact is made less positive the probability of holes reaching the emitter is reduced.

Secondly, the gain is dependant on the probability of electrons leaving the emitter, diffusing across the base and being accelerated by the high field in the collector to the level where they are able to produce a hole electron pair in one of their collisions with the lattice. This depends on the electric field strength which is in turn dependant on the collector voltage.

Thus for a given voltage at the base there is a corresponding maximum collector voltage before breakdown will occur. With the base contact shorted to the emitter, or at a lower potential than the emitter, the full breakdown voltage of the transistor is achieved ($V_{CESMmax}$). With the base contact open circuit, or at a *higher* potential than the emitter, the breakdown voltage is lower (V_{CEOmax}) because in this case the emitter is active and it provides the breakdown mechanism with gain.

With the base connected to the emitter by a non zero impedance, the breakdown voltage will be somewhere between the $V_{CESMmax}$ and the V_{CEOmax}. A low impedance approximates to the shorted base, 'zero gain', case and a high impedance approximates to the open base, 'high gain', case. With a base emitter impedance of 47 Ω and no externally applied base voltage, the breakdown voltage is typically 10% higher than the V_{CEOmax}.

Current limiting values

The maximum allowed DC current is limited by the size of the bond wires to the base and emitter. Exceeding the DC limiting values I_{Cmax} and I_{Bmax}, for any significant length of time, may blow these bond wires. If the current pulses are short and of a low duty cycle then values greatly in excess of the DC values are allowed. The I_{CMmax} and I_{BMmax} ratings are recommendations for peak current values. For a duty cycle of 0.01 and a pulse width of 10ms these values will typically be double the DC values.

If the pulses are shorter than 10ms then even the recommended peak values can be exceeded under worst case conditions. However, it should be noted that combinations of high collector current and high collector voltage can lead to failure by second breakdown (discussed later). As the collector current is increased, the collector voltage required to trigger second breakdown drops, and so allowing large collector current spikes increases the risk of failure by second breakdown. It is therefore advised that the peak values given in the data book are used as design limits in order to maximise the component reliability.

In emitter drive circuits, the peak reverse base current is equal to the peak collector current. The pulse widths and duty cycles involved are small, and this mode of operation is within the capability of all Philips high voltage transistors.

Power limiting value

The P_{totmax} given in device data is not generally an achievable parameter because in practice it is obtainable only if the mounting base temperature can be held to 25 ˚C. In practice, the maximum power dissipation capability of a given device is limited by the heatsink size and the ambient temperature. The maximum power dissipation capability for a particular circuit can be calculated as follows;

T_{jmax} is the maximum junction temperature given in the data sheet. The value normally quoted is 150 ˚C. T_{amb} is the ambient temperature around the device heatsink. A typical value in practice could be 65 ˚C. R_{thj-mb} is the device thermal resistance given in the data sheet, but to obtain a value of junction to *ambient* thermal resistance, R_{thj-a}, the thermal resistance of the mica spacer (if used), heatsink and heatsink compound should be added to this.

The maximum power which can be dissipated under a given set of circuit conditions is calculated using;

$$P_{max} = (T_{jmax} - T_{amb})/R_{thj-a}$$

For a BUT11AF, in an ambient temperature of 65 ˚C, mounted on a 10 K/W heatsink with heatsink compound, this gives;

$$R_{thj-a} = 3.95\ \mathrm{K/W} + 10\ \mathrm{K/W} = 13.95\ \mathrm{K/W}$$

and hence the maximum power capable of being dissipated under these conditions is;

$$P_{max} = (150-65)/13.95 = 6\ \mathrm{W}$$

Exceeding the maximum junction temperature, T_{jmax}, is not recommended. All of the quality and reliability work carried out on the device is based on the maximum junction temperature quoted in data. If T_{jmax} is exceeded in the circuit then the reliability of the device is no longer guaranteed.

Secondary breakdown

Pure silicon, also known as *'intrinsic'* silicon, contains few mobile charge carriers at room temperature and so its conductivity is low. By doping the silicon (ie introducing atoms of elements other than silicon) the number of mobile charge carriers, and hence the conductivity, can be increased. Silicon doped in such a way as to increase the number of mobile electrons (negative charge) is called n type silicon. Silicon doped in such a way as to increase the number of mobile holes (positive charge) is called p type silicon. Thus the base region of an npn transistor contains an excess of mobile holes and the collector and emitter regions contain an excess of mobile electrons.

When a high voltage is applied to the transistor, and the collector base junction is reverse biased, a depletion region is developed. This was shown in Fig. 4. The depletion region supports the applied voltage. The electric field distribution within the depletion region was shown in Fig. 5.

The term *depletion region* refers to a region depleted of mobile charge carriers. Therefore, within the depletion region, the base will have lost some holes and hence it is left with a net negative charge. Similarly the collector will have lost some electrons and hence it is left with a net positive charge. The collector is said to have a 'positive space charge' (and the base a 'negative space charge'.)

Consider the case where a transistor is in its off state supporting a high voltage which is within its voltage capability. The resulting electric field distribution is shown in Fig. 7.

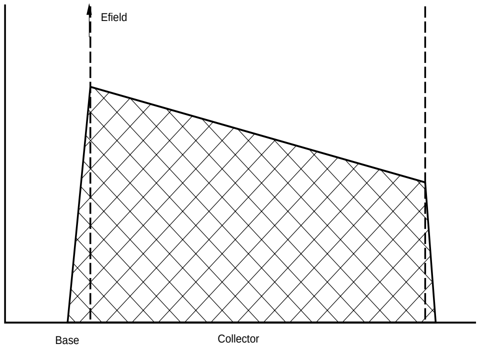


Fig. 7 V_{CE} high, I_C = 0.

If the collector voltage is held constant, and the collector current increased so that there is now some collector current flowing, this current will modify the charge distribution within the depletion region. The effect this has on the base is negligible because the base is very highly doped. The effect this has on the collector is significant because the collector is only lightly doped.

The collector current is due to the flow of electrons from the emitter to the collector. As the collector current increases, the collector current density increases. This increase in collector current density is reflected in Fig. 8 by an increase in the electron concentration in the collector.

At a certain collector current density, the negative charge of the electrons neutralises the positive space charge of the collector. The gradient of the electric field, dE/dx, is proportional to charge density. If the space charge is neutralised then the gradient of the electric field becomes zero. This is the situation illustrated in Fig. 8. Note that the shaded area remains constant because the applied voltage remains constant. Therefore the peak value of electric field drops slightly.

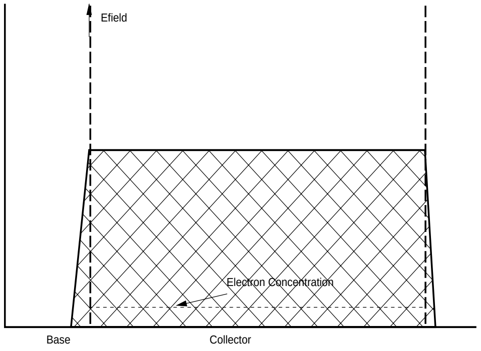


Fig. 8 V_{CE} high, I_C>0.

Keeping the collector-emitter voltage constant, and pushing up the collector current density another step, increases the concentration of electrons in the collector still further. Thus the collector charge density is now negative, the gradient of electric field in the collector is now positive, and the peak electric field has shifted from the collector-base junction to the collector-back diffusion interface. This is shown in Fig. 9.

Increasing the collector current density another step will further increase the positive gradient of electric field. The collector voltage is unchanged and so the shaded area must remain unchanged. Therefore the peak electric field is forced upwards. This is shown in Fig. 10.

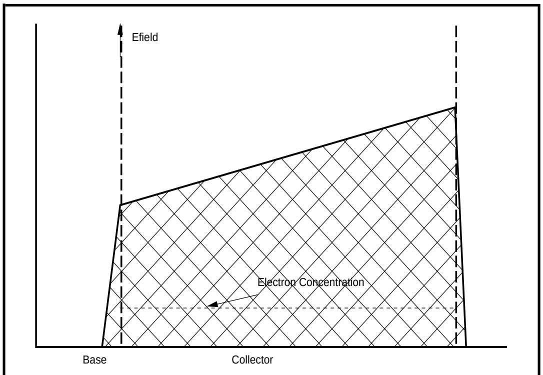


Fig. 9 V_{CE} high, I_C increased further.

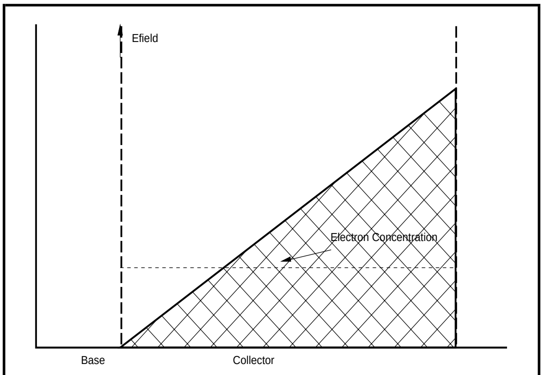


Fig. 10 V_{CE} high, I_C increased further.

At a certain critical value of peak electric field, E_{crit}, a regenerative breakdown mechanism takes place which causes the electron concentration in the collector to increase uncontrollably by a process known as *avalanche multiplication*. As the electron concentration increases, the gradient of electric field increases (because the gradient of electric field is proportional to charge density). The peak electric field is clamped by the breakdown and so the collector voltage drops. In most circuits the collapsing collector voltage will result in a further rise in collector current density, causing a further rise in electron concentration (ie positive feedback). This is shown in Fig. 11.

At approximately 30 V, the holes produced by the avalanche multiplication build up sufficiently to temporarily stabilize the system. However, with 30 V across the device and a high collector current flowing through it, a considerable amount of heat will be generated. Within less than one microsecond thermal breakdown will take place, followed by device destruction.

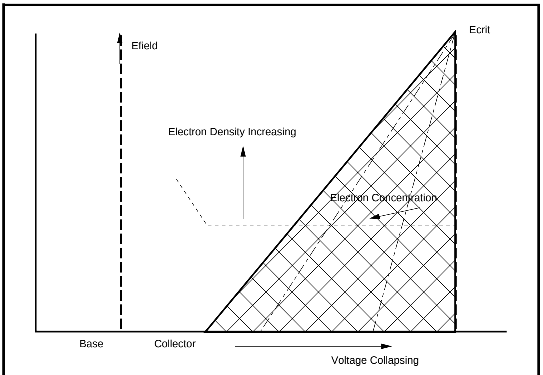


Fig.11 V_{CE} falling, I_C increasing

Safe Operating Area

It has been shown that the electric field profile, and hence the peak electric field, is dependent on the combination of collector current density and applied collector voltage. The peak electric field increases with increasing collector voltage (increase in shaded area in Figs. 7 to 11). It also increases with increasing collector current density (increase in gradient of electric field). At all times the peak electric field must remain below the critical value. If the collector voltage is lowered then a higher collector current density is permitted. If the collector current density is lowered then a higher collector voltage is permitted.

Potentially destructive combinations of collector current density and collector voltage are most likely to occur during switching and during fault conditions in the circuit (eg a short circuited load). The safe operating areas give information about the capability of a given device under these conditions.

The collector current density is dependent on the collector current and the degree of current crowding in certain areas of the collector. The degree of current crowding is different for turn-on (positive base voltage) and turn-off (negative base voltage). Therefore the allowed combinations of collector current and collector voltage, collectively known as the safe operating area (SOA) of the transistor, will be different for turn-on of the transistor and turn-off.

Forward SOA

With a positive voltage applied to the base, the shape of the safe operating area for DC operation is that shown in Fig. 12. Operation outside the safe operating area is not allowed.

For pulsed operation the forward SOA increases, and for small, low duty cycle pulses it becomes square. The forward SOA provides useful information about the capabilities of the transistor under fault conditions in the circuit (eg. a short circuited load).

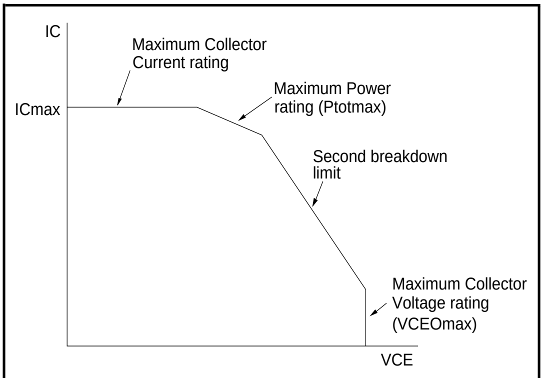


Fig. 12 Forward SOA.

The safe operating area is designed to protect the current, power, voltage and second breakdown limits of the transistor. The current, power and voltage limits of the transistor have already been discussed. Note that the peak voltage rating is the V_{CEOmax} rating and not the $V_{CESMmax}$ rating. The $V_{CESMmax}$ rating only applies if the base emitter voltage is not greater than zero volts.

Sometimes shown on forward SOA curves is an extension allowing higher voltages than V_{CEOmax} to be tolerated for short periods (of the order of 0.5 µs). This allows turn-on of the transistor from a higher voltage than V_{CEOmax}. However, the pulses allowed are very short, and unless it can be guaranteed that the rated maximum pulse time will never be exceeded, transistor failures will occur. If the circuit conditions can be guaranteed then there is no danger in making use of this capability.

As mentioned in the previous section, second breakdown is triggered by combinations of high collector voltage and high collector current density. With a positive voltage applied to the base, the region of highest current density is at the edges of the emitter as shown in Fig. 13.

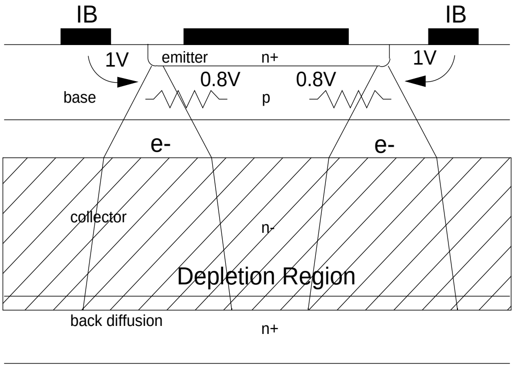


Fig. 13 Forward biased second breakdown.

The base region under the emitter constitutes a resistance (known as the *sub emitter resistance*). With a positive voltage applied to the base, the sub emitter resistance will mean that the areas of the emitter which are nearest to the base have a higher forward bias voltage than the areas furthest from the base. Therefore the *edges* of the emitter have a higher forward bias voltage than the centre and so they receive a higher base current.

As a result of this the edges of the emitter conduct a substantial proportion of the collector current when the base is forward biased. If the collector current is high then the current density at the edges of the emitter is also high. There will be some spreading out of this current as it traverses the base. When the edge of the depletion region is reached, the current is sucked across by the electric field.

If the transistor is conducting a high current and also supporting a high voltage, then the current density will be high when the current reaches the edge of the depletion region. If the current density is beyond that allowed at the applied voltage, then the second breakdown mechanism is triggered (as explained in the previous section) and the device will be destroyed.

With a positive base current flowing, the region of highest current density is at the edges of the emitter. A forward SOA failure will therefore produce burns which originate from the edge of one of the emitter fingers.

Forward SOA failure becomes more likely as pulse width and/or duty cycle is increased. Because the edges of the emitter are conducting more current than the centre, they will get hotter. The temperature of the emitter edges at the end of each current pulse is a function of the pulse width and the emitter current. Longer pulse widths will increase the temperature of the emitter edges at the end of each current pulse. Higher duty cycles will leave insufficient time for this heat to spread. In this manner, combinations of long pulse width and high duty cycle can give rise to cumulative heating effects. Current will crowd towards the hottest part of the emitter. There is therefore a tendency for current to become concentrated in very narrow regions at the edges of the emitter fingers, and as pulse width and/or duty cycle is increased the degree of current crowding increases. This is the reason why the forward SOA for DC operation is as shown in Fig. 12, but for pulsed operation it is enlarged and for small, low duty cycle pulses it becomes square.

Reverse SOA

During turn-on of the transistor, the high resistance of the collector region is reduced by the introduction of holes (from the base) and electrons (from the emitter). This process, known as *conductivity modulation*, is the reason why bipolar transistors are able to achieve such a low collector voltage during the on state, typically 0.2 V. However, during turn-off of the transistor, these extra holes and electrons constitute a stored charge which must be removed from the collector before the voltage supporting depletion region can develop.

To turn off the transistor, a negative voltage is applied to the base and a reverse base current flows. During turn-off of the transistor, it is essential that the device stays within its reverse bias safe operating area (RBSOA). The shape of a typical RBSOA curve is as shown in Fig. 14.

With no negative voltage applied to the base, the RBSOA is very much reduced, as shown in Fig. 14. This is particularly important to note at power up and power down of power supplies, when rail voltages are not well defined (see section on improving reliability).

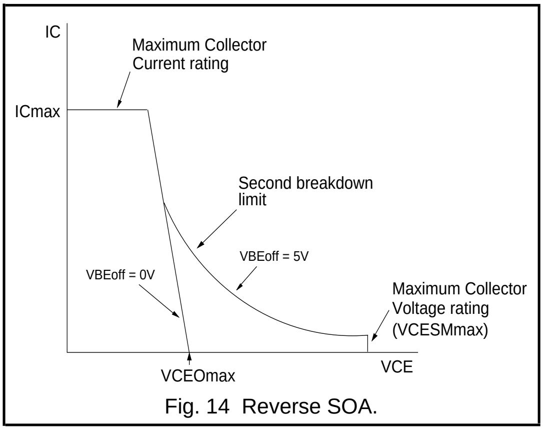


Fig. 14 Reverse SOA.

On applying a negative voltage to the base, the charge stored in the collector areas nearest to the base contacts will be extracted, followed by the charge stored in the remaining collector area. Holes not extracted through the base contact are free to diffuse into the emitter where they constitute a base current which keeps the emitter active. During the transistor storage time, the collector charge is being extracted through the base, but the emitter is still active and so the collector current continues to flow.

During the transistor fall time, the voltage supporting depletion region is being developed and therefore the collector voltage is rising. In addition to this, the negative voltage on the base is causing holes to drift towards the base contact where they are neutralised, thus preventing holes from diffusing towards the emitter.

This has two effects on the collector current. Firstly, the rising collector voltage results in a reduction in the voltage across the collector load, and so the collector current starts to drop. Secondly, the extraction of holes through the base will be most efficient nearest to the base contacts (due to the sub emitter resistance), and so the collector current becomes concentrated into narrow regions under the centre of the emitter fingers (furthest from the base). This is shown in Fig. 15. This current crowding effect leads to an increase in the collector current density during turn off, even though the collector current itself is falling.

Thus for a portion of the fall time, the collector voltage is rising and the collector current density is also rising. This is a critical period in the turn-off phase. If the turn-off is not carefully controlled, the transistor may be destroyed during this period due to the onset of the second breakdown mechanism described earlier.

During this critical period, the collector current is concentrated into a narrow region under the centre of the emitter. RBSOA failure will therefore produce burns which originate from the centre of one of the emitter fingers.

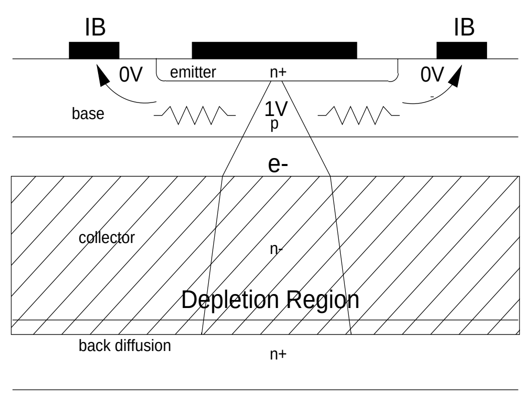


Fig. 15 Reverse biased second breakdown.

Useful tips as an aid to circuit design

In recent years, the Philips Components Power Semiconductor Applications Laboratory (P.S.A.L.) has worked closely with a number of HVT users. It has become apparent that there are some important circuit design features which, if overlooked, invariably give rise to circuit reliability problems. This section addresses each of these areas and offers guidelines which, if followed, will enhance the overall performance and reliability of any power supply.

Improving turn-on

There is more to turning on a high voltage transistor than simply applying a positive base drive. The positive base drive must be at least sufficient to keep the transistor saturated at the current it is required to conduct. However, transistor gain as specified in data sheets tends to be assessed under static conditions and therefore assumes the device is already on.

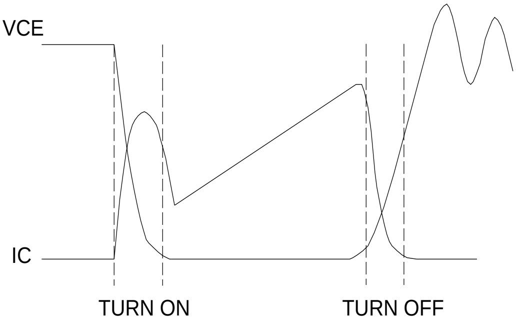


Fig. 16 Transistor switching waveforms in a typical power supply.

Note 1. *The base current requirements at turn-on of the transistor are higher than the static gain would suggest.*

The conductivity modulation process, described at the beginning of the previous section, occurs every time the transistor is turned on. The faster the charges are introduced into the collector, the faster the collector resistance will drop, allowing the collector voltage to drop to its saturation level. The rate at which the collector charge is built up is dependent on the applied base current and the applied collector current. In order to turn the transistor on quickly, and hence minimise the turn-on dissipation, the transistor needs to be overdriven until the collector voltage has dropped to its saturation level. This is achieved by having a period of overshoot at the start of the base current pulse. The turn-on waveforms are shown in Fig. 17.

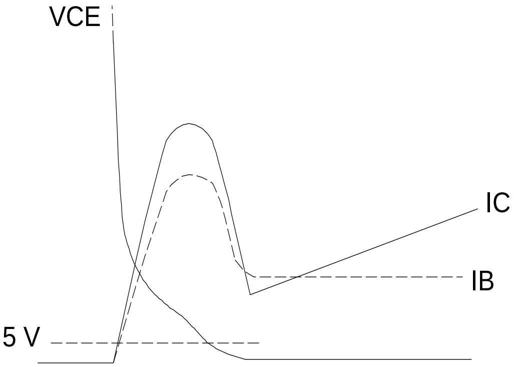


Fig. 17 Turn on waveforms.

Note 2. *A fast rising base current pulse with an initial period of overshoot is a desirable design feature in order to keep the turn-on dissipation low.*

The base current overshoot is achieved by having a capacitor in parallel with the forward base drive resistor (see Fig. 18). The RC time constant determines the overshoot period and as a first approximation it should be comparable to the transistor storage time. The capacitor value is then adjusted until the overshoot period is almost over by the time the transistor is saturated. This is the optimum drive condition. A resistor in series with the capacitor (typically R/2) can be used to limit the peak base current overshoot and remove any undesirable oscillations.

The initial period of overshoot is especially necessary in circuits where the collector current rises quickly (ie square wave switching circuits and circuits with a high snubber discharge current). In these circuits the transistor would otherwise be conducting a high collector current during the early stages of the turn-on period where the collector voltage can still be high. This would lead to an unacceptable level of turn-on dissipation.

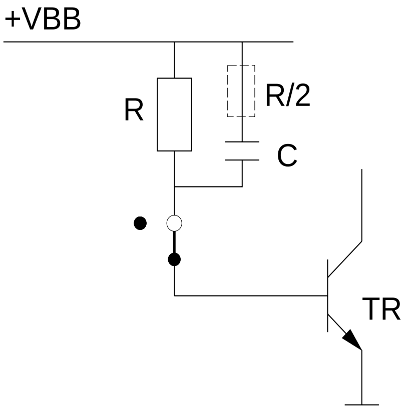


Fig. 18 Forward base drive circuit.

Note 3. *Square wave switching circuits, and circuits with a high snubber discharge current, are very susceptible to high turn-on dissipation. Using an RC network in series with the forward base current path increases the turn-on speed and therefore overcomes this problem.*

It should also be noted that during power up of power supply units, when all the output capacitors of the supply are discharged, the collector current waveform is often very different to that seen under normal running conditions. The rising edge of the collector current waveform is often faster, the collector current pulse width is often wider and the peak collector current value is often higher.

In order to prevent excessive collector current levels (and transformer saturation) a 'soft start' could be used to limit the collector current pulse width during power up. Alternatively, since many power supply designs are now using current mode control, excessive collector current can be avoided simply by setting the overcurrent threshold at an acceptable level.

Note 4. *Using the 'soft start' and/or the overcurrent protection capability of the SMPS control IC prevents excessive collector current levels at power up.*

Improving turn-off

As far as the collector current is concerned, optimum turn-off for a particular device is determined by how quickly the structure of the device will allow the stored charge to be extracted. If the device is turned off too quickly, charge gets trapped in the collector when the collector base junction recovers. Trapped charge takes time to recombine leading to a long collector current tail at turn-off and hence high turn-off losses. On the other hand, if the device is turned off too slowly, the collector voltage starts to rise prematurely (ie while the collector current is at its peak). This would also lead to high turn-off losses.

Note 1. *Turning the transistor off either too quickly or too slowly leads to high turn-off losses.*

Optimum turn-off is achieved by using the correct combination of reverse base drive and storage time control. Reverse base drive is necessary to prevent storage times from being too long (and also to give the maximum RBSOA). Storage time control is necessary to prevent storage times from being too short.

Storage time control is achieved by the use of a small inductor in series with the reverse base current path (see Fig. 19). This controls the slope of the reverse base current (as shown in Fig. 20) and hence the rate at which charge is extracted from the collector. The inductor, or *'base coil'*, is typically between 1 and 6 µH, depending on the reverse base voltage and the required storage time.

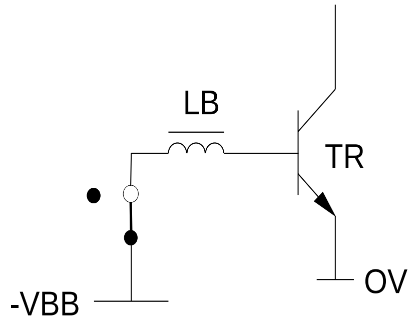


Fig. 19 Reverse base drive circuit.

Note 2. *Applying a base coil in series with the reverse base current path increases the transistor storage time but reduces both the fall time and the turn-off losses.*

Applying this small base inductor will usually mean that the base emitter junction of the transistor is brought into breakdown during part of the turn-off cycle. This is not a problem for the device because the current is controlled by the coil and the duty cycle is low.

If the transistor being used is replaced by a transistor of the same technology but having either a higher current rating or a higher voltage rating, then the volume of the collector increases. If the collector volume increases then the volume of charge in the collector, measured at the same saturation voltage, also increases. Therefore the required storage time for optimum turn-off increases and also the required negative drive energy increases.

Overdriving the transistor (ie. driving it well into saturation) also increases the volume of stored charge and hence the required storage time for optimum turn-off. Conversely, the required storage time for a particular device can be reduced by using a desaturation network such as a Baker clamp. The Baker clamp reduces the volume of stored charge by holding the transistor out of heavy saturation.

Note 3. *The required storage time for optimum turn-off and the required negative drive energy will both increase as the volume of stored charge in the collector is increased.*

The reverse base current reaches its peak value at about the same time as the collector current reaches its peak value. The turn-off waveforms are shown in Fig. 20.

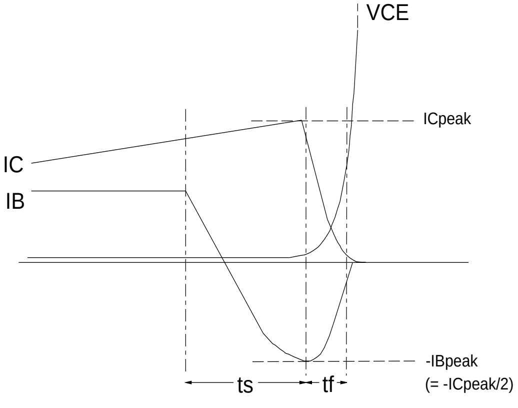


Fig. 20 Turn off waveforms.

Note 4. *For optimum turn-off of any transistor, the peak reverse base current should be half of the peak collector current and the negative drive voltage should be between 2 and 5 volts.*

As far as the collector voltage is concerned, the slower the dV/dt the lower the turn-off dissipation. Control of the collector dV/dt is achieved by the use of a snubber network (see Fig. 21). The snubber capacitor also controls the collector voltage overshoot and thus prevents overvoltage of the transistor.

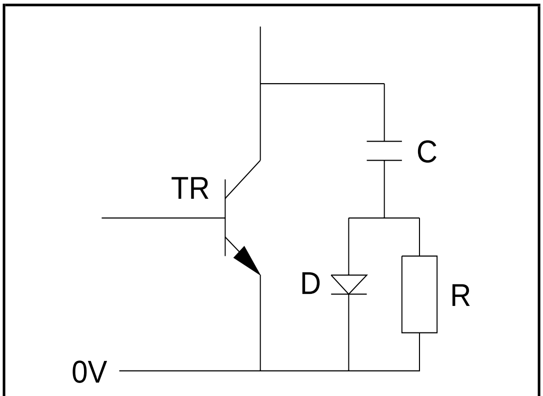


Fig. 21 RCD snubber.

High collector dV/dt at turn-off can bring an additional problem for the transistor. A charging current flows through the collector-base (Miller) capacitance of the device, and according to the law, I = C x dV/dt, this charging current increases in magnitude with increasing dV/dt. If this current enters the base then the transistor can begin to turn back on. Control of the collector dV/dt is usually enough to prevent this from happening. If this is insufficient then the base-emitter impedance must be reduced by applying a resistor and/or capacitor between base and emitter to shunt some of this current.

Note 5. *High collector dV/dt at turn-off leads to parasitic turn-on if the charging current of the transistor Miller capacitance is not shunted away from the base.*

High collector dI/dt at turn-off can also bring problems if the inductance between the emitter and the base ground reference is too high. The falling collector current will induce a voltage across this inductance which takes the emitter more negative. If the voltage on the emitter falls below the voltage on the base then the transistor can begin to turn back on. This problem is more rare but if it does arise then adding a resistor and/or capacitor between base and emitter helps to keep the base and emitter more closely coupled. At all times it is important to keep the length of the snubber wiring to an absolute minimum.

Note 6. *High collector dI/dt at turn-off leads to parasitic turn-on if the inductance between the emitter and the base ground reference is too high.*

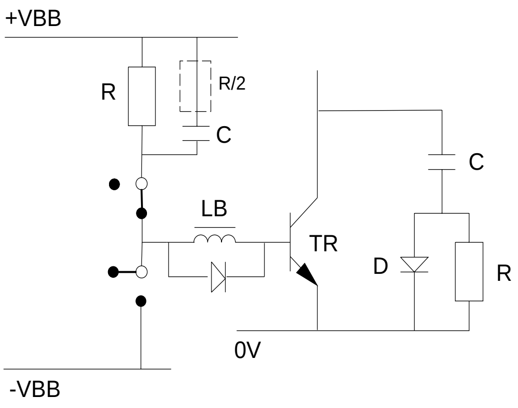


Fig. 22 HVT environment.

Improving reliability

In the majority of cases, the most stressful circuit conditions occur during power up of the SMPS, when the base drive is least well defined and the collector current is often at its highest value. However, the electrical environment at power up is very often hardly considered, and potentially destructive operating conditions go unnoticed.

A very common circuit reliability problem is RBSOA failure occurring on the very first switching cycle, because the reverse drive to the base needs several cycles to become established. With no negative drive voltage on the base of the transistor, the RBSOA is reduced (as discussed earlier). To avoid RBSOA failure, the collector voltage must be kept below V_{CEOmax} until there is sufficient reverse drive energy available to hold the base voltage negative during the turn-off phase.

Even with the full RBSOA available, control of the rate of rising collector voltage through the use of a snubber is often essential in order to keep the device within the specified operating limits.

Note 1. *The conditions at power up often come close to the safe operating limits. Until the negative drive voltage supply is fully established, the transistor must be kept below its* V_{CEOmax}.

Another factor which increases the stress on many components is increased ambient temperature. It is essential that the transistor performance is assessed at the full operating temperature of the circuit. As the temperature of the transistor chip is increased, both turn-on and turn-off losses may also increase. In addition to this, the quantity of stored charge in the device rises with temperature, leading to higher reverse base drive energy requirements.

Note 2. *Transistor performance should be assessed under all operating conditions of the circuit, in particular the maximum ambient temperature.*

A significant proportion of power supply reliability problems could be avoided by applying these two guidelines alone. By making use of the information on how to improve turn-on and turn-off, small design changes can be made to the circuit which will enhance the electrical performance and reliability of the transistor, leading to a considerable improvement in the performance and reliability of the power supply as a whole.

2.1.3 Base Circuit Design for High Voltage Bipolar Transistors in Power Converters

Fast, high voltage switching transistors such as the BUT211, BUT11, BUT12, BUT18, BUW13, BU1508, BU2508, BU1706 and BU1708 have all helped to simplify the design of converter circuits for power supply applications. Because the breakdown voltage of these transistors is high (from 850 to 1750V), they are suitable for operation direct from the rectified 110V or 230V mains supply. Furthermore, their fast switching properties allow the use of converter operating frequencies up to 30kHz (with emitter switching techniques pushing this figure past 100kHz).

The design of converter circuits using high-voltage switching transistors requires a careful approach. This is because the construction of these transistors and their behaviour in practical circuits is different from those of their low-voltage counterparts. In this article, solutions to base circuit design for transistor converters and comparable circuits are developed from a consideration of the construction and the inherent circuit behaviour of high voltage switching transistors.

Switching behaviour

Figure 1 shows a complete period of typical collector voltage and current waveforms for a power transistor in a switching converter. The turn-on and turn-off intervals are indicated. The switching behaviour of the transistor during these two intervals, and the way it is influenced by the transistor base drive, will now be examined.

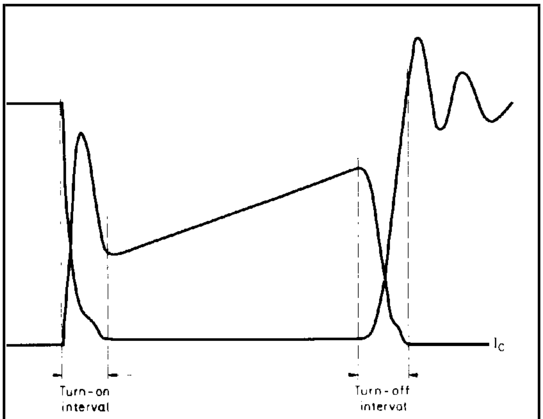


Fig. 1 V_{CE} and I_C waveforms during the conduction period for a power transistor in an S.M.P.S.

Turn-on behaviour

A particular set of voltage and current waveforms at the collector and base of a converter transistor during the turn-on interval is shown in Fig. 2(a). Such waveforms are found in a power converter circuit in which a (parasitic) capacitance is discharged by a collector current pulse at transistor turn-on. The current pulse due to this discharge can be considered to be superimposed on the trapezoidal current waveform found in basic converter operation.

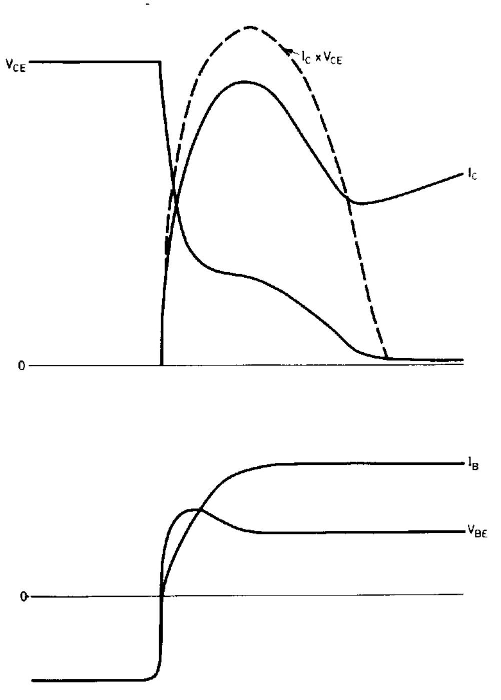


Fig. 2(a) Turn-on waveforms of a practical converter circuit.

A positive base current pulse I_B turns on the transistor. The collector-emitter voltage V_{CE} starts to decrease rapidly and the collector current I_C starts to increase. After some time, the rate of decrease of V_{CE} reduces considerably and V_{CE} remains relatively high because of the large collector current due to the discharge of the capacitance. Thus, the turn-on transient dissipation (shown by a broken line) reaches a high value.

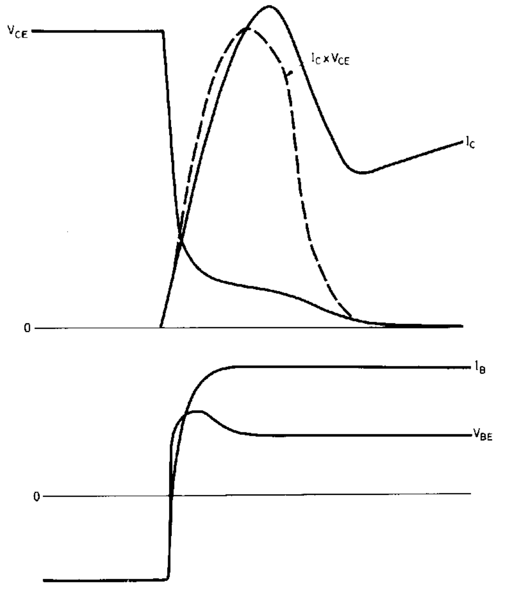


Fig. 2(b) Turn-on waveforms: fast-rising base current pulse.

The collector current then decreases to a trough before assuming the normal trapezoidal waveform. This is again followed by a rapid decrease in V_{CE}, which reaches the saturation value defined by the collector current and base current of the particular transistor.

Figure 2(b) depicts a similar situation but for a greater rate of rise of the base current. The initial rapid decrease in V_{CE} is maintained until a lower value is reached, and it can be seen that the peak and average values of turn-on dissipation are smaller than they are in Fig. 2(a).

Figure 2(c) shows the effect on the transistor turn-on behaviour of a very fast rising base current pulse which initially overshoots the final value. The collector-emitter voltage decreases rapidly to very nearly the transistor saturation voltage. The turn-on dissipation pulse is now lower and much narrower than those of Figs. 2(a) and 2(b).

From the situations depicted in Figs. 2(a), 2(b) and 2(c), it follows that for the power transistor of a converter circuit the turn-on conditions are most favourable when the driving base current pulse has a fast leading edge and overshoots the final value of I_B.

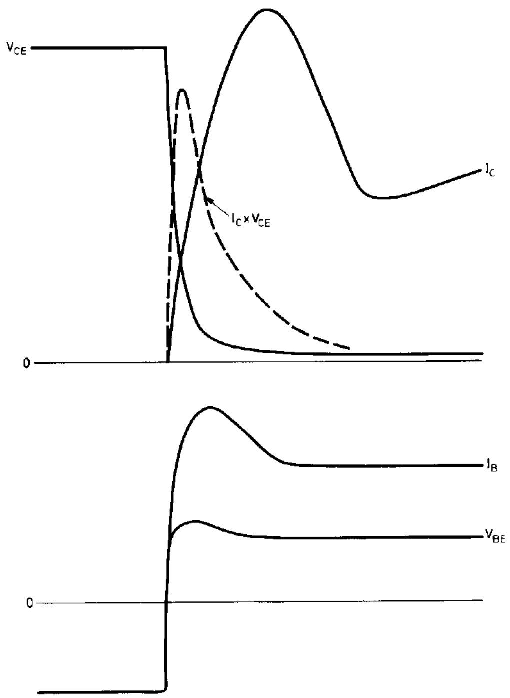


Fig. 2(c) Turn-on waveforms: very fast-rising base current pulse with overshoot.

Turn-off behaviour

The waveforms which occur during the turn-off interval indicated in Fig. 1 are shown on an expanded timescale and with four different base drive arrangements in Figs. 3(a) to 3(d). These waveforms can be provided by base drive circuits as shown in Figs. 4(a) to 4(c). The circuit of Fig. 4(a) provides the waveforms of Fig. 3(a); the circuit of Fig. 4(b) those of Fig. 3(b) and, with an increased reverse drive voltage, Fig. 3(c). The circuit of Fig. 4(c) provides the waveforms of Fig. 3(d). The waveforms shown are typical of those found in the power switching stages of S.M.P.S. and television horizontal deflection circuits, using high-voltage transistors.

In practical circuits, the waveform of the collector-emitter voltage is mainly determined by the arrangement of the collector circuit. The damping effect of the transistor on the base circuit is negligible except during the initial part of the turn-off period, when it only causes some delay in the rise of the V_{CE} pulse.

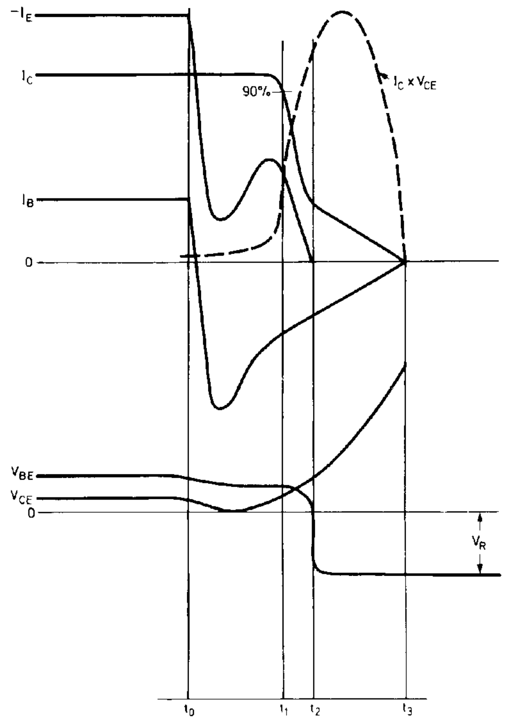


Fig. 3(a) Turn-off waveforms; circuit with speed-up capacitor.

The $I_C \times V_{CE}$ (turn-off dissipation) pulse is dependent on both the transistor turn-off time and the collector current waveshape during turn-off. Turn-off dissipation pulses are indicated in Figs. 3(a) to 3(d) by the dashed lines.

The circuit of Fig. 4(a) incorporates a speed-up capacitor, an arrangement often used with low-voltage transistors. The effect of this is as shown in Fig. 3(a), a very rapid decrease in the base current I_B, which passes through a negative peak value, and becomes zero at t_3. The collector current I_C remains virtually constant until the end of the storage time, at t_1, and then decreases, reaching zero at t_3. The waveform of the emitter current, I_E, is determined by I_C and I_B, until it reaches zero at t_2, when the polarity of the base-emitter voltage V_{BE} is reversed.

After time t_2, when V_{BE} is negative and I_E is zero, the collector base currents are equal and opposite, and the emitter is no longer effective. Thus, the further decrease of collector current is governed by the reverse recovery process of the transistor collector-base diode. The reverse recovery 'tail' of I_C (from t_2 to t_3) is relatively long, and it is clear the turn-off dissipation is high.

In the circuit of Fig. 4(b) the capacitor is omitted. Fig. 3(b) shows that the negative base current is limited to a considerably lower value than in the previous case. All the currents I_B, I_C and I_E reach zero at time t_3. The transistor emitter base junction becomes reverse biased at t_2, so that during the short interval from t_2 to t_3 a small negative emitter current flows.

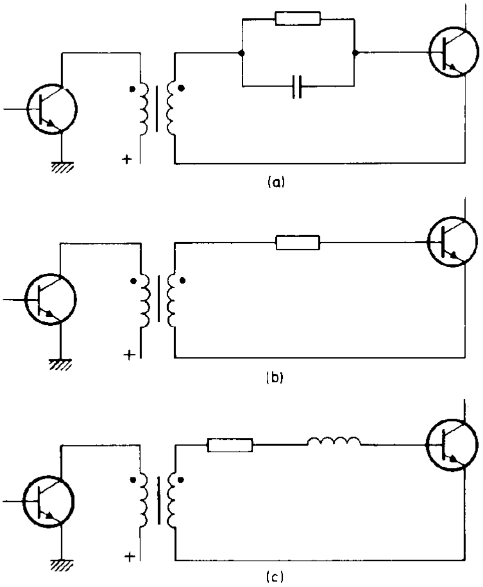


Fig. 4 Base circuits for turn-off base drive. The driver transistor is assumed to be bottomed to turn off the power transistor.
(a) With speed-up capacitor.
(b) Without speed up capacitor.
(c) With series inductor.

The emitter current, determined by the collector current and by the (driven) base current, therefore maintains control over the collector until it reaches zero. Furthermore, the collector current has a less pronounced tail and so the fall time is considerably shorter than that of Fig. 3(a). The turn-off dissipation is also lower than in the previous case.

Increasing the reverse base drive voltage in the circuit of Fig. 4(b), with the base series resistance adjusted so that the same maximum reverse base current flows, gives rise to the waveforms shown in Fig. 3(c). The collector current tail is even less pronounced, and the fall time shorter than in Fig. 3(b).

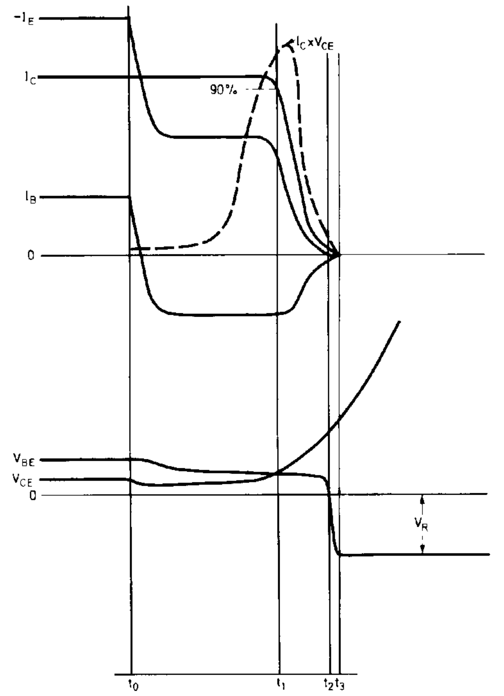


Fig. 3(b) Turn-off waveforms: circuit without speed-up capacitor.

A further improvement in turn-off behaviour can be seen in the waveforms of Fig. 3(d), which are obtained by including an inductor in the base circuit as in Fig. 4(c). The rate of change of the negative base current is smaller than in the preceding cases, and the negative peak value of the base current is smaller than in Fig. 3(a). The collector current I_C reaches zero at t_3, and from t_3 to t_4 the emitter and base currents are equal. At time t_2 the polarity of V_{BE} is reversed and the base-emitter junction breaks down. At time t_4 the negative base-emitter voltage decreases from the breakdown value $V_{(BR)EBO}$ to the voltage V_R produced by the drive circuit.

The collector current fall time in Fig. 3(d) is shorter than in any of the previous cases. The emitter current maintains control of the collector current throughout its decay. The large negative value of V_{BE} during the final part of the collector current decay drives the base-emitter junction into breakdown, and the junction breakdown voltage determines the largest possible reverse voltage. The turn-off of the transistor is considerably accelerated by the application (correctly timed) of this large base emitter-voltage, and the circuit gives the lowest turn-off dissipation of those considered.

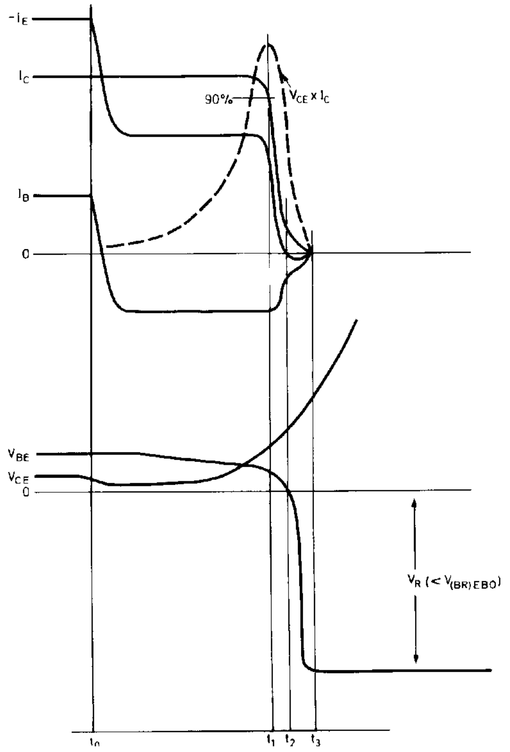


Fig. 3(c) Turn-off waveforms: circuit without speed-up capacitor, with increased reverse drive voltage.

The operation of the base-emitter junction in breakdown during transistor turn-off, as shown in Fig. 3(d), has no detrimental effect on the behaviour of transistors such as the BUT11 or BU2508 types. Published data on these transistors allow operation in breakdown as a method of achieving reliable turn-off, provided that the $-I_{B(AV)}$ and $-I_{BM}$ ratings are not exceeded.

It is evident from Figs. 3(a) to 3(d) that the respective turn-off dissipation values are related by:-

$$P_{off(a)} > P_{off(b)} > P_{off(c)} > P_{off(d)}$$

The fall times (related in each case to the interval from t_1 to t_3) are given by:-

$$t_{f(a)} > t_{f(b)} > t_{f(c)} > t_{f(d)}$$

The storage times (equal to the interval from t_0 to t_1) are:-

$$t_{s(a)} < t_{s(b)} < t_{s(d)}$$

where the subscripts (a), (b), (c) and (d) refer to the waveforms of Figs. 3(a), 3(b), 3(c) and 3(d) respectively. It follows that the circuit of Fig. 4(c), which provides the waveforms of Fig. 3(d), gives the most favourable turn-off power dissipation. It has, however, the longest storage time.

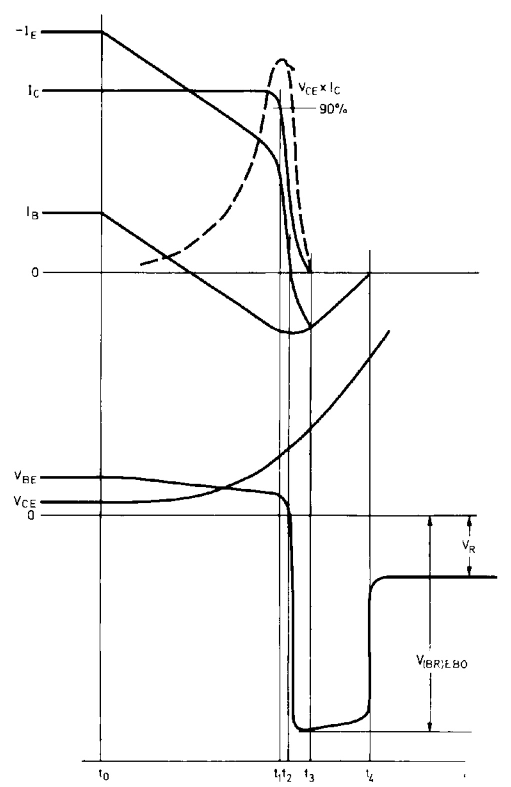


Fig. 3(d) Turn-off waveforms: circuit with series inductor.

From consideration of the waveforms in Figs. 3(a) to 3(d), it can be concluded that optimum turn-off of a high voltage transistor requires a sufficiently long storage time determined by the turn-off base current and a sufficiently large negative base-emitter voltage correctly timed with respect to the collector current waveform.

The phenomena which have been described in this section become more pronounced when the temperature of the operating junction of the transistor is increased: in particular, the fall times and storage times are increased. The design of a base drive circuit should therefore be checked by observing the waveforms obtained at elevated temperatures.

Optimum base drive circuitry

From the foregoing study of the required base current and base-emitter voltage waveforms, a fundamental base circuit arrangement to give optimum turn-on and turn-off of high voltage switching transistors will now be determined. It will be assumed that the driver stage is transformer-coupled to the base, as in Fig. 5(a), and that the driver transformer primary circuit is such that a low impedance is seen, looking into the secondary, during both the forward and reverse drive pulses. The complete driver circuit can then be represented as an equivalent voltage source of $+V_1$ volts during the forward drive period and $-V_2$ volts during the reverse drive/bias period. This is shown in Fig. 5(b).

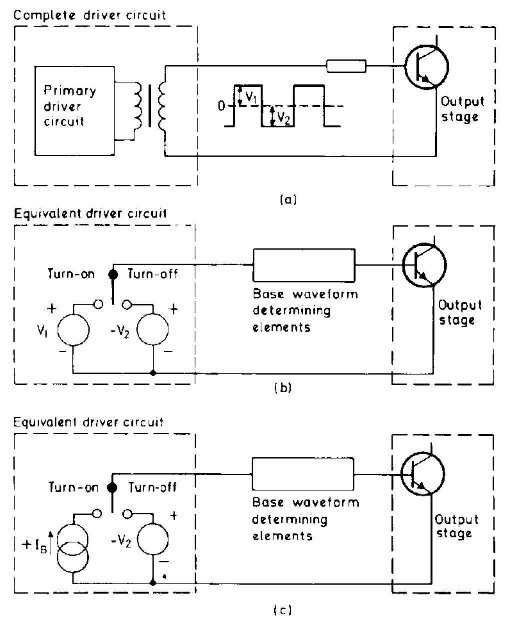


Fig. 5 (a) Schematic drive circuit arrangement.
(b) Equivalent drive circuit arrangement.
(c) Equivalent circuit for current source forward drive.

Forward base drive can also be obtained from a circuit which acts as a current source rather than a voltage source. This situation, where the reverse drive is still obtained from a voltage source, is represented in Fig. 5(c). The basic circuit arrangements of Figs. 5(b) and 5(c) differ only with respect to forward drive, and will where necessary be considered separately.

Comparable base drive waveforms can, of course, be obtained from circuits differing from those shown in Figs. 5(b) and 5(c). For such alternative circuit configurations the following discussion is equally valid.

Base series resistor

Most drive circuits incorporate a resistor R_B in series with the base. The influence of the value of this resistor on the drive characteristic will be briefly discussed.

Voltage source forward drive.

In circuits with a voltage source for forward drive, shown in a simplified form in Fig. 6(a), the following parameters determine the base current:-

The transistor base characteristic ;

The value of the base resistor R_B;

The forward drive voltage V_1.

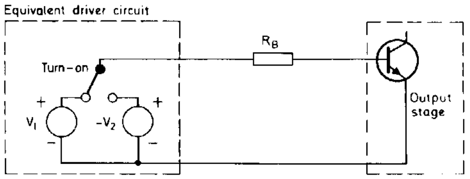


Fig. 6(a) Drive circuit with base resistor R_B and voltage source forward drive.

Figure 6(b) shows how the tolerances in these parameters affect the base current. It is clear that to avoid large variations in I_B, the tolerances in R_B and V_1 should be minimised. The voltage drop across R_B reduces the dependence of I_B on the spreads and variations of the transistor $V_{BE(on)}$. For good results the voltage drop across R_B must not be less than $V_{BE(on)}$.

Current source forward drive

In circuits where a current source is used for forward drive, the forward base current is independent of spreads and variations of $V_{BE(on)}$. The base current level and tolerances are governed entirely by the level and tolerances of the drive. A separate base series resistor is therefore unnecessary, but is nevertheless included in many practical current-source-driven circuits, to simplify the drive circuit design. The following discussions will assume that a series base resistor R_B always forms part of the base drive network.

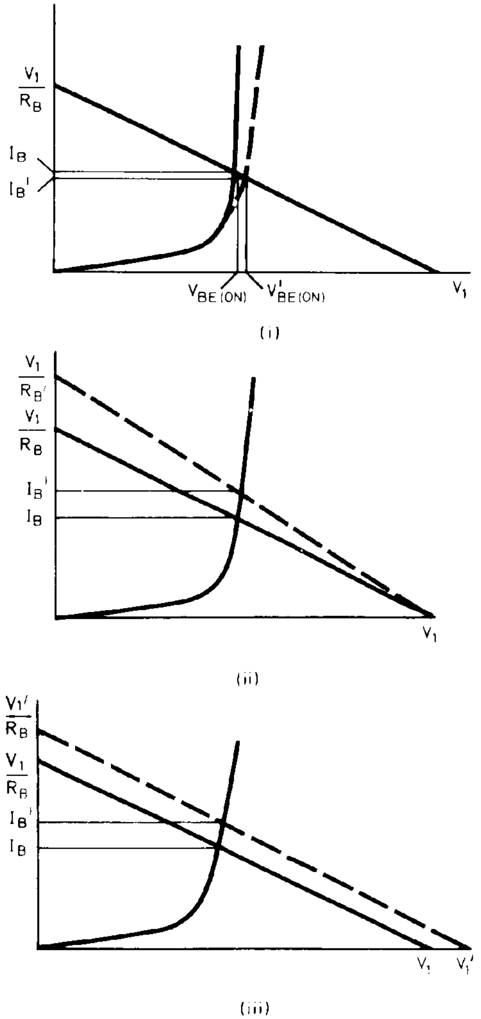


Fig. 6(b) Effects on the value of I_B on circuit tolerances.
(i) Variation of transistor base characteristic.
(ii) Variation of value of resistor R_B.
(iii) Variation of drive voltage V_1.

Turn-off arrangement

To initiate collector current turn-off, the drive voltage is switched at time t_0 from the forward value $+V_1$ to the reverse value $-V_2$.

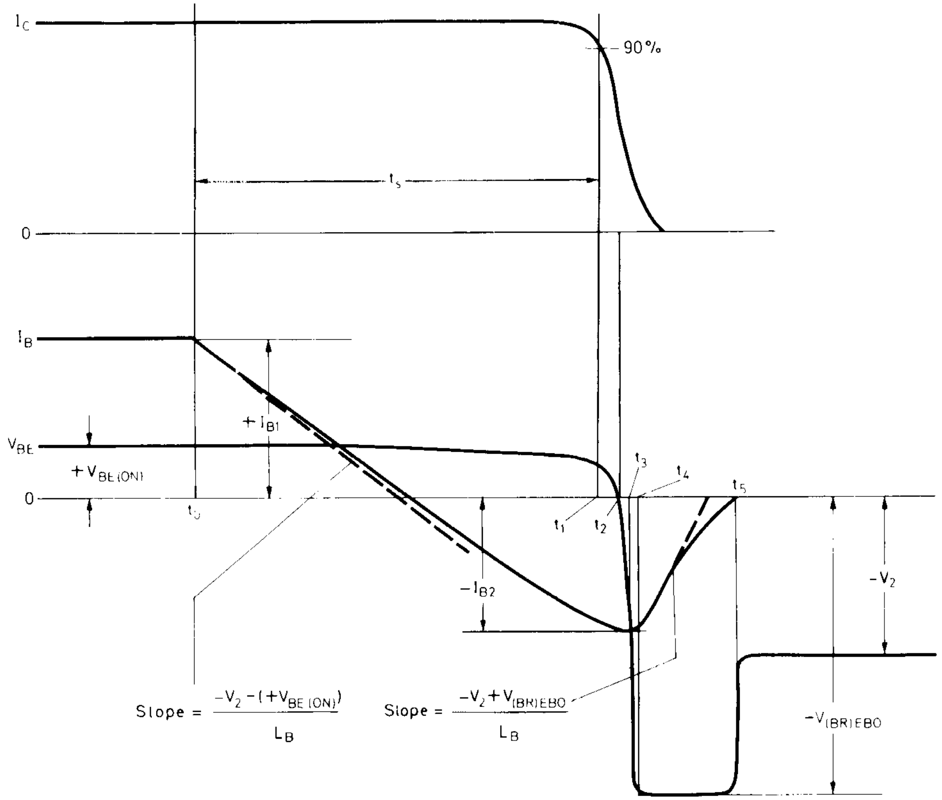


Fig. 7(a) Turn-off waveforms of the circuit of Fig. 7(b).

The desired turn-off voltage and current waveforms are obtained by adding various circuit elements to the basic resistive circuit of Fig. 6(a). A convenient method of achieving the desired slowly-decreasing base current is to use a series inductor L_B as shown in Fig. 7(b). The turn-off waveforms obtained by this method are shown in Fig. 7(a).

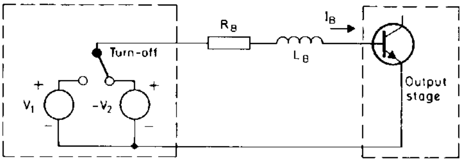


Fig. 7(b) Base drive circuit with series inductor.

Base series inductor

At time t_0 the base current starts to decrease from the forward drive value I_{B1} with a slope equal to:-

$$\frac{-V_2 \quad - \quad (+V_{BE(on)})}{L_B}$$

For a considerable time after t_0, the (decreasing) input capacitance of the transistor maintains a charge such that there is no perceptible change in V_{BE}. At time t_2 the amount of charge removed by the negative base current ($-I_B$) is insufficient to maintain this current, and its slope decreases.

At time t_3, when:-

$$\frac{d\,I_B}{dt}=0 \quad where \quad I_B=I_{B2}$$

$$V_{BE} \quad = \quad -V_2 - R_B I_{B2}$$

Immediately after t_3, the stored energy in L_B gives rise to a voltage peak tending to increase the reverse bias of the transistor. The voltage is clamped by the base-emitter breakdown voltage, so that:-

$$V_{BE} \quad = \quad -V_{(BR)EBO}$$

At time t_4 the negative base current starts to decrease with an initial slope equal to:-

$$\frac{-V_2 \quad + \quad V_{(BR)EBO}}{L_B}$$

At t_5 the base current reaches zero. The base-emitter voltage then changes from $-V_{(BR)EBO}$ to the value $-V_2$, the level of the drive voltage. As has been demonstrated, the collector storage time, t_s, is an important parameter of the drive circuit turn-off behaviour. Fig. 7(a) shows that the value of t_s can be calculated approximately from:-

$$\frac{-V_2 \quad + \quad V_{(BR)EBO}}{L_B} . t_s \quad = \quad I_{B1} - I_{B2}$$

and this expression is sufficiently accurate in practice. In most cases the base current values are related by:-

$$\left(\frac{I_{B2}}{I_{B1}} \right) \quad \approx \quad 1 \quad to \quad 3$$

In the case where $(-I_{B2} / I_{B1}) = 2$, the collector storage time is given by:-

$$t_s \quad = \quad \frac{3 I_{B1} L_B}{-V_2 \quad - \quad (+V_{BE(on)})}$$

In practical circuits, design considerations frequently indicate a relatively small value for V_2. The required value of t_s is then obtained with a small value of L_B, and consequently the energy stored in the inductor $(1/2\ L_B I_{B2}^2)$ is insufficient to maintain the base-emitter junction in the breakdown condition. Figure 7(a) shows that breakdown should continue at least until the collector current is completely turned off. The higher the transistor junction temperature, the more stored energy is necessary to maintain breakdown throughout the increased turn-off time.

These phenomena are more serious in applications where the storage time must be short, as is the case for the BUT12 or BUW13 transistors, for example. For horizontal deflection output transistors such as the BU508 and BU2508, which require a much longer storage time, the base inductance usually stores sufficient energy for correct turn-off behaviour.

Diode assisted base inductor

It is possible to ensure the storage of sufficient turn-off energy by choosing a relatively large value for V_2. Where a driver transformer is employed, there is then a corresponding increase in V_1. To obtain the desired value of forward base current, the base resistance R_B must also be large. A large value of R_B, however, diminishes the effect of L_B on the transistor turn-off behaviour, unless R_B is bypassed by a diode as in Fig. 8.

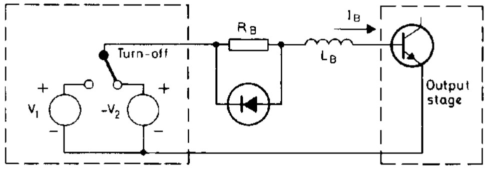


Fig. 8 Base drive circuit with diode-assisted series inductor.

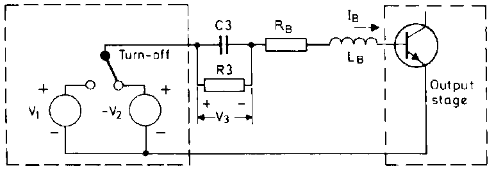


Fig. 9 Base drive circuit extended for improved turn-off behaviour.

Turn-off RC network

Improved turn-off behaviour can be obtained without increasing V_2, if additional circuit elements are used. An arrangement used in practice is shown in Fig. 9, and consists of network R_3C_3 which is connected in series with R_B and L_B.

A voltage V_3 is developed across C_3 because of the forward base current. (This voltage drop must be compensated by a higher value of V_1). When reverse current flows at turn-off, the polarity of V_3 is such that it assists the turn-off drive voltage V_2. Using the same approximation as before, the storage time is given by:-

$$t_s \quad = \quad \frac{3 I_{B1} L_B}{-(V_2 + V_3) \quad - \quad (+V_{BE(on)})}$$

The same value of t_s now requires a larger value of L_B. The energy stored in L_B is therefore greater and the transistor can more reliably be driven into breakdown for the time required.

The waveforms of Fig. 7(a) are equally applicable to the circuit of Fig. 9, if V_2 is replaced by $(V_2 + V_3)$. In practice V_3 will not remain constant throughout the storage time, and replacing V_3 by its instantaneous value will make a slight difference to the waveforms.

Turn-on arrangements

It has been shown that for optimum turn-on of a high voltage switching transistor, the turn-on base current pulse must have a large amplitude and a fast leading edge with overshoot. However, the inductance L_B included in the circuits derived for optimum turn-off (Figs. 7 to 9) makes it difficult to produce such a turn-on pulse. The additional components (R_1, C_1, D_1) in the circuit of Fig. 10(a) help to solve this problem as shown by the waveforms of Fig. 10(b).

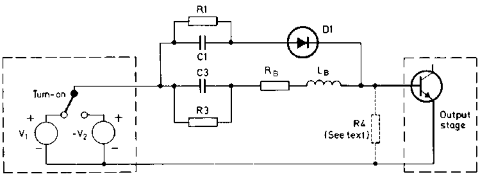


Fig. 10(a) Base drive circuit extended for improved turn-on behaviour with voltage source drive.

At the instant of turn-on, network R_1C_1 in series with D_1 provides a steep forward base current pulse. The turn-off network is effectively by-passed during the turn-on period by C_1 and D_1. The time-constant R_1C_1 of the turn-on network should be chosen so that the forward current pulse amplitude is reduced virtually to zero by the time the transistor is turned on.

The turn-on network of Fig. 10(a) can also be added to the diode-assisted turn-off circuit of Fig. 8. In circuits which are forward driven by a current source, the overshoot required on the turn-on base current pulse must be achieved by appropriate current source design.

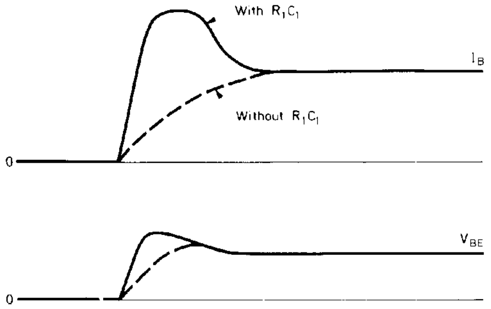


Fig. 10(b) Turn-on waveforms of the circuit of Fig.10(a).

Practical circuit design

The base drive circuit of Fig. 10(a) combines the drive voltage sources $+V_1$ and $-V_2$ with circuit elements R_B, L_B, R_3C_3 and $R_1C_1D_1$ which, if correctly dimensioned, allow optimum transient behaviour of the switching transistor. Not all these elements, however, will be necessary in every case for good results.

In circuits where the collector current rate of rise is limited by collector circuit inductance, the turn-on network $R_1C_1D_1$ can be omitted without danger of excessive collector dissipation at turn-on. In circuits where the base series inductance L_B is sufficiently large to give complete turn-off, network R_3C_3 can be omitted. Networks $R_1C_1D_1$ and R_3C_3 are superfluous in horizontal deflection circuits which use BU508, BU2508 transistors or similar types.

A discrete component for inductance L_B need not always be included, because the leakage inductance of the driver transformer is sometimes sufficient.

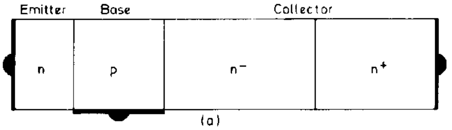
The omission of R_B from circuits which are forward driven by a voltage source should generally be considered bad design practice. It is, however, possible to select component values such that the functions of R_1C_1 and R_3C_3 are combined in a single network.

In some cases, the circuits of Figs. 7 to 10 may generate parasitic oscillations (ringing). These can usually be eliminated by connecting a damping resistor R_4 between the transistor base and emitter, as shown in broken lines in Fig. 10(a).

Physical behaviour of high-voltage switching transistors

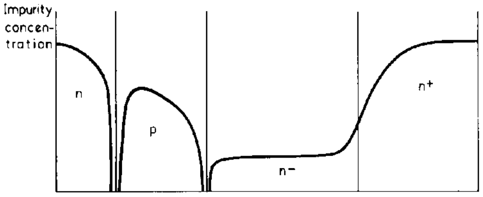
Base circuit design for high-voltage switching transistors will now be considered with respect to the physical construction of the devices. To achieve a high breakdown voltage, the collector includes a thick region of high resistivity material. This is the major difference in the construction of high and low voltage transistors.

The construction of a triple-diffused high voltage transistor is represented schematically in Fig. 11(a). The collector region of an n-p-n transistor comprises a high resistivity n-region and a low resistivity n+ region. Most of the collector voltage is dropped across the n- region. For semiconductor material of a chosen resistivity, the thickness of the n- region is determined by the desired collector breakdown voltage. The thickness of the n+ region is determined by technological considerations, in particular the mechanical construction of the device. Fig. 11(b) shows the impurity concentration profile of the transistor of Fig. 11(a).



(a)

Fig. a — Schematic representation of a triple-diffused high-voltage n-p-n transistor



(b)

Fig.b — Impurity concentration profile of the transistor

Fig. 11 High voltage switching transistor.

For good switching performance, the high voltage blocking characteristic of the transistor structure must be modified at transistor turn-on, so that a low forward voltage condition is exhibited. One method of achieving this is to inject a large number of carriers through the base to the collector region. The high resistivity of the n- region is then "swamped" by excess carriers. This effect is often referred to as a collector-width modulation.

The following discussion of the physical changes which occur at transistor turn-on and turn-off is based on a much simplified transistor model; that is, the one dimensional charge control model. Fig. 12 shows such a model of a low-voltage transistor, and assumes a large free carrier-to-doping concentration ratio in the base due to the carriers injected from the emitter. Line *a* represents the free carrier concentration in the base for transistor operation in the active region (V_{CB}>0), and line *c* that for the saturated condition (V_{CB}<0). Line *b* represents the concentration at the onset of saturation, where V_{CB}=0. The slope of the free carrier concentration line at the collector junction is proportional to the collector current density, and therefore, to the collector current.

Turn-on behaviour

The carrier concentration profile of a high-voltage transistor during turn-on is shown in Fig. 13(a). Line 1 represents a condition where relatively few carriers are injected into the base from the emitter. Let line 1 be defined as representing the onset of saturation for the metallurgic collector junction; that is, point 1(C'). In this case, V_{CB}=0, whereas the externally measured collector voltage is very high because of the voltage drop across the high-resistivity collector region.

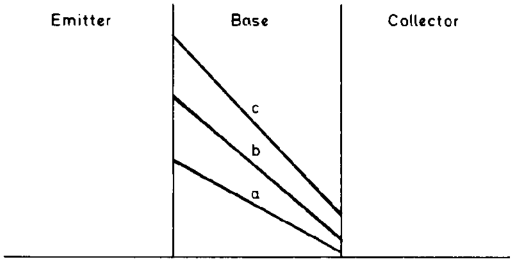


Fig. 12 Charge-control representation of a low-voltage transistor:
Line *a* in the active region
Line *b* nearing the onset of saturation
Line *c* heavily saturated condition

Line 2 in Fig. 13(a) represents a high level of carrier injection into the base from the emitter. Carriers have also penetrated the high-resistivity collector region as far as point 2(C'), and so the base region is now, in effect, extended to this point and the effective width of the collector region is reduced. The voltage drop across the collector region, caused by the collector current which is proportional to the concentration gradient at point 2(C'), is therefore less than the voltage drop which occurred with the level of carrier injection on line 1.

Lines 3, 4 and 5 represent still higher carrier injection levels, and hence decreasing effective collector widths. The voltage drop across the effective collector also decreases.

In the situation represented by line 6, the entire high resistivity collector region has been flooded with excess carriers. The collector-base voltage is therefore so low that the transistor is effectively saturated. The low saturation voltage has been obtained at the expense of a large base current, and this explains why a high-voltage transistor has a low current gain, especially at large collector currents.

Figure 13(b) shows simplified collector current/voltage characteristics for a typical high voltage transistor. Between lines OQ and OP, voltage V_{CE} progressively decreases as excess carriers swamp the high-resistivity collector region. Line OP can be regarded as the 'saturation' line.

When the transistor is turned on, the carrier injection level increases from the very small cut-off level (not shown in Fig. 13(a)) to the level represented by line 6 in Fig. 13(a). The transistor operating point therefore moves from the cut-off position along the locus shown in Fig. 13(b) to position 6, which corresponds to line 6 in Fig. 13(a). The effect of this process on I_C and V_{CE} is shown in Fig. 13(c), where the time axis is labelled 0 to 6 to correspond to the

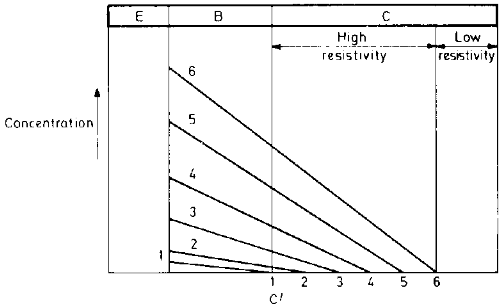


Fig.a — Turn-on behaviour of a high-voltage switching transistor: charge concentration during turn-on

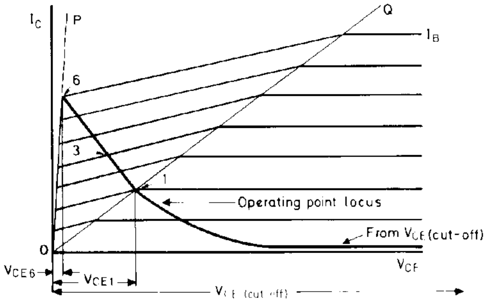


Fig. b — Turn-on excursion locus

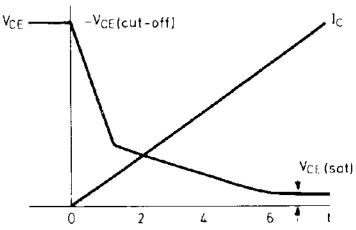


Fig.c — Turn-on waveforms

Fig. 13 Turn-on behaviour of high voltage switching transistor.

numbered positions on the operating point locus of Fig. 13(b) and the numbered lines on the carrier concentration diagram of Fig. 13(a).

The time taken to reach the emitter injection level 6 is directly proportional to the turn-on time of the transistor. The rate of build-up of emitter injection depends on the peak amplitude and rise time of the turn-on base current pulse. The shortest turn-on time is obtained from a large amplitude base current pulse with a fast leading edge. Thus, physical considerations support the conclusion already drawn from a study of the circuit behaviour of the transistor.

Turn-off behaviour

The carrier concentration in the saturated transistor at the beginning of the turn-off period is represented by line 0 in Fig. 14(a), corresponding to line 6 in Fig. 13(a). As shown in Fig. 14(b), the base current I_B gradually decreases, but I_C remains almost constant for some time, and $-I_E$ therefore decreases to match I_B. The resulting carrier concentration patterns are shown as lines 1 and 2 in Fig. 14(a). This process is plotted against time in Fig. 14(b) where, again, the graduation of the horizontal axis corresponds to that of the lines in Fig. 14(a).

At time point 3 the emitter current has reduced to zero, and is slightly negative until point 6. Thus the carrier concentration lines 4 and 5 have negative slope. Complete collector current cut-off is reached before point 6. (This situation is not represented in Fig. 14).

Excess carriers present in the collector region are gradually removed from point 0 onwards. This results in increasing collector voltage because of the increasing effective width of the high-resistivity collector region.

Figures 14(a) and 14(b) depict a typical turn-off process giving good results with high voltage transistors; the waveforms of Fig. 14(b) should be compared with those of Figs. 3(d) and 7(a). A different process is shown in Figs. 15(a) and 15(b). The initial situation is similar (line 0, Fig. 15(a)) but the base current has a steep negative slope. At time point 1 of Fig. 15(b), the emitter current $-I_E$ has reached zero, and so the carrier concentration line 1 has zero slope at the emitter junction. The emitter-base junction is effectively cut off and only the relatively small leakage current (not shown in Fig. 15(b)) is flowing. From point 1 onwards, therefore, the emitter has no influence on the behaviour of the transistor. The switching process is no longer 'transistor action', but the reverse recovery process of a diode. The carrier concentration pattern during this process is shown in Fig. 15(a) in broken lines, with zero slope at the emitter junction because the emitter is inoperative.

The reverse recovery process is slow because of the high resistivity of the collector region and the consequent slow decrease of collector current. (Collector and base currents are, of course, equal and opposite when the emitter is cut off). The turn-off dissipation increases progressively as the transition time from collector saturation to cut-off increases. Furthermore, at higher junction temperatures the reverse recovery charge, and hence the duration of the recovery process, is greater.

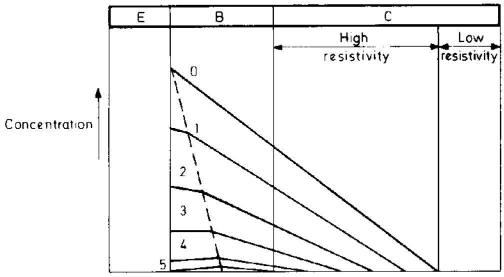


Fig. a — Turn-off behaviour of a correctly-driven high-voltage switching transistor: charge concentration during turn-off

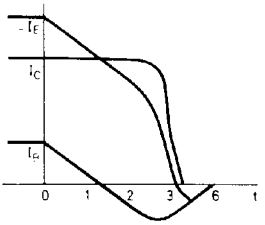


Fig. b — Turn-off waveforms

Fig. 14 Turn-off behaviour.

The longer the turn-off time, the greater the turn-off dissipation and, hence, the higher the device temperature which itself causes a further increase in turn-off time and dissipation. To avoid the risk of thermal runaway and subsequent transistor destruction which arises under these conditions, the turn-off drive must be such that no part of the turn-off is governed by the reverse recovery process of the collector base diode. Actual transistor action should be maintained throughout the time when an appreciable amount of charge is present in the transistor collector and base regions, and therefore the emitter should continue to operate to remove the excess charge.

There are many conditions of transistor turn-off which lie between the extreme cases of Figs. 14(a) and 15(a). Circuits in which the operating conditions tend towards those shown in Fig. 15(a) must be regarded as a potential source of unreliability, and so the performance of such circuits at elevated temperatures should be carefully assessed.

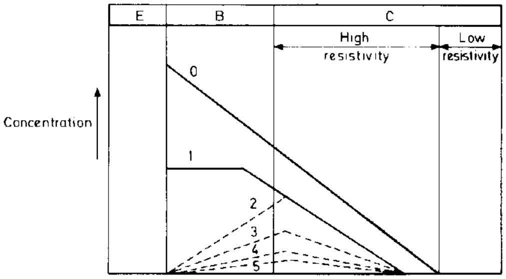


Fig. a — Turn-off behaviour of a high-voltage switching transistor with incorrect base drive: charge concentration during turn-off

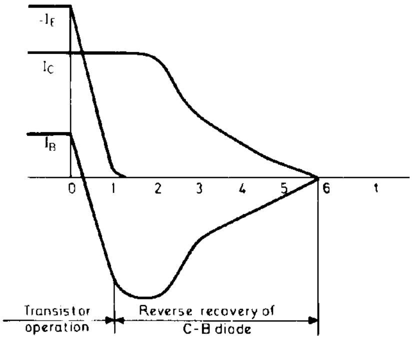


Fig. b — Turn-off waveforms

Fig. 15 Further turn-off waveforms.

2.1.4 Isolated Power Semiconductors for High Frequency Power Supply Applications

This section describes a 100 W off-line switcher using the latest component and application technology for cost-effective miniaturisation (see Ref.1). The power supply has a switching frequency of 500kHz with 1MHz output ripple. The section focuses on new power semiconductor components and, in particular, the need for good thermal management and electrical isolation. The isolated F-pack - SOT-186, SOT-199 and the new SOT-186A - are introduced. Philips has developed these packages for applications in S.M.P.S. The importance of screening to minimise conducted R.F.I. is covered and supported with experimental results.

Introduction

There is an ever-growing interest in high frequency power supplies and examples are now appearing in the market place. The strong motivation for miniaturisation is well founded and a comprehensive range of high frequency components is evolving to meet this important new application area, including:-

The output filter capacitor, which was traditionally an electrolytic type, can be replaced by the lower impedance multi-layer ceramic type.

The output filter choke may be reduced in size and complexity to a simple U-core with only a few turns.

The benefits of reduced transformer size can be realised at high frequency by using core materials such as 3F3. However, transformer size is ultimately limited by creepage and clearance distances defined by international safety standards.

Power MOSFETs provide the almost ideal switch, since they are majority carrier devices with very low switching losses. Similarly, Schottky diodes are the best choice for the output rectifiers.

This paper concentrates on the semiconductors and introduces three isolated encapsulations:- the ’F-packs’ - SOT-186, SOT-186A and SOT-199 - and applies them to high frequency S.M.P.S.

Power MOSFETs in isolated packages

Making power supplies smaller requires devices such as MOSFETs to be used as the power switch at high frequency. At this high frequency the size and efficiency of the output filter can be dramatically improved. Present abstract perception of acceptable inefficiency in power semiconductors remains constant i.e. 5 to 10% overall semiconductor loss at 500kHz is just as acceptable as at 50kHz. So throughout the trend to higher frequencies, the heatsink size has remained constant.

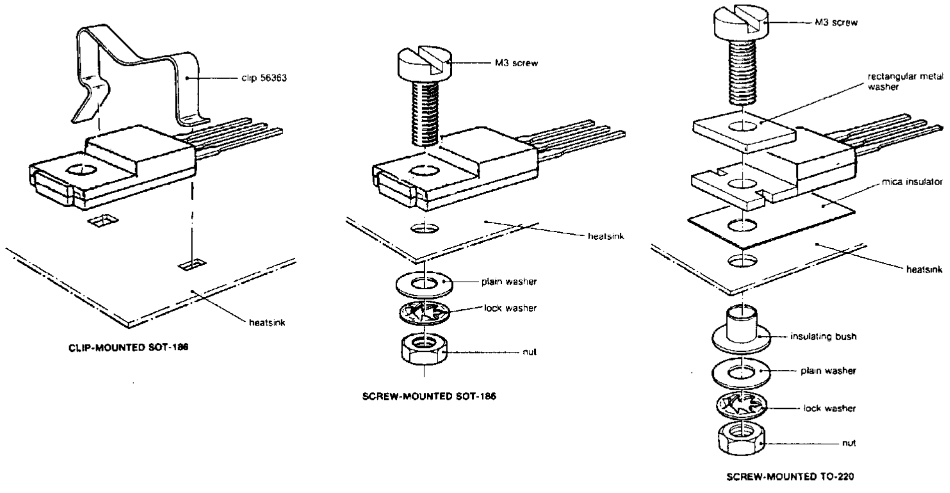


Fig. 1 Mounting of SOT-186 and TO-220 compared.

At 50kHz it is possible to use the earthed open frame of the power supply as the heatsink. Then all semiconductors are laid out around the periphery of the p.c.b. and mounted with isolation onto the heatsink. To gain the minimum overall size from high frequency operation, this technique must become standard practice to avoid having to leave clearance distances between primary and secondary side heatsinks. The component manufacturers are responding to the need for transistors with isolation by making them with a fully isolated package - the F-pack.

F-pack, SOT-186, is an encapsulation with a functionally isolating epoxy layer moulded onto its header; see Fig. 1. This allows a common heatsink to be used with no further isolation components. With just a spring clip, an insulated mounting (up to 1000V) of virtually all existing TO-220 components is possible without degrading performance. Screw mounted, the SOT-186 is still simplicity itself; there is no need for metal spacers, insulation bushes and mica insulators. Mounted either way, the F-pack reduces mounting hardware compared with that required for a standard TO-220.

The insulating layer of a SOT-186 can withstand more than 1000V, but the maximum voltage between adjacent leads is limited to 1000V. This is slightly less than the breakdown voltage between TO-220 legs due to the distance between the legs being reduced from 1.6mm to 1.05mm. However, the 375 µm thick epoxy gives more creepage and clearance between transistor legs and heatsink than a traditional mica washer of 50 µm. The capacitive coupling to an earthed heatsink is therefore reduced from 40pF to 13pF. This can be of significant help with the control of R.F.I.

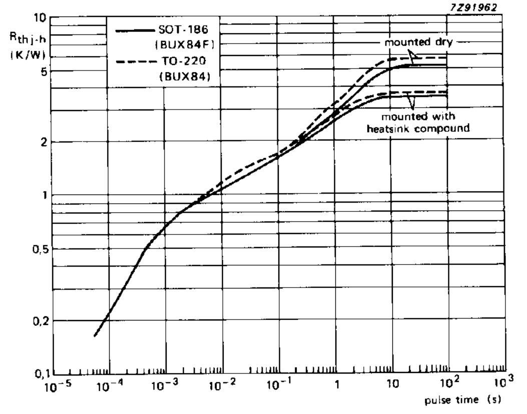


Fig. 2 Typical transient thermal response of SOT-186 and TO-220 packages (experimental).

The latest isolated package introduced by Philips is the SOT-186A. This is a fully encapsulated TO-220 replacement which provides true isolation from the heatsink of 2500V RMS. It is fully pin-compatible with the TO-220 package since it possesses the same distance between the leads and the back of the tab where thermal contact is made with the heatsink.

The transient thermal response of the SOT-186 and TO-220 encapsulations is shown in Fig. 2. A BUX84F (SOT-186) and a BUX84 (TO-220) were used for the test. Each transistor was mounted on a heatsink at 25˚C. The BUX84 was mounted on a mica washer. The test conditions were given by: Mounting force = 30N; I_E = 1A; V_{CB} = 10V.

The thermal resistance of the F-pack is better than the standard package in free air because it is all black and slightly larger. The difference is quite small, 55K/W for the SOT-186 and 70K/W for the TO-220. Mounted on a heatsink, the typical thermal resistance of the SOT-186 is slightly better than the standard TO-220, see Fig. 2. However, the exact value of $R_{th(mb\text{-}hs)}$ depends on the following:

- Whether heatsink compound is used.
- The screw's torque or pressure on the encapsulation.
- The flatness of the heatsink.

The flatness of the TO-220 metal heatsink is more controllable than the moulded epoxy on the back of the SOT-186. Therefore, the use of a heatsink compound with SOT-186 is of great importance. Once this is done the thermal characteristics of the two approaches are similar.

Schottky diodes in isolated packages

To be consistent with the small, single heatsink approach, the output rectifying diodes must be isolated from the heatsink too. Schottky diodes in SOT-186 are available, and encapsulations accommodating larger crystal sizes are available for higher powers. The F-pack version of the larger SOT-93 package is the SOT-199. Two Schottky diodes can be mounted in SOT-199 for power outputs up to a maximum of $I_{F(AV)}$ equal to 30 A. The SOT-199 package is similar to, but larger than, the SOT-186 shown in Fig. 1, and can be mounted similarly.

The epoxy isolation is thicker at 475µm. This further reduces the capacitive coupling to heatsink when compared to a Schottky diode isolated with either 50µm mica or 250µm alumina. Equally important is the increase in the breakdown voltage, from a guaranteed 1000V to 1500V. As with SOT-186, the use of heatsink compound is advised to give good thermal contact.

In conclusion, the combination of isolated packages allows an S.M.P.S. to be designed with many devices thermally connected to, but electrically isolated from, a single common heatsink.

Transistor characteristics affecting choice of high frequency converter

In this exercise only MOSFETs were considered practical for the target operating frequency of 500kHz. The range of converters to choose from is enormous if all the resonant circuits are included. The choice in this case is reduced by considering only the square wave types because:-

- The p.w.m technique is well understood.
- The main output is easily controlled over a wide range of input voltages and output loads.
- A resonant tank circuit, which may increase size, is not needed.

It is recognised that there are many situations and components which equally affect the choice of converter. The transformer component has been studied in Ref. 1. For maximum power through the transformer in a mains input, 500kHz, 100W power supply, a half-bridge converter configuration was chosen. The influence of the transistor is now examined.

The relationship of on-resistance $R_{DS(on)}$, with drain-source breakdown voltage, $V_{(BR)DSS}$, has been examined in Ref. 2. It was shown that $R_{DS(on)}$ is proportional to $V_{(BR)DSS}$ raised to the power 2. This implies equal losses for equal total silicon area. The advantage is therefore with the forward / flyback circuits because they have easier drive arrangements and often only require one encapsulation. Particular attention is paid to the frequency dependent losses, which are now considered.

C_{OSS} and the loss during turn-on

No matter how fast the transistor is switched in an attempt to avoid switching losses, there are always capacitances associated with the structure of the transistor which will dissipate energy each time the transistor is turned on and off. For a BUK456-800A, 800V MOSFET of 20mm^2 chip area, the turn-off waveform is shown in Fig. 3.

All loads have been reduced to nearly zero to highlight the turn-on current spike due to the capacitance of the circuit. The discharge of the output capacitance of the device will be similar but is unseen by the oscilloscope because it is completely internal to the device. The discharge of the energy is done in two different stages:-

Stage 1 - From the flyback voltage to the D.C link voltage.

This energy is mainly either returned to the supply or clamped in the inductance of the transformer by the secondary diodes, which release it to supply the load when the primary switch turns on. This energy is not dissipated in the power supply.

Stage 2 - From the link voltage to the on-state voltage.

This energy is dissipated in the transistor when it turns on. The calculation of the effective output capacitance at this voltage involves integration to take into account the varying nature of the capacitance with the applied drain voltage. The general expression for energy stored in the output capacitance of a MOSFET is:-

$$E = 3.3 \quad C_{oss(25V)} \quad V_d^{1.5}$$

For a BUK456-800A switching on with V_{DS} = 325V, the energy is 1.6 µJ. Gate to drain capacitance is not taken into account but would probably add about 20% extra dissipation to take it to 1.9µJ. This is for a transistor operating in a fixed frequency flyback, forward, or push-pull converter. A transistor in the half bridge circuit switches on from half the line voltage and so the losses in each transistor would be approximately a quarter of those in the previous converters. In self-oscillating power supplies the transistor switches on from 750 V. This would dissipate all of the stage (1) energy as well and so that could make approximately four times the loss in the transistor in this configuration. This example of a BUK456-800A operating at 500kHz, in a fixed frequency forward, flyback, or push pull system would dissipate 0.95 W internal to the device.

Stray capacitance around the circuit includes mounting base to heatsink capacitance, which for a ceramic isolator is 18pF. The energy for this is simply calculated by using 0.5 CV^2, and is 1µJ when charged to 325 V. F-pack reduces this by about a factor of two.

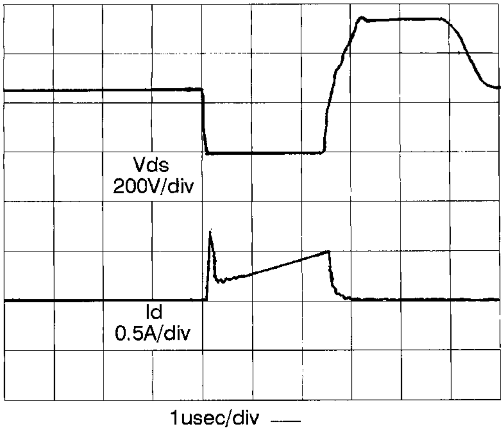


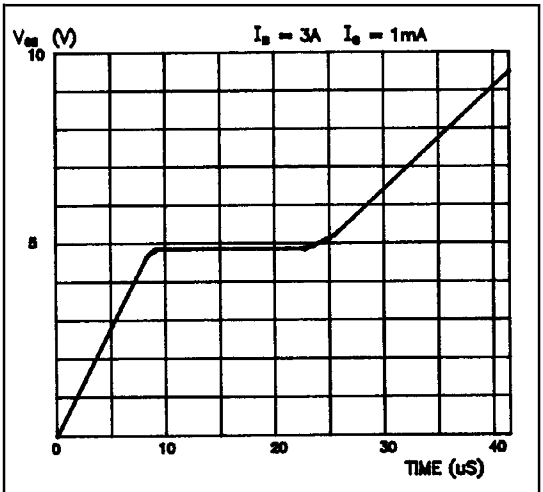
Fig. 3 MOSFET voltage and current waveforms in a forward converter.

In conclusion, the fixed frequency half-bridge system benefits from discharging from only half the d.c. link voltage and is the best choice to minimise these effects. There are two switches, so the overall benefit is only half, but the thermal resistance is also half, so the temperature rise of each transistor is actually four times less than in a forward converter. This makes this internal loss at 500kHz, 0.25 W in each transistor.

C_{ISS} and drive circuit losses

It is common to drive MOSFETs from a voltage source, through a series gate resistor. This gate resistor is seen usually to dampen stray inductance ringing with the gate capacitance during turn-on and turn-off of the transistor. This effectively prevents spurious turn-on. The resistor has another function when operating at a frequency of 500kHz, and that is to remove the dissipation of the energy of the gate capacitance from inside to outside the transistor. This is important because at frequencies in the MHz region the dissipation becomes the order of 1 W. A graph of charging the gate with a constant 1mA current source is shown in Fig. 4. The area under the curve was measured as 220µVs.

Therefore, at 10kHz, the power dissipation is 2mW and at 10MHz, 2W.



BUK455-500A
Fig. 4 Change of gate voltage with time for a power MOSFET with a 1mA constant charge current.

If the system chosen has two transistors, as in the half-bridge, then the dissipation will be doubled. Therefore, a single transistor solution is the most efficient to minimise these losses.

Concluding this section on the significant transistor characteristics, the power loss due to discharging internal MOSFET capacitances is seen to become significant around 500kHz to 1MHz, affecting the efficiency of a 100W converter. The predominant loss is output capacitance, which is discharged by, and dissipated in $R_{DS(on)}$. Converters which reduce this loss are those which switch from a lower V_{DS}, i.e.:-

- Resonant converters which switch at zero voltage.
- Converters designed for rectified 110V a.c. mains rather than 230V a.c. mains.
- Square-wave converters which use a half-bridge configuration rather than forward, flyback, or push-pull circuits.

Self oscillating power supplies give higher losses because they discharge from the flyback voltage of 750V at turn-on.

SMPS design considerations

There are two major areas which influence the choice of converter to be considered here:-

- multiple outputs

- R.F.I.

The influence of multiple outputs on the choice of converter.

If only one output is required then the half-bridge would be selected to minimise the loss due to output capacitance, as described above.

If multiple outputs are specified, and some of these require rectifying diodes other than Schottky diodes, then the switching loss of power epitaxial diodes has to be considered. Before the arrival of 100V Schottky diodes, epitaxial diodes would have been a natural first choice for outputs higher than 5V. However, a 12V auxiliary output often has less current than a 5V output, so MOSFETs can compete better on forward volt drop. Then there is switching loss: a MOSFET can have less loss than an epitaxial diode, but the actual frequency at which it becomes effective is debatable.

Synchronous MOSFET rectifiers were first seen as a threat to Schottky diodes for use in low voltage outputs. They could rectify with less forward volt drop, albeit sometimes at a cost. MOSFET rectifiers are now more of a threat to epitaxial diodes in higher voltage outputs above 15 to 20V. Applying these transistors is not as straightforward as it may first appear. Looking at flyback, forward and bridge outputs in turn:-

Flyback converter

A diode rectified output is replaced by a MOSFET, with no extra components added, (Fig. 5). Putting the transistor in the negative line and orientating it with the cathode of the parasitic diode connected to the transformer allows it to be driven well and does not threaten the gate oxide isolation. If the drive is slowed down by the addition of a gate resistor, the voltage across R_{DS} during transient switching can be large enough such that, when added to the output voltage, gives V_{GS} greater than that recommended in data. Fast turn-on is therefore essential for the good health of the transistor.

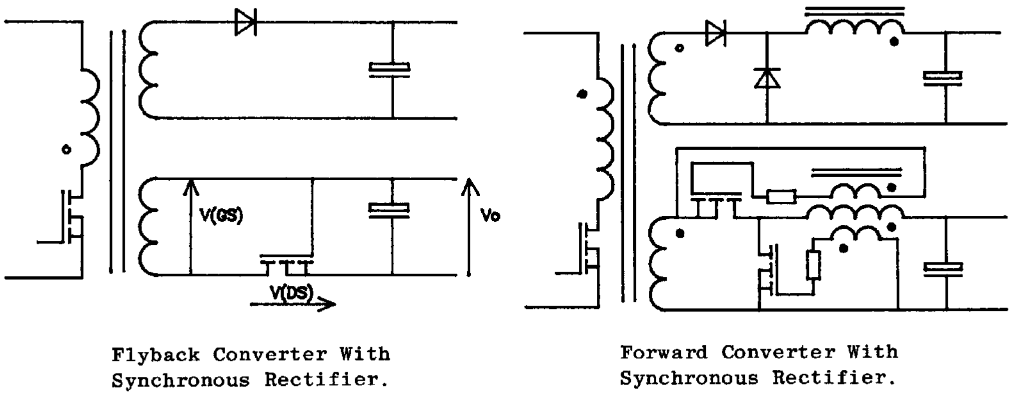

V(GS)
Vo
V(DS)
Flyback Converter With Synchronous Rectifier.
Forward Converter With Synchronous Rectifier.

Fig. 5 Flyback and Forward converters with Synchronous Rectification.

Forward converter

Normal diode rectifiers are replaced by MOSFETs in a forward output, as shown in Fig. 5, with no extra components added. However, there is a problem at maximum input voltage. At minimum volts, the transformer winding supplies $V_{out} + V_{choke}$, where:-

$$V_{out} = V_{choke} = 12V \text{ (for a 12V output) at 50\% mark/space ratio.}$$

$$V_{trans} = 24V$$

At maximum input volts, the choke may have 2 or 3 times the voltage across it, which makes the total 36V or 48V. With the gate rated at 20V, the choke is necessary for the forward transistor, as shown in Fig. 5, to supply the correct voltage. It may also be necessary for the freewheel diode, but this may be marginal depending on the input voltage range specified. This costs even more money, but may be considered good value if the loss in an epitaxial diode costs too much in efficiency.

Bridge converters

The circuit shown in Fig. 6 at first glance looks attractive. Parasitic diodes are arranged never to come on, and thus do not cause switching losses themselves. Also, the choke voltage drop is less than in the forward case, which may indicate that the MOSFETs can be used without extra overwinds to protect the gate voltage.

However, the simple drive waveforms used here, which are naturally synchronised to the primary switches, do not bias the rectifying transistors on when both the switches are off. During this time the transformer magnetising currents need a path to freewheel around. Normally this path is provided by the diodes. When the drive has been removed in the circuit example of Fig. 6, this path no longer exists. To turn the transistor around so that their body diode can conduct during this freewheel time would only give diode turn-off loss, which is what the technique is intended to avoid. Any bypass diode has the same drawback. The correct drive waveforms are not even available from the choke. They can be generated most easily in conjunction with the primary switch waveforms, but involves expensive isolating drive toroids.

The conclusions on which converters are most suitable, and how to connect the MOSFETs in the most cost-effective manner for a 12V output are:-

- A flyback MOSFET rectifier can be connected with no extra components.
- A forward MOSFET needs one overwind, maybe two.
- A bridge output requires drive toroids whose signal is not easily derivable from the secondary side waveforms.

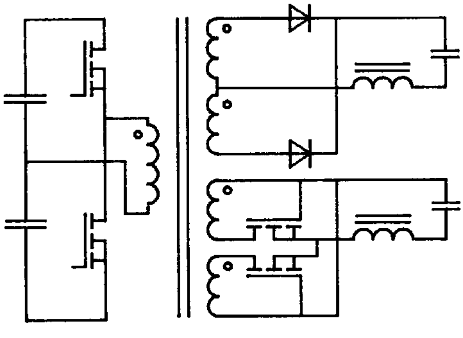


Fig. 6 Half-Bridge converter with Synchronous Rectification.

Even though MOSFETs may have less switching loss than epitaxial diodes, they do have capacitance discharged each cycle. The only consolation is that it has a built-in 'anti-snap-off' feature. If the rectifiers are switching at low V_{DS} then this loss is indeed very low.

Influence of R.F.I. on the choice of converter

This section deals with R.F.I. considerations of primary switches and secondary rectifying diodes only. The techniques will be applied to a power supply operating at 500kHz that has been developed to deliver a single 5V output at 15A, from 250V a.c. mains input. The converter choice is a half bridge circuit to minimise the loss in the circuit due to C_{OSS}.

A single heatsink arrangement is required to minimise size, so primary and secondary semiconductors need to be thermally cooled on the same heatsink. R.F.I. currents need to be prevented from coupling primary to secondary through the heatsink. Connection of R.F.I. screens underneath all components attached to the metal is not necessary when the structure of the semiconductors is understood.

Taking the rectifiers first:-

The arrangement of the output bridge is shown in Fig. 7. The cathodes of the diodes are connected to the substrate within their encapsulation. Thus, as long as the cathodes are connected as close as possible to the ceramic capacitor, C3, of the output filter, the common cathode/capacitor junction is a solid a.c. earth point. Therefore, no R.F.I. currents are connected into the common heatsink. An isolated encapsulation for an electrical arrangement such as this is all that is needed to minimise R.F.I. from diodes to heatsink.

Considering next the primary power transistors:-

The arrangement of power transistors is also shown in Fig. 7. The drains of the transistors are connected to the substrates of their encapsulations. Thus, as long as TR1 is connected as close as possible to the film-foil bridge capacitors, C1 and C2, the common drain/capacitor junction is a solid a.c. earth point. A SOT-186, SOT-186A, SOT-199 or TO-220 with mica washers may be suitable for TR1, the final selection being dependent on the isolation requirements. For TR2, the drain and therefore the substrate is modulated by the action of the circuit. Thus, without preventive action, R.F.I. currents will be coupled to the heatsink.

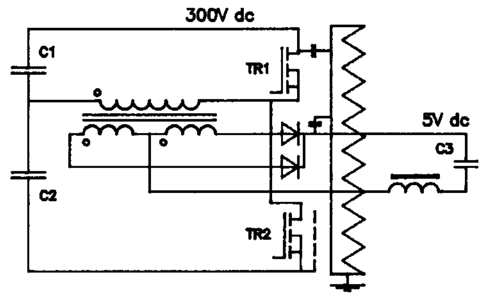


Fig. 7 Half-Bridge converter power stage.

The transistor TR2 is in a similar situation to one in a flyback or forward configuration. A simple solution is to use a SOT-186 (F-pack), plus copper screen connected to the transistor source lead and the film-foil capacitor, C2, plus whatever degree of isolation is required to the heatsink. This assembly was tested, and the result was that the screen reduced the line R.F.I. peaks by an average of 10dB over the range 500kHz to 10MHz. A small percentage of this can be attributed to the distance that the copper screen moves the substrate away from the heatsink. Nevertheless, the majority is due to the inclusion of the 0.1mm thick copper screen.

The conclusion is that a variety of encapsulations is necessary to allow R.F.I. to be minimised when the power supply is constructed.

Conclusions

This paper shows how to calculate some of the limiting parameters in the application of semiconductors to high frequency SMPS. It also highlights new encapsulations developed for high frequency power conversion applications. Some of the range of encapsulations were demonstrated in a 500kHz half-bridge off-line switcher.

References

1. Improved ferrite materials and core outlines for high frequency power supplies. Chapter 2.4.1

2. PowerMOS introduction. Chapter 1.2.1

Output Rectification

2.2.1 Fast Recovery Epitaxial Diodes for use in High Frequency Rectification

In the world of switched-mode power supply (S.M.P.S.) design, one of the most pronounced advances in recent years has been the implementation of ever increasing switching frequencies. The advantages include improved efficiency and an overall reduction in size, obtained by the shrinking volume of the magnetics and filtering components when operated at higher frequencies.

Developments in switching speeds and efficiency of the active switching power devices such as bipolars, Darlingtons and especially power MOSFETs, have meant that switching frequencies of 100kHz are now typical. Some manufacturers are presently designing p.w.m. versions at up to 500kHz, with resonant mode topologies (currently an area of intensive academic research) allowing frequencies of 1MHz and above to be achievable.

These changes have further increased demands on the other fundamental power semiconductor device within the S.M.P.S. - the power rectification diode.

Key Rectifier Characteristics.

In the requirements for efficient high frequency S.M.P.S. rectification, the diode has to meet the following critical requirements:-

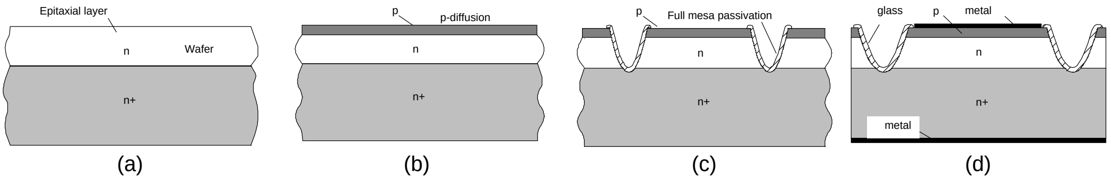
- Short reverse recovery time, t_{rr} ,for compatibility with high frequency use.
- Low forward voltage drop, V_F , to maximise overall converter efficiency.
- Low loss switching characteristics, which reduce the major frequency dependent loss in the diode.
- A soft reverse recovery waveform, with a low dI_R/dt rate, reduces the generation of unwanted R.F.I. within the supply.

The Philips range of fast recovery epitaxial diodes (FREDs) has been developed to meet the requirements of high frequency, high power rectification. With many years' experience in the development of epitaxial device technology, Philips offers a comprehensive range of FREDs. Some of their standard characteristics include:-

- A reverse blocking voltage range from 100V to 800V, and forward current handling capability from 1A to 30A. Thus, they are compatible for use in a wide range of S.M.P.S. applications, from low voltage dc/dc converters right through to off-line ac/dc supplies. Philips epitaxial diodes are compatible with a range of output voltages from 10V to 200V, with the capability of supplying a large range of output powers. Several different package outlines are also available, offering the engineer flexibility in design.
- Very fast reverse recovery time, t_{rr} , as low as 20ns, coupled with inherent low switching losses permits the diode to be switched at frequencies up to 1MHz.
- Low V_F values, typically 0.8V, produce smaller on-state diode loss and increased S.M.P.S. efficiency. This is particularly important for low output voltage requirements.
- Soft recovery is assured with the whole range of FREDs, resulting in minimal R.F.I. generation.

Structure of the power diode

All silicon power diodes consist of some type of P-I-N structure, made up of a highly doped P type region on one side, and a highly doped N+ type on the other, both separated by a near intrinsic middle region called the base. The properties of this base region such as width, doping levels and recombination lifetime determine the most important diode characteristics, such as reverse blocking voltage capability, on-state voltage drop V_F, and switching speed, all critical for efficient high frequency rectification.



(a) (b) (c) (d)

Fig. 1 Main steps in epitaxial diode process.

A high blocking voltage requires a wide lightly doped base, whereas a low V_F needs a narrow base. Using a short base recombination lifetime produces faster recovery times, but this also increases V_F. Furthermore, in any P-N junction rectifier operating at high currents, carrier injection into the base takes place from both the P and N+ regions, helping to maintain a low V_F.

Technology

High voltage power diodes are usually manufactured using either double-diffused or an epitaxial technology. High injection efficiency into the base coupled with a narrow base width are essential for achieving a low V_F. High injection efficiency requires the slope of the diffusion profile at the P^+N and N^+N junctions to be very steep. Achieving a minimum base width requires very tight control of the lightly doped base layer. Both these criteria can be met using epitaxial technology.

Epitaxial process

The epitaxial method involves growing a very lightly doped layer of silicon onto a highly doped N+ type wafer; see Fig. 1(a). A very shallow P type diffusion into the epi layer is then made to produce the required P-I-N structure (Fig. 1(b)). This gives accurate control of the base thickness such that very narrow widths may be produced. Abrupt junction transitions are also obtained, thus providing for the required high carrier injection efficiency. The tighter control of width and junction profile also provides a tighter control of Q_s, hence, the switching recovery times are typically ten times faster than double diffused types.

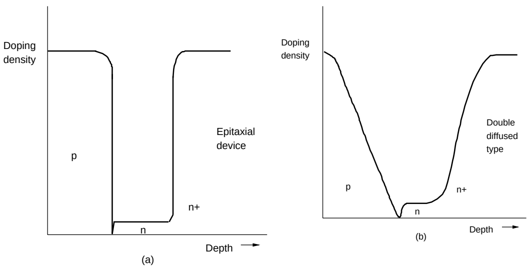


Fig. 2 Comparison of diffusion profiles.
(a) fast recovery epitaxial diode
(b) standard double diffused type

Double-diffused process

Double diffusion requires deep diffusions of the P+ and N+ regions into a slice of lightly doped silicon, to produce the required base width. This method is fraught with tolerance problems, resulting in poor control of the base region. The junction transitions are also very gentle, producing a poor carrier injection efficiency. The combination of the two produces a higher V_F value, and also a poor control of stored charge Q_s in the base, leading to a relatively slow switching speed.

Figure 2 gives a comparison of the diffusion profiles for the two methods.

Lifetime control

To achieve the very fast recovery time and low stored charge, Q_s, required for high frequency rectification, it is necessary to introduce lifetime killing (gold doping) into the base of the diode. This produces a lower Q_s and faster reverse recovery time, t_{rr}. Unfortunately, doping also has the effect of increasing V_F. Fig. 3 shows a graph of normalised V_F versus the minority carrier lifetime for a 200V and 500V device. It can be seen that there is an optimum lifetime for each voltage grade, below which the V_F increases dramatically.

Philips has been using gold-killing techniques for well over twenty years, and combining this with epitaxial technology results in the excellent low V_F, t_{rr} and Q_s combinations found in the FRED range.

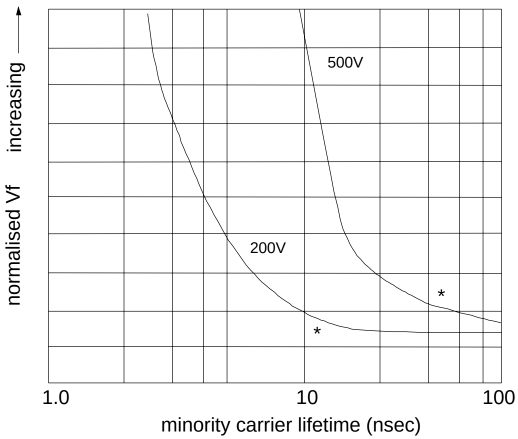


Fig. 3 Normalised V_F versus minority carrier lifetime.

Passivation

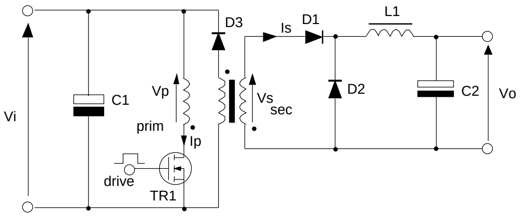
To ensure that the maximum reverse blocking potential of the diode is achieved, it is necessary to ensure that high fields do not occur around the edges of the chip. This is achieved by etching a trough in the epitaxial layer and depositing a special glass into it (Fig. 1(c)). Known as full mesa glass passivation, it achieves stable reverse blocking characteristics at high voltages by reducing charge build-up, and produces a strong chip edge, reducing the risk of assembly damage. This means that the diodes are rugged and reliable, and also allows all devices to be fully tested on-slice.

Finally, Fig. 1(d) shows the chip after it has been diced and metallised. The rectifier is then assembled into a wide selection of different power packages, the standard TO-220 outline being one example.

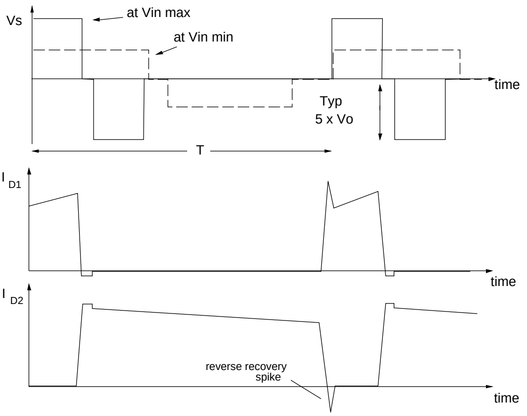
Characteristics

Forward conduction loss

Forward conduction loss is normally the major component of power loss in the output rectification diodes of an S.M.P.S. For all buck derived output stages, for example the forward converter shown in Fig. 4, the choke current always flows in one or other of the output diodes (D1 and D2).



Simple forward converter circuit



Secondary voltage and diode current waveforms

Fig. 4 Forward converter schematic.

The output voltage is always lowered by the diode forward voltage drop V_F such that:-

$$V_o + V_f = V_s D \tag{1}$$

Where D is the transistor duty cycle. Thus, the resulting power loss due to V_F of the output rectifiers is:-

$$P_{on} loss = V_f I_o \tag{2}$$

where I_o is the output load current of the converter. The loss as a percentage of the output power is thus:-

$$\frac{V_f I_o}{V_o I_o} = \frac{V_f}{V_o} \tag{3}$$

This loss in efficiency for a range of standard S.M.P.S. outputs is shown in Fig. 5. It is clear that V_f needs to be kept to an absolute minimum particularly for low output voltages if reasonable efficiency is to be achieved.

To accommodate variations in the input voltage, the output rectifiers are usually chosen such that their blocking voltage capability is between 4 and 8 times the output voltage. For the lowest output voltages, Schottky diodes should be the first choice. Unfortunately, the characteristically low V_f of the Schottky cannot be maintained at voltages much higher than 100V. For outputs above 24V, fast recovery epitaxial diodes are the most suitable rectifiers.

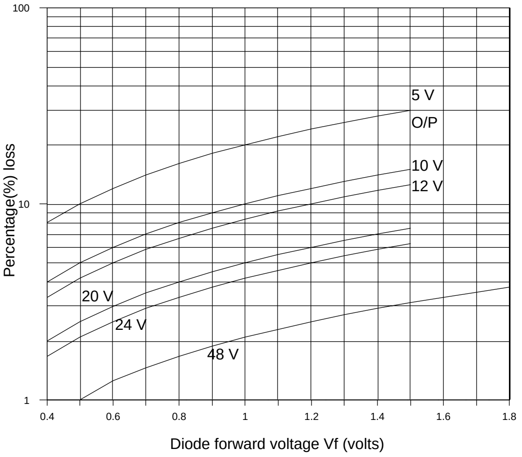


Fig. 5 Percentage S.M.P.S. loss versus V_F for some standard output voltages.

Figure 6 shows an example of V_F versus forward current I_F for the Philips BYV32 series, rated from 50V to 200V and with a maximum output current of 20A. This reveals the low V_F values typical of the epitaxial technique.

From Fig. 6 and equation 2, it is possible to estimate the loss due to the output rectifiers in an S.M.P.S. For example, for a 12V, 20A output, a conduction loss of 17W typical and 20W maximum is obtained. This corresponds to a worst case loss of 8% of total output power, normally an acceptable figure.

Philips devices offer some of the lowest V_F values on the market. Maximum as well as typical values are always quoted at full rated currents in the datasheets. However this is not the case with all manufacturers, and care should be taken when comparing Philips devices with those of other manufacturers.

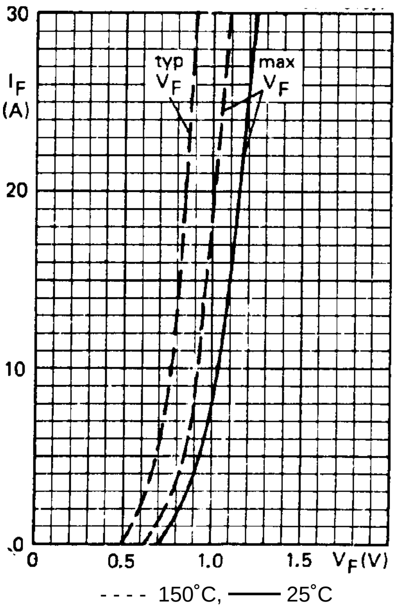


Fig. 6 V_F vs I_F for the Philips BYV32 series.

Reverse recovery

a) Q_S, t_{rr} and I_{rrm}

Following V_F, the most important feature of a high frequency rectifier is the reverse recovery characteristic. This affects S.M.P.S. performance in several ways. These include increased diode switching loss, higher peak turn-on current and dissipation in the power transistors, and increased generation of electro-magnetic interference (e.m.i.) and voltage transient oscillations in the outputs. Clearly, the rectifier must have optimum reverse recovery characteristics to keep this catalogue of effects to a minimum.

When the P-N diode is conducting forward current, a charge is built up in the base region, consisting of both electrons and holes. It is the presence of this charge which is the key to achieving low V_f. The higher the forward current, the greater is this stored charge. In order to commutate the diode (i.e switch the device from forward conduction into reverse blocking mode) this charge has to be removed from the diode before the base can sustain any reverse blocking voltage. The removal of this charge manifests itself as a substantial transient reverse current spike, which can also generate a reverse voltage overshoot oscillation across the diode.

The waveforms of the reverse recovery for a fast rectifier are shown in Fig. 7. The rectifier is switched from its forward conduction at a particular rate, called dI_F/dt. Stored charge begins to be extracted after the current passes through zero, and an excess reverse current flows. At this point the charge is being removed by both the forcing action of the circuit, and recombination within the device (dependent upon the base characteristics and doping levels).

At some point the charge has fallen to a low enough level for a depletion region to be supported across the base, thus allowing the diode to support reverse voltage. The peak of reverse current, I_{rrm} occurs just after this point. The time for the current to pass through zero to its peak reverse value is called t_a. From then on, the rectifier is in blocking mode, and the reverse current then falls back to zero, as the remainder of the stored charge is removed mostly by recombination. The time for the peak reverse current to fall from its maximum to 10% of this value is called t_b.

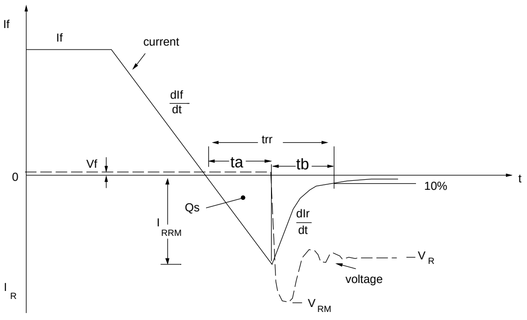


Fig. 7 Rectifier diode reverse recovery waveforms.

The stored charge, Q_s, is the area under the current-time curve and is normally quoted in nano-Coulombs. The sum of t_a and t_b is called the rectifier reverse recovery time, t_{rr} and gives a measure of the switching speed of the rectifier.

Factors influencing reverse recovery

In practice, the three major parameters t_{rr}, Q_s and I_{rrm} are all dependent upon the operating condition of the rectifier. This is summarised as follows:-

- Increasing the forward current, I_F, increases t_{rr}, Q_s and I_{rrm}.
- Increasing the dI_F/dt rate by using a faster transistor and reducing stray inductance, significantly decreases t_{rr}, but increases Q_s and I_{rrm}. High dI_F/dt rates occur in the high frequency square wave switching found in S.M.P.S. applications. (MOSFETs can produce very small fall times, resulting in very fast dI_F/dt).
- Increasing diode junction temperature, T_j increases all three.
- Reducing the reverse voltage across the diode, V_r , also slightly increases all three.

Specifying reverse recovery

Presently, all manufacturers universally quote the t_{rr} figure as a guide. This figure is obtained using fixed test procedures. There are two standard test methods normally used:-

Method 1
Referring to the waveform of Fig. 7:
I_F = 1A; dI_F/dt =50A/µsec; V_r > 30V; T_j= 25˚C.
t_{rr} is measured to 10% of I_{rrm}.

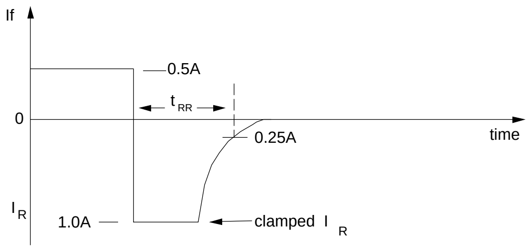


Fig. 8 E.I.A. t_{rr} test procedure.

Method 2
I_F = 0.5A, the reverse current is clamped to 1A and t_{rr} is measured to 0.25A.
This is the Electronics Industries Association (E.I.A.) test procedure, and is outlined in Fig. 8.

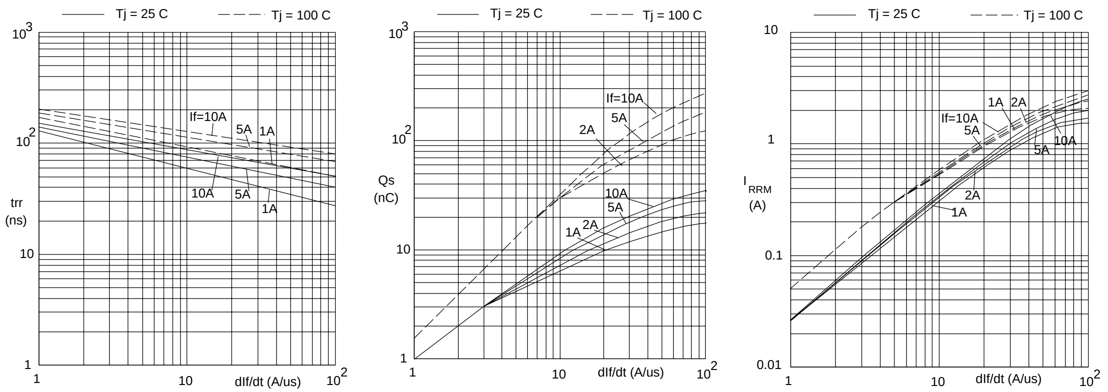
The first and more stringent test is the one used by Philips. The second method, used by the majority of competitors will give a t_{rr} figure typically 30% lower than the first, i.e. will make the devices look faster. Even so, Philips have the best t_{rr} / Q_s devices available on the market. For example, the Philips BYW29 200V, 8A device has a t_{rr} of 25ns, the competitor devices quote 35ns using the easier second test. This figure would be even higher using test method 1.

Reverse recovery is specified in data by Philips in terms of all three parameters t_{rr}, Q_s and I_{rrm}. Each of these parameters however is dependent on exact circuit conditions. A set of characteristics is therefore provided showing how each varies as a function of dI_f/dt, forward current and temperature, Fig. 9. These curves enable engineers to realise what the precise reverse recovery performance will be under circuit operating conditions. This performance will normally be worse than indicated by the quoted figures, which generally speaking do not reflect circuit conditions. For example, a BYW29 is quoted as having a t_{rr} of 25 ns but from the curves it may be as high as 90 ns when operated at full current and high dI_F/dt. Similarly a quoted Q_s of 11 nC compares with the full current worst case of 170 nC.

In the higher voltage devices (500V and 800V types) t_{rr} and Q_s are much higher, and will probably be the most critical parameters in the rectification process. Care must be taken to ensure that actual operating conditions are used when estimating more realistic values.

Frequency range

Figure 10 compares the recovery of a Philips 200V FRED with a double diffused type. The FRED may be switched approximately 10 times faster than the double diffused type. This allows frequencies of up to 1MHz to be achieved with the 200V range.



(a) Maximum trr

(b) Maximum Qs

(c) Maximumm I RRM

Fig. 9 Reverse recovery curves for BYW29.

In the higher voltage devices where the base width is increased to sustain the reverse voltage, the amount of stored charge increases, as does the t_{rr}. For a 500V device, 500kHz operation is possible, and for 800V typically 200kHz is realistic.

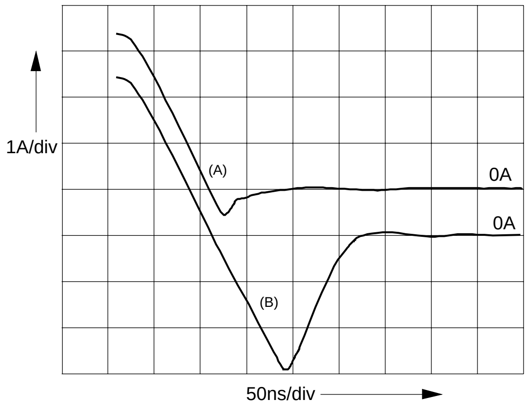


Fig. 10 Comparison of reverse recovery of FRED vs double diffused.
(a) Philips 200V FRED.
(b) Double-diffused diode.

Effects on S.M.P.S operation

In order to analyse the effects of reverse recovery on the power supply, a simple non-isolated buck converter shown in Fig. 11 is considered. The rectifier D1 in this application is used in freewheel mode, and conducts forward current during the transistor off-time.

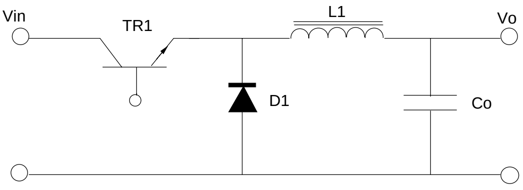


Fig. 11 Buck converter.

The waveforms for the diode and transistor switch during the reverse recovery of the diode when the transistor turns on again are given in Fig. 12.

As the transistor turns on, the current ramps up in the transistor as it decays and reverses in the diode. The dI_F/dt is mainly dependent on the transistor fall time and, to some extent, the circuit parasitic inductances. During the period t_a the diode has no blocking capability and therefore the transistor must support the supply voltage. The transistor thus simultaneously supports a high voltage and conducts both the load current and the reverse recovery current, implying a high internal power dissipation. After time t_a the diode blocking capability is restored and the voltage across the transistor begins to fall. It is clear that a diode with an I_{rrm} half the value of I_F will effectively double the peak power dissipation in the transistor at turn-on. In severe cases where a high I_{rrm} / t_{rr} rectifier is used, transistor failure could occur by exceeding the peak current or power dissipation rating of the device.

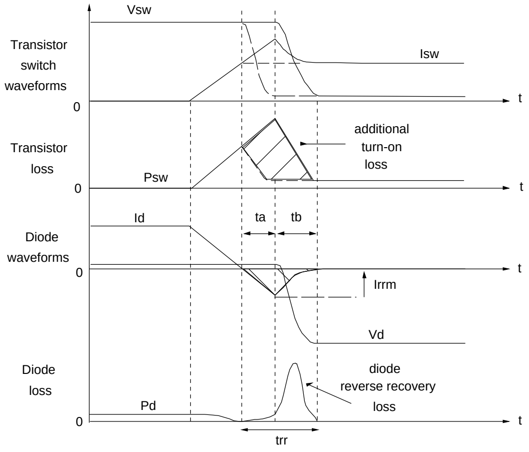


Fig. 12 Reverse recovery diode and transistor waveforms.

There is also an additional loss in the diode to be considered. This is a product of the peak I_{rrm} and the diode reverse voltage, V_r. The duration of current recovery to zero will affect the magnitude of the diode loss. However, in most cases the additional transistor loss is much greater than the diode loss.

Diode loss calculation

As an example of the typical loss in the diode, consider the BYW29, 8A, 200V device as the buck freewheel diode, for the following conditions:-

I_F = 8A; V_r =100V; dI_F/dt = 50A/µs;
T_j = 25˚C; duty ratio D = 0.5; f = 100KHz.

The diode reverse recovery loss is given by:-

$$P_{rr} = \frac{1}{2} \cdot V_r \cdot I_{rrm} \cdot t_b \cdot f$$

From the curves of Fig. 7, t_{rr}=35ns, I_{rrm} = 1.5A. Assuming $t_b = t_{rr}/2$ gives:

$$P_{rr} = \frac{1}{2} \cdot 100 \cdot 1.5 \cdot 17.5 \cdot 100\mathrm{k} = 132\mathrm{mW}$$

This is still small compared to the diode V_F conduction loss of approximately 3.6 W. However, at T_j=100˚C, dI_F/dt=100A/µs and f=200kHz, the loss becomes 1.05W, which is fairly significant. In the higher voltage devices where t_{rr} and I_{rrm} are significantly worse, then the frequency dependent switching loss will tend to dominate, and can be higher than the conduction loss. This will limit the upper frequency of operation of the diode.

The turn-on current spike generated in the primary circuits due to diode reverse recovery can also seriously affect the control of the S.M.P.S. when current mode control is used (where the peak current is sensed). An RC snubber is usually required to remove the spike from the sense inputs. Good reverse recovery removes the need for these additional components.

b) Softness and dI_R/dt

When considering the reverse recovery characteristics, it is not just the magnitude (t_{rr} and I_{rrm}) which is important, but also the shape of the recovery waveform. The rate at which the peak reverse current I_{rrm} falls to zero during time t_b is also important. The maximum rate of this slope is called dI_R/dt and is especially significant. If this slope is very fast, it will generate significant radiated and conducted electrical noise in the supply, causing R.F.I. problems. It will also generate high transient voltages across circuit inductances in series with the diode, which in severe cases may cause damage to the diode or the transistor switch by exceeding breakdown limits.

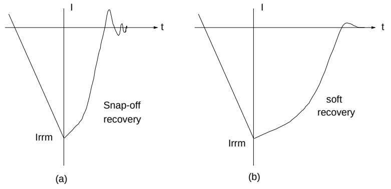


Fig. 13 "Soft" and "snappy" reverse recovery.

A diode which exhibits an extremely fast dI_R/dt is said to have a "snap-off" or "abrupt" recovery, and one which returns at a relatively smooth, gentle rate to zero is said to have a soft recovery. These two cases are shown in the waveforms in Fig. 13. The softness is dependent upon whether there is enough charge left in the base, after the full spread of the depletion region in blocking mode, to allow the current to return to zero smoothly. It is mainly by the recombination mechanism that this remaining charge is removed during t_b.

Maintaining t_b at a minimum would obviously give some reduction to the diode internal loss. However, a snappy rectifier will produce far more R.F.I. and transient voltages. The power saving must therefore be weighed against the additional cost of the snubbers and filtering which would otherwise be required if the rectifier had a snappy characteristic.

The frequency range of R.F.I. generated by dI_R/dt typically lies in the range of 1MHz to 30MHz, the magnitude being dependent upon how abrupt the device is. One secondary effect that is rarely mentioned is the additional transformer losses that will occur due to the extremely high frequencies generated inside it by the diode recovery waveform. For example, core loss at 10MHz for a material designed to operate at 100kHz can be significant. There will also be additional high frequency loss in the windings due to the skin effect. In this case the use of a soft device which generates a lower frequency noise range will reduce these losses.

Characterising softness

A method currently used by some manufacturers to characterise the softness of a device is called the softness factor, S. This is defined as the ratio of t_b over t_a.

$$\text{softness factor}, \qquad S = \frac{t_b}{t_a}$$

An abrupt device would have S much less than 1, and a soft device would have S greater than 1. A compromise between R.F.I. and diode loss is usually required, and a softness factor equal to 1 would be the most suitable value for a fast epitaxial diode.

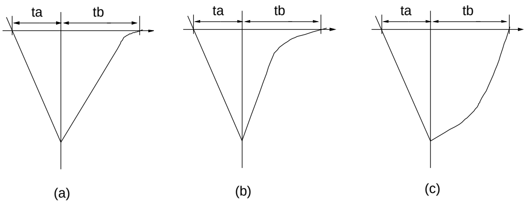


Fig. 14 Different diode dI_R/dt rates for same softness factor.

Although the softness factor does give a rough guide to the type of recovery and helps in the calculation of the diode switching loss, it does not give the designer any real idea of the dI_R/dt that the rectifier will produce. Hence, levels of R.F.I. and overvoltages could be different for devices with the same softness factor. This is shown in Fig. 14, where the three characteristics have the same softness factor but completely different dI_R/dt rates.

In practice, a suitable level for dI_R/dt would be to have it very similar in magnitude to dI_F/dt. This would keep the noise generated to a minimum.

At present there is no universal procedure used by manufacturers to characterise softness, and so any figures quoted must be viewed closely to check the conditions of the test.

Comparison with competitor devices

Figure 15 compares a BYV32 with an equivalent competitor device. This test was carried out using an L.E.M. Q_s test unit.

The conditions for each diode were identical. The results were as follows:-

BYV32:- S = 1.2, dI_R/dt = 40A/μs,
Voltage overshoot = 5V

Competitor:- S = 0.34, dI_R/dt = 200A/μs,
Voltage overshoot = 22V

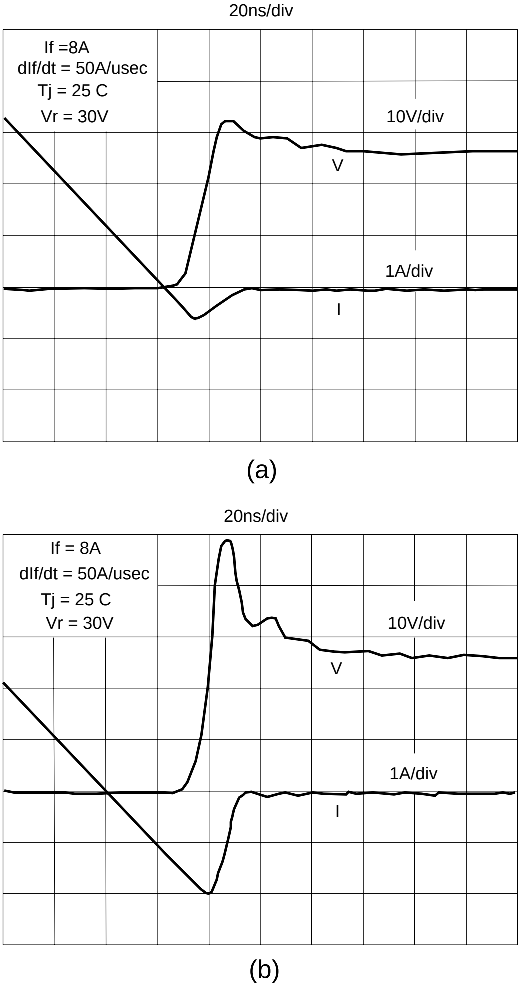


Fig. 15 Comparison of softness of reverse recovery.
(a) Philips BYV32 200V 8A device
(b) Equivalent competitor device

For the Philips device, apart from the very low Q_s and I_{rrm} values obtained, the S factor was near 1 and the dI_R/dt rate was less than the original dI_F/dt of 50A/μs. These excellent parameters produce minimal noise and the very small overshoot voltage shown. The competitor device was much snappier, the dI_R/dt was 4 times the original dI_F/dt, and caused a much more severe overshoot voltage with the associated greater R.F.I. The diode loss is also higher in the competitor device even though it is more abrupt, since Q_s and I_{rrm} are larger.

The low Q_s of the Philips FRED range thus maintains diode loss to a minimum while providing very soft recovery. This means using a Philips type will significantly reduce R.F.I. and dangerous voltage transients, and in many cases reduce the power supply component count by removing the need for diode snubbers.

Forward recovery

A further diode characteristic which can affect S.M.P.S. operation is the forward recovery voltage V_{fr}. Although this is not normally as important as the reverse recovery effects in rectification, it can be particularly critical in some special applications.

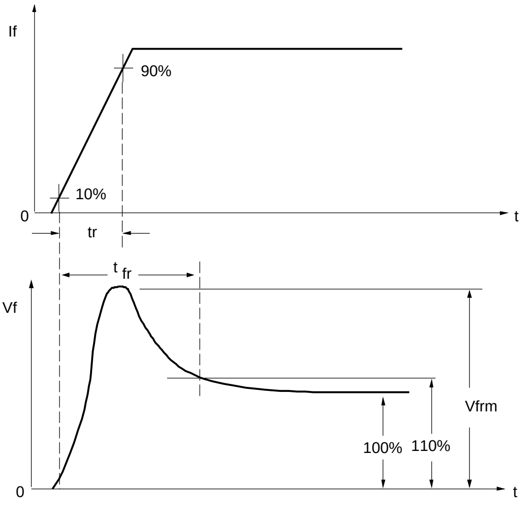


Fig. 16 Forward recovery characteristics.

Forward recovery is caused by the lack of minority carriers in the rectifier p-n junction during diode turn-on. At the instant a forward bias is applied, there are no carriers present at the junction. This means that at the start of conduction, the diode impedance is high, and an initial forward voltage overshoot will occur. As the current flows and charge builds up, conductivity modulation (minority carrier injection) takes place. The impedance of the rectifier falls and hence, the forward voltage drop falls rapidly back to the steady state value.

The peak value of the forward voltage is known as the forward recovery voltage, $V_{frm.}$ The time from the forward current reaching 10% of the steady state value to the time the forward voltage falls to within 10% of the final steady state value is known as the forward recovery time (Fig. 16).

The magnitude and duration of the forward recovery is normally dependent upon the device and the way it is commutated in the circuit. High voltage devices will produce larger V_{frm} values, since the base width and resistivity (impedance) is greater.

The main operating conditions which affect V_{fr} are:-

- I_f; high forward current, which produces higher V_{fr}.
- Current rise time, t_r; a fast rise time produces higher V_{fr}.

Effects on s.m.p.s.

The rate of rise in forward current in the diode is normally controlled by the switching speed of the power transistor. When the transistor is turned off, the voltage across it rises, and the reverse voltage bias across the associated rectifier falls. Once the diode becomes forward biased there is a delay before conduction is observed. During this time, the transistor voltage overshoots the d.c supply voltage while it is still conducting a high current. This can result in the failure of the transistor in extreme cases if the voltage limiting value is exceeded. If not, it will simply add to the transistor and diode dissipation. Waveforms showing this effect are given in Fig. 17.

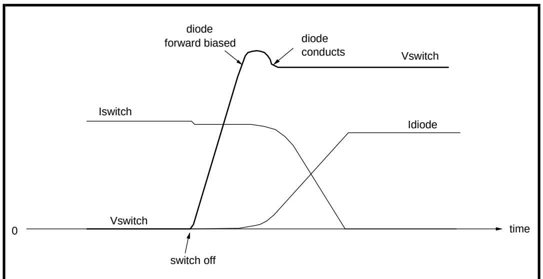


Fig. 17 Forward recovery effect on transistor voltage.

Table 1 outlines typical V_{frm} values specified for rectifiers of different voltage rating. This shows the relatively low values obtained. No comparable data for any of the competitor devices could be found in their datasheets. It should be noted that in most S.M.P.S. rectifier applications, forward recovery can be considered the least important factor in the selection of the rectifier.

Device type	V_{BR} (Volts)	I_f (Amps)	dI_f/dt (A/µs)	typ V_{frm} (Volts)
BYW29	200	1.0	10	0.9
BYV29	500	10	10	2.5
BYR29	800	10	10	5.0

Table 1. V_{frm} values for different Philips devices.

Reverse leakage current

When a P-N junction is reverse biased, there is always an inherent reverse leakage current that flows. In any piece of undoped semiconductor material there is a thermally generated background level of electron and hole pairs. These pairs also naturally recombine, such that an equilibrium is established. In a p-n junction under reverse voltage conditions, the electric field generated will sweep some of the free carriers generated out of the device before they can recombine, hence causing a leakage current. This phenomenon is shown in Fig. 18.

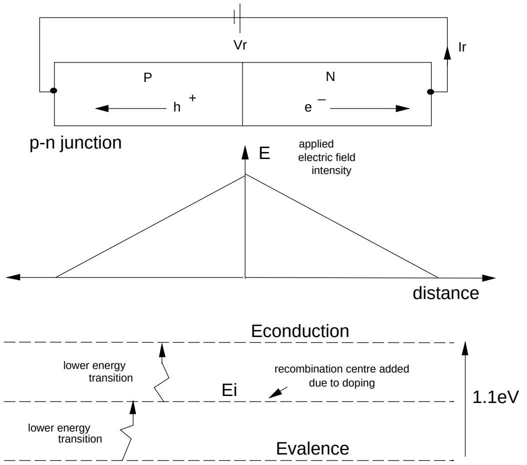


Fig. 18 Clarification of reverse leakage current.

When the rectifier base is gold doped to decrease Q_s and t_{rr}, a new energy level is introduced very close to the centre of the semiconductor energy band gap. This provides lower energy transition paths as shown, and thermal generation (and recombination) of hole-electron pairs is more frequent. Thus, the reverse leakage current is greater still in the killed, fast rectifier.

Since the pairs are generated thermally, it is obvious that raising the junction temperature will increase the leakage significantly. For example, the leakage current of a FRED can increase by up to 20 times by raising the junction temperature, T_j from 25˚C to 100˚C. This increase can be far greater in other diode technologies.

Many S.M.P.S. designers have a misconception about leakage current, and believe that it renders the rectifier poor quality, giving high losses, and is unreliable. This is not so. Leakage is a naturally occurring effect, and is present in all rectifiers. The leakage in an S.M.P.S. diode is normally extremely small and stable, with very little effect on the rectification process. Some manufacturers have over-emphasised the benefits of very low leakage devices, claiming that they have great advantages. However, this will be shown to be groundless, since any reduction in the overall diode power loss will be minimal.

In practice, the reverse leakage current only becomes significant at high operating temperatures (above 75˚C) and for high reverse blocking voltages (above 500V), where the product of reverse voltage and leakage current (hence, power loss) is higher. Even then, the leakage current is still usually lower than 1mA.

Table 2 lists the maximum leakage currents for some of the devices from the Philips range (gold killed), revealing low levels, even in the higher voltage devices, achieved through optimised doping.

Device type	$V_{BR(max)}$ (Volts)	max I_r (mA) T_j =100˚C full V_{rrm}	max I_r (µA) T_j=25˚C full V_{rrm}
BYW29	200	0.6	10
BYV29	500	0.35	10
BYR29	800	0.2	10

Table 2. Maximum reverse leakage currents for Philips devices.

The power dissipation due to leakage is a static loss and depends on the product of the reverse voltage and the leakage current over a switching cycle. A worst case example is given below where the data sheet leakage current maximum is used at maximum reverse blocking voltage of the diode.

S.M.P.S example:-Flyback converter

Consider first the BYV29-500 as the output rectifier in the discontinuous flyback converter (Note: the reverse blocking occurs during the transistor on time, and a minimum duty of 0.25 has been assumed.) The BYV29-500 could generate a possible maximum output voltage of 125V. The maximum leakage power loss is:-

$$P_L = 500\mathrm{V}\cdot 0.35\mathrm{mA}\cdot 0.25 = 43.75\mathrm{mW}$$

Alternatively, for the BYR29-800, maximum rectified output is approximately 200V, and by similar calculations, its maximum loss is 40mW. Lower output voltages would give leakage losses lower than this figure.

These types of calculation can be carried out for other topologies, when similar low values are obtained.

Conclusion

Philips produces a comprehensive range of Fast Recovery Epitaxial Diodes. The devices have been designed to exhibit the lowest possible V_f while minimising the major reverse recovery parameters, Q_s, t_{rr} and I_{rrm}. Because of the low Q_s, switching losses within the circuit are minimised, allowing use up to very high frequencies. The soft recovery characteristic engineered into all devices makes them suitable for use in today’s applications where low R.F.I. is an important consideration. Soft recovery also provides additional benefits such as reduced high frequency losses in the transformer core and, in some cases, the removal of snubbing components.

FRED Selection Guide

Single Diodes

Type Number	Outline	$I_{F(AV)}$ max	Voltage Grades								
		Amps	100	150	200	300	400	500	600	700	800
BYW29E	TO-220AC	8	*	*	*						
BYV29	TO-220AC	9				*	*	*			
BYR29	TO-220AC	8						*	*	*	*
BYV79E	TO-220AC	14	*	*	*						
BYT79	TO-220AC	14				*	*	*			

Dual Diodes (Common cathode)

Type Number	Outline	I_O max	Voltage Grades								
		Amps	100	150	200	300	400	500	600	700	800
BYV40	SOT-223	1.5	*	*	*						
BYQ27	SOT-82	10	*	*	*						
BYQ28E	TO-220AB	10	*	*	*						
BYT28	TO-220AB	10				*	*	*			
BYV32E	TO-220AB	20	*	*	*						
BYV34	TO-220AB	20				*	*	*			
BYV42E	TO-220AB	30	*	*	*						
BYV72E	SOT-93	30	*	*	*						
BYV44	TO-220AB	30				*	*	*			
BYV74	SOT-93	30				*	*	*			

’E’ denotes rugged device.

Single Diodes (Electrically isolated Package)

Type Number	Outline	$I_{F(AV)}$ max Amps	Voltage Grades								
			100	150	200	300	400	500	600	700	800
BYW29F	SOT-186	8	*	*	*						
BYV29F	SOT-186	9				*	*	*			
BYR29F	SOT-186	8							*	*	*

Dual Diodes (Electrically Isolated Package)

Type Number	Outline	I_O max	Voltage Grades								
			100	150	200	300	400	500	600	700	800
BYQ28F	SOT-186	10	*	*	*						
BYV32F	SOT-186	12	*	*	*						
BYV72F	SOT-199	20	*	*	*						
BYV74F	SOT-199	20				*	*	*			

2.2.2 Schottky Diodes from Philips Semiconductors

The Schottky diodes from Philips have always had good forward characteristics and excellent switching performance. With this new, more extensive range of Schottky diodes come the additional benefits of stable, low leakage reverse characteristics and unsurpassed levels of guaranteed ruggedness.

The performance improvements have been achieved by changing both the design and the processing of Schottky diode wafers. The changes are the products of the continuing programme of research in the field of Schottky barrier technology being carried out at Stockport.

This report will look at the new range, the improvements that have been made and the changes that have produced them.

New process

The manufacturing process for all the devices in the new range includes several changes which have significantly improved the quality and performance of the product.

Perhaps the most significant change is moving the production of the Schottky wafers from the bipolar processing facility into the PowerMOS clean room. The Schottky diode is a ’surface’ device - its active region is right at the conductor / semiconductor interface, not deep within the silicon crystal lattice. This means that it can usefully exploit the high precision equipments and extremely clean conditions needed to produce MOS transistors. In some respects Schottkies have more in common with MOS transistors than they do with traditional bipolar products. In one respect they are identical - their quality can be dramatically improved by:-

- growing purer oxide layers,
- depositing metal onto cleaner silicon,
- more precise control of ion implantation.

Another change has been in the method of producing the Schottky barrier. The original method was to ’evaporate’ molybdenum onto the surface of the silicon. In the new process a Pt/Ni layer is ’sputtered’ onto the surface and then a heat treatment is used to produce a Pt/Ni silicide. This has the effect of moving the actual conductor / semiconductor interface a small distance away from the surface and into the silicon.

The advantage of this change is that it puts the barrier in an environment where the conditions are more homogeneous, resulting in a more consistent barrier. This consistency produces devices in which every part of the active area has the same reverse characteristic.

Ruggedness

The RUGGEDNESS of a Schottky diode is a measure of its ability to withstand the surge of power generated by the reverse current which flows through it when the applied reverse voltage exceeds its breakdown voltage. Operation in this mode is, of course, outside the boundaries of normal operation - it always exceeds the V_{RRM} rating of the device. However, situations can arise where the voltages present in the circuit far exceed the expectations of the designer. If devices are damaged by these conditions then the equipment they are in may fail. Such failures often result in equipments being condemned as unreliable. In recognition of this, Philips will now supply devices which operate reliably during both normal and abnormal operation.

All the Schottky diodes supplied by Philips now have two guaranteed reverse surge current ratings:-

I_{RRM} - guarantees that devices can withstand repetitive reverse current pulses ($t_p = 2\mu s$; $\Delta = 0.001$) of greater than the quoted value,

I_{RSM} - guarantees that single, 100µs pulses of the rated value can be applied without damage.

At the moment these ratings are quoted as either 1A or 2A, depending on device size. It should be understood that these figures do not represent the limit of device capability. They do, however, represent the limit of what, experience suggests, might be needed in most abnormal operational situations.

In an attempt to determine the actual ruggedness of the new devices, a series of destructive tests was carried out. The results shown in Fig. 1 give the measured reverse ruggedness of different sizes of device. It clearly shows that even small devices easily survive the 1A I_{RRM} / I_{RSM} limit and that the larger devices can withstand reverse currents greater than the 85A that the test gear was designed to deliver.

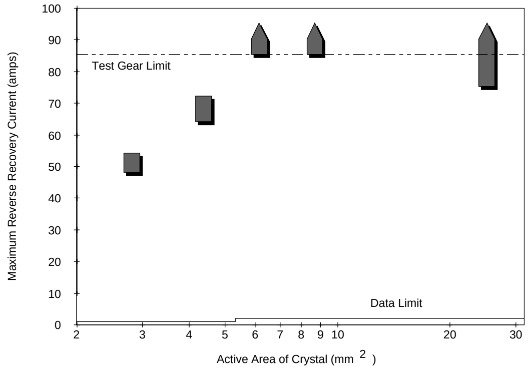


Fig. 1 Typical reverse ruggedness

Reverse leakage

The reverse characteristic of any diode depends upon two factors - 'bulk' and 'edge' leakage. The first is the current which leaks through the reverse biased junction in the main active area of the device. The second is the leakage through the junction around its periphery - where the junction meets the outside world. Attention must be paid to both of these factors if a high performance diode is to be produced. During the development of the new range of Philips Schottky diodes both of these factors received particular attention.

Bulk leakage

To achieve low forward voltage drop and very fast switching, Schottky diodes use the rectifying properties of a conductor / semiconductor interface. The 'height' of the potential barrier has a significant effect upon both the forward voltage drop and the reverse leakage. High barriers raise the V_F and lower the general reverse leakage level. Conversely low barrier devices have a lower V_F but higher leakage. So the choice of barrier height must result in the best compromise between leakage and V_F to produce devices with the best allround performance.

The height of a Schottky barrier depends, to a large extent, upon the composition of the materials at the interface. So the selection of the barrier metal and the process used for its deposition is very important. The final decision was made with the help of the extensive research and device modelling facilities available within the Philips organisation. The materials and processes that were selected have significantly reduced the bulk leakage of the new range of Schottky diodes. It is believed that this present design gives the optimum balance between leakage and V_f that is currently achievable.

Edge leakage

The other component influencing the reverse characteristic is edge leakage. In a diffused diode the mechanisms which operate at the edge of the active area - where the junction meets the outside world - are different from those which operate in the centre. The Schottky barrier is the same as a diffused junction in this respect. The field at the edge of a simple (untreated in any way) Schottky barrier is very high and as a consequence the leakage through the junction at the periphery can also be very high.

In diffused diodes the edge of the junction is treated by 'passivating' it. In a Schottky diode the edge of the barrier is treated by implanting a shallow, very low dose, p region around the periphery of the active area. This region, called a 'guard ring', effectively replaces the high field periphery of the barrier. It is now the characteristics of the guard ring which determine the edge leakage and not those of the Schottky barrier.

In this way the mechanisms controlling the two elements of leakage are now independent and can be adjusted separately, eliminating the need for compromises. This freedom, and a combination of good design and the close tolerance control - achievable with ion implantation - ensures that the characteristics are excellent, having both good stability and very low leakage.

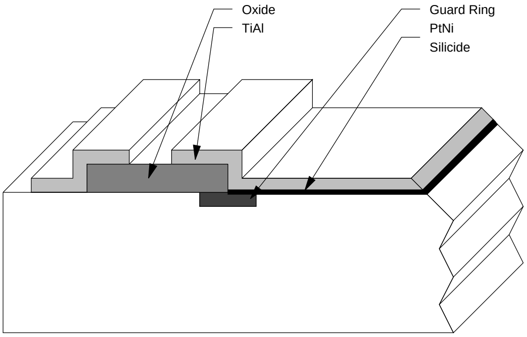


Fig. 2 Cross Section of Schottky Diode

Overall leakage

As mentioned earlier, good reverse characteristics rely upon both the edge and bulk leakages being good. By eliminating the interactions between the mechanisms and by concentrating on optimising each, it has been possible to improve both edge and bulk leakage characteristics. This has allowed Philips to produce Schottky diodes with typical room temperature reverse currents as low as 20µA, or 100µA max (PBYR645CT) - considerably lower than was ever achieved with molybdenum barrier devices.

Range

The Schottky diode was originally designed to be used as the rectifier and freewheel diode in the 5V output of high frequency SMPS. The arrival of the new 100V Schottkies has now extended this up to 24V outputs. These supplies are fitted into equipments whose power requirements vary widely. Satisfying these needs efficiently means that an equally wide range of supplies has to be produced. In recognition of this, Philips has produced a range of diode packages with current ratings from 6A to 30A. With this range it is possible to produce power supplies of 20W to 500W output - higher powers are achievable with parallelling.

The full range of Philips Schottky diodes is shown in Table 1. At the heart of the range are the ’PBYR’ devices. The numbers and letters following the PBYR prefix are compatible with industry standards. These figures give an indication of a device’s structure (single or dual) and its current and voltage rating. An explanation of the numbers is given in Table 2. Care has been taken to ensure compatibility between Philips devices and those from other suppliers, which share number/letter suffices. It is hoped that this will ease the process of equivalent type selection.

Included in the range is a group of devices with ’BYV1xx’ numbers. These devices are a selection of the most popular types from the previous Philips Schottky range. They have proved to be conveniently sized devices which have a mix of ratings and characteristics not matched by other manufacturers. Although these are ’old’ numbers, delivered devices will have been manufactured by the new process and will therefore be better. However, changing the production process of established types can often cause concern amongst customers. Philips has recognised this and, during the development, took particular care to ensure that all the new devices would be as closely comparable as possible with previously delivered product. Clarification is given in the cross reference guide given in Table 3.

Summary

This range of Schottky diodes enhances the ability of Philips Components to meet all the requirements and needs of the SMPS designer. The well established range of epitaxial diodes, bipolar and PowerMOS transistors, ICs and passive components is now complemented by a range of Schottky diodes with:-

- very low forward voltage drop,
- extremely fast reverse recovery,
- low leakage reverse characteristics, achieved WITHOUT compromising overall system efficiency
- stable characteristics at both high and low temperatures
- guaranteed ruggedness, giving reliability under both normal and abnormal operating conditions.

Table 1 Range of Schottky Diodes

Single Diode

Type Number	Outline	$I_{F(AV)}$ (A) per diode	I_O (A) per device	Voltage Grades (V)					
				35	40	45	60	80	100
PBYR7**	TO-220AC	7.5	7.5	*	*	*			
PBYR10**	TO-220AC	10	10	*	*	*	*	*	*
PBYR16**	TO-220AC	16	16	*	*	*			

Dual Diodes - Common Cathode

Type Number	Outline	$I_{F(AV)}$ (A) per diode	I_O (A) per device	Voltage Grades (V)					
				35	40	45	60	80	100
PBYR2**CT	SOT-223	1	2	*	*	*			
PBYR6**CT	SOT-82	3	6	*	*	*			
BYV118**	TO-220AB	5	10	*	*	*			
PBYR15**CT	TO-220AB	7.5	15	*	*	*			
BYV133**	TO-220AB	10	20	*	*	*			
PBYR20**CT	TO-220AB	10	20	*	*	*	*	*	*
BYV143**	TO-220AB	15	30	*	*	*			
PBYR25**CT	TO-220AB	15	30	*	*	*			
PBYR30**PT	SOT-93	15	30	*	*	*	*	*	*

Dual Diodes - Common Cathode (Electrically Isolated Package)

Type Number	Outline	$I_{F(AV)}$ (A) per diode	I_O (A) per device	Voltage Grades (V)					
				35	40	45	60	80	100
BYV118F**	SOT-186 (3 leg)	5	10	*	*	*			
PBYR15**CTF	SOT-186 (3 leg)	7.5	15	*	*	*			
BYV133F**	SOT-186 (3 leg)	10	20	*	*	*			
PBYR20**CTF	SOT-186 (3 leg)	10	20	*	*	*			
BYV143F**	SOT-186 (3 leg)	15	30	*	*	*			
PBYR25**CTF	SOT-186 (3 leg)	15	30	*	*	*			
PBYR30**PTF	SOT-199	15	30	*	*	*			

Single Diodes (Electrically Isolated Package)

Type Number	Outline	$I_{F(AV)}$ (A) per diode	I_O (A) per device	Voltage Grades (V)					
				35	40	45	60	80	100
PBYR7**F	SOT-186 (2 leg)	7.5	7.5	*	*	*			
PBYR10**F	SOT-186 (2 leg)	10	10	*	*	*			
PBYR16**F	SOT-186 (2 leg)	16	16	*	*	*			

Table 2 ’PBYR’ Types - explanation of the numbering system.

The numerical part of the type number gives information about the current and voltage rating of the devices. The final two digits are the voltage grade. The number(s) preceding these give an indication of the current rating. This figure must be used with care. Single and dual devices derive this number in different ways so the data sheet should be consulted before final selection is made.

Letters after the type number indicate that the device is NOT a single diode package. The codes used by Philips can be interpreted as follows:-

CT - means that the device is dual and the cathodes of the two diodes are connected together.
PT - means the device is a dual with common cathode but for compatibility reasons ’CT’ cannot be used.

For example
PBYR1645 a device consisting of a single diode with an average current rating ($I_{F(AV)}$) of 16 A and a reverse voltage capability of 45 V.

Table 3 Cross Reference Guide

Single Diodes

Old Type	Intermediate Type	New Type
BYV19-**	none	PBYR7**
none	none	PBYR10**
BYV39-**	none	PBYR16**
BYV20-**	BYV120-**	none
BYV21-**	BYV121-**	none
BYV22-**	withdrawn	none
BYV23-**	withdrawn	none

Dual Diodes - Common Cathode

Old Type	Intermediate Type	New Type
none	none	PBYR6**CT
BYV18-**	BYV118-**	none
BYV33-**	BYV133-**	PBYR15**CT
none	none	PBYR20**CT
BYV43-**	BYV143-**	PBYR25**CT
BYV73-**	none	PBYR30**PT

FULL PACK Dual Diodes - Common Cathode

Old Type	Intermediate Type	New Type
none	BYV118F-**	none
BYV33F-**	BYV133F-**	PBYR15**CTF
none	none	PBYR20**CTF
BYV43F-**	BYV143F-**	PBYR25**CTF

2.2.3 An Introduction to Synchronous Rectifier Circuits using PowerMOS Transistors

Replacing diodes with very low $R_{DS(on)}$ POWERMOS transistors as the output rectifiers in Switch Mode Power Supplies operating at high operating frequencies can lead to significant increases in overall efficiency. However, this is at the expense of the extra circuitry required for transistor drive and protection. In applications where efficiency is of overriding importance (such as high current outputs below 5V) then synchronous rectification becomes viable.

This paper investigates two methods of driving synchronous rectifiers:-

(i) Using extra transformer windings.

(ii) Self-driven without extra windings.

Multi-output power supplies do not easily lend themselves to extra transformer windings (although there is usually only one very low output voltage required in each supply). Therefore, the self-driven approach is of more interest. If the additional circuitry and power devices were integrated, an easy to use, highly efficient rectifier could result.

Introduction.

The voltage drop across the output diode rectifiers during forward conduction in an SMPS absorbs a high percentage of the watts lost in the power supply. This is a major problem for low output voltage applications below 5V (See section 2.2.1). The conduction loss of this component can be reduced and hence, overall supply efficiency increased by using very low $R_{DS(on)}$ POWERMOS transistors as synchronous rectifiers (for example, the BUK456-60A).

The cost penalties involved with the additional circuitry required are usually only justified in the area of high frequency, low volume supplies with very low output voltages. The methods used to provide these drive waveforms have been investigated for various circuit configurations, in order to assess the suitability of the POWERMOS as a rectifier.

The main part of the paper describes these circuit configurations which include flyback, forward and push-pull topologies. To control the synchronous rectifiers they either use extra windings taken from the power transformer or self-driven techniques.

The PowerMOS as a synchronous rectifier.

POWERMOS transistors have become more suitable for low voltage synchronisation for the following reasons:-

(1) The cost of the POWERMOS transistor has fallen sharply in recent years.

(2) Very low $R_{DS(on)}$ versions which yield very low conduction losses have been developed.

(3) The excellent POWERMOS switching characteristics and low gate drive requirements make them ideal for high frequency applications.

(4) Parallelling the POWERMOS devices (which is normally straightforward) will significantly reduce the $R_{DS(on)}$, thus providing further increases in efficiency. This process is not possible with rectifier diodes since they have inherent forward voltage offset levels.

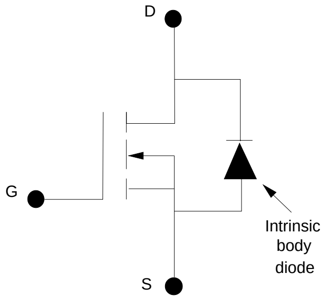


Fig. 1 POWERMOS transistor showing body diode.

Design constraints.

When the POWERMOS transistor shown in Fig. 1 is used as a synchronous rectifier, the device is configured such that the current flow is opposite to that for normal operation i.e. from source to drain. This is to ensure reverse voltage blocking capability when the transistor is turned off, since there will be no current path through the parasitic body diode. This orientation also gives a degree of safety. If the gate drive is lost, the body diode will then perform the rectification, albeit at a much reduced efficiency.

Unfortunately, this configuration has limitations in the way in which it can be driven. The device gate voltage must always be kept below ± 30V. The on-resistance ($R_{DS(on)}$) of the device must be low enough to ensure that the on-state voltage drop is always lower than the V_f of the POWERMOS intrinsic body diode. The gate drive waveforms have to be derived from the circuit in such a way as to ensure that the body diode remains off over the full switching period. For some configurations this will be costly since it can involve discrete driver I.C.s and isolation techniques.

If the body diode were to turn on at any point, it would result in a significant increase in the POWERMOS conduction loss. It would also introduce the reverse recovery characteristic of the body diode, which could seriously degrade switching performance and limit the maximum allowable frequency of operation.

It is well known that the $R_{DS(on)}$ of the POWERMOS is temperature dependent and will rise as the device junction temperature increases during operation. This means that the transistor conduction loss will also increase, hence, lowering the rectification efficiency. Therefore, to achieve optimum efficiency with the synchronous rectifier it is important that careful design considerations are taken (for example good heat-sinking) to ensure that the devices will operate at as low a junction temperature as possible.

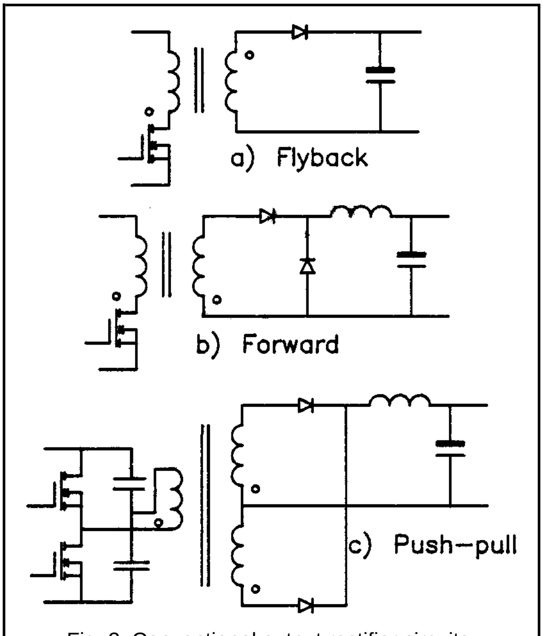


Fig. 2 Conventional output rectifier circuits.

Transformer Driven Synchronous Rectifiers.

The conventional output rectifier circuits for the flyback, forward and push-pull converters are shown in Fig. 2. These diodes can be replaced by POWERMOS transistors which are driven off the transformer as shown in Fig. 3. These configurations can be summarised as follows:-

(a) Flyback converter - this is very straightforward; the gate voltage can be maintained at below 30V and the body diode will not come on.

(b) Forward converter - the gate drives for the two transistors can be maintained below 30V. However, due to the shape of the transformer waveforms, the freewheel rectifier will not have a square wave signal and the body diode could come on.

(c) Push-pull converter - deriving the gate drives for the two synchronous rectifiers from the transformer means that during the dead time which occurs in each switching cycle, both transistors are off. There is nowhere for the circulating current to go and body diodes will come on to conduct this current. This is not permissible because of the slow characteristics of the less than ideal body diode. Therefore, the push-pull configuration cannot be used for synchronous rectification without the costly derivation of complex drive waveforms.

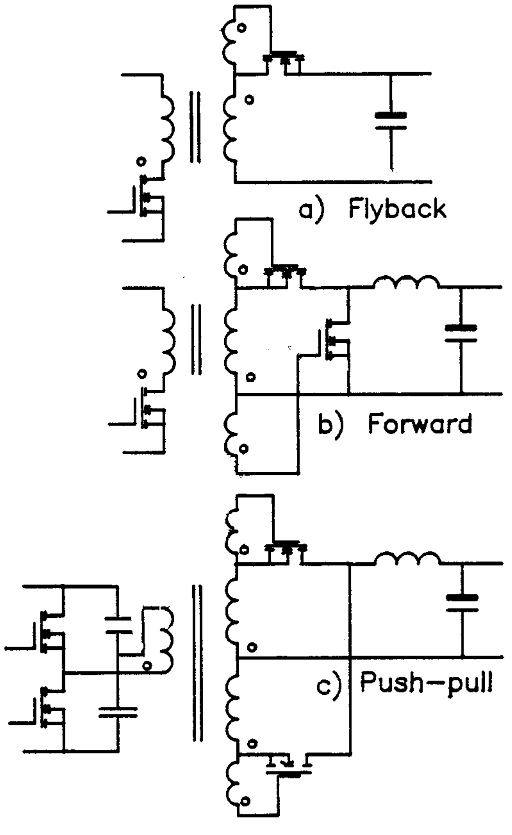


Fig. 3 Synchronous rectifier circuits with windings.

One significant advantage of using this topology is that the r.m.s. current of the rectifiers and, hence, overall conduction loss is significantly lower in the push-pull than it is in the forward or flyback versions.

Self-Driven Synchronous Rectifiers.

The disadvantage of the transformer driven POWERMOS is the requirement for extra windings and extra pins on the power transformer. This may cause problems, especially for multi-output supplies. A method of driving the transistors without the extra transformer windings would probably be more practical. For this reason basic self-driven synchronous rectifier circuits were investigated.

It should be noted that the following circuits were based upon an output of 5V at 10A. In practice, applications requiring lower voltages such as 3 or 3.3 volts at output currents above 20A will benefit to a far greater extent by using synchronous rectification. For these conditions the efficiency gains will be far more significant. However, the 5V output was considered useful as a starting point for an introductory investigation.

(a) The Flyback converter.

An experimental circuit featuring the flyback converter self-oscillating power supply was developed. This was designed to operate at a switching frequency of 40kHz and delivered 50W (5V at 10A).

Directly substituting the single rectifier diode with the POWERMOS transistor as is shown in Fig. 4(a) does not work because the gate will always be held on. The gate is Vo above the source so the device will not switch.

Therefore, some additional circuitry is required to perform the switching, and the circuitry used is shown in Fig. 4(b). The BUK456-60A POWERMOS transistor which features a typical $R_{DS(on)}$ of 24mΩ (at 25˚C) was used as the synchronous rectifier for these basic configurations.

The drive circuit operates as follows: the pnp transistor switches on the POWERMOS and the npn switches it off. Good control of the POWERMOS transistor is possible and the body diode does not come on. The waveforms obtained are also shown in Fig. 4.

If the small bipolar transistors were replaced by small POWERMOS devices, then this drive circuit would be a good candidate for miniaturisation in a Power Integrated Circuit. This could provide good control with low drive power requirements.

Unfortunately, the single rectifier in a flyback converter must conduct a much higher r.m.s. current than the two output diodes of the buck derived versions (for the same output power levels). Since the conduction loss in a POWERMOS is given by $I_{D(RMS)}^{2}.R_{DS(on)}$, it is clear that the flyback, although simple, does not lend itself as well to achieving large increases in efficiency when compared to other topologies that utilise POWERMOS synchronous rectifiers.

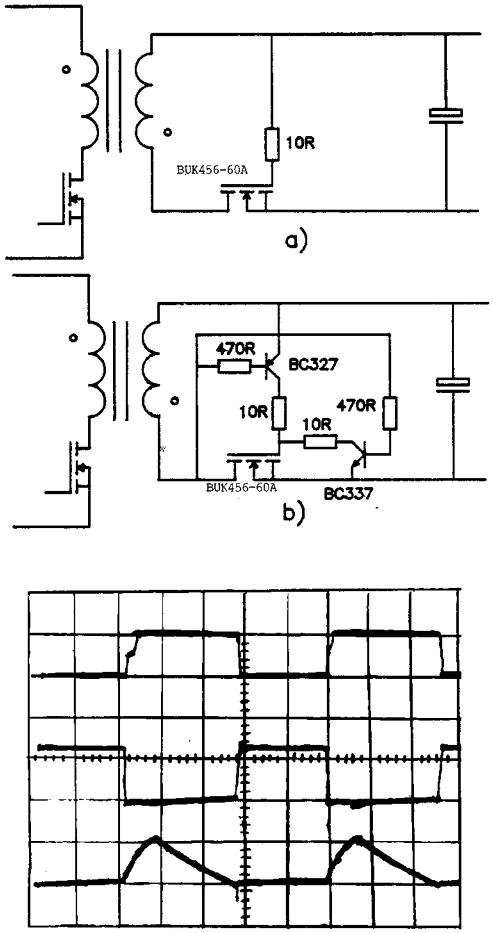
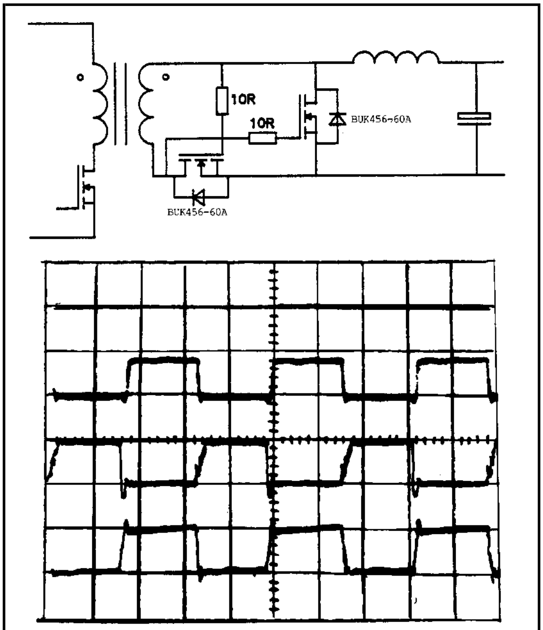


Fig. 4 Flyback self-driven synchronous rectifier circuits.

(b) The Forward converter.

An experimental self-driven circuit based on the forward converter was then investigated. In this version the frequency of operation was raised to 300kHz with the supply again delivering 5V at 10A.

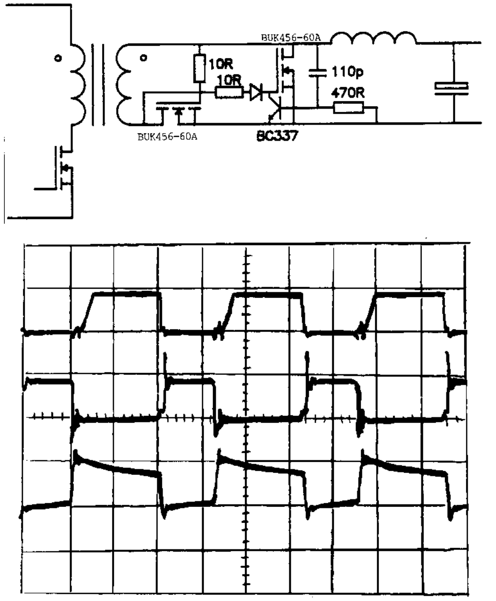
The direct replacement of the output diodes with POWERMOS transistors is shown in Fig. 5. In this arrangement, the gate sees the full voltage across the transformer winding. Therefore, the supply input voltage range must be restricted to ensure the gate of the POWERMOS is not driven by excessively high voltages. This would occur during low primary transistor duty cycle conditions. The waveforms obtained for the forward synchronous rectifier in this configuration are also shown in Fig. 5.



(Forward rectifier) Timebase: 1µs/div
Top trace: V_{GS} - 20V/div
Middle: V_{DS} - 20V/div
Bottom: I_D - 10A/div
Fig. 5 Forward converter with synchronous rectification - direct replacement with POWERMOS.

In this case the method of control is such that the gate is referenced to the source via the drain-source body diode. This clamps the gate, enabling it to rise to a voltage which will turn the POWERMOS on. If the body diode was not present, the gate would always remain negative with respect to the source and an additional diode would have to be added to provide the same function.

Additional circuitry is required to turn off the freewheel synchronous rectifier. This is due to the fact that when the freewheel POWERMOS conducts, the body diode will take the current first before the gate drive turns the device on. An additional transistor can be used to turn off the POWERMOS in order to keep conduction out of the body diode. This additional transistor will short the gate to ground and ensures the proper turn-off of the POWERMOS. The circuit with this additional circuitry and the resulting freewheel rectifier waveforms are given in Fig. 6.



(Freewheel rectifier) Timebase: 1µs/div
Top waveform: V_{GS} - 20V/div
Middle: V_{DS} - 20V/div
Bottom: I_D - 10A/div
Fig. 6 Forward converter with synchronous rectification - additional circuitry to turn-off body diode.

A very simple circuit configuration can be used in which body diode conduction in the freewheel synchronous rectifier does not occur. By driving the freewheel rectifier from the output choke via a closely coupled winding, a much faster turn-on can be achieved because the body diode does not come on. This circuit configuration and associated waveforms are shown in Fig. 7.

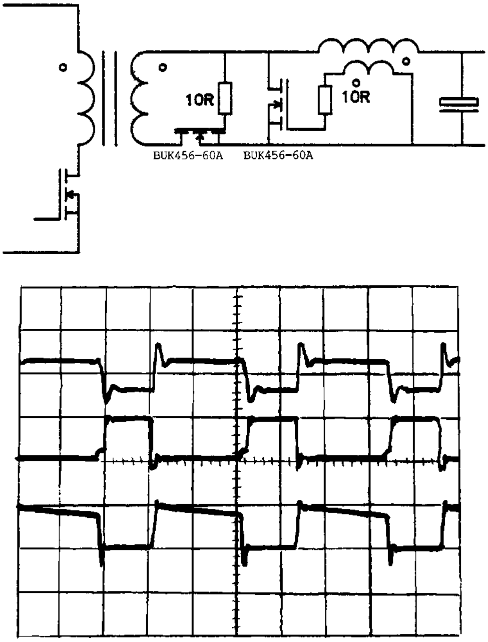
To avoid gate over-voltage problems a toroid can been added which will provide the safe drive levels. This toroid effectively simulates extra transformer windings without complicating the main power transformer design. The limitations of this approach are that there will be extra leakage inductance and that an additional wound component is required. The applicable circuit and waveforms for this arrangement are given in Fig. 8.

Conclusions

The main advantage of POWERMOS synchronous rectifiers over existing epitaxial and Schottky diode rectifiers is the increase in efficiency. This is especially true for applications below 5V, since the development of very low $R_{DS(on)}$ POWERMOS transistors allows very significant efficiency increases. It is also very easy to parallel the POWERMOS transistors in order to achieve even greater efficiency levels.

The difficulties involved with generating suitable drives for the POWERMOS synchronous rectifiers tend to restrict the number of circuits for which they are suitable. It will also significantly increase the cost of the supply compared with standard rectifier technology.

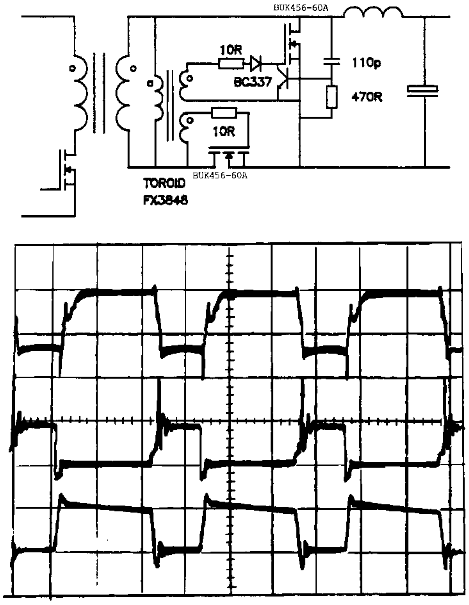
The circuit examples outlined in this paper were very basic. However, they did show what can be achieved. The flyback configuration was the simplest, and there were various possibilities for the forward converters.



(Freewheel rectifier) Timebase: 1µs/div
Top waveform: V_{GS} - 20V/div
Middle: V_{DS} - 20V/div
Bottom: I_D - 10A/div
Fig. 7 Forward converter with synchronous rectification - avoiding body diode conduction.

Recent work has shown that there are topologies more suited to using MOSFET synchronous rectifiers (featuring low rectifier r.m.s. current levels) such as the push-pull. These can achieve overall power supply efficiency levels of up to 90% for outputs of 5V and below. However, the discrete control circuitry required is quite complex and requires optical/magnetic isolation, since the waveforms must be derived from the primary-side control.

The true advantage of synchronous rectifiers may only be reached when the drive circuit and POWERMOS devices are hybridised into Power Integrated Circuits. However, in applications where the efficiency performance is of more importance than the additional costs incurred, then POWERMOS synchronous rectification is presently the most suitable technique to use.



(Freewheel rectifier) Timebase: 1µs/div
Top waveform: V_{GS} - 20V/div
Middle: V_{DS} - 20V/div
Bottom: I_D - 10A/div
Fig. 8 Forward converter with synchronous rectifiers - method of protecting the gate inputs.

Design Examples

2.3.1 Mains Input 100 W Forward Converter SMPS: MOSFET and Bipolar Transistor Solutions featuring ETD Cores

The following two switched-mode power supplies described are low cost easy to assemble units, intended primarily for the large number of equipment manufacturers who wish to build power supplies in-house.

The designs are based upon recent technologies and both feature ETD (Economic Transformer Design) ferrite cores. The first design features a high voltage Bipolar transistor, the BUT11 at a switching frequency of 50kHz. The second design is based around a power MOSFET transistor, the BUK456-800A whose superior switching characteristics allow higher switching frequencies to be implemented. In this case 100kHz was selected for the MOSFET version allowing the use of smaller and cheaper magnetic components compared with the lower frequency version.

Both supplies operate from either 110/120 or 220/240 V mains input, and supply 100W of regulated output power up to 20A at 5V, with low power auxiliary outputs at ±12V. The PowerMOS solution provides an increase in efficiency of 5% compared with the Bipolar version, and both have been designed to meet stringent R.F.I. specifications.

ETD ferrite cores have round centre poles and constant cross-sectional area, making them ideally suited for the windings required in high-frequency S.M.P.S. converters. The cores are available with clips for rapid assembly, and the coil formers are suitable for direct mounting onto printed circuit boards.

The ETD cores, power transistors and power rectifiers featured are part of a comprehensive range of up-to-date components available from Philips from which cost effective and efficient S.M.P.S. designs can be produced.

50kHz Bipolar version

Circuit description

The circuit design which utilises the Bipolar transistor is shown in Fig. 1. This is based upon the forward converter topology, which has the advantage that only one power switching transistor is required.

An operating frequency of 50kHz was implemented using a BUT11 transistor (available in TO-220 package or isolated SOT-186 version). This was achieved by optimising the switching performance of the BUT11 Bipolar power transistor TR5, by careful design of the base drive circuitry and by the use of a Baker clamp. The 50kHz operating frequency allows the size and the cost of the transformer and choke to be reduced compared with older Bipolar based systems which worked around 20kHz.

The base drive waveform generated by IC1 is buffered through TR3 and TR4 to the switching transistor TR5. Although operating from a single auxiliary supply line, the drive circuit provides optimum waveforms. At turn-off, inductor L3 controls the rate of change of reverse bias current ($-dI_B/dt$). The reverse base-emitter voltage is provided by capacitor C16 (charged during the on-time). The resulting collector current and voltage waveforms are profiled by a snubber network to ensure that the transistor SOA limits are not exceeded.

Voltage regulation of the 5V output is effected by means of an error signal which is fed back, via the CNX82A opto-coulper, to IC1 which adjusts the transistor duty cycle. Over-current protection of this output is provided by monitoring the voltage developed across the 1Ω resistor, R28 and comparing this with an internal reference in IC1. Voltage regulation and overcurrent protection for the 12V outputs are provided by the linear regulating integrated circuits IC4 and IC5.

Specification and performance (Bipolar version)

Input

220/240 V a.c. nominal	(range 187 to 264 V a.c.)
110/120 V a.c. nominal	(range 94 to 132 V a.c.)

Output

Total output power = 100 W.

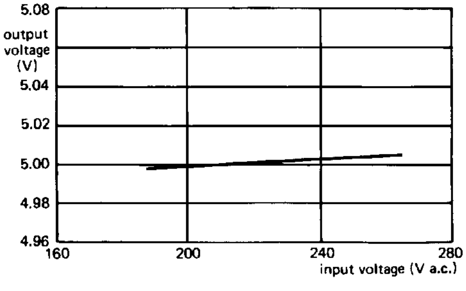


Fig. 2 Output voltage versus input voltage - (I_{out} = 20A).

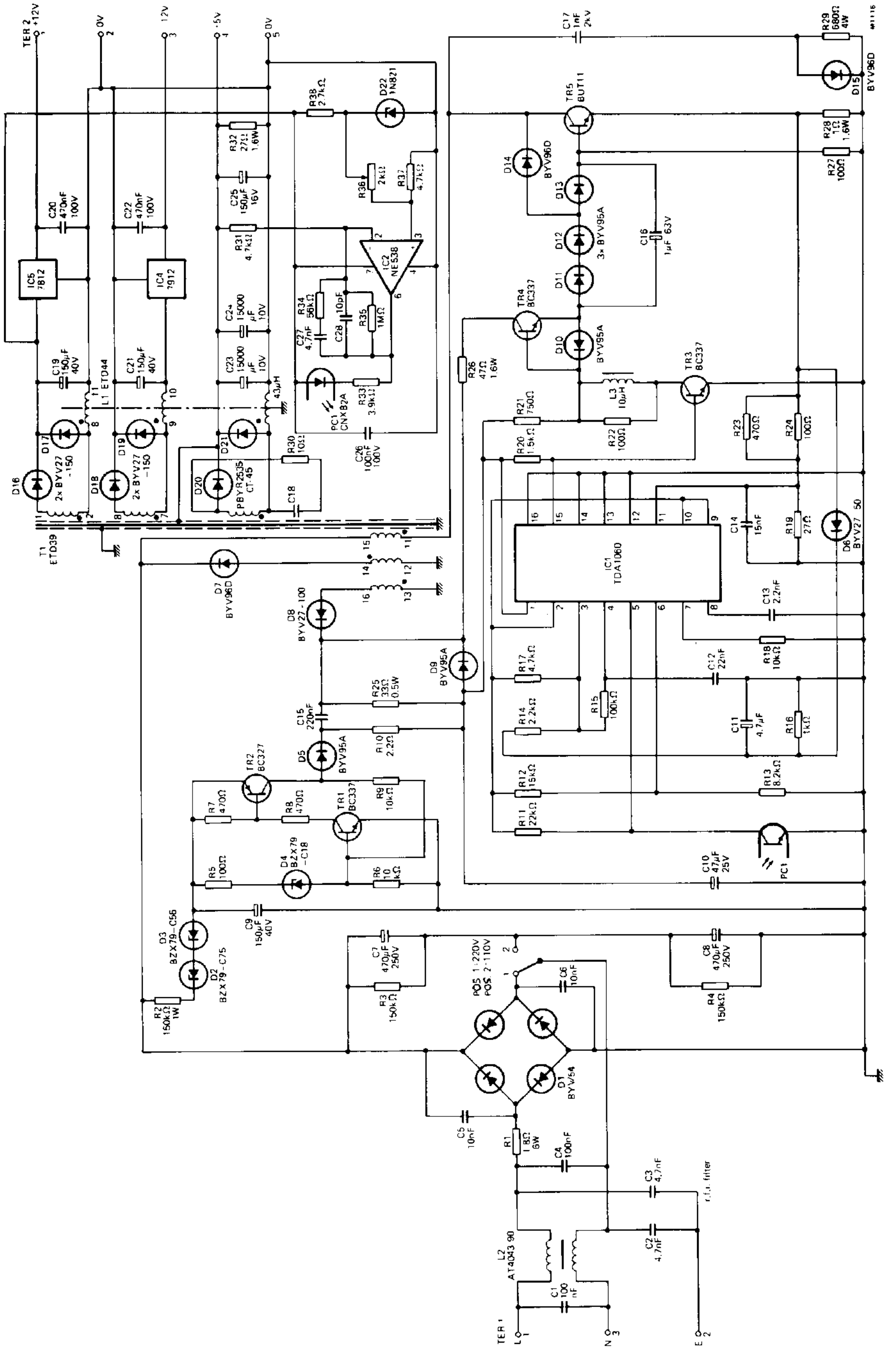

TER 2
+12V 1
0V 2
12V 3
+5V 4
0V 5
C17 1nF 2kV
R29 680Ω 4W
D15 BYV96D
TR5 BUT11
R28 1Ω 1.6W
R27 100Ω
D14 BYV96D
D13
D12 3× BYV95A
D11
C16 1µF 63V
TR4 BC337
D10 BYV95A
TR3 BC337
R26 47Ω 1.6W
R21 750Ω
L3 10µH
R22 100Ω
R20 1.5kΩ
R23 470Ω
R24 100Ω
IC1 TDA1060
C14 15nF
R19 27Ω
D6 BYV27 50
C13 2.2nF
R18 10kΩ
R17 4.7kΩ
C12 22nF
R14 2.2kΩ
R15 100kΩ
C11 4.7µF
R16 1kΩ
R12 15kΩ
R13 8.2kΩ
R11 22kΩ
PC1
C10 47µF 25V
R38 2.7kΩ
D22 1N821
R32 27Ω 1.6W
C25 150µF 16V
R36 2kΩ
R37 4.7kΩ
R31 4.7kΩ
IC2 NE538
C24 15000 µF 10V
R34 56kΩ
C27 4.7nF
C28 10pF
R35 1MΩ
C23 15000 µF 10V
PC1 CNX82A
R33 3.9kΩ
43µH
C26 100nF 100V
R30 10Ω
D21
D20 PBYR2535 CT-45
C18
C20 470nF 100V
IC5 7812
C22 470nF 100V
IC4 7912
C19 150µF 40V
C21 150µF 40V
L1 ETD44
D17
D16 2× BYV27 -150
D19
D18 2× BYV27 -150
T1 ETD39
D7 BYV96D
D8 BYV27-100
D9 BYV95A
R25 33Ω 0.5W
C15 220nF
R10 2.2Ω
D5 BYV95A
TR2 BC327
R7 470Ω
R8 470Ω
TR1 BC337
R9 10kΩ
R5 100Ω
D4 BZX79 -C18
R6 10 kΩ
C9 150µF 40V
D3 BZX79-C56
D2 BZX79-C75
R2 150kΩ 1W
C7 470µF 250V
R3 150kΩ
POS 1: 220V
POS 2: 110V
C6 10nF
C8 470µF 250V
R4 150kΩ
D1 BYW54
C5 10nF
R1 1.8Ω 6W
C4 100nF
C3 4.7nF
r.f.i. filter
C2 4.7nF
L2 AT4043 90
C1 100 nF
TER 1
L 1
N 3
E 2

Fig. 1 100W SMPS circuit diagram (50kHz Bipolar transistor version).

Main output

5V at 20A max output power - Adjustment range ±5%.

Line regulation

The change in output voltage over the full input voltage range of 187 to 264 V is typically 0.2%; see Fig. 2.

Load regulation

The change in output voltage over the full load range of zero to 100 W is typically 0.4%; see Fig. 3.

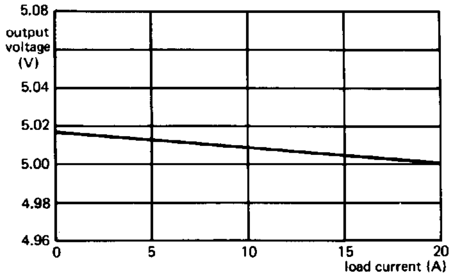


Fig. 3 Output voltage as a function of output current (input voltage = 220Vac).

Auxiliary outputs

±12V at 0.1A.
Regulation (worst-case condition of max change in input voltage and output load) < 0.4%.

Ripple and Noise

0.2% r.m.s. 1.0% pk-pk (d.c. to 100MHz).

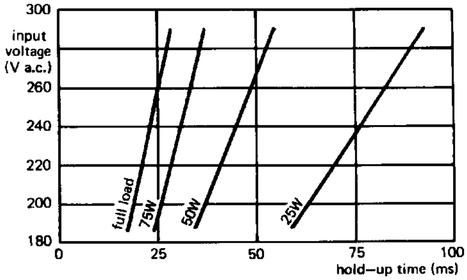


Fig. 4 Output hold-up during mains drop-out at input.

Output hold-up

Both the main and auxiliary outputs will remain within specification for a missing half-cycle (18ms) at full load and minimum input voltage; see Fig. 4.

Isolation

Input to output ground	2kV r.m.s.
Output to ground	500V r.m.s.

Efficiency

The ratio of the d.c output power to the a.c input power is typically 71% at full load; See Fig. 5.

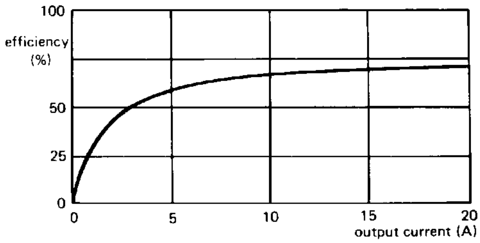


Fig. 5 Efficiency as a function of output current.

Radio frequency interference

R.F.I. fed back to the mains meets VDE0875N and BS800.

Transient response

The response to a 50% change in load is less than 200mV and the output returns to the regulation band within 400µs: See Fig. 6.

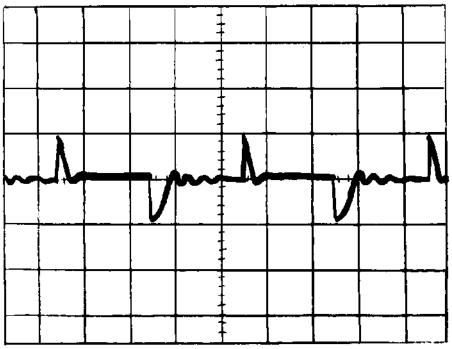


Fig. 6 Response to 50% change in load with nominal 220Vmains input.
Vertical scale: 200nV/div
Horizontal scale: 1ms/div

Optimum drive of high voltage Bipolar transistor (H.V.T.)

A feature of the high voltage Bipolar transistor is the very low conduction loss that can be obtained. This is made possible by the "conductivity modulation" process that takes place due to the influence of minority carriers in the collector region of the device. However, the presence of these carriers means that a stored charge will exist within the collector region (especially in high voltage types) which has the effect of producing relatively slow switching speeds. This leads to significant switching losses, limiting the maximum frequency of operation to around 50kHz.

To effectively utilise the power switching H.V.T. the base drive must be optimised to produce the lowest switching losses possible. This is achieved by accurate control of the injection and more importantly the removal of the stored charge during the switching periods. This is fulfilled by controlling the transistor base drive current. (The Bipolar transistor is a current-controlled device). The simple steps taken to achieve this are summarised as follows:-

(1) A fast turn-on "kick-up" pulse in the base current should be provided to minimise the turn-on time and associated switching loss.

(2) Provide the correct level of forward base current during conduction, based upon the high current gain of the transistor. This ensures the device is neither over-driven (which will cause a long turn-off current tail) nor under-driven (coming out of saturation causing higher conduction loss). The Baker clamp arrangement used (see Fig. 1) prevents transistor over-drive (hard saturation).

(3) The correct level of negative base drive current must be produced to remove the stored charge from the transistor at turn-off. The majority of this charge is removed during the transistor storage time t_s. This cannot be swept out too quickly, otherwise a "crowding effect" will taken place causing a turn-off current tail with very high switching loss. This accurate control of the charge is provided by a series inductor placed in the path of the negative base drive circuit. (For further information see sections 1.3.2. and 2.1.3).

BUT11 waveforms

These techniques have been applied in the BUT11 drive circuit shown in Fig. 1, and the resulting base drive waveforms are given in Fig. 7.

Optimised base drive minimises both turn-on and turn-off switching loss, limiting the power dissipation in both the transistor and snubber resistor allowing acceptable operation at 50kHz. This is outlined in Fig. 8 which gives the BUT11 collector current (I_C) and collector-emitter voltage (V_{CE}) waveforms.

The transistor $V_{CE(sat)}$ would normally be as low as 0.3V. However, the use of the Baker clamp limits it to about 1V. Even so this still yields a transistor conduction loss of only 0.76W for the full output load condition.

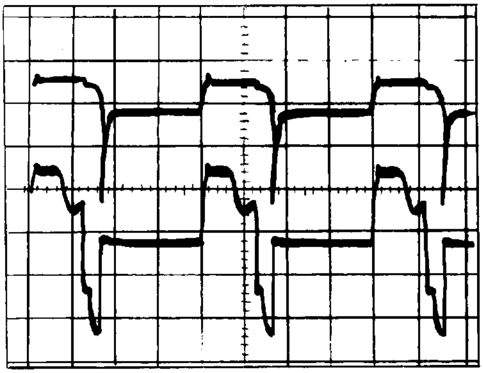


Fig. 7 Base voltage V_B and base current I_B of BUT11 with nominal 220V input and full 5V, 20A output.
Upper trace V_B: 5V/div
Lower trace I_B: 0.2A/div
Horizontal scale: 5µs/div

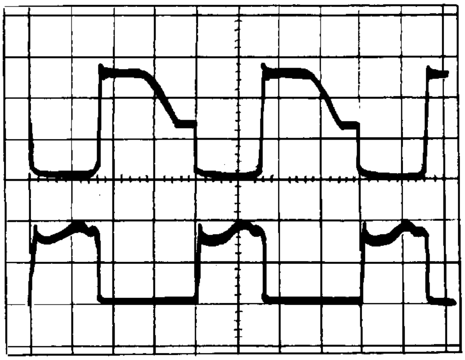


Fig. 8 Collector-emitter voltage V_{CE} and collector current I_C for the BUT11 with nominal 220V mains input and full 5V, 20A output.
Upper trace V_{CE}: 200V/div
Lower trace I_C: 1A/div
Horizontal scale: 5µs/div

50kHz Magnetics design

Output Transformer

For 50kHz operation the transformer was designed using an ETD39 core. The winding details are given in Fig. 9 and listed as follows:-

Winding

1.	1/2 demag	42 turns 0.315mm dia. enamelled copper wire (e.c.w.) (single layer).
2, 3	1/2 primary	42 turns 0.315mm e.c.w.(2 layers in parallel).
4, 5	r.f.i. screens	each 1 turn 0.05 x 16.5mm copper strip.
6.	5V sec	6 turns 0.2 x 16.5mm copper strip.
7.	±12V sec	18 turns 0.355mm e.c.w. bifilar wound (1 wire each output).
8, 9	r.f.i. screens	each 1 turn 0.05 x 16.55mm copper strip.
10, 11	1/2 prim	42 turns 0.315mm e.c.w. (2 layers in parallel).
12.	1/2 demag	42 turns 0.315 e.c.w (single layer).
13.	primary drive	7 turns 0.2mm e.c.w.
-	interleaving	0.04mm film insulation.

Airgap 0.1mm total in centre pole.

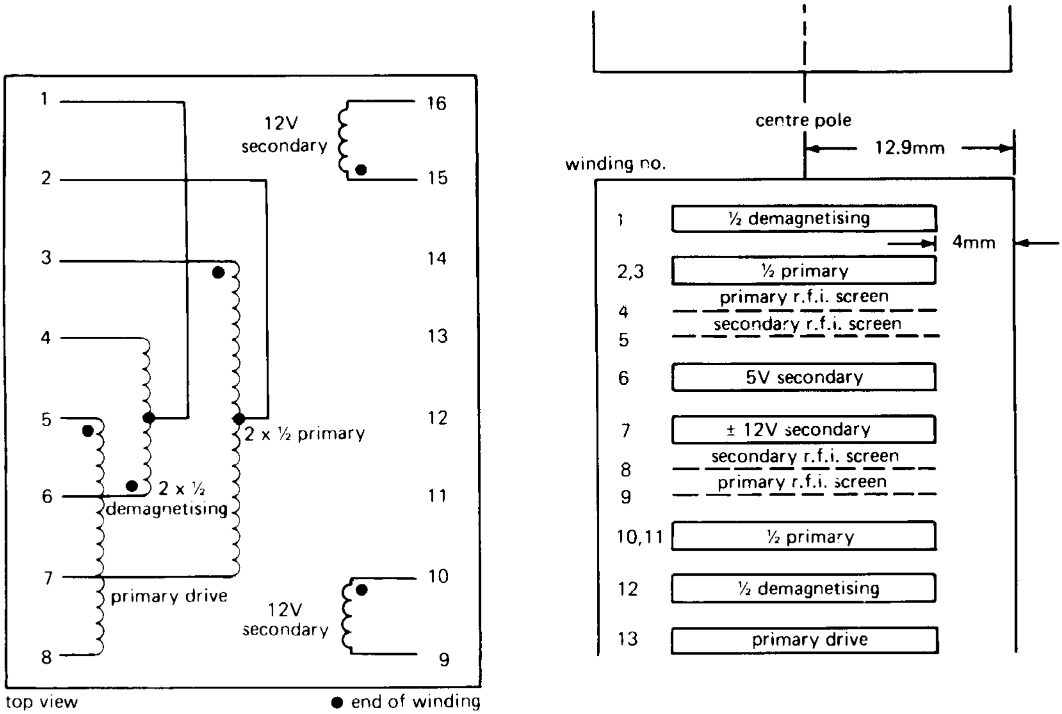

1
2
3
4
5
6
7
8
16
15
14
13
12
11
10
9
12V secondary
2 x ½ primary
2 x ½ demagnetising
primary drive
12V secondary
top view
● end of winding
centre pole
12.9mm
winding no.
4mm
1
½ demagnetising
2,3
½ primary
primary r.f.i. screen
4
secondary r.f.i. screen
5
6
5V secondary
7
± 12V secondary
secondary r.f.i. screen
8
primary r.f.i. screen
9
10,11
½ primary
12
½ demagnetising
13
primary drive

Fig. 9 50kHz Output transformer winding details. The 5V secondary and r.f.i. screens are connected together by flying leads. Pin numbering is consistent with the ETD39 coil former.

(The insulation has been added to meet isolation and safety requirements for a mains input SMPS.)

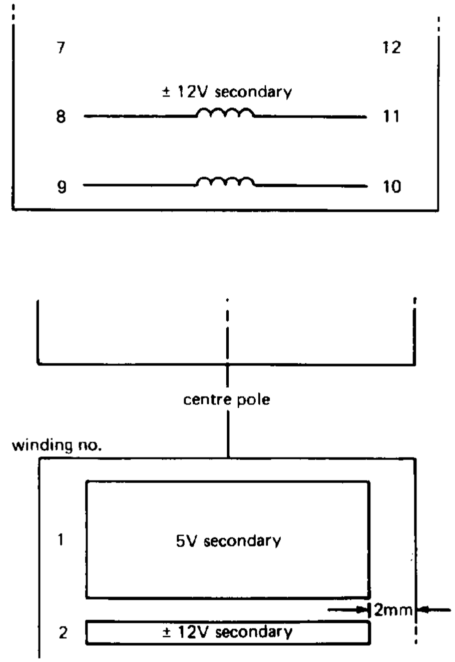


Fig. 10 50kHz output choke L1, winding details.
Inductance of 5V winding = 43µH.
Coupled Inductor technique.

50kHz output chokes

All of the output chokes have been wound on a single core; i.e. using the coupled inductor approach. This reduces overall volume of the supply and provides better dynamic cross-regulation between the outputs. The design of this choke, L1, is based upon 43µH for the main 5V output, using an ETD44 core which was suitable for 100W, 50kHz operation.

The winding details are shown in Fig. 10 and are specified as follows :-

Windings

1. 19 turns 0.25 x 25mm copper strip.
2. 57 turns 0.4mm e.c.w. bifilar wound.

Airgap 2.5mm total in centre pole.

Note. Choke L3 was wound with 1 turn 0.4mm e.c.w.

100kHz MOSFET version

The circuit version of the 100W forward converter based around the high voltage power MOSFET is shown in Fig. 11. The operating frequency in this case has been doubled to 100kHz.

Feedback is again via opto-coupler IC1, the CNX83A which controls the output by changing the duty cycle of the drive waveform to the power MOSFET transistor, TR3 which is the BUK456-800A (available in TO-220 package or the fully isolated SOT-186 version). The transistor is driven by IC4 via R16 and operates within its SOA without a snubber: see the waveforms of Fig. 15. There is low auxiliary supply voltage protection and primary cycle by cycle current limiting which inhibit output drive pulses and protect the supply.

The power supply control and transistor drive circuitry (enclosed within the broken lines in Fig. 11) have low current requirements (5mA). This allows dropper resistors R2 and R3 to provide the supply for these circuits directly from the d.c. link thereby removing the supply winding requirement from the transformer.

Specification and performance (MOSFET version)

The specification and performance of the 100kHz MOSFET version is the same as the earlier 50kHz Bipolar version with the exception of the following parameters:-

Output ripple and noise

< 10 mV r.m.s.
< 40mV pk-pk (100MHz bandwidth) See Fig. 12.

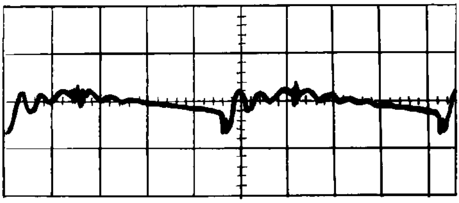


Fig. 12 Output voltage and noise at full load for 100kHz version.
Vertical scale: 50mV/div.
Horizontal scale: 2µs/div.

Transient response

The transient response has been improved to a 100mV line deviation returning to normal regulation limits within 100µs for a 10A change in load current.

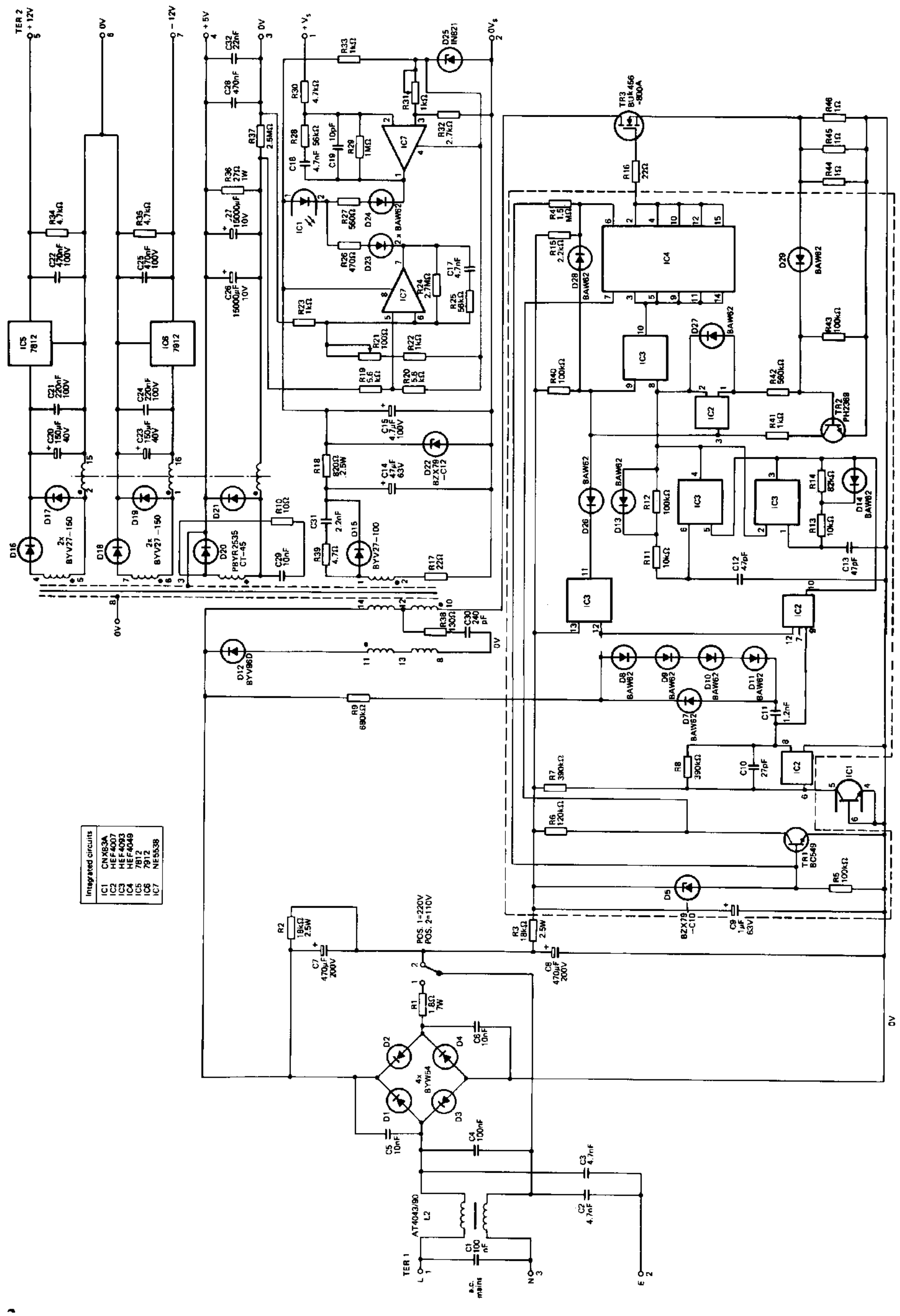

TER 2
+12V
5
0V
6
−12V
7
+5V
4
0V
3
+Vs
1
0Vs
2
D25 1N821
R33 1kΩ
C32 22nF
C28 470nF
R30 4.7kΩ
R31 1kΩ
R32 2.7kΩ
R28 56kΩ
C18 4.7nF
C19 10pF
R29 1MΩ
IC7
R37 2.6MΩ
R36 27Ω 1W
C27 15000µF 10V
C26 15000µF 10V
IC1
R27 560Ω
D24
2 x BAW62
R26 470Ω
D23
C17 4.7nF
R24 2.7MΩ
R25 56kΩ
R23 1kΩ
R21 100Ω
R22 1kΩ
R19 5.6kΩ
R20 5.6kΩ
C15 4.7µF 100V
D22 BZX79-C12
R18 820Ω 2.5W
C14 47µF 63V
C31 2.2nF
R39 4.7Ω
D15 BYV27-100
R17 22Ω
R34 4.7kΩ
C22 470nF 100V
R35 4.7kΩ
C25 470nF 100V
IC5 7812
IC6 7912
C21 220nF 100V
C24 220nF 100V
C20 150µF 40V
C23 150µF 40V
D16
D17
2x BYV27-150
D18
D19
2x BYV27-150
D21
D20
PBYR2535 CT-45
R10 10Ω
C29 10nF
0V
R38 130Ω
C30 240pF
D12 BYV96D
R9 680kΩ
TR3 BUK456-800A
R16 22Ω
R46 1Ω
R45 1Ω
R44 1Ω
R41 1.5MΩ
R15 2.2kΩ
D28 BAW62
IC4
D29 BAW62
D27 BAW62
IC3
R40 100kΩ
R42 560kΩ
R43 100kΩ
IC2
R41 1kΩ
TR2 PH2369
D26 BAW62
D13 BAW62
R12 100kΩ
R11 10kΩ
R14 82kΩ
R13 10kΩ
D14 BAW62
C12 47pF
C13 47pF
D8 BAW62
D9 BAW62
D10 BAW62
D11 BAW62
D7 BAW62
C11 1.2nF
R8 390kΩ
C10 27pF
R7 390kΩ
R6 120kΩ
TR1 BC549
R5 100kΩ
D5 BZX79-C10
C9 1µF 63V
Integrated circuits
IC1 CNX83A
IC2 HEF4007
IC3 HEF4093
IC4 HEF4049
IC5 7812
IC6 7912
IC7 NE5538
R2 18kΩ 2.5W
C7 470µF 200V
POS. 1=220V
POS. 2=110V
R3 18kΩ 2.5W
C8 470µF 200V
R1 1.8Ω 7W
C6 10nF
D1
D2
D3
D4
4x BYW54
C5 10nF
C4 100nF
C3 4.7nF
C2 4.7nF
L2 AT4043/90
C1 100nF
TER 1
L
N
E
a.c. mains
0V

FIG.11 100W SMPS circuit diagram (100kHz MOSFET version)

Radio frequency interference

The 100kHz version meets BS800 and CISPRA recommendations; see Fig. 13.

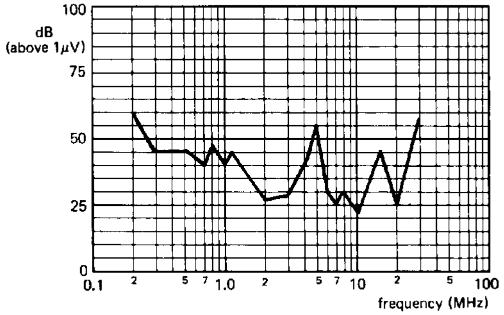


Fig. 13 Measured r.f.i. at supply terminals.

Efficiency

The overall efficiency has been improved by up to 5% compared to the Bipolar version, achieving 76% at full output load. This is mainly due to the more efficient switching characteristics of the MOSFET allowing the removal of the lossy snubber, reduced transistor drive power requirements and lower control circuit power requirements. Fig. 14 shows the overall efficiency of the power supply against load current.

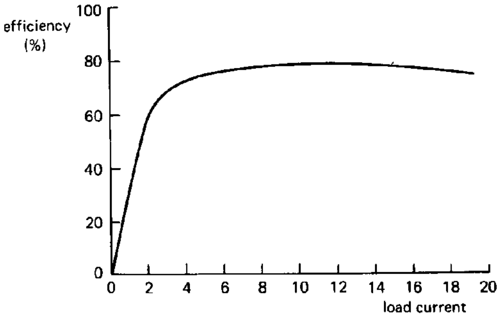


Fig. 14 Efficiency vs load current (V_{IN} = 220V a.c.).

It should be noted that for the high current and low voltage (5V) main output, a large portion of the efficiency loss will be due solely to the output rectifiers' forward voltage drop V_F. Therefore, these two output rectifiers are required to be low loss, very low V_F power Schottky diodes in order to keep overall converter efficiency as high as possible. In this case the Dual PBYR2535CT device was selected for the 5V output. This is available in the TO-220 package and will comfortably rectify an average output current well above the 20A required, providing a suitably sized heat-sink is added.

Mains isolation

The mains isolation conforms to IEC435.

The power MOSFET as a high frequency switch

Power MOSFET transistors are well known for their ease of drive and very fast switching characteristics. Since these are majority carrier devices, they are free from the charge storage effects which lessen the switching performance of the Bipolar products. Driving the MOSFET is far simpler and requires much less drive power than the equivalent Bipolar version.

The speed at which a MOSFET can be switched is determined by the rate at which its internal capacitances can be charged and discharged by the drive circuit. In practice these capacitances are very small (e.g the input capacitance C_{iss} for the BUK456-800A is quoted as 1000pF) allowing MOSFET rise and fall times in the tens of nano-seconds region. The MOSFET can conduct full current when the gate-source voltage V_{GS}, is typically 4V to 6V. However, further increases in V_{GS} are usually employed to reduce the device on-resistance and 8V to 10V is normally the final level applied to ensure a lower conduction loss.

With such fast switching times, the associated switching losses will be very low, giving the MOSFET the ability to operate as an extremely high frequency switch. Power switching in the MHz region can be obtained by using a MOSFET.

One major disadvantage of the MOSFET is that it has a relatively high conduction loss in comparison with bipolar types. This is due to the absence of the minority carriers meaning no "conductivity modulation" takes place.

MOSFET on-resistance

The conduction loss is normally calculated by using the MOSFET "on-resistance", $R_{DS(on)}$, expressed in Ohms. The voltage developed across the device during conduction is an Ohmic drop and will rise as the drain current increases. Therefore, the conduction loss is strongly dependent upon the operating current. Furthermore, the value of the MOSFET $R_{DS(on)}$ is strongly dependent upon temperature, and increases as the junction temperature of the device rises during operation. Clearly, the MOSFET does not compare well to the Bipolar which has a stable low saturation voltage drop $V_{CE(sat)}$, and is relatively independent of operating current or temperature.

It should be noted that the $R_{DS(on)}$ of the MOSFET also increases as the breakdown voltage capability of the device is increased.

How fast should the MOSFET be switched?

Although very fast switching times are achievable with the power MOSFET, it is not always suitable or necessary to use the highest frequency possible. A major limiting factor in S.M.P.S. design is the magnetics. Present high frequency core loss for high grade ferrite core materials such as 3C85 limits the maximum operating frequency to about 200kHz, although new types such as 3F3 are now suitable for use at 500kHz.

There has always been a drive to use ever higher operating frequencies with the aim of reducing magnetics and filter component sizes. However, most S.M.P.S. designs still operate below 300kHz, since these frequencies are quite adequate for most applications. There is no reason to go to higher frequencies unneccessarily, since very high frequency design is fraught with extra technical difficulties.

Furthermore, although the very fast MOSFET switching times reduce switching loss, the increased dI/dt and dV/dt rates will generate far worse oscillations in the circuit parasitics requiring lossy snubbers. The R.F.I. levels generated will also be far more severe, requiring additional filtering to bring the supply within specification. The golden rule in S.M.P.S. square wave switching design is to use the lowest operating frequency and switching times that the application will tolerate.

Estimating required switching times

In the 100kHz example presented here, the typical conduction time of the transistor will be approximately 3μs. A rule of thumb is to keep the sum of the turn-on and turn-off times below 10% of the conduction time. This ensures a wide duty cycle control range with acceptable levels of switching loss. Hence, the target here was to produce switching times of the order of 100ns to 150ns.

Gate drive requirements

The capacitances of the power MOSFET are related to the overall chip size with the gate-source capacitance typically in the range 1nF to 2nF. However, these capacitances are very voltage dependent and are not suitable for estimating the amount of drive current required to obtain the desired switching times. A more accurate method is to use the information contained in the turn-on gate charge (Q_G) characteristic given in the data-sheets. The graph of Q_G for the BUK456-800A for a maximum d.c. rated drain current of 4A is shown in Fig. 15.

The shape of this characteristic needs explaining. The initial slope shows the rise of V_{GS} to the device 4A threshold voltage V_{th}. This requires very little charge, and at the top point of this slope the MOSFET can then conduct full current. However, further gate charge is required while V_{DS} falls from its off-state high voltage to its low on-state level. This is the flat part of the characteristic and at the end of this region the MOSFET is fully switched on. (This is shown for a range of initial off state voltages). The second slope characterises any further increase in Q_G and V_{GS} that may be employed to minimise the device on-resistance.

Note. Since the turn-off mechanism involving the removal of gate charge is almost identical to the turn-on mechanism, the required turn-off gate charge can also be estimated from the turn-on gate charge plot.

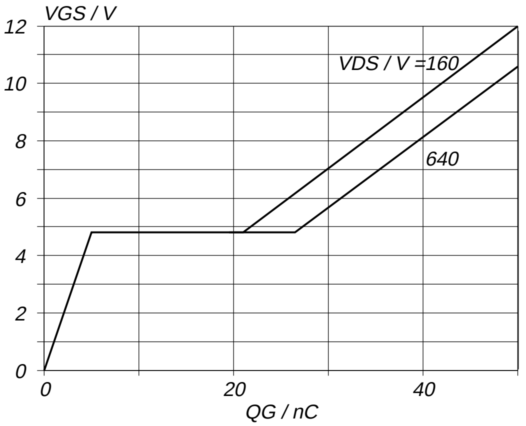


Fig. 15 Typical turn-on gate charge versus V_{GS} for BUK456-800A
Conditions: I_D = 4A; plotted for a range of V_{DS}.

In this topology the typical d.c. link voltage is 280V, hence the MOSFET V_{DS} prior to turn-on will be 280V, doubling to 560V at turn-off. From Fig. 14, for these two V_{DS} levels it can be estimated that the BUK456-800A will require 23nC to fully turn on and 27nC to turn off. It should be noted that this estimation of gate charge is for the 4A condition. In this present application the peak current is under 2A and in practice the actual Q_G required will be slightly less.

To a first approximation the gate current required can be estimated as follows:-

$$Q_G \quad = \quad I_G\, t_{sw}$$

where t_{sw} is the applicable switching time. If an initial value of the turn-on and turn-off time is taken to be 125ns then the required gate current is given by:-

$$I_{G(on)} = \frac{23\text{nC}}{125\text{ns}} = 0.184\text{A}; \qquad I_{G(off)} = \frac{27\text{nC}}{125\text{ns}} = 0.216A$$

In the majority of MOSFET drive circuits the peak currents and resulting switching times are controlled by using a series gate resistor R_G. An initial estimation of the value of this resistor can be found as follows:-

$$R_G = \frac{V_{drive} - V_{th}}{I_{G(ave)}}$$

where $I_{G(ave)}$ is the average value of the turn-on and turn-off peak gate current. In this example the gate driver I.C.4. consists of 5 parallel T.T.L. gates in order to provide high enough current sink and source capability. The driver supply voltage was approximately 10V, the MOSFET threshold voltage was 5V and the average peak gate current was 0.2A.

This gives a value for R_G of 25Ω. A value of 22Ω was selected, and the resulting gate drive waveforms for TR3 under these conditions at the full 100W output power are given in Fig. 16.

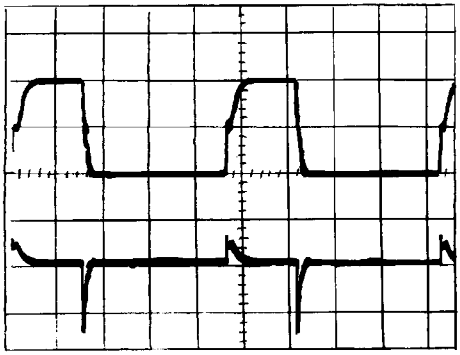


Fig. 16 PowerMOS TR3 gate drive waveforms.
Upper V_{GS}=5V/div; Lower I_G=0.2A/div
Horizontal 2µs/div.

This shows a peak I_G of 0.17A at turn-on and 0.28A at turn-off. The magnitudes of the turn-on and turn-off peak gate currents in operation are slightly different to the calculated values. This is due to the effect of the internal impedance of the driver, where the impedance while sinking current is much lower than while sourcing, hence the discrepancy.

These drive conditions correspond to a turn-on time of 143ns and turn-off time of 97ns, which are reasonably close to the initial target values.

In this application, and for the majority of simple gate drive arrangements which contain a series gate resistor (see section 1.1.3) the total power dissipation of the gate drive circuit can be expressed by:-

$$P_G = Q_G.V_{GS}.f$$

where Q_G is the peak gate charge and V_{GS} is the operating gate-source voltage. From Fig. 15, taking Q_G to be 43nC for a V_{GS} of 10V gives a maximum gate drive power dissipation of only 43mW, which is very small and can be neglected.

MOSFET losses

Switching losses

The waveforms for the drain current and drain-source voltage at full output load for the drive conditions specified are given in Fig. 17. In this case no transistor snubbing was required.

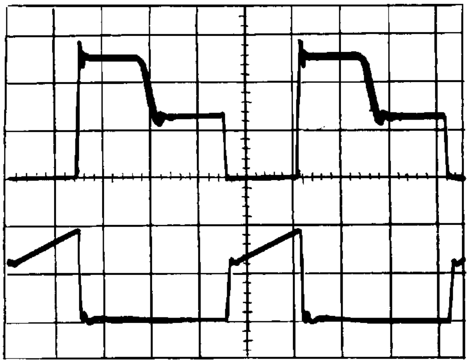


Fig. 17 PowerMOS drain-source voltage and drain current at full load.
Upper V_{DS}=200V/div; Lower I_D=1A/div
Horizontal scale 2µs/div

The waveforms of I_D and V_{DS} were found to cross at approximately half their maximum values for both turn on and turn-off. The switching loss can therefore be approximated to two triangular cross-conduction pulses shown in Fig. 18.

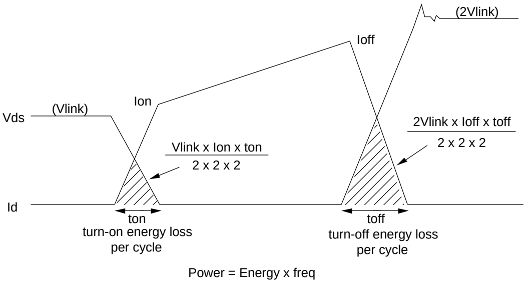


Fig. 18 Graphical approximation of MOSFET switching loss.

Hence, the total switching loss can be expressed by the following simplified equation:-

$$P_{sw} = \frac{1}{8} f\,(I_{Don}\,V_{link}\,t_{on} + I_{Doff}\,2V_{link}\,t_{off})$$

Inserting the correct values for this example gives:-

$$P_{sw} = 0.125 \times 100\text{k}(1.3 \times 280 \times 147\text{n} + 1.95 \times 560 \times 97\text{n})$$

$$= \quad 0.67\mathrm{W} + 1.06\mathrm{W} = 1.73\mathrm{W}$$

The MOSFET switching loss in this application is a very respectable 1.73W. It should be noted that a direct comparison with the switching loss of the earlier Bipolar version is not practical. It was necessary to use a snubber with the Bipolar in order to remove a large amount of the excessive switching loss generated by the device. Furthermore, the MOSFET switching frequency implemented was double that of the Bipolar version.

If a direct comparison were to be made under the same circuit conditions, the Bipolar switching loss would always be far in excess of the low values achievable with the MOSFET.

Conduction loss

The conduction loss for a power MOSFET is calculated by estimating $(I_{D(rms)})^2R_{DS(on)}$. The drain current at full output load is as shown in Fig. 17 and the r.m.s. value of the trapezoidal current waveforms found in the forward converter is given by:-

$$I_{rms} = \sqrt{D\left(\frac{I_{\min}^2 + I_{\min}I_{\max} + I_{\max}^2}{3}\right)} \qquad D = \frac{t_{ON}}{T}$$

At full load, these values can be seen to be I_{min}=1.25A; I_{max}=1.95A; D= 0.346. Substituting these values into the above equation gives an $I_{D(rms)}$ = 0.95A.

The typical $R_{DS(on)}$ value for the BUK456-800A is quoted as 2.7Ω. However, this is for a junction temperature of 25˚C. The value at higher operating junction temperatures can be calculated from the normalisation curve given in the data-sheets. If a more realistic operating temperature of 100˚C is assumed, the weighting factor is 1.75. Hence, the correct $R_{DS(on)}$ to use is 4.725Ω. Therefore, the conduction loss is given by:-

$$P_{cond} \quad = \quad (0.95)^2\,4.723 \quad = \quad 4.26\mathrm{W}$$

The conduction loss of 4.26W is over double the switching loss. However, this is typical for a high voltage MOSFET operated around this frequency. The MOSFET conduction loss is much higher than was previously obtained using the Bipolar transistor at 50kHz, as expected.

The total loss for the MOSFET device thus comes to 6W i.e. 6% of the total output power.

It should be remembered that this figure has been calculated for the full output load condition which will be a transient worst case condition. A more realistic typical dissipation of approximately 4W has been estimated for the half load condition, where the conduction loss is approximately halved. This 4W figure should be used when estimating the heatsink requirement. In this case a relatively small heatsink with a thermal co-efficient of around 10˚C/W would be adequate.

For more information on MOSFET switching refer to chapters 1.2.2. and 1.2.3. of this handbook.

100kHz magnetics design

Output transformer

Doubling the switching frequency to 100kHz has allowed the use of the smaller sized ETD34 core for the transformer. This transformer has been designed with a 0.1mm centre pole air gap. The winding details are shown in Fig. 19 and listed as follows:-

Winding

2 to 1	Regln supply	
5 to 4	+12V sec	3 x 12 turns 0.4mm e.c.w. in 1 layer.
6 to 7	-12V sec	3 x 12 turns 0.4mm e.c.w. in 1 layer.
8	r.f.i. screen	1 turn 0.1 x 13mm copper strip.
10 to 12	1/2 prim	28 turns 0.355mm e.c.w. bifilar in two layers.
11 to 13	1/2 demagn	28 turns 0.355mm e.c.w. in 1 layer.
12 to 14	1/2 prim	28 turns 0.355mm e.c.w. bifilar in 2 layers.
13 to 8	1/2 demagn	28 turns 0.355mm e.c.w. in 1 layer.

Interleaving:- 1turn 0.04mm insulation between each layer except 3 turns between r.f.i. screens.

Output choke

Again the implementation of the higher frequency has allowed the use of the smaller sized ETD39 core for the coupled output inductor. A centre pole air-gap of 2mm was utilised. The winding details are shown in Fig. 20 and are listed as follows:-

Winding

Copper strip	+5V	15 turns 0.3 x 21mm copper strip.
2 to 15	-12V	45 turns 0.4mm e.c.w. in 1 layer.
1 to 16	+12V	45 turns 0.4mm e.c.w. in 1 layer.

Interleave:- 1 layer 0.04mm insulation between each strip and winding.

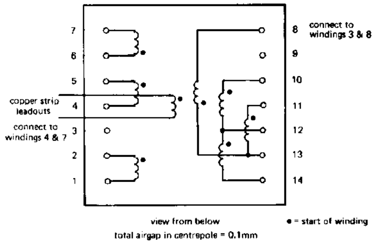

7
6
5
copper strip leadouts
4
connect to windings 4 & 7
3
2
1
8
connect to windings 3 & 8
9
10
11
12
13
14
view from below
total airgap in centrepole = 0.1mm
● = start of winding

Fig. 19 100kHz transformer construction.

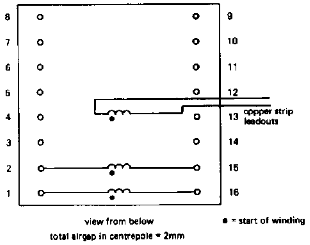

8
7
6
5
4
3
2
1
9
10
11
12
13
copper strip leadouts
14
15
16
view from below
total airgap in centrepole = 2mm
● = start of winding

Fig. 20 100kHz inductor construction.

2.3.2 Flexible, Low Cost, Self-Oscillating Power Supply using an ETD34 Two-Part Coil Former and 3C85 Ferrite

This section describes a low-cost, flexible, full performance, Self Oscillating Power Supply (SOPS) using the flyback principle.

The circuit is based around an ETD34 transformer using a two-part coil former and 3C85 ferrite material. The feedback regulation is controlled from the secondary side by means of a small U10 transformer.

The circuit is described and the details of the magnetic design using the two-part coil former is given. The advantages of the two-part coil former are highlighted together with 3C85 material properties. Power supply performance of a 50W SMPS design example is given.

Introduction.

A recently developed low-cost full-performance switched-mode power supply design is presented, highlighting a new transformer concept using a novel ETD34 two-part coil former and 3C85 low-loss material. The SMPS is of the Self Oscillating Power Supply (SOPS) type and uses the flyback principle for minimum component count and ultra-low cost/watt.

Compliance with safety and isolation specifications has always been a headache for magnetics designers. Now, the introduction of the ETD34 two-part coil former solves the problem of the 4+4mm creepage and clearance distances by increasing the available winding area and consequently decreasing copper losses. It also offers the advantage of a more flexible approach with the possibility of using a standard 'plug-in' primary and a customised secondary to meet any set of output requirements.

3C85 is a recently developed material superseding 3C8 and offers lower core loss, better quality control and higher frequency operation at no extra cost.

These products are illustrated in the following 50W SMPS design example, which is suitable for microcomputer applications.

SOPS

The principle of the Self-Oscillating Power Supply is shown in Fig. 1 and is based on the flyback converter principle. Stabilisation of the output voltage against mains and load variation is achieved by varying the duty cycle of the powerMOS switching transistor. The on-time varies mainly with input voltage, whereas the off-time varies only with the load. This means that both the duty cycle and the frequency vary due to the control circuit. The switching frequency is therefore at a maximum for maximum input voltage and minimum load. Regulation is achieved by varying the point at which the POWERMOS transistor is switched off. A.C. magnetic coupling is used in preference to opto-couplers for long-term life stability and guaranteed creepage and clearance. This circuit has the inherent property of self limiting energy transfer, since the maximum energy $1/2LI^2$, is defined by the bipolar transistor V_{BE} threshold and the source resistance value.

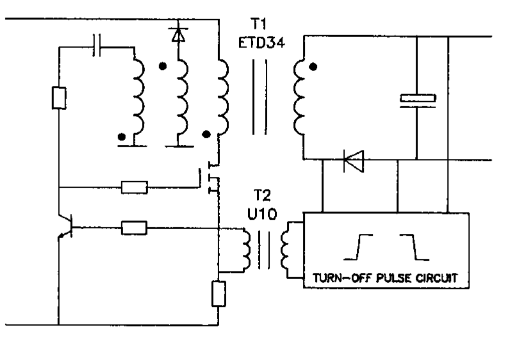


Fig. 1 Principle of S.O.P.S. with magnetic feedback for isolation.

The Transformer

The transformer uses the versatile ETD system. This is the range of four IEC standardised cores based on an E-core shape with a round centre pole. This permits easy winding especially for copper foil and standard wire. The ETD system includes coil formers into which the cores are clip assembled. The coil formers are designed for automatic winding and comply with all the standard safety specifications.

The two-part coil former was especially designed for the ETD34, and is shown in Fig. 2. There is 25% more winding area compared to the standard coil former yet full safety isolation is provided so that the creepage and clearance specifications are fully met. The inner part is a "click" fit into the outer part, such that the former is mechanically stable even with the cores removed. This two-part construction leads to a very versatile winding approach where standard primaries can be wound and assembled, yet still retaining the flexibility for various secondaries to be added for different requirements.

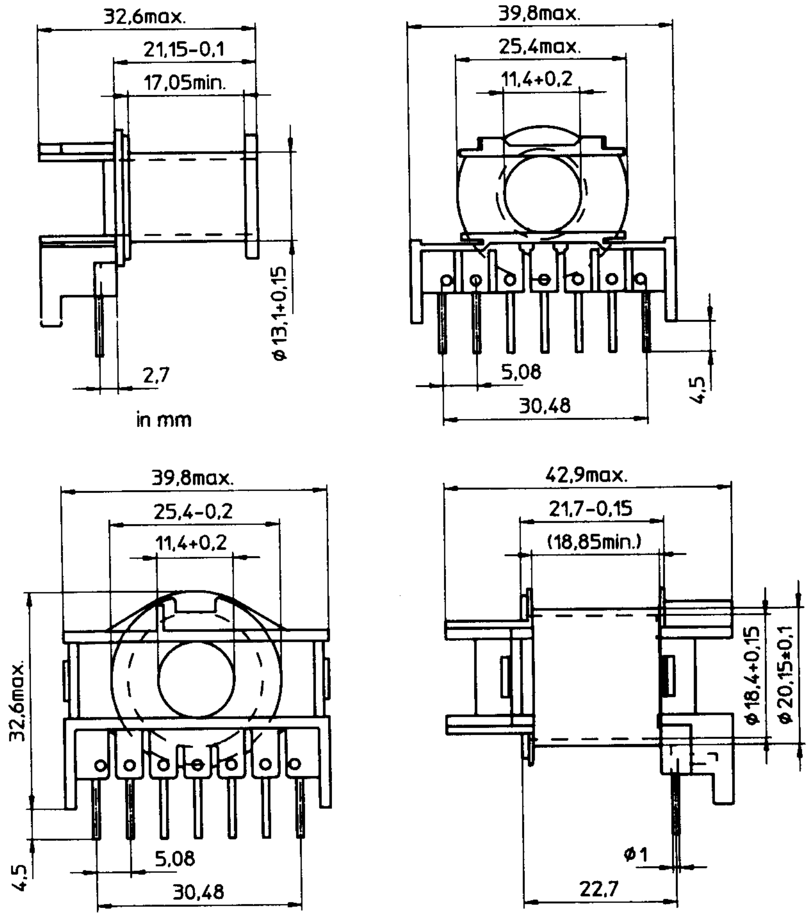


Fig. 2 ETD34 Two Part Coil Former.

Leakage inductance is always a problem with flyback transformers, but using this special construction the increase in leakage can be almost offset by the greater winding area of the two-part coil former when compared to the standard product with 4 + 4mm creepage and clearance. Fig. 3 shows standard and two part transformer cross-sections, where the leakage inductance is not more than 20% greater for the two-part coil former for this 50W design.

The transformer details for the 50W microcomputer power supply design example are shown in Fig. 4. The primary side consists of three windings:- a feedback winding of 5 turns, the main primary winding and a bifilar voltage clamp winding of 92 turns. This is achieved with 4 layers to fill the inner coil space area. The secondaries consist of a 5V winding of 3 turns and the ±12V windings of 7 turns each. As there are so few turns, the winding area is most effectively filled with stranded wire, copper strip or parallel windings, and these are therefore all possible choices.

In addition to the improved windings possibilities with the two-part coil former, the ETD core material has been enhanced. The quality of the 3C85 material is much improved compared to the older 3C8 type. Fig. 5 compares curves of core loss versus frequency for 3C85 against 3C8. The 30% improvement in 3C85 has been due to refining the material composition and tighter process quality control.

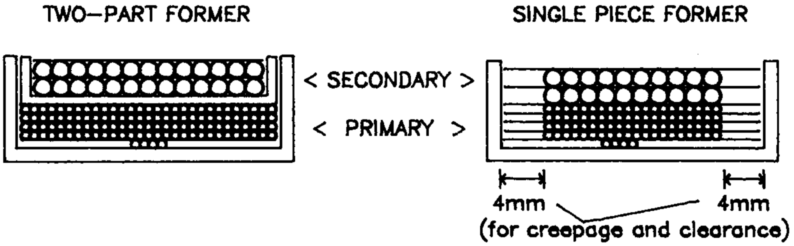

TWO-PART FORMER
SINGLE PIECE FORMER
< SECONDARY >
< PRIMARY >
4mm
4mm
(for creepage and clearance)

Fig. 3 The two types of transformer construction compared.

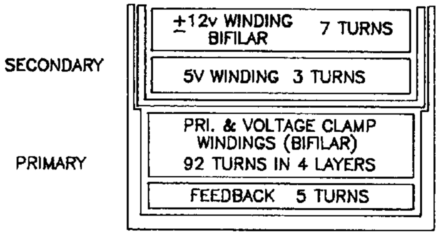

SECONDARY
PRIMARY
±12v WINDING BIFILAR 7 TURNS
5V WINDING 3 TURNS
PRI. & VOLTAGE CLAMP WINDINGS (BIFILAR) 92 TURNS IN 4 LAYERS
FEEDBACK 5 TURNS

Fig. 4 Transformer winding details using two part coil former.

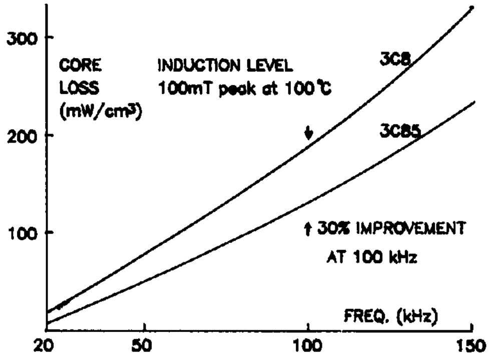


Fig. 5 Core loss versus frequency for 3C8 and 3C85.

Application and Operation of SOPS

The SOPS circuit is ideally suited for microcomputer systems, where full performance at low cost is required. The 50W output power is split between a regulated 5V output at 5A for the logic, a +12V output at 1.8A and a -12V output at 0.2A for the peripherals. The circuit diagram of the power supply is shown in Fig. 6. The operating frequency varies from 250kHz at open circuit to 35kHz at full load. The circuit works as follows:-

The mains input is filtered (L1), rectified (D1-D4) and smoothed (C7) to provide a d.c. rail. This supply rail utilises a single electrolytic capacitor which is a low profile , low cost, snap-fit 055 type.

The main switching transistor, Q1, is a TO-220 powerMOS device, the BUK456-800A. Starting current is provided via R1 to Q1 to start the self-oscillating operation. Feedback current is provided by a small winding on the transformer (T1), via C8 to maintain bias. Duty cycle control is via R5 and T2, with final control being achieved with R5, T2 and Q2. The triangular transformer magnetising current is seen across R5 as a voltage ramp, (see Fig. 7). This is fed to the base of Q2, via a small U10 transformer, T2. When the voltage becomes greater than the V_{BE} of the transistor, Q2 is turned on, causing the gate of Q1 to be taken to the negative rail, so terminating the magnetisation of the transformer T1. The output voltage is controlled by feeding back a turn-off pulse by means of T2, thus causing Q2 to turn on earlier.

A voltage clamp winding is bifilar wound with the primary to limit voltage overshoots on the drain of Q1 at turn-off, thus ensuring that the transistor operates within its voltage rating.

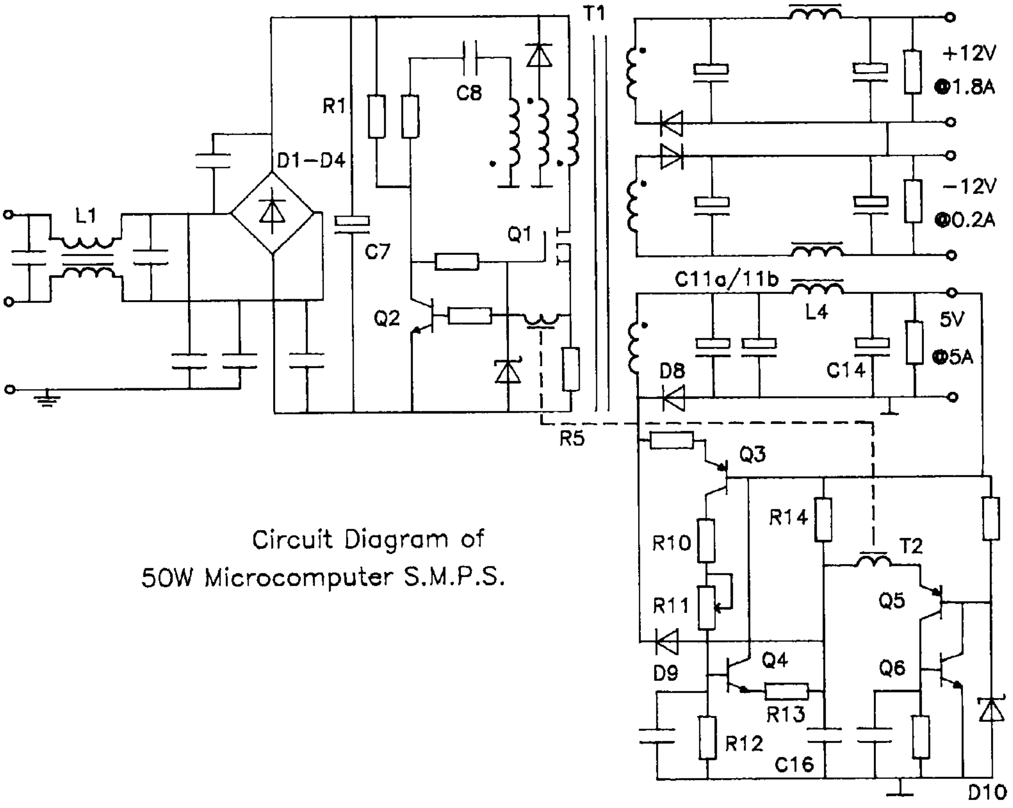


Fig. 6 Circuit diagram of 50W S.M.P.S.

Maximum throughput power is determined by the value of R5: the higher its resistance value, the lower the maximum power. The same drive and control circuit can be used for different throughput powers, ETD core sizes and powerMOS transistors.

The 5V secondary uses a single plastic TO-220 Schottky diode, the PBYR1635 shown as D8. The output filter is a pi type giving acceptable output ripple voltage together with good transient response. Two electrolytic capacitors are used in parallel, C11a/C11b (to accommodate the ripple current inherent in flyback systems), together with a small inductor wound on a mushroom core, L4, and a second capacitor, C14.

The turn-off pulse is created, cycle-by-cycle, by charging a capacitor from the output and comparing it with a reference, D10 and by using the transition signal to feed back a turn-off pulse via transformer T2. A potential divider is present across the output 5V rail, consisting of R10, R11 and R12, via Q3. The potential divider controls the base voltage of the transistor Q4, which charges capacitor C16 via R13. The voltage on C16 ramps up to a voltage equal to that on the base of the transistor less the V_{BE}, causing Q4 to switch off. The capacitor continues to charge more slowly via resistor R14, i.e. a ramp and pedestal (see Fig. 8), until the voltage on the emitter of Q5 is equal to the voltage determined by the band-gap reference D10 (2.45V) plus the V_{BE} drop of Q5. When this voltage is reached, Q5 switches on, causing Q6 to switch on, pulling Q5 on harder. The edge produced is transmitted across T2 and adds to the voltage on the base of Q2. Transistor Q3 is there to maintain the voltage level at the end of the 'on' period of the waveform to prevent premature switching. Capacitor C16 is reset by diode D9 on the edge of the switching waveform of the schottky diode, D8.

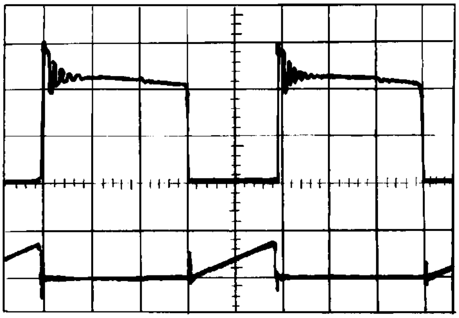


Fig. 7 BUK456-800A powerMOS transistor switching waveforms.
Top trace - Drain voltage V_{DS} 200V/div
Bottom trace - Source current I_S 1A peak (across R5)
Timebase - 5µs/div

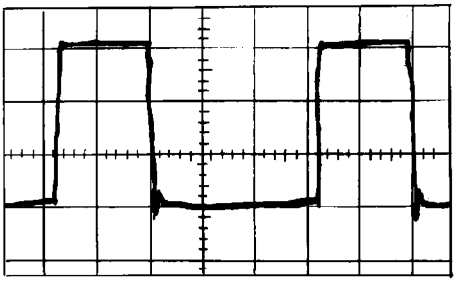


Fig. 8 Ramp and pedestal control waveforms across C16 = 1V/div, 5µs/div.

Performance

The performance of the supply is as follows:- the 5V output has load regulation of 1.2% from 0.5A to 5A load current. The line regulation is 0.5% for 187V to 264V a.c. mains input voltage.

The 12V secondaries are unregulated, and therefore have an inferior regulation compared to the 5V output. Each rail has a load regulation of 6% from open-circuit to full load. This is adequate for typical microcomputer peripheral requirements.

The efficiency of the power supply is typically 80%. The ripple and noise on all outputs is less than 75mV peak to peak. The radio frequency interference is less than 50dB (above 1µV) from 150kHz to 30MHz and complies with VDEO875 and BS800, based on a 150Ω V network. See Fig. 9. The transient response of the 5V output due to a 2A to 5A step load change gives a deviation of 100mV.

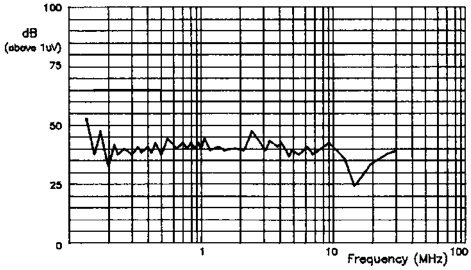


Fig. 9 Conducted R.F.I. on the supply terminals complying with VDE0875 and BS800.

Conclusion

A novel Self Oscillating Power Supply has been introduced featuring two recently developed products, increasing the cost effectiveness and efficiency of low-power SMPS:-

The new ETD34 two-part coil transformer featuring:

* solving of isolation problems

* standard 'plug-in' primaries

* suitable for automatic winding

* ETD system compatible.

The 3C85 ferrite material offers:

* 30% lower loss than 3C8

* comparable price with 3C8

* high frequency operation, up to 150kHz

* improved quality

Magnetics Design

2.4.1 Improved Ferrite Materials and Core Outlines for High Frequency Power Supplies

Increasing switching frequency reduces the size of magnetic components. The current trend is to promote SMPS miniaturisation by using this method. The maximum switching frequency used to be limited by the performance of available semiconductors. Nowadays however, Power MOSFETs are capable of square-wave switching at 1MHz and beyond. The ESL of the output capacitor had until recently limited any major size reduction in output filter above 100kHz. The advent of multi-layer ceramic capacitor stacks of up to 100µF removed this obstacle. This allowed the operating frequency to be raised significantly, providing a dramatic reduction in the size of the output filter (by an order of magnitude). The transformer has now become the largest single component in the power stage, and reducing its size is very important. The transformer frequency dependent core losses are now found to be a major contributing factor in limiting the operating frequency of the supply.

Part 1 of this section highlights the improvements in ferrite material properties for higher frequency operation. The standard 3C8 with its much improved version the 3C85 are discussed. However, the section concentrates on the new high frequency power ferrite, 3F3. This material features very low switching losses at higher frequencies, allowing the process of miniaturisation to be advanced yet further.

The popular ETD system shown in Fig. 1 is also outlined, and used as an example to compare the losses obtained with the above three materials.

In Part 2, the new EFD (Efficient Flat Design) core shape is introduced. These cores have been specifically designed for applications where a very low build height is important, such as the on-card d.c. - d.c. converters used in distributed power systems.

Circuit topologies suitable for high frequency applications are considered in the final part. Optimum winding designs for the high frequency transformer, which maximise the throughput power of the material are described.

PART 1: Improved magnetic materials

The ETD core system

The very widely used ETD core shape is shown in Fig. 1, which also outlines the method of coil-former assembly. The ETD range meets IEC standardisation, and is based on an E-core shape with a round centre pole. This permits easy winding especially for copper foil and stranded wire. The ETD system includes coil-formers into which the cores are clipped for quick, simple and reliable assembly. The coil-formers are designed for automatic winding and enable conformance with all standard safety specifications including UL.

ETD cores are suitable for a wide range of transformer and inductor designs, and are very commonly featured in off-line power supply transformers because the ease of winding allows insulation and creepage specifications to be met.

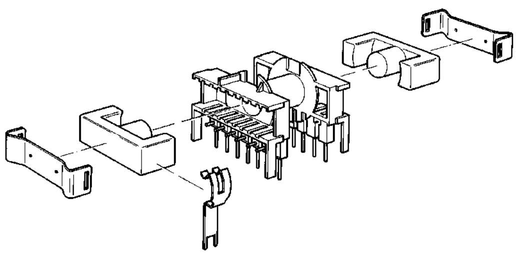


Fig. 1 The ETD core and assembly system.

Core materials

Three types of ferrite core material are compared. The standard 3C8 which is applicable for 50kHz use, the popular 3C85 which is usable at up to 200kHz, and the new high frequency core material 3F3, which has been optimised for use from 200kHz upwards.

The throughput power of a ferrite transformer is, neglecting core losses, directly proportional to (amongst other things) the operating frequency and the cross-sectional area of the core. Hence for a given core, an increase in the operating frequency raises the throughput power, or for a given power requirement, raising the frequency allows smaller cores and higher power densities. This is expressed by the following equation:-

$$P_{th} = W_d \times C_d \times f \times B$$

where W_d is the winding parameter, C_d is the core design parameter, f is the switching frequency and B is the induction (flux density) in Tesla.

Unfortunately, the core losses are also frequency dependent, and increasing frequency can substantially increase the core losses. Thus an increase in the core volume is required to maintain the desired power throughput without overheating the core. This means the transformer bulk in a higher frequency supply could limit the size reduction target.

The new 3F3 material with low-loss characteristics at high frequencies will reduce this problem, allowing new levels of miniaturisation to be obtained. An example of the practical size (and weight) reduction possible by moving to higher operating frequencies is given in Fig. 2. In comparison with the 50kHz examples, there is a significant reduction in transformer size when switched at 500kHz, and an even more impressive shrinking of the output inductor when operated at 1MHz.

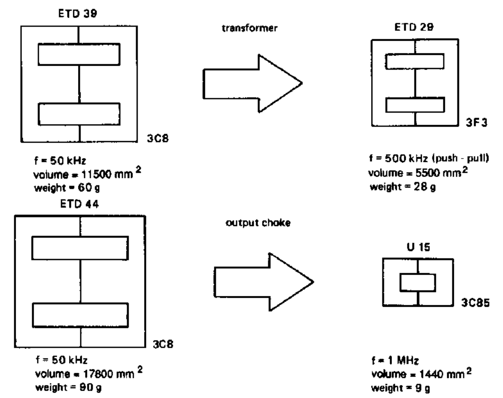


Fig. 2 Size reduction possible using 3F3 ferrite.

Note. The size of the output capacitor and inductor required to filter the high frequency output ripple components is greatly reduced - up to 90% smaller, resulting in excellent volume savings and very low ripple outputs.

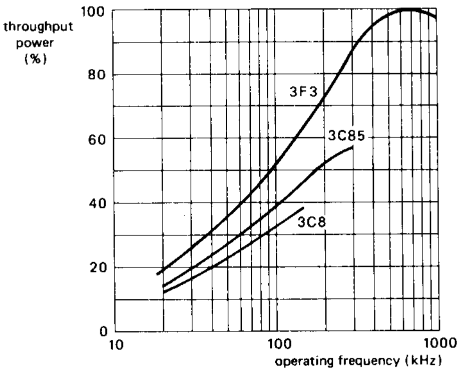


Fig. 3 Performance factor (f.B_{max}) as a function of frequency for material grades 3C8, 3C85 and 3F3.

The performance factor (f.B_{max}) is a measure of the power throughput that a ferrite core can handle at a loss of 200mW/cm^3. This level is considered acceptable for a well designed medium size transformer. The performance factors for the three different material grades 3C8, 3C85 and 3F3 are shown in Fig. 3. For frequencies below 100kHz (the approximate transition frequency, f_t) the power throughput is limited by core saturation and there is not much difference between the grades. However for frequencies above 100kHz, core loss is the limitation, which reduces the allowable throughput power level by overheating the core. Therefore, in order to utilise higher frequencies to increase throughput power or reduce core size, it is important that the core losses must first be minimised.

Reducing the losses

There are three main identifiable types of ferrite material losses: namely, hysteresis, eddy current and residual.

Hysteresis loss

This occurs because the induced flux, B, lags the driving field H. The B/H graph is a closed loop and hysteresis loss per cycle is proportional to the area of the loop. This loss is expressed as:-

$$P_{hyst} = C_a \times f^x \times B_{pk}{}^y$$

where C_a is a constant, B_{pk} is the peak flux density, f is the frequency with x and y experimentally derived values.

Eddy current loss

This loss is caused by energy from the magnetic flux, B, setting up small currents in the ferrite which causes heat dissipation. The energy lost is represented by:-

$$P_{ec} = \frac{C_b \times f^2 \times B_{pk}^2 \times A_e}{\sigma}$$

C_b is a constant, A_e is the effective cross-sectional core area and σ is the material resistivity.

Residual/Resonant loss

Residual losses are due to the reversal of the orientation of magnetic domains in the material at high frequencies. When the driving frequency is in resonance with the natural frequency at which the magnetic domains flip, there is a large peak in the power absorption. This gives:-

$$P_{res} = C_c \times f \times B_{pk}^2 \times \frac{\tan\delta}{\delta}$$

where

$$\tan\delta = \textit{loss angle} = \frac{\mu''}{\mu'} \qquad \mu = \mu' + j\mu''$$

Comparison of different materials

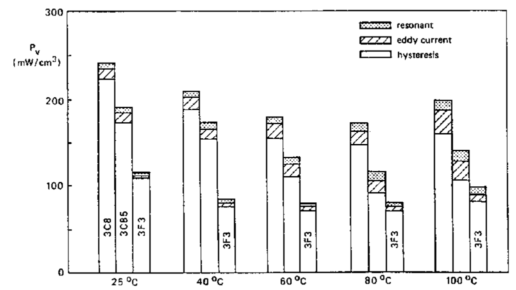


Fig. 4 Core losses in 3C85,3C8 and 3F3 for various temperatures at 100kHz and 100mT.

These losses (in mW/cm^3) are now presented for the three material grades in a partitioned form. These are given for various operating temperatures under two different operating conditions. Fig. 4 shows performance at 100kHz and a peak flux density of 100mT, which is typical for the 3C8 and 3C85 materials. The hysteresis loss is clearly dominant at this frequency. Inspection reveals a reasonable loss reduction when comparing 3C85 to the cheaper 3C8 grade. More significantly however, even at this lower frequency the new 3F3 grade can be seen to offer substantial loss reduction compared to 3C85 (especially at lower operating temperatures).

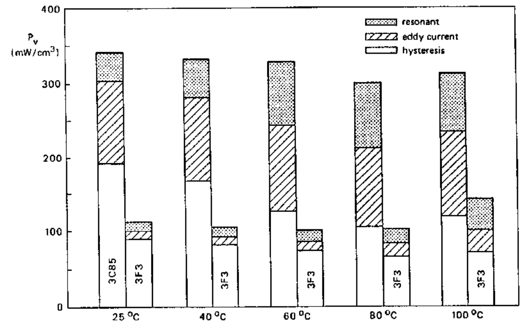


Fig. 5 Core losses in 3F3 and 3C85 for various temperatures at 400kHz and 50mT.

At higher operating frequencies well above 100kHz, eddy currents and residual losses are far more dominant. Fig. 5 gives the values for 400kHz and 50mT high frequency operation. This shows the superiority of the 3F3 material, offering significant reductions (60% vs 3C85) in all magnitudes, particularly in the eddy currents and residual losses.

Figure 6 gives a comparison of the peak operating flux density versus frequency at a core loss of 200mW/cm^3 for each grade. This shows that the maximum allowable operating frequency for 3F3 is always higher than for the other two types, hence, making it much more suitable for miniaturisation purposes. For example, at 100mT, 3F3 can operate at 280kHz, compared to 170kHz for 3C85 and 100kHz for 3C8.

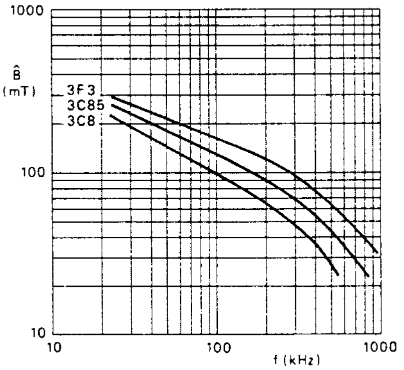


Fig. 6 Peak flux density versus frequency for 3F3, 3C85 and 3C8 at constant 200mW/cm^3 core loss.

Figure 7 compares the three types of core material in terms of complex permeabilities μ' and μ" over the frequency range 1 to 10 MHz, at very low flux density levels of < 0.1 mT. It can be seen that the resonant loss peaks at a higher frequency for 3F3, producing much lower high frequency residual losses right up to 1MHz.

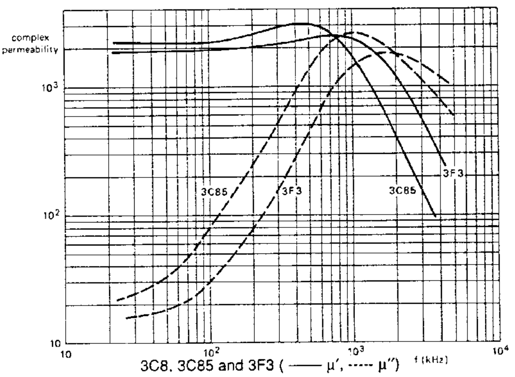


Fig. 7 Complex permeability versus operating frequency for 3F3 and 3C85/3C8.

Material	**3C8**		**3C85**			**3F3**		
B_{sat} (mT) at f = 25kHz H = 250A/m	≥ 320		≥ 320			≥ 320		
Core type	A_L ± 25% nH/N^2	P_V Watts	A_L ± 25% nH/N^2	P_V Watts	P_V Watts	A_L ± 25% nH/N^2	P_V Watts	P_V Watts
f	10kHz	25kHz	10kHz	25kHz	100kHz	10kHz	100kHz	400kHz
B	0.1mT	200mT	0.1mT	200mT	100mT	0.1mT	100mT	50mT
ETD29	-	-	2100	≤ 0.8	≤ 1.0	1900	≤ 0.6	≤ 1.0
ETD34	2500	≤ 1.6	2500	≤ 1.1	≤ 1.3	2300	≤ 0.85	≤ 1.5
ETD39	2800	≤ 2.2	2800	≤ 1.6	≤ 1.9	2600	≤ 1.3	≤ 2.3
ETD44	3500	≤ 3.6	3500	≤ 2.5	≤ 3.0	3200	≤ 2.0	≤ 3.7
ETD49	4000	≤ 4.6	4000	≤ 3.4	≤ 4.0	3600	≤ 2.6	≤ 5.2

Table 1. Comparison of material properties for the ETD range

Comparison of material grade properties for the ETD range

The values shown in Table 1 are for a core set under power conditions at an operating temperature of 100˚C.

3F3 offers a major improvement over existing ferrites for SMPS transformers. With reduced losses across the entire frequency range (but most markedly at 400kHz and higher) 3F3 enables significant reductions in core volume while still maintaining the desired power throughput.

As well as the ETD range, 3F3 is also available in the following shapes:-

- RM core
- P core
- EP core
- EF core
- E core
- ring core
- new EFD core

The new EFD core system which also offers size reduction capabilities shall now be described.

PART 2: The EFD core (Economic flat design)

The newly developed EFD power transformer core system shown in Fig. 8 offers a further significant advance in circuit miniaturisation. Their low build height and high throughput power density make them ideally suited to applications where space is at a premium.

One such application is with distributed power systems, which is becoming an increasingly popular method of power conversion, especially in the telecommunication and EDP market. Such power-systems convert a mains voltage into an unregulated voltage of about 44 to 80V d.c. This is then fed to individual sub-units, where d.c. - d.c. converters produce the required stabilised voltages. These converters are usually mounted on PCBs which in modern systems, are stacked close together to save space. The d.c. - d.c. converter, therefore, has to be designed with a very low build height.

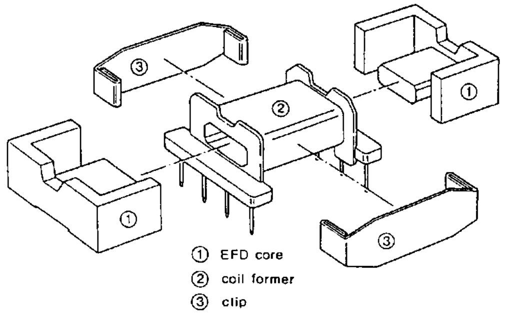


Fig. 8 The EFD core assembly and accessories.

The low-profile design

The EFD core offers a significant reduction in transformer core height. The ETD core combines extreme flatness with a very high throughput power-density. The range consists of four core assemblies complemented by a complete range of accessories. It is planned that the EFD outline will become a new European standard in d.c. - d.c. power transformer design.

The four core assemblies have a maximum finished height of 8mm, 10mm or 12.5mm. The type numbers are:-

- 8mm height - EFD 15/8/5
- 10mm height - EFD 20/10/7
- 12.5mm height - EFD 25/13/9 and EFD 30/15/9

Figure 9 shows that the EFD range has a lower build height than any other existing low profile design with the same magnetic volume.

Integrated product design

Because there is no room in a closely packed PCB for heavily built coil formers, they must be as small and light as possible. For this reason high quality thermo-setting plastics are used. This ensures that the connecting pins in the base remain positioned correctly.

To ensure suitability for winding equipment the connecting pins have been designed with a square base, saving time in wire terminating. To allow thick wire or copper foil windings to be easily led out, both core and coil former have a cut-out at the top (see Fig. 8).

To increase efficiency and reduce size, the ferrite core has been designed with the centre pole symmetrically positioned within the wound coil former. This is clearly shown in the cross-sectional view in Fig. 10.

Because of this, the full winding area can be used, resulting in an extremely flat design which is ideally suited for surface-mounting technology (SMT). SMT designs are already under consideration.

Maximising throughput power-density

Besides their extreme flatness, the most important feature of the EFD transformer is the very high throughput power density. This is especially true when the core is manufactured from the high-frequency low loss 3F3 material, which was described in the previous section. Combining EFD with 3F3 can provide throughput power densities (in terms of transformer volume) between 10 and 20 W/cm^3. Furthermore, with a usable frequency range from 100kHz to 1MHz, the EFD transformer will cover most applications.

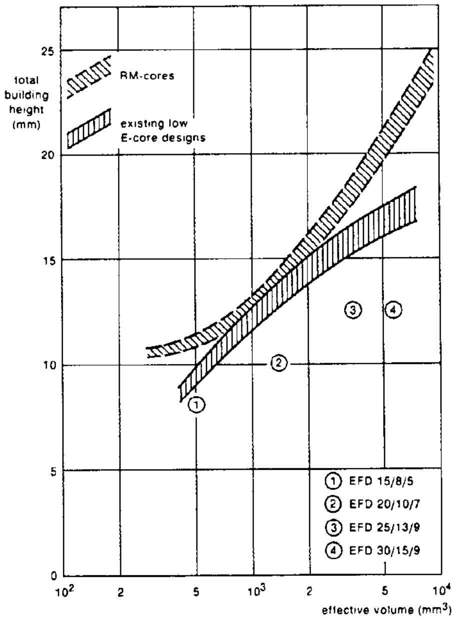


Fig. 9 EFD build height compared to existing designs.

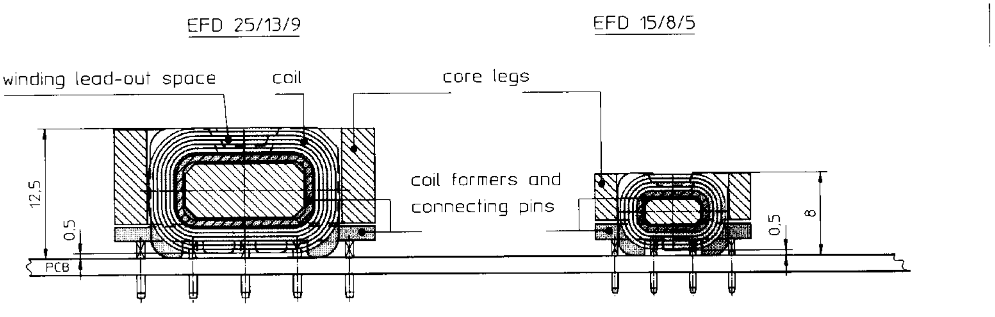


Fig. 10 Cross-section of EFD based transformers.

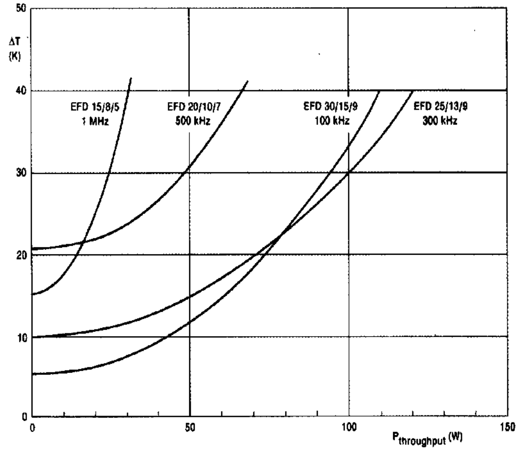


Fig. 11 Temp rise versus P_{th} for ETD based transformers with 3F3 material.

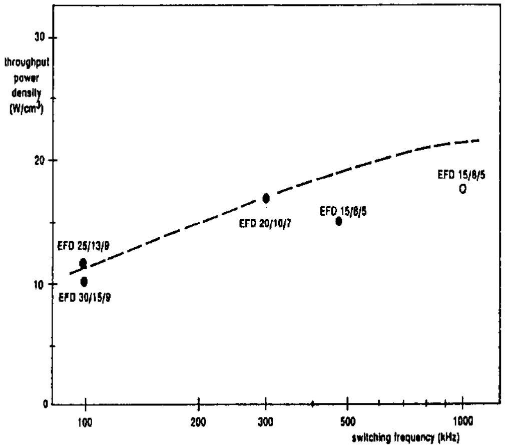


Fig. 12 P_{th} for forward mode transformers based on EFD core with 3F3 material.

As described earlier, high frequency transformer design (above 100kHz) is mainly limited by the temperature rise, caused by heat dissipation from the high frequency core losses as well as the power dissipation in the windings themselves. So the extent of transformer miniaturisation at high frequencies is limited by this rise in temperature (The curie temperature of a typical power ferrite material is around 200˚C). As a general rule, maximum transformer efficiency is reached when about 40% of the loss is in the ferrite core, and 60% in the windings. The temperature rise for a range of throughput powers for transformers based on the EFD range in 3F3 material is shown in Fig. 11.

In order to optimise the core dimensions and winding area, a sophisticated computer aided design (CAD) model of a d.c. - d.c. forward mode converter was used. This predicted the temperature rise of the transformer as a function of throughput power. The following parameters were assumed:-

Ferrite core - 3F3.

V_{in} = 44V to 80V; V_{out} = 5V, +12V and -12V.

T_{amb} = 60˚C; T_{rise} = 40˚C.

Primary - Cu wire; Secondary - Cu foil.

(Split sandwiched winding with 2 screens).

The CAD program was used to find an optimised design for the EFD transformer at well chosen frequency bands. The dotted line in Fig. 12 indicates the theoretical result derived from the CAD model. This shows in practice how well the EFD range approximates to the ideal model. The open circle for EFD 15/8/5 in Fig. 12 indicates the maximum optimal switching frequency.

From these results the range was grouped, depending upon core size into their optimal frequency bands.

- 100 to 300kHz - EFD 30/15/9 and EFD 25/13/9.
- 300 to 500kHz - EFD 20/10/7.
- 500kHz to 1MHz - EFD 15/8/5.

These are the recommended frequency ranges for each EFD type. The transformers can operate outside these ranges, but at a reduced efficiency, since the ratio of their core to winding areas would be less than ideal. Table 2 lists the power throughput at certain frequencies for each EFD core.

Core type	100 kHz	300kHz	500kHz	1MHz
EFD 30/15/9	90 - 100 W	110-140W	--	--
EFD 25/13/9	70 - 85 W	90 - 120 W	--	--
EFD 20/10/7	--	50 - 65 W	55 - 70 W	--
EFD 15/8/5	--	--	20 - 30 W	25 - 35 W

Table 2. Power handling capacity for EFD range.

Valid for single-ended forward d.c. - d.c. converter
(V_{in} = 60V; V_{out} = 5V)

Typical EFD throughput power curves given in Fig. 13 show the performance of the low loss 3F3 material as well as 3C85. These results were confirmed from measurements taken during tests on EFD cores in a transformer testing set up. As expected these show that, especially above 300kHz, the 3F3 (compared to 3C85) significantly improves throughput power.

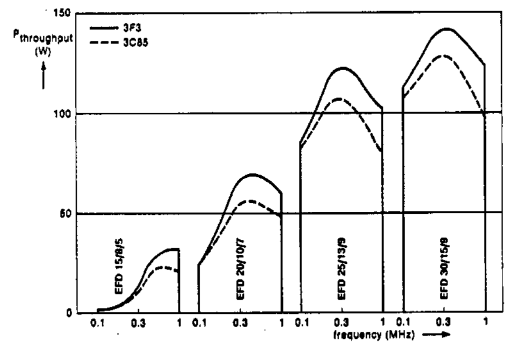


Fig. 13 ETD performance for 3F3 and 3C85 material.

PART 3: Applications

Circuit (transformer) configurations

Forward, flyback and push-pull circuit configurations have been used successfully for many different SMPS applications. This includes mains-isolated square-wave switching over the frequency range 20-100kHz, and with output powers up to 200W. Recent transformer designs have been developed to minimise the effects of leakage inductance and stray capacitance upon these circuits. The influences of the transformer characteristics on the choice of circuit configuration for higher switching frequency applications are now discussed.

The flyback converter

The flyback converter shown in Fig. 14 has leakage inductance between the primary and secondary windings which delays the transfer of power when the primary power transistor turns off. For the example waveforms shown in Fig. 14, the delay lasts for 600ns. During this time, power is returned to the d.c. supply. The circulating power increases with the switching frequency, and in this case would produce 50W at 1MHz. This tends to limit the maximum operating frequency for flyback converters.

The forward converter

The power transistor in the forward converter shown in Fig. 15 normally has a snubber network (and stray circuit capacitance) which protects the transistor at turn-off. This is necessary because the energy stored in the leakage inductance between the primary and secondary windings would produce a large voltage spike at transistor turn-off.

At transistor turn-on the energy stored in the capacitance is discharged and dissipated. For the example waveforms given in Fig. 15, this would be 7.5W at a switching frequency of 1MHz. Furthermore, as in the flyback converter, the circulating magnetising power can also be as high as 50W at 1MHz, hence reducing the efficiency of the transformer. These characteristics limit the maximum frequency at which forward converters can be usefully applied.

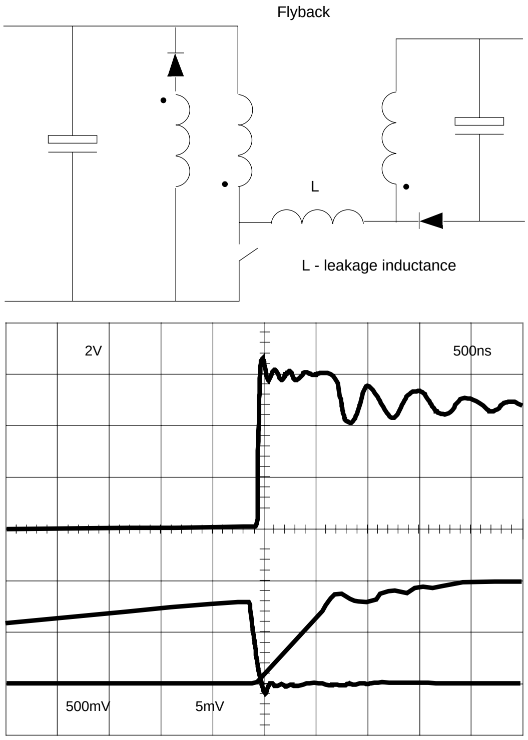


Fig. 14 Flyback converter and leakage inductance effect.

Centre-tapped push-pull converter

The centre-tapped push-pull circuit configuration given in Fig. 16 uses magnetic B/H loop symmetry when driving the transformer. Therefore, when either transistor is turned off, the magnetising current is circulated around the secondary diodes, thereby reducing energy recovery problems or the need for voltage clamping.

However, the transformer must be correctly "flux balanced" by monitoring the current in the transistors to prevent transformer saturation and subsequent transistor failure.

The drain current and voltage waveforms resulting from two examples of push-pull transformer winding construction are also shown in Fig. 16. In Fig. 16(a) (most serious case) the leakage inductance has distorted the waveforms. In Fig. 16(b) it is the circuit capacitance which produces the distortion. These distortions mean that the transistor current sense waveforms must be adequately filtered, so that the control circuit can vary mark/space correctly and prevent transformer saturation.

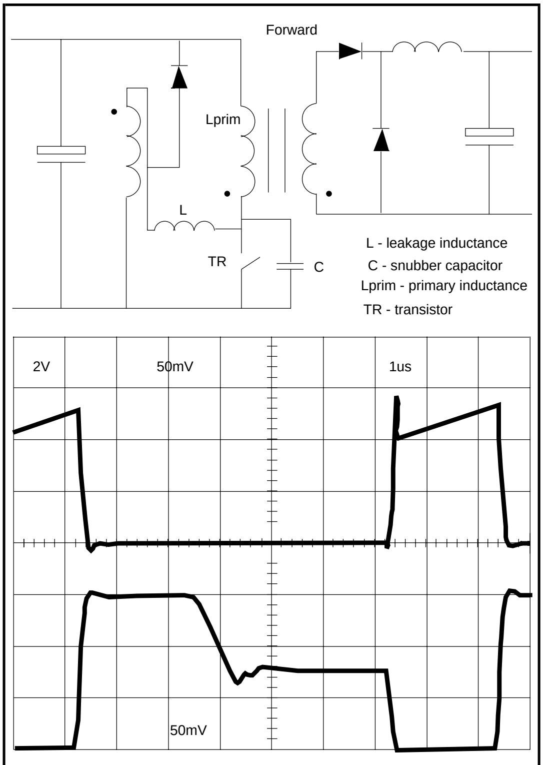
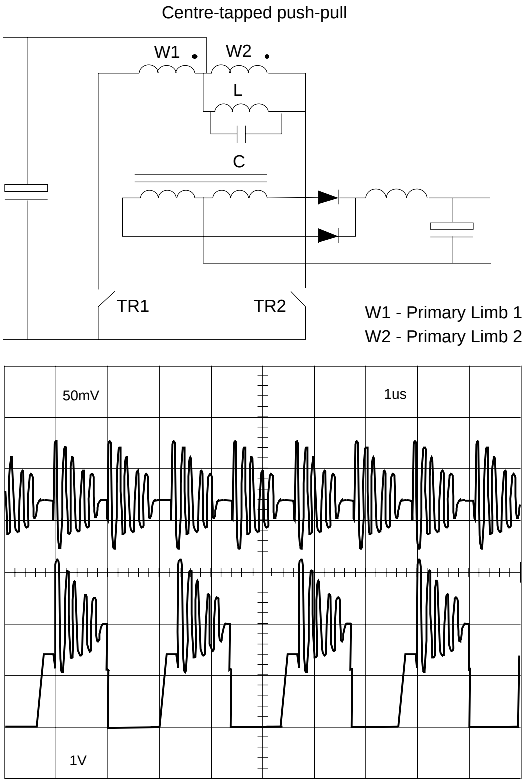

Forward
Lprim
L
TR
C
L - leakage inductance
C - snubber capacitor
Lprim - primary inductance
TR - transistor
2V
50mV
1us
50mV

Fig. 15 Forward converter and effects of parasitics.

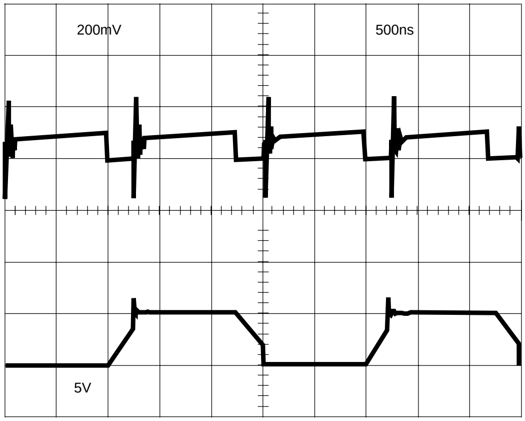
As the switching frequency is increased, the accuracy of the current balancing information is reduced by the action of the filtering and there might be a point at which this becomes unacceptable. The filter itself is also dissipative and will also produce a high frequency loss.

The half-bridge converter

The half-bridge push-pull transformer shown in Fig. 17 is inherently self-balancing. Standard winding methods for transformer construction using this configuration are possible at frequencies up to around 1MHz. Fig. 17 also gives waveform examples for the half-bridge transformer. This design allows the most flexibility when choosing a particular switching frequency.


Centre-tapped push-pull
W1
W2
L
C
TR1
TR2
W1 - Primary Limb 1
W2 - Primary Limb 2
50mV
1us
1V

(a) Oscillation due to leakage inductance.



(b) Oscillation due to winding capacitance.
Fig. 16 Push-pull transformer configuration.

Switching frequency

When designing a transformer and calculating the core loss, the exponent for frequency in the hysteresis loss equation is assumed to be constant at all frequencies. Only the fundamental is considered significant compared to all other harmonics of the square wave. This is a reasonable approximation to make from 20kHz to 100kHz because the contribution of eddy losses and resonant losses to the overall core loss is negligible (see Fig. 4).

As the frequency increases to 1MHz and beyond, the resonant and eddy current losses contribute proportionally more to the overall core loss. This means that the harmonics of a 1MHz square wave have more significance in determining the core loss than those at 100kHz. When the mark/space is reduced, the harmonics increase, and the loss will increase proportionally. This effectively limits the upper frequency of a fixed frequency square-wave, mark/space controlled power supply. However, as outlined, new materials such as 3F3 have been specially developed to keep these high frequency transformer losses as low as possible.

Transformer construction

In the half-bridge push-pull configuration of Fig. 17, during the period that the two primary transistors are off, there is zero volts across the secondary winding. Therefore, the secondary diodes are both conducting and share the choke current. The primary side should also have zero volts across it, but it rings because of the stray capacitance and leakage inductance between the primary and the secondary windings (see waveform of Fig. 17). At 500kHz, using an ETD29 or an EFD20 core, for example, a 1+1 copper strip secondary winding is suitable for providing an output of 5V. This is preferable to using more turns for the secondary winding because the leakage inductance and the amplitude of the ringing during the period that the MOSFETs are off is minimised. Reducing the ringing is of vital importance for the following reasons:-

1. It prevents the anti-parallel diode inherent in the upper MOSFET switch from conducting when the lower transistor is turned on. This will increase the MOSFET dV/dt rating typically by a factor 10, allowing the switching speed to be maximised and the switching losses to be reduced.

2. For low voltage outputs, the ringing will only be slightly reduced by the 1+1 construction. However, the core losses increase significantly at the actual frequency of the ringing (5-10MHz). Hence, any reduction in the ringing amplitude will be beneficial to core loss.

To further optimise the operation of the transformer, and reduce the ringing, the output clamping diodes should be operated with the minimum of secondary leakage inductance and mounted physically close to the transformer.

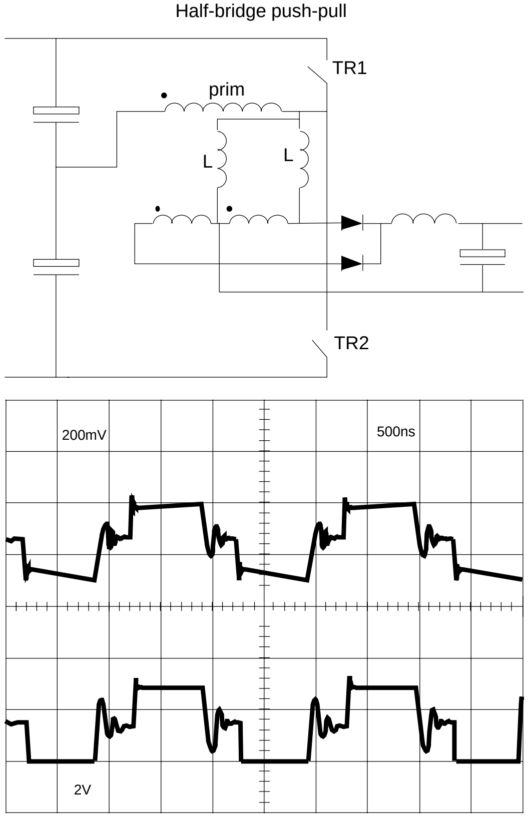


Fig. 17 Half-Bridge transformer configuration with typical waveforms.

Conclusions

To advance the trend towards SMPS miniaturisation, low-loss ferrites for high frequency have been specially developed. A new ferrite material has been presented, the 3F3, which offers excellent high-frequency, low loss characteristics.

A wide range of power ferrite materials is now available which offers performance/cost optimisation for each application. The particular SMPS application slots for the three ferrites discussed in this paper are summarised as follows:-

- 3C8 for low-cost 20-100kHz frequency range.
- 3C85 for high performance 20-150kHz.
- 3F3 for miniaturised high performance power supplies in the frequency range above 150kHz.

A new type of power core shape, the EFD was also introduced. The use of the EFD core also allows further SMPS miniaturisation by providing extremely low build heights in conjunction with very high throughput power densities. Optimum use of the EFD design can be made if the 3F3 material grade is selected. The EFD system is intended for applications with very low height restrictions, and is ideal for use in the d.c. - d.c. converter designs found in modern distributed power systems.

Different transformer winding configurations were also described (particularly for mains isolated SMPS.) It was found that to obtain the greatest size reduction using the new 3F3 material at very high frequencies, the following application ideas are useful:-

- Use the half-bridge push-pull circuit configuration.
- Minimize the transformer leakage inductance by careful winding construction.
- Minimise the lead-lengths from the transformer to rectifier diodes.

Resonant Power Supplies

2.5.1. An Introduction To Resonant Power Supplies

Whilst many application requirements can be satisfied by the use of conventional switching topologies, their shortcomings, particularly the switching losses in high power / high frequency circuits, are becoming a serious limitation. Some of the problems can be overcome by the use of resonant, or quasi-resonant, converters.

A resonant converter is a switching converter in which the natural resonance between inductors and capacitors is used to shape the current and voltage waveforms.

There are many ways in which inductors, capacitors and switches can be combined to form resonant circuits. Each of the configurations will have advantages and disadvantages in terms of stress placed on the circuit components.

To reduce switching loss, a resonant converter which allows the switching to be performed at zero current and low dI/dt is needed. A range of such circuits can be produced by taking any of the standard converter topologies and replacing the conventional switch with a resonant switch.

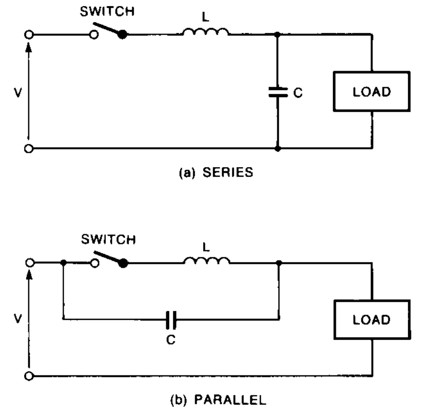


Fig.1 Basic resonant switch circuits

Resonant switch

A resonant switch consists of an active element (the switch) plus an additional inductor, L, and capacitor, C. The values of L and C are chosen so that, during the on time of the switch, the resonant action between them dominates. This ensures that the current through the switch, instead of just increasing linearly and having to be turned off, forms a sinusoid which rises to a peak and falls to zero again.

Two basic resonant switch configurations are shown in Fig.1. Before the switch is closed, C is in a state where it has a small negative charge. With the switch closed, C is discharged into L and then recharged positively. During the recharging extra energy is drawn from the supply to replace that delivered to the load during the previous cylce. With C charged positively, the switch is opened. The energy in C is now transfered to the load, either directly or via the main inductor of the converter. In the process of this transfer, C becomes negatively charged.

Figure 2 shows the three basic SMPS topologies - buck, boost and buck / boost - with both conventional (a) and resonant (b) switches. It should be noted that parasitic inductance and capacitance could form part, or even all, of the components of the resonant network.

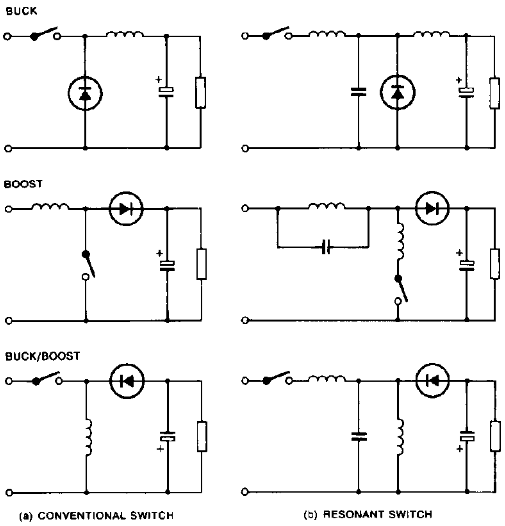


Fig.2 Standard SMPS circuits using
(a) conventional switch
(b) resonant switch

Flyback converter

To show how the resonant switch circuit reduces switching loss we will now consider the operation of the flyback converter, firstly with a conventional switch and then with a resonant switch.

Conventional switch

The basic flyback converter circuit is shown in Fig.3(a). If the transformer is assumed to have negligible leakage inductance it can be replaced by a single equivalent inductor Lm and the circuit becomes as shown in Fig.3(b), which is the same as a buck-boost converter shown in Fig.2.

Before the switch S is closed, a current Io will be flowing in the loop formed by Lm, diode D and the output smoothing capacitor Co. When S closes, voltage Es reverse biases the diode, which switches off and blocks the flow of Io. A current Is then flows via S and Lm. The only limitations on the initial rate of change of current are the stray inductance in the circuit and the switching speed of S. This means that switching current Is rises very quickly, leading to large turn-on losses in S and D.

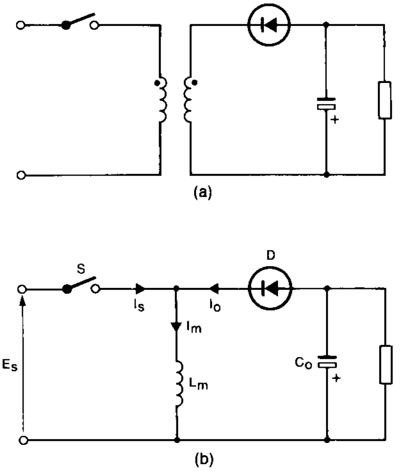


Fig.3 Conventional switch flyback converter
(a) circuit
(b) equivalent circuit

The current Is rises linearly from Io until the switch is forced to reopen. The diode is then no longer reverse biased and the current switches back from Is to Io via D, with Co then acting as a voltage source. The losses in this switching will also be very high due to the high level of Is and the rapid application of the off-state voltage. Io now falls linearly, delivering a charging current to Co, until the switch closes again.

Figure 4 shows the current waveforms for Io and Is and the current in inductor Lm.

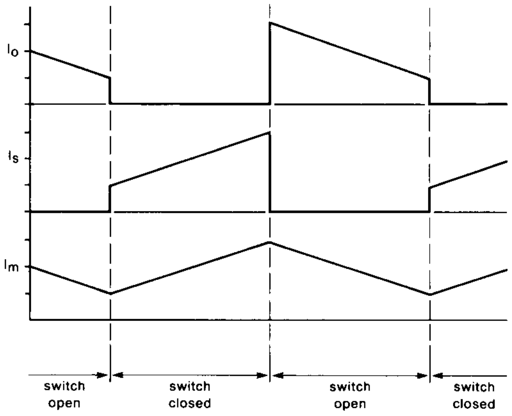


Fig.4 Waveforms for conventional switch flyback converter

Resonant switch

The resonant switch flyback converter circuit is shown in Fig.5(a). The equivalent circuit (Fig.5 (b)) is the same as that for the conventional switch except for the addition of the inductor La and capacitor Ca whose values are very much less than those of Lm and Co respectively.

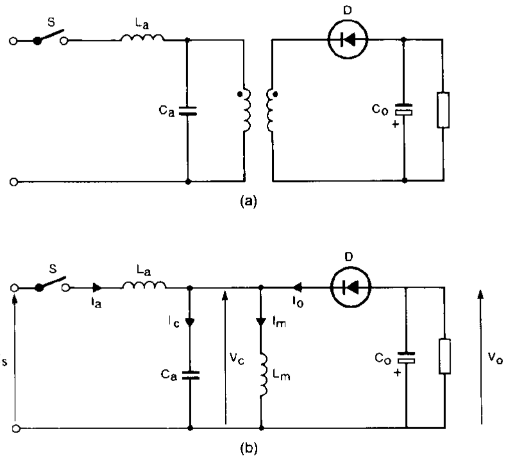


Fig.5 Resonant switch flyback converter
(a) circuit
(b) equivalent circuit

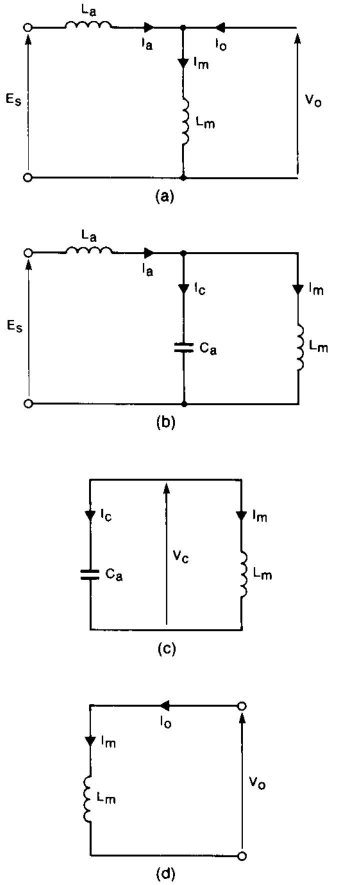


Fig.6 Resonant switch flyback converter operating modes
(a) Mode 1: S close , D on
(b) Mode 2: S closed, D off
(c) Mode 3: S open, D off
(d) Mode 4: S open, D on

If it is assumed that the switch is closed before the current in Lm has fallen to zero, then the initial equivalent circuit will be as shown in Fig.6(a). The rate of rise of current in S is determined by the value of La which, although small, is much larger than the stray inductance that limits current rise in a conventional switch. Turn-on losses are thus significantly reduced. Co, being much larger than Ca, acts as a voltage source (Vo) preventing current from flowing into Ca and maintaining a constant rate of change of current in Lm. Ia will increase linearly until it equals Im at which time Io is zero and diode D turns off.

With D turned off, the equivalent circuit becomes as shown in Fig.6(b). The resonant circuit, La, Ca and Lm, causes Ia to increase sinusoidally to a peak and then fall back to zero. S can then be opened again with very low losses.

With the switch open, the circuit is as shown in Fig.6(c). The resonant action between Ca and Lm causes energy to be transferred from the capacitor to the inductor. Vc will fall, passing through zero as Im reaches a peak, and then will increase in the opposite direction until it exceeds Vo. At which point D becomes forward biased, so it will turn on.

As D turns on (Fig.6(d)) the voltage across Ca becomes clamped and Im now flows into Co. Im falls linearly until the switch is closed again and the cycle repeats.

Voltage and current waveforms for a complete cycle of operation are shown in Fig.7.

From the description of operation it can be seen that the reduced switching losses result from:

- La acting as a di/dt limiter at switch on
- The resonant circuit La, Lm and Ca ensuring that the current is zero at turn-off

These factors combine to allow the switching devices to be operated at higher frequencies and power levels than was previously possible.

Circuit design

Correct operation of a resonant switch converter depends on the choice of suitable values for the inductors and capacitors. It is not possible to determine these values directly but they can be selected using simple computer models. An example of a model for a resonant switch flyback converter is given below to demonstrate the basic technique that can be used to analyse many different types of resonant circuits. Writing the final computer program will be a simple task for anyone with proramming experience and the model will run relatively quickly on even small personnel computers.

Circuit analysis

Here we analyse the operation of a resonant flyback converter circuit in mathemtical terms, assuming ideal circuit components.

In the equivalent circuit of the flyback converter, Fig.5(b), there are two switching elements S and D and the circuit has four possible modes of operation:

Mode 1	S closed	D on
Mode 2	S closed	D off
Mode 3	S open	D off
Mode 4	S open	D on

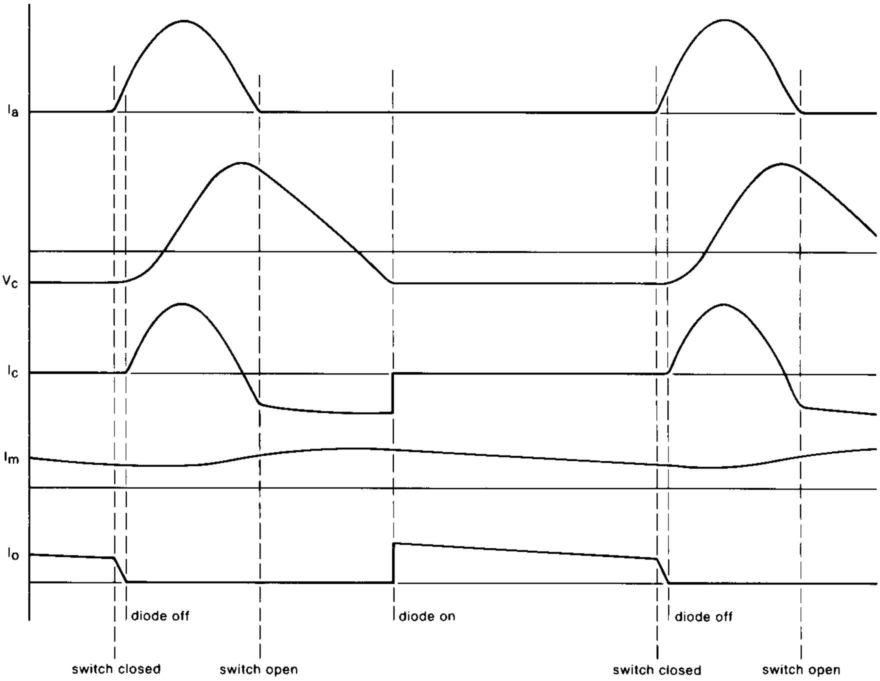


Fig.7 Waveforms for resonant switch flyback converter

Using Laplace analysis of the equivalent circuit for each operating mode, equations can be written for Ia, Ic, Im, Io and Vc.

J and U are the values of, Im and Vc respectively at the start of each operating mode i.e. when t = 0.

Mode 1

Figure 6(a) shows the equivalent circuit when S is closed and D is on. The large output capacitor Co as shown acts as voltage source (Vo).

The equations are:

$$Ia = \frac{Es - U}{La}.t$$

$$Im = \frac{U}{Lm}.t + J$$

$$Ic = 0$$

$$Vc = U$$

$$Io = Im - Ia$$

Mode 2

Figure 6(b) shows the equivalent circuit when S is closed and D is off.

The equations are:

$$Ia = J + A1.t + \frac{A2 - A1}{\omega 1}.\sin(\omega 1.t)$$

$$Im = J + A1.t + \frac{A3 - A1}{\omega 1}.\sin(\omega 1.t)$$

$$Ic = Ia - Im$$

$$Vc = U + \left(\frac{Lm.(Es - U) - La.U}{La + Lm}\right).(1 - \cos(\omega 1.t))$$

$$Io = 0$$

where,

$$A1 = \frac{Es}{La + Lm}$$

$$A2 = \frac{Es - U}{La}$$

$$A3 = \frac{U}{Lm}$$

$$\omega 1 = \sqrt{\left(\frac{La + Lm}{Lm.Ca.La}\right)}$$

Mode 3

Figure 6(c) shows the equivalent circuit when S is open and D is off.

The equations are:

$$Ia = 0$$

$$Im = J.\cos(\omega 2.t) + \frac{U}{Lm.\omega 2}.\sin(\omega 2.t)$$

$$Ic = -Im$$

$$Vc = U.\cos(\omega 2.t) + \frac{J}{Ca.\omega 2}.\sin(\omega 2.t)$$

$$Io = 0$$

where,

$$\omega 2 = \sqrt{\left(\frac{1}{Lm.Ca}\right)}$$

Mode 4

Figure 6(d) shows the equivalent circuit when S is open and D is on.

The equations are

$$Ia = 0$$

$$Im = J + \frac{U}{Lm}.t$$

$$Ic = 0$$

$$Vc = U$$

$$Io = Im$$

Computer simulation

Using the previous equations, it is possible to write a computer program which will simulate the operation of the circuit.

If S is closed before Im falls to zero, then during a complete cycle each of the operating modes occurs only once, in the sequence mode 1 to mode 4.

The first function of the program is to determine the duration of each mode.

Mode 1

The time between the switch turning on and the current Ia reach Im is given by:

$$T1 = \frac{J1.Lm.La}{Lm.(Es - Vo) - U1.La}$$

J1, the initial value of Im chosen by the designer, determines the average output current. U1 is the initial value of Vc. If Im is greater than zero, D will still be on so Vc and therefore U1 will equal Vo.

Mode 2

The duration, T2, of the second mode cannot be found directly and must be determined by numerical methods. T2 ends when Ia falls back to zero, so by successive approximation of t in the mode 2 equation for Ia, it is possible to find T2.

J and U at the start of mode 2, i.e., J2 and U2, are found by solving the mode 1 equations for Im and Vc respectivley at t = T1.

For any given set of circuit values there is a value of J1 above which Ia will not reach zero. This condition has to be detected by the program. Decreasing the value of La or increasing the value of Lm or Ca will allow Ia to reach zero.

Mode 3

Mode 3 operation ends when Vc = Vo. The duration, T3, is given by:

$$T3 = \frac{1}{\omega}2.\left\{\cos^{-1}\left(\frac{Vo}{\sqrt{U3^2 + A4^2}}\right) - \tan^{-1}\left(\frac{A4}{U3}\right)\right\}$$

where,

$$A4 = \frac{J3}{Ca.\omega 2}$$

and J3 and U3 are the values of Im and Vc respectively at the start of mode 3.

Mode 4

If the circuit operation is stable then the value of Im, when S is again closed, will equal J1 and the duration of the mode will be

$$T4 = \frac{Lm.(J4 - J1)}{U4}$$

Where J4 and U4 are the values of Im and Vc at the start of mode 4.

Calculation of Io and Vs

Having found the durations of the four modes, the average output current in D can be calculated, from:

$$Io(av) = \frac{T4.(J4 + J1) + T1.J1}{2.(T1 + T2 + T3 + T4)}$$

Peak, RMS and average values of the current in S (Ia) can be determined by numerical analysis during modes 1 and 2. The voltage across S is given by

$$Vs = Es - Vc$$

These values will be needed when the components S and D are chosen.

Conclusions

Resonant combinations of inductors and capacitors can be used to shape the current and voltage waveforms in switching converters. This shaping can be used to:

- reduce RFI and EMI,
- eliminate the effects of parasitic inductance and capacitance,
- introduce a degree of self limiting under fault conditions,
- reduce switching losses.

The resonant switch configuration is one way of reducing switching losses in the main active device. It can be adapted for use in all the standard square wave circuit topologies and with all device types.

Although the analysis of resonant circuits is more complex than the analysis of square wave circuits, it is still straightforward if the operation of the circuit is broken down into its different modes. Such an analysis will yield a set of equations which can be combined into a computer program, to produce a model of the system which can be run relatively quickly on even small computers.

2.5.2. Resonant Power Supply Converters - The Solution For Mains Pollution Problems

Many switch mode power supplies which operate directly from the mains supply, use an electrolytic buffer capacitor, after the bridge rectifier, to smooth the 100/120 Hz ripple on the DC supply to the switching circuit. This capacitive input filter causes mains pollution by introducing harmonic currents and therefore cannot be used in supplies with output powers above 165W. (TV, IEC norm 555-2, part 2: Harmonics, sub clause 4.2).

The smoothing capacitor can be charged only when the mains voltage is greater than the DC voltage. Therefore the input current will take the form of high amplitude, short duration pulses. For comparison, the load current for a 220W resistive load (an RMS current of 1A for 220V mains/line) and the load current for a 220W rectifier with capacitive input buffer are shown in Fig. 1.

The peak value of the current with the capacitor load is 5 times higher than for the resistive load, while the RMS current is doubled. It is understandable that the electricity supply authorities do not like this kind of load, because it results in high levels of harmonic current and a power factor below 0.5. It is, therefore, necessary to find alternative methods of generating a smooth DC voltage from the mains.

The PRE-CONVERTER switched mode supply is one possible solution. Such a converter can operate from the unsmoothed rectified mains/line voltage and can produce a DC voltage with only a small 100/120 Hz ripple. By adding a HF transformer it is possible to produce any value of DC voltage and provide isolation if necessary.

By proper frequency modulation of the pre-converter, the input current can be made sinusoidal and in-phase with the voltage. The mains/line now 'sees' a resistive load, the harmonic distortion will be reduced to very low levels and the power factor will be close to 1.

A pre-converter has to be able to operate from input voltages between zero (at the zero crossings) and the peak value of mains/line voltage and still give a constant output voltage. The SMPS converter that can fulfil these conditions is the 'flyback' or 'ringing' choke converter. This SMPS converter has the boost and buck properties needed by a pre-converter. However, the possibility of stability problems under 'no load' operation and its moderate conversion efficiency, means that this converter is not the most attractive solution for this application.

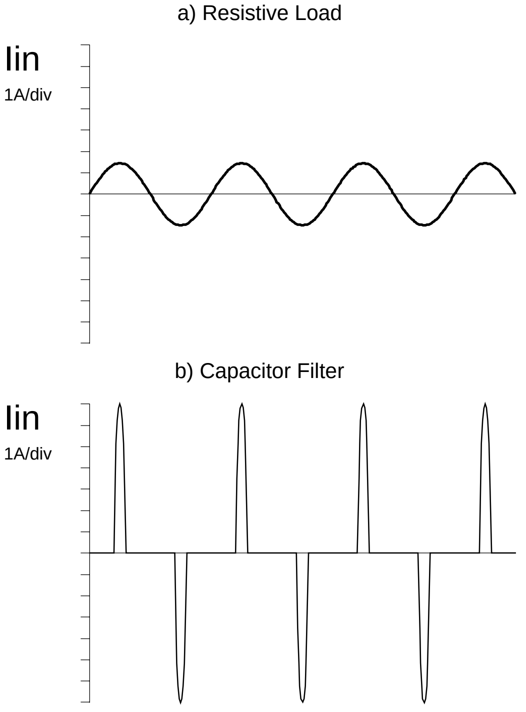


Fig. 1 Current taken from mains

The RESONANT POWER SUPPLY (RPS) has the right properties for pre-converter systems. The boost and buck properties of a resonant L-C circuit around its resonant frequency are well known. In principle any current can be boosted up to any voltage for a PARALLEL RESONANT L-C circuit. Furthermore, the current and voltage wave forms in a resonant converter are more or less sinusoidal, resulting in a good conversion efficiency and there are no stability problems at no load operating conditions.

Resonant pre-converter circuits

There are two basic resonant power supply (RPS) principles that can be considered, namely:

- The SERIES RESONANT POWER SUPPLY (SRPS), where a series resonant L-C circuit determines the no load operation cycle time. The output power increases with increasing operation cycle time (thus with decreasing operation frequency).

- The PARALLEL RESONANT POWER SUPPLY (PRPS), where a parallel resonant L-C circuit determines the no load operation cycle time. The output power increases with decreasing operation cycle time (thus with increasing operation frequency).

The basic SRPS converter circuit

A basic SRPS converter topology is shown in Fig. 2. For simplicity in the following description, the input voltage Ep is taken to be constant - 310 VDC for the 220VAC mains/line. If the circuit is to appear as a ’resistive’ load to the mains, then the output power of the pre-converter has to be proportional to the square of the instantaneous value of Ep. This means that the peak output power of the circuit must be equal to twice the average output power. So a 250W pre-converter has to be delivering 500W when Ep is at its peak.

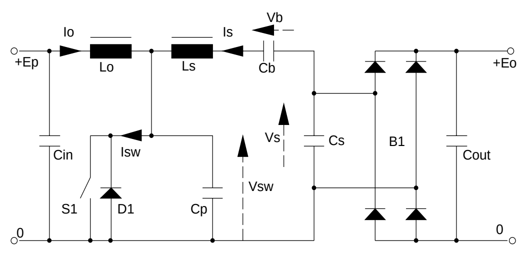


Fig. 2 Basic SRPS Pre-converter Circuit

In Fig. 2, the semiconductor switch S1 has an anti-parallel diode D1 to avoid a negative voltages across S1. Principally, a diode in series with S1 also gives a suitable SRPS pre-converter, but it slightly increases the positive peak voltage on S1 without giving an advantage over the circuit with anti-parallel diode. The lower value of the RMS current in S1 and thus the reduction in its on-state losses is completely cancelled by increased turn-on losses in this device.

Furthermore, stability problems can occur under no load conditions for the circuit with series diode (infinitely small current pulses in S1). The circuit with anti-parallel diode has no infinitely short current pulses under no load conditions, because the positive current in S1 will be preceded by the negative current in D1. As a result, no nett DC current is supplied to the circuit at finite pulse widths.

The input inductance Lo forms the connection between the input voltage and the switch voltage Vsw. A ’SERIES’ resonant L-C circuit, consisting of the capacitor Cp (when both S1 and D1 are OFF), the inductance Ls, the DC voltage blocking capacitor Cb and the capacitor Cs (when B1 is OFF), determines the no load operation frequency. The influence of the input inductance Lo can be neglected if its value is several times that of Ls.

A practical SRPS pre-converter for 250W nett output power (500W peak power conversion) can have component values shown in Table 1.

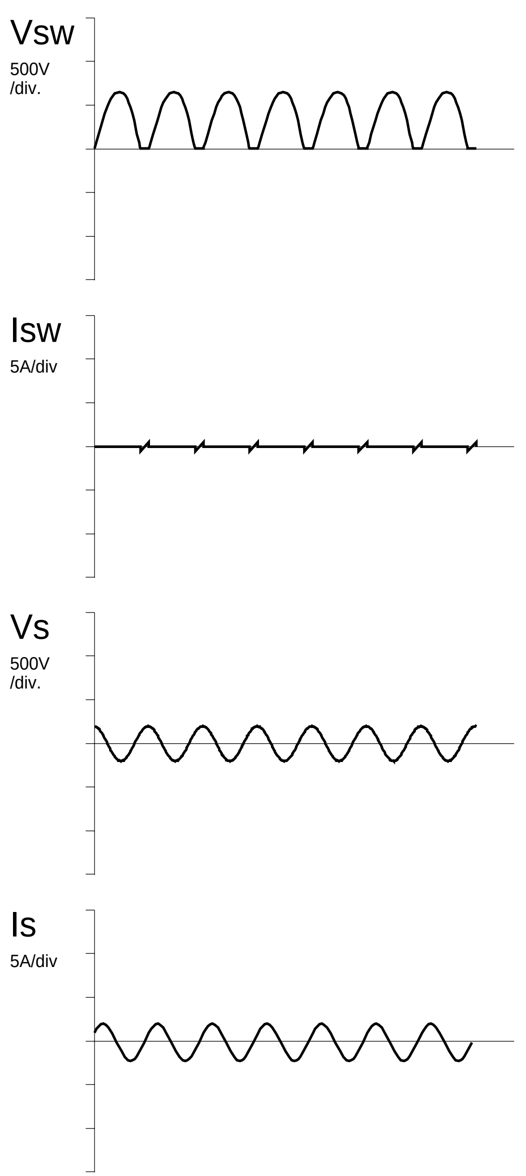


Fig. 3 Waveforms of Basic SRPS Circuit
(Tcycle = 1.01 x Tref, no load, Ep = 310V)

Capacitor Cp changes the voltage waveform across switch S1/D1 from the rectangular shape associated with SMPS converters, to the sinusoidal shape of an SRPS converter.

Lo	4 mH	8 x Ls
Cp	16 nF	Cs / 1.5
Ls	500 µH	
Cs	24 nF	
Cb	360 nF	15 x Cs
Tref	13.3 µs	minimum cycle time

Table 1 Component Values for SRPS circuit

The output rectifier bridge B1 has been connected in parallel with the output capacitor Cs. The whole converter also can be viewed as a parametric amplifier, where the switch S1 or the diode D1 modulate the value of Cp between Cp and infinity, while the output bridge B1 has similar influence on the value of the capacitor Cs. Heavier load means longer conduction of S1/D1 and of B1, so that some automatic frequency adaptation of the SRPS circuit takes place at operation frequencies below the no load resonant frequency. The output power of the SRPS increases with decreasing operation frequency.

Fig. 3 shows time plots of some of the voltages and currents of the basic SRPS circuit for the minimum ON time of S1/D1.

Under no load operation, the voltage Vsw is a pure sine wave superimposed on the input voltage with an amplitude equal to this voltage. The operation cycle time is approximately equal to the series resonant circuit cycle time, Tref, for no load conditions. The voltage Vsw and Vs and the current Is are sine waves with a low harmonic distortion. The input current Io is a low amplitude sine wave and it has no DC component for zero load.

In order to give an impression of the boosting properties of the SRPS converter, the no load voltages and currents for an operation cycle time of 1.25 x Tref are plotted in Fig. 4.

Fig. 3 gives the minimum 'ON' time condition for the S1/D1 switch and thus the minimum output voltage amplitude for a given input voltage. The minimum ratio of the amplitude of Vs and the input voltage Ep, with the component values given earlier, has been found to be:

$$\frac{Vs}{Ep} = 0.7$$

It will be obvious, that the value of the output voltage Eo has to be in excess of the minimum amplitude of Vs. Thus:

$$Eo > 0.7 \times Ep$$

A practical value of Eo has to be about 10% in excess of this minimum value in order to deal with tolerances in component values, thus:

$$Eo > 0.8 \times Ep$$

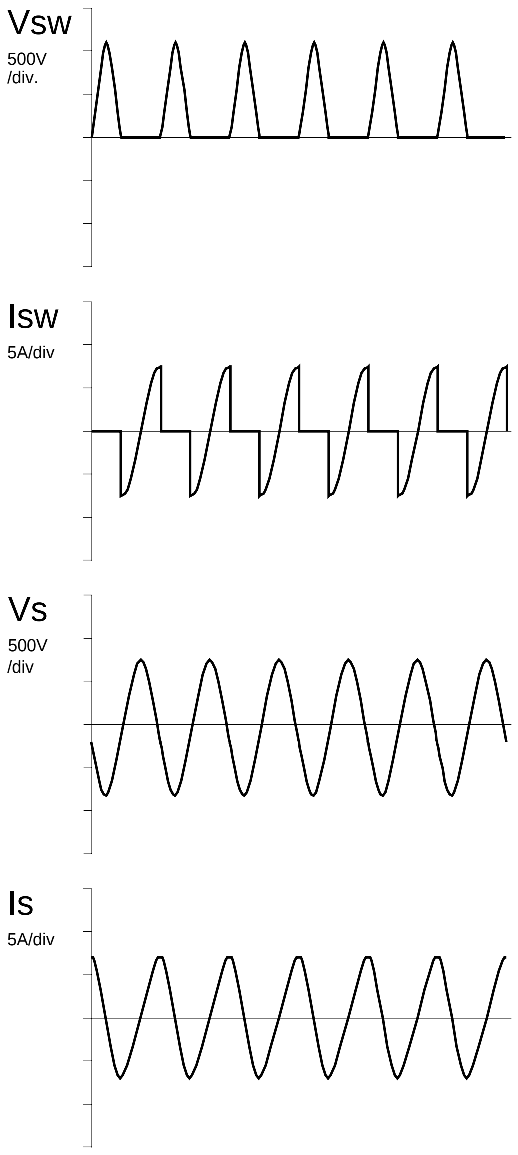


Fig. 4 Waveforms of Basic SRPS Circuit
(Tcycle = 1.25 x Tref, no load, Ep = 310V)

To realise the situation shown in Fig. 4, the output voltage Eo has to be increased considerably for no load operation for the same Ep or Ep can be decreased considerably for the same Eo. In fact, the relation between Eo and Ep in this figure is found to be:

$$Eo > 2.7 \times Ep$$

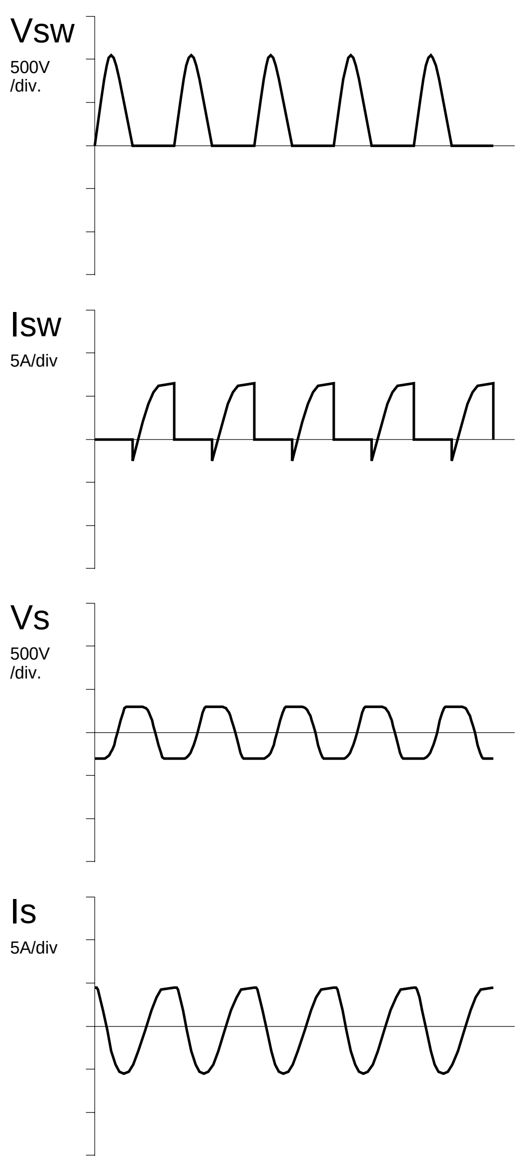


Fig. 5 Waveforms of Basic SRPS Circuit (Tcycle = 1.462 x Tref, 500W output, Ep = 310V)

Finally, Fig. 5 shows the voltages and currents for full load (Pout = 500W) at Ep = 310V and Eo = 300V. The input current Io is not shown but is a DC current of 1.6A with a small ripple current. The cycle time has been increased to 1.45 x Tref to get the 500W output power, giving an operating frequency of about 50 kHz.

It should be noted that S1 has to switch 'OFF' a high current at a relatively high dV/dt, resulting in significant turn-off losses. These losses are the main reason to prefer PRPS over SRPS for pre-converter applications.

The basic PRPS converter circuit

A basic PRPS converter topology is shown in Fig. 6. Just as for the basic SRPS pre-converter, we will assume a DC supply voltage Ep of 310 Vdc and a peak output power of 500W, i.e. a nett output power of 250W average.

The topology of Fig. 6 (PRPS) is almost identical to the topology of Fig. 2 (SRPS), except for the following points:

- Diode D1 is now in series with the switch S1 instead of in anti-parallel.

- Capacitor Cp has been omitted.

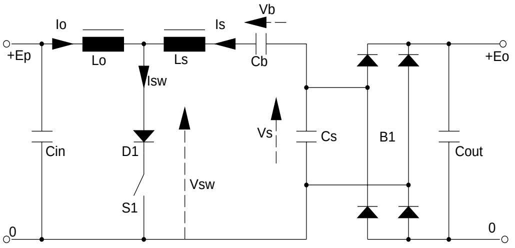


Fig. 6 Basic PRPS Pre-converter Circuit

The value of the two inductors Lo and Ls remain the same as they were in the SRPS, but the values of Cb and Cs are changed to obtain proper PRPS circuit operation. Having D1 in series with S1 does not lead to 'no-load' stability problems because, in the PRPS circuit, both the amplitude and the duration of the S1 current pulse are reduced as the output power decreases.

The input inductance Lo again forms the connection between the input voltage Ep and the switch voltage Vsw (across D1 and S1 in series). A 'PARALLEL' resonant L-C circuit, consisting of the series connection of Lo and Ls, the DC voltage blocking capacitor Cb and the capacitor Cs (both the switch S1 and the diode bridge B1 OFF) now determines the no load operation frequency. The value of the input capacitor Cin is chosen to be sufficiently large with respect to Cs to be neglected with respect to the no load operation frequency.

A practical PRPS pre-converter for 250W nett output power (500W peak power) can have component values as shown in Table 2.

Lo	4 mH	8 x Ls
Ls	500 µH	
Cs	24 nF	
Cb	48 nF	2 x Cs

Table 2 Component Values for PRPS circuit

To be able to put a full wave rectifier across capacitor Cs, the DC voltage blocking capacitor Cb cannot have a value of several times Cs. Therefore, a value of only twice Cs has been chosen for Cb. This ratio gives good practical results in combination with an output voltage, Eo, of 450V.

The parallel L-C circuit consists of series combinations of Lo and Ls and Cb and Cs. The output rectifier bridge now modulates the value of the capacitor between 2/3 Cs and 2 Cs (Cb and Cs in series and Cb only). It should be noted that the resonant frequencies of the two states differ by a factor of $\sqrt{3}$.

The switch S1 modulates the inductance value of the parallel L-C circuit between Lo + Ls and Ls. This is combined with a change in input voltage from zero (S1 ON) and Ep (S1 OFF). Again, the PRPS can be seen as a parametric amplifier, but now with both inductance and capacitance modulation.

In contrast with the SRPS circuit, the output power of a PRPS converter will increase with increasing operation frequency, thus with decreasing operation cycle time.

Under no load conditions and maximum operation cycle time, the output voltage and current will be near sinusoidal and will have their minimum no load values. This minimum output voltage can be calculated from

$$Vs > Ep.\frac{(Lo + Lp)}{Lo}.\frac{Cb}{(Cb + Cs)}$$

Substituting the values for Lo, Ls, Cb and Cs in the formula gives

$$Vs > 0.75 \times Ep$$

An output voltage choice of Eo = 450 V for Ep = 375 V will, therefore, be amply sufficient.

The voltage Vsw, the current Isw, the output voltage Vs and the current Is for the maximum operation cycle time, i.e. about equal to Tref, are shown in Fig. 7.

To get an impression of the boosting properties of the PRPS circuit, the no load voltages and currents are shown, for an operation cycle time Tcycle = 0.975 x Tref, in Fig. 8. It can be seen that the output voltage has been increased by a factor 2.5 with only a very small decrease of operation cycle time.

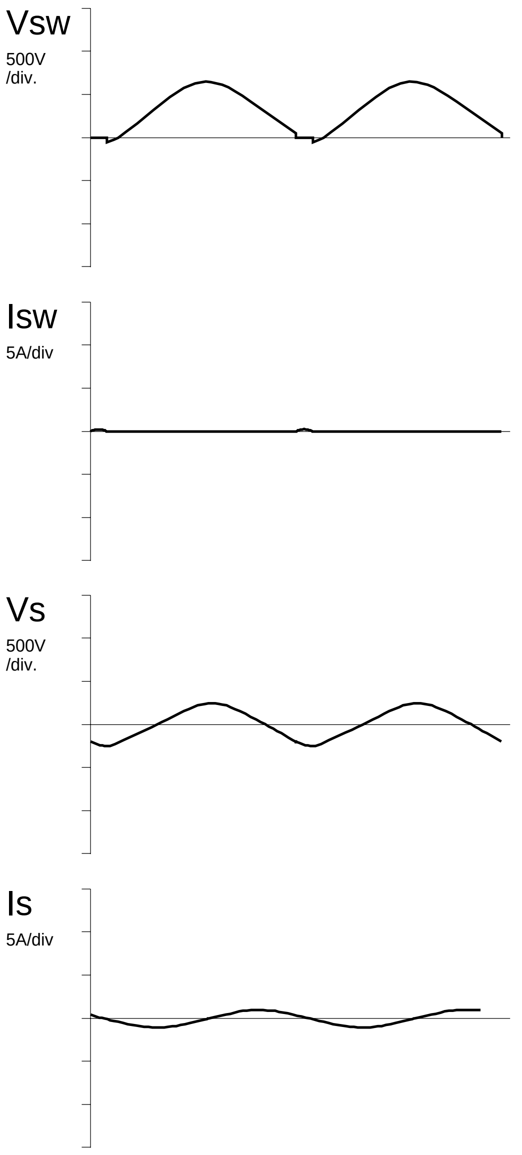


Fig. 7 Waveforms of Basic PRPS Circuit
(Tcycle = 0.995 x Tref, no load, Ep = 310V)

Finally, the full load voltages and currents are shown in Fig. 9 (output power 500W at Eo = 450V and Ep = 310V). It should be noted that the operation cycle time has been decreased to .5694 x Tref.

The significant feature of the PRPS circuit is that the current in the main switching device S1 is brought down to zero by the circuit and not by the device itself. Device S1 can now be turned off without loss. The negative voltage which causes the current to fall, is supported by diode D1, which needs to be a fast recovery type like the BYR79. The reverse recovery loss in D1 is small because the resonant action of the circuit make the rate of fall of current relatively slow - up to two orders of magnitude slower than in a standard SMPS.

SRPS and PRPS compared

A pre-conditioner can be implemented using either an SRPS or PRPS topology. The capacitor and inductor values are roughly the same, as are the peak values of voltage and current. The main difference between the circuits is in the switching requirements of S1 and D1.

In the SRPS, the turn on loss of S1 is very low - the voltage across S1 is zero and the current rises relatively slowly. However the turn off loss is large - S1 has to turn off a large current and, although the dVsw/dt is moderated by Cp it is still relatively fast. On the other hand, the turn off loss in D1 is negligible - no voltage is applied to the diode until S1 is turned off giving plenty of time for reverse recovery - but the turn on loss may be significant because the dIsw/dt is un-restrained.

In the PRPS circuit, however, the turn off loss in S1 is close to zero but the recovery loss in D1 is not negligible - Isw falls through zero and the negative voltage appears across the diode. S1 is turned on from a high voltage so there will be some loss in both S1 and D1 even though the rate of rise of current is moderated by Ls.

It is generally true that reducing turn off loss produces a bigger cost/performance benefit than reducing turn on loss. It is also true that losses in diodes are usually much lower than in their associated switching device. Since the PRPS configuration reduces turn off loss in S1 to zero it appears that PRPS is a better choice than SRPS as a resonant pre-converter.

Therefore, the remainder of this paper will concentrate on PRPS circuits.

PRPS transformer for >1kW

The practical PRPS circuits in this paper all use a transformer with a built-in leakage inductance to give mains isolation and inductance Ls. The inexpensive U-64 core, used in large quantities in the line deflection and EHT circuits in colour TV sets, can be used successfully as the transformer core in PRPS converters with a nett output power in excess of 1000W.

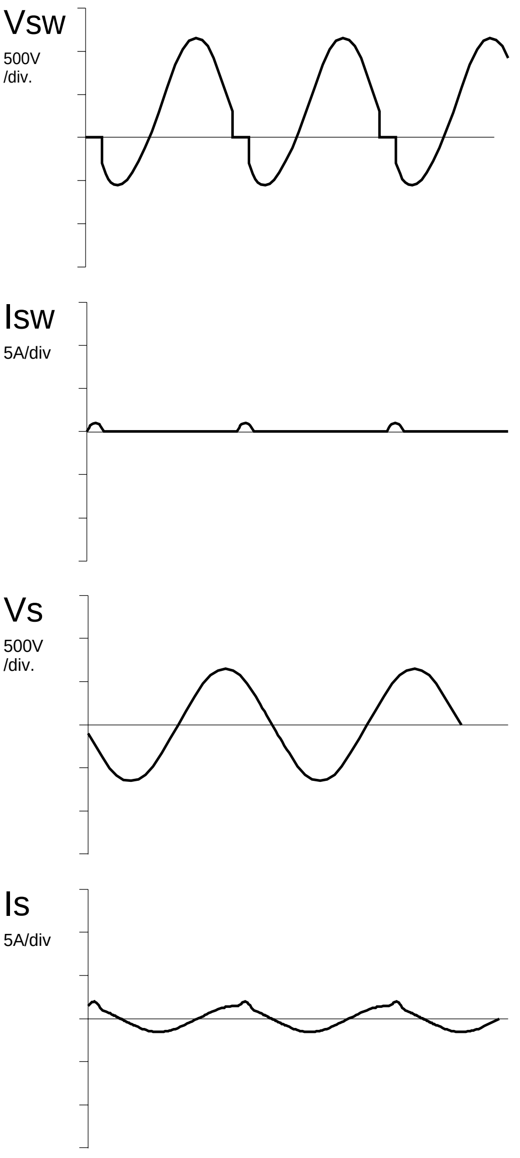


Fig. 8 Waveforms of Basic PRPS Circuit
(Tcycle = 0.975 x Tref, no load, Ep = 310V)

Fig. 10 illustrates a PRPS transformer constructed with a pair of U-64 cores. Both the primary and secondary windings are split into two halves. Each leg of the U-core is fitted with a two-chamber coil former with a primary and a secondary winding. To achieve a reasonable 'leakage inductance' Ls, the primary and secondary coils are crossed. Thus each U-core has one primary and one secondary coil.

A pre-converter transformer with this arrangement offers several advantages over the 'standard' SMPS transformer using E-cores.

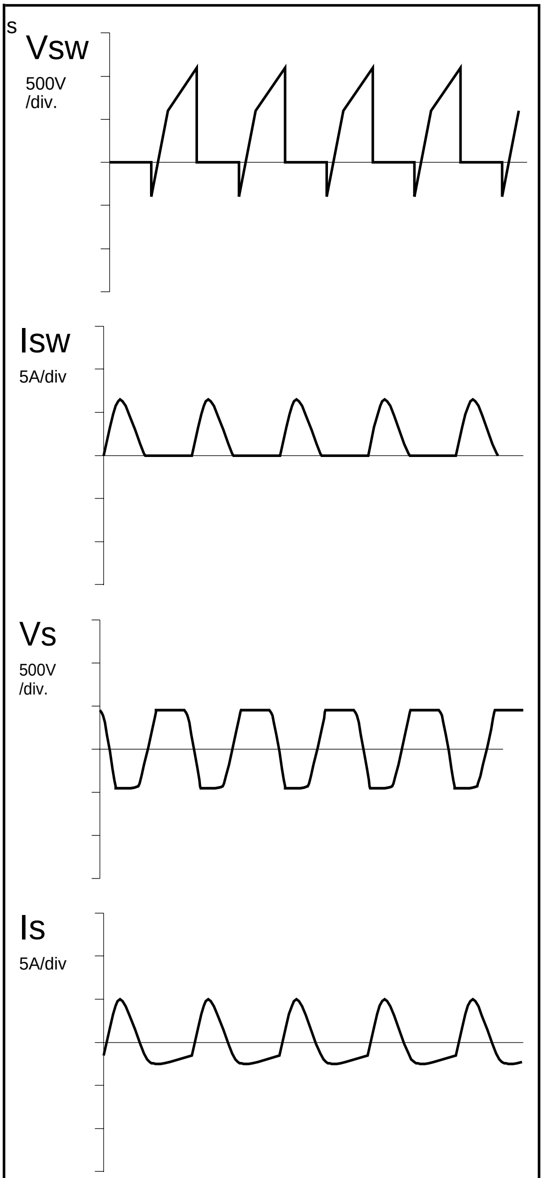


Fig. 9 Waveforms of Basic PRPS Circuit
(Tcycle = 0.5694 x Tref, 500W output, Ep = 310V)

- It will be easier to meet the mains isolation requirements, particularly with respect to creepage distances.
- The thermal properties will be much better because the winding is distributed over both core legs.
- The mean length of a turn is less than with a single core leg, reducing copper loss.
- The two leg arrangement will need only 70% of the turns of the one leg design. This is because of the active (magnetic) fluxing of both legs.
- It is a simpler and hence less expensive transformer to wind.

One disadvantage of this arrangement is that the windings are not layered. This means that 'skin effect' will have to be overcome by using Litz wire for both the primary and secondary windings.

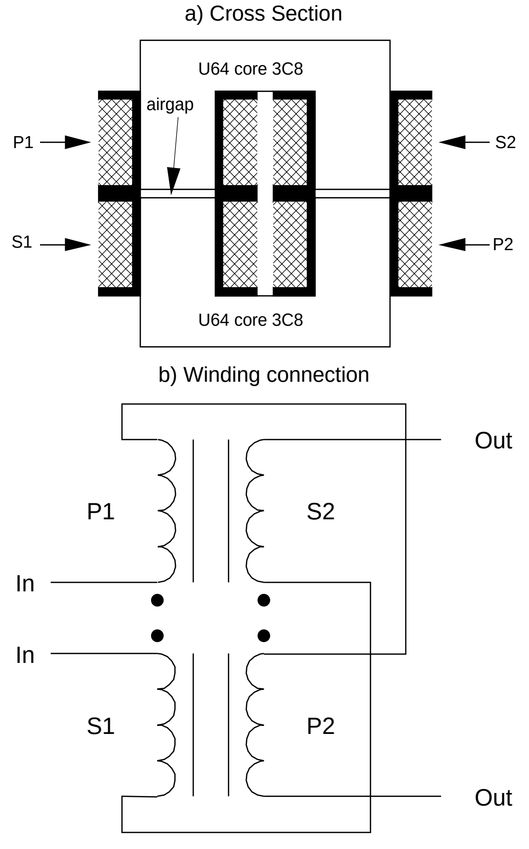


Fig. 10 PRPS transformer using U-64 cores

The equivalent electrical circuit diagram of the PRPS transformer is given in Fig. 11. It is the well known 'Tee' circuit with primary winding(s) leakage inductance Llp, a magnetisation inductance Lm and secondary winding(s) leakage inductance Lls, followed by an 'ideal' transformer for the output voltage transformation.

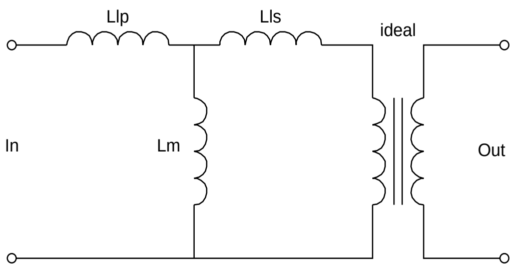


Fig. 11 PRPS transformer equivalent circuit

The primary and secondary leakage inductance is determined by the transformer construction and, in particular, by the positioning of the windings. In the symmetrical arrangement of Fig. 10, the values of Llp and Lls will be equal. Llp and Lls are also proportional to the square of the number of primary turns as is Lm. However, Lm is also strongly dependent on the width of the 'airgap' between the two U-cores. The airgap can be adjusted to give a value of Lm between 2 and 100 times Llp+Lls.

The transformer can be characterised by two inductance measurements:

- Lx, the measured primary inductance with the secondary winding(s) shorted.
- Ly, the measured primary inductance with the secondary winding(s) open circuit

It can be seen from the equivalent circuit diagram that,

$$Lx = Llp + \frac{Lm.Lls}{Lm + Lls}$$

$$Ly = Llp + Lm$$

If the transformer is assumed to be symmetrical then,

$$Llp = Lls$$

rearranging gives,

$$Llp = Ly - \sqrt{Ly^2 - Lx.Ly}$$

$$Lm = \sqrt{Ly^2 - Lx.Ly}$$

If the airgap is <50µm then Lm will be at least 100 times the value of Llp or Lls. In this case,

$$Lx \approx Llp + Lls$$

and

$$Ly \approx Lm$$

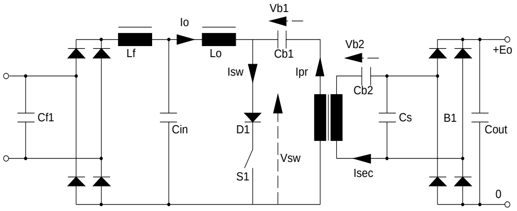


Fig. 12 PRPS pre-converter for 250V output

A PRPS pre-converter transformer for 1250W nett output has been constructed to the arrangement shown in Fig. 10. It had a primary consisting of two 36 turn windings connected in series, wound using 600 x 0.07mm Litz wire. The number of turns on the secondary varied depending on the required output voltage. Measurements of this transformer gave the following values for Lx and Ly.

Lx = 200 µH

Ly = 1600 µH (Note that this value is strongly influenced by the size of the airgap)

PRPS pre-converter for high output voltages

The circuit shown in Fig. 12 is a PRPS pre-converter using the type of transformer mentioned earlier. This circuit is intended to deliver 1250W at a relatively high voltage - in this case 250V. To achieve an final output voltage of 250V with an effective output voltage, Eo, of 450V means having a transformer with a turns ratio of 8:5.

Cf1	2µF	2 x 1µF
Cin	2µF	2 x 1µF
Cb1	0.2µF	2 x 0.1µF
Cb2	1.36µF	2 x 0.68µF
Cs	0.3µF	2 x 0.15µF
Lf	1600µH	
Lo	1600µH	
Lx	200µH	
Ly	1600µH	

Table 3 Component Values for High Output Voltage PRPS circuit

The transformer has replaced the inductance Ls in the basic circuit diagram of Fig. 6. The DC voltage blocking capacitor Cb has been split up into a primary blocking capacitor Cb1 and a secondary blocking capacitor Cb2. There will, therefore, be no DC current in Tr1 so in principle the transformer does not need an air gap. However, experience

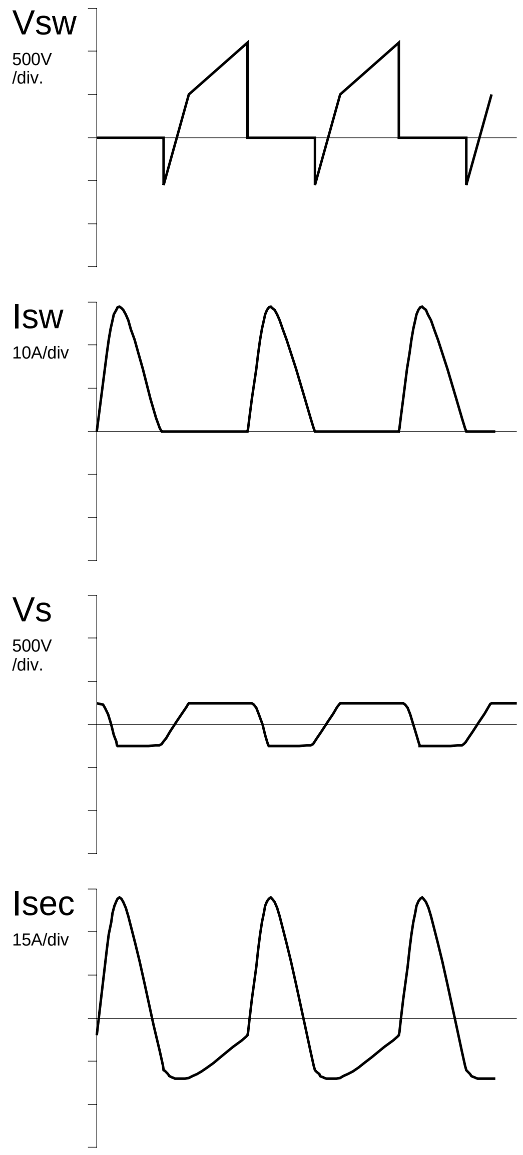


Fig. 13 Waveforms of high voltage pre-converter (Tcycle=0.7446 x Tref, 2.5kW output, Ep=310V)

has shown that a limited value of magnetisation inductance improves the operation of the circuit, so an airgap has been included which keeps the Ly value, of Tr1, equal to Lo.

The pre-converter circuit has been completed by the addition of capacitor Cf1, rectifier bridge and filter inductor Lf (an iron cored choke). The combination of Cf1, Lf, Cin and Lo prevents a significant switching frequency signal appearing at the mains terminals.

The component values shown in table 3 are used in the circuit of Fig. 12. With these values the no load reference cycle time will be 49.7 µs. Therefore, the no load operating frequency is just over 20 kHz.

Figs. 13 and 14 show the waveforms associated with the circuit when the input voltage is 310 V and the circuit is delivering 2.5 kW

Ep	Pout (PRPS)	Pout (R load)	% Deviation
310.0	2501	2501	0.0%
308.3	2476	2474	0.1%
303.2	2389	2392	-0.1%
294.8	2249	2262	-0.6%
283.2	2068	2087	-0.9%
268.5	1857	1876	-1.0%
250.8	1621	1637	-1.0%
230.4	1375	1382	-0.5%
207.4	1128	1119	0.8%
182.2	890	864	3.0%
155.0	668	625	6.8%
126.1	472	414	14.1%
95.8	305	239	27.7%
64.5	171	108	57.9%
32.4	70	27	156.2%

Table 4 Output power of PRPS pre-converter.

Of particular interest is Io because it can be easily measured with a low value resistor. This current will be used to control power output of the PRPS pre-converter. Io will be compared with a reference, Ioref, which will be proportional to input voltage Ep. The comparison of Io and Ioref should be done at the right time, namely during the period when Io has a negative slope. The switch S1 is turned ON as soon as the value of Io drops below Ioref.

The computed values of Pout for 15 values of Ep which would be achieved using this control strategy are given in Table 4. As a comparison the output power for a resistive load is also shown in Table 4.

It can be seen from Table 4, that the PRPS output power closely matches the power of a purely resistive load except for Ep values near the zero crossings of the mains/line voltage.

Of course, an average output power control loop (with a time constant far in excess of the 10 (8.3) ms cycle time of a half mains/line period) is required to determine the

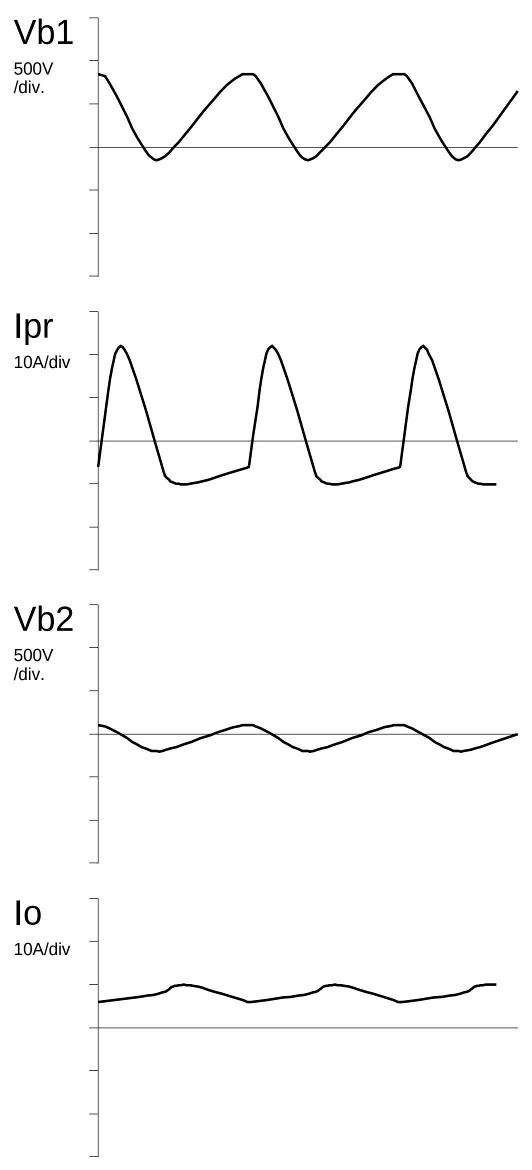


Fig. 14 Waveforms of high voltage pre-converter (Tcycle=0.7446 x Tref, 2.5kW output, Ep=310V)

proportionality constant between the mains/line voltage and Ioref for the mains/line voltage variations and for the output power control.

It can also be concluded, from table 4, that the PRPS circuit can indeed fulfil the pre-converter action successfully, i.e. a resistive load for the mains voltage can be easily achieved, thus no mains distortion and a power factor >0.99 is possible.

The circuit shown in Fig. 12 is only suitable for high output voltages. At low output voltages (below 100V for output powers in excess of 1000W), the secondary blocking capacitor Cb2 has to have a high value and pass a large current and is, therefore, an expensive component. If a low output voltage pre-converter is required, then an alternative arrangement is needed.

PRPS pre-converter for low output voltages

The high cost of Cb2, in a low output voltage PRPS pre-converter, could be avoided if it could be eliminated from the circuit. The problem is that removing Cb2 allows a DC current to flow in the transformer. The resulting flux can be handled by increasing the airgap between the cores of the transformer. This will have the additional effect of reducing Ly from 1600 µH to 800 µH. This change has been incorporated in the circuit shown in Fig. 15, which is intended to deliver 1200W at 60V.

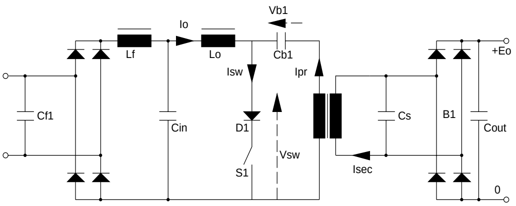


Fig. 15 PRPS pre-converter for 60V output

To get 1200W nett from a transformer of the type shown in Fig. 10 it is necessary to change the number of primary turns Np and thus decrease the value of Lx. Suitable values would be:

Np (primary turns)	2 x 28	(600 x .07 mm Litz wire)
Ns (secondary turns)	2 x 4	(flat Litz wire 7 mm2)

The air gap in the transformer should be adjusted to give an Lx of 125 µH.

Suitable values for the other components are given in table 5. The reference cycle time, Tref, with these values will be 39 µs.

The inductance Lo can be made with either a pair of U-64 cores - with the winding distributed over both legs- or with a pair of E-cores.

Cf1	2µF	2 x 1µF
Cin	2µF	2 x 1µF
Cb1	0.15µF	
Cs	3.75µF	5 x 0.75µF
Lf	1600µH	
Lo	1600µH	

Table 5 Component Values for Low Output Voltage PRPS circuit

In practice, PRPS pre-converters produce about 150W for each Amp(rms) flowing in the primary winding. So for a 1200W converter:

Ipr = 8A
Isec = 56A (at 60V and 20A)

The voltage and current wave forms for the circuit of Fig. 15 are similar to those shown in Figs. 13 and 14, except for the amplitudes in the secondary side.

This configuration of PRPS pre-converter is viable for output voltages as low as 40 V. Below this, however, the value and current rating of Cs becomes excessive and it is likely that alternative configurations would be more cost effective.

Control circuit for PRPS converters

Figure 16 shows a simple control circuit for PRPS converters. In is constructed from MOS ICs and standard comparators. The analogue control section for the output power stabilisation is not shown because it will, in principle, be no different than for an SMPS converter.

The PRPS control circuit comprises of a dual sawtooth oscillator whose frequency can be adjusted by applying a voltage to X1. The output of this oscillator is fed to the clock pulse input of a divide-by-8 counter. The highest oscillator frequency needs to be just over 8x the highest expected operating frequency of the PRPS power section.

The oscillator can be stopped by applying a hold up signal (low) to G1. This hold-up input is used to modulate the cycle time of the control circuit. As soon as this 'hold up' signal is removed (high), a pulse will sent to the divide-by-8 circuit which then advances one position.

The counter has 8 outputs, Q0-Q7. Output Q0 will go high either synchronously following Q7 or asynchronously with a high on pin15. Output Q0 sets a flip-flop consisting of a 2 and a 3 input NOR-gate. The output terminal X8 then goes high to indicate that the main switching device S1 should turn on.

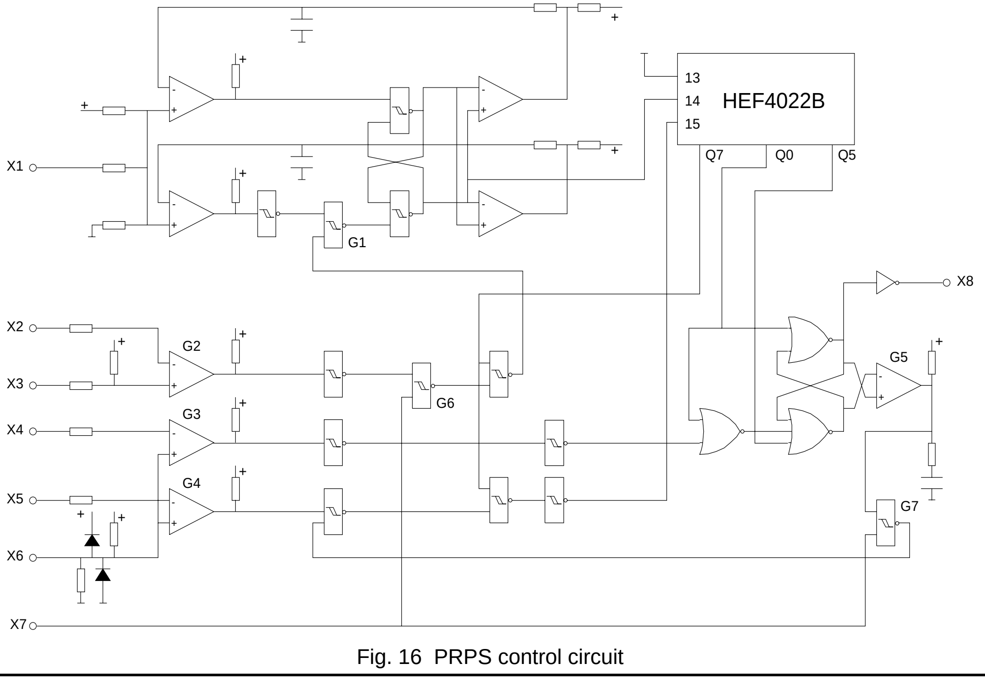


Fig. 16 PRPS control circuit

The Q7 output is used to enable both the 'hold-up' signal for the oscillator and the reset input for the divide-by-8, i.e. both the 'hold-up' and the reset only can be active if there is a '1' at Q7. The output flip-flop is reset either by the negative voltage across S1-D1 - via comparator G3 - or by the sixth position, Q5, of the counter. To prevent the possibility of immediate reset of the flip-flop, the indication of negative voltage across S1-D1 is blanked out while Q0 is high.

The voltage across S1-D1 is connected to terminal X6 via a high value resistor (220 kΩ). X4 is connected to the negative supply line of the power circuit. Comparator G3 then gives logical information about the polarity of the voltage across S1-D1.

Information about the amplitude of this voltage is obtained via comparator G4. A reference voltage, proportional to the mains voltage, is connected to X5. If the attenuated S1-D1 voltage falls below this reference, and Q7 is high, the counter will be reset and S1 will be turned ON. This is an emergency measure in case the normal current control loop via the comparator G2 fails to disable the 'hold up' signal. This could occur if there were a false current reference signal at X2.

The best strategy for the control of a PRPS pre-converter is by comparing the current, Io, in the input inductor, Lo, with a mains proportional reference current. In Fig. 16 a signal, proportional to Io, is connected to X3 and the reference signal to X2. As soon as Io falls below the reference value the 'hold-up' signal is removed, the counter is advanced from Q7 to Q0 and S1 is turned ON.

A '1' at input X7 allows the control circuit to run, whereas a '0' will cause the PRPS to switch OFF in a controlled manner. When X7 goes high, the output of NAND gate G7 goes low. This signal is used to reset the counter which takes Q0 high, turns on S1 and starts the operating cycle. The output of G5, which was pulled high while the circuit was stopped, is now driven low and is kept low by the RC network as long as S1 continues to be switched. This 'low' keeps the output of G7 high and allows the correct signal to be fed from G4 to the counter reset. The high on X7 also enables G6 and lets the information from G2 - the 'current' comparator - through to the 'hold up' circuit.

If X7 is taken low then G6 is disabled and the signal which would start the next switching cycle is not allowed to get through. The counter will continue to run until Q7 goes high at which time the circuit will be 'held up' and the operating cycle will be halted.

The cycle time will be adjusted by changing the reference value at X2. This signal will be a series of half sinewaves whose peak value is proportional to the power that the pre-converter needs to deliver to the keep the output voltage at the required level. This control strategy has been tested on various PRPS circuits and fulfils all the requirements properly.

Modelling PRPS pre-converters

There are no equations which summarise the overall behaviour of a PRPS pre-converter circuit. Determining factors like the throughput power of the circuit and the peak voltages and currents, means developing a computer model. In this model the operation of the circuit is broken down into its separate modes and the appropriate equations derived for each of them.

The circuit of Fig. 6 has, basically, two switches which determine its mode of operation. The first is the combination of S1 and D1 - this is the controllable switch - and the second is the bridge rectifier B1.

Therefore the circuit has four different modes of operation. For all these modes, the time functions for the currents and voltages can be derived by circuit analysis. The four modes are given below:

Mode	S1-D1	Bridge
I	ON	ON
II	ON	OFF
III	OFF	OFF
IV	OFF	ON

Table 6 PRPS Operating Modes

Using Laplace transformation it is possible to derive the time functions for currents Io and Is, for the circuit in each of its 4 modes. This method allows the initial values of the currents and voltages to be easily introduced into the equations. The initial conditions of Io, Is, Vb1 and Vs will be indicated by Jo, Js, Ub1 and Us respectively.

Mode I

We will start with the derivation of the time functions for the operation of the PRPS circuit in mode I (S1-D1 ON and B1 ON). The initial conditions are:

$$Io = Jo$$

$$Is = Js = -Jo$$

$$Vb1 = Ub1$$

$$Vs = Us = Eo$$

Calculation starts at t = 0 with the switching ON of S1-D1, while B1 is already conducting, i.e. $Jo > 0$. The following Laplace equations are then valid:

$$\frac{Ep}{s} + Lo.Jo = Io.s.Lo$$

$$\frac{Ub1+Us}{s}+Ls.Js=Is.\left(s.Ls+\frac{1}{s.Cb1}\right)$$

Note: B1 is conducting, so $Vs=Us=Eo$, i.e. Cs is infinitely large and has no influence on Is.

If we define the following:

$$\omega=\sqrt{\frac{1}{Ls.Cb1}}$$

$$F1=Jo$$

$$F2=\frac{Ep}{Lo}$$

$$G1=Js$$

$$G2=\frac{Ub1+Us}{Ls}$$

The Laplace equations for Io and Is can then be written as:

$$Io=\frac{F1}{s}+\frac{F2}{s^2}$$

$$Is=\frac{G1.s}{s^2+\omega^2}+\frac{G2}{s^2+\omega^2}$$

The inverse Laplace transformation of these two equations gives the following time functions:

$$Io=F1+F2.t$$

$$Is=G1.\cos(\omega.t)+\frac{G2}{\omega}.\sin(\omega.t)$$

To calculate the input power and the voltage Vb1 and Vs, these time functions can be integrated to give Ioint and Isint, thus:

$$Ioint=F1.t+\frac{F2}{2}.t^2$$

$$Isint=\frac{G1}{\omega}.\sin(\omega.t)+\frac{G2}{\omega^2}.(1-\cos(\omega.t))$$

The input power during the validity of mode I (i.e. during a time interval of length T1) is equal to:

$$Pin(T1)=\frac{Ep.Ioint}{T1}$$

The voltages Vb1 and Vs are equal to:

$$Vb1=Ub1-\frac{Isint}{Cb1}$$

$$Vs=Us=Eo$$

In the computer program, these formulae will be stored in a subroutine called sub1.

Mode II

The initial conditions for mode II operation (S1-D1 ON and B1 OFF) are:

$$Io=Jo$$

$$Is=Js$$

$$Vb1=Ub1$$

$Vs=Us$ (either +Eo or -Eo)

The Laplace equations for Io and Is are now:

$$\frac{Ep}{s}+Lo.Jo=Io.s.Lo$$

$$(Ub1+Us).s+Ls.Js=Is.\left(s.Ls+\frac{Cb1+Cs}{s.Cb1.Cs}\right)$$

Define:

$$\omega=\sqrt{\frac{Cb1+Cs}{Ls.Cb1.Cs}}$$

$$F1=Jo$$

$$F2=\frac{Ep}{Lo}$$

$$G1=Js$$

$$G2=\frac{Ub1+Us}{Ls}$$

The Laplace functions for Io and Is are now identical to those for mode I, so the time functions are:.

$$Io=F1+F2.t$$

$$Is=G1.\cos(\omega.t)+\frac{G2}{\omega}.\sin(\omega.t)$$

$$Ioint=F1.t+\frac{F2}{2}.t^2$$

$$Isint=\frac{G1}{\omega}.\sin(\omega.t)+\frac{G2}{\omega^2}.(1-\cos(\omega.t))$$

$$Pin(T2)=\frac{Ep.Ioint}{T2}$$

$$Vb1=Ub1-\frac{Isint}{Cb1}$$

$$Vs=Us-\frac{Isint}{Cs}$$

In the computer program, these formulae will be stored in a subroutine called sub2.

Mode III

The initial conditions for mode III operation (S1-D1 OFF and B1 OFF) are:

$$Io = Jo$$

$$Is = Js = -Jo$$

$$Vb1 = Ub1$$

$$Vs = Us$$

The correct Laplace equation for Is ($Io = -Is$) can be expressed by the relationship:

$$\frac{Ub1 + Us - Ep}{s} + (Lo + Ls).Js = Is.\left(s.(Lo + Ls) + \frac{Cb1 + Cs}{s.Cb1.Cs} \right)$$

Define:

$$\omega = \sqrt{\frac{Cb1 + Cs}{(Lo + Ls).Cb1.Cs}}$$

$$G1 = Js$$

$$G2 = \frac{Ub1 + Us - Ep}{Lo + Ls}$$

The time functions can then be expressed by:

$$Is = G1.\cos(\omega.t) + \frac{G2}{\omega}.\sin(\omega.t)$$

$$Io = -Is$$

$$Isint = \frac{G1}{\omega}.\sin(\omega.t) + \frac{G2}{\omega^{2.}}(1 - \cos(\omega.t))$$

$$Ioint = Isint$$

$$Pin(T3) = \frac{Ep.Ioint}{T3}$$

$$Vb1 = Ub1 - \frac{Isint}{Cb1}$$

$$Vs = Us - \frac{Isint}{Cs}$$

In the computer program, these formulae will be stored in a subroutine called sub3.

Mode IV

The initial conditions for the mode IV operation (S1-D1 OFF and B1 ON) are given below:

$$Io = Jo$$

$$Is = Js = -Jo$$

$$Vb1 = Ub1$$

$$Vs = Us = Eo$$

The Laplace equation for current Is is now:

$$\frac{Ub1 + Us - Ep}{s} + (Lo + Ls).Js = Is.\left(s.(Lo + Ls) + \frac{1}{(s.Cb1)} \right)$$

Define:

$$\omega = \sqrt{\frac{1}{(Lo + Ls).Cb1}}$$

$$G1 = Js$$

$$G2 = \frac{Ub1 + Us - Ep}{Lo + Ls}$$

The time functions are given by,

$$Is = G1.\cos(\omega.t) + \frac{G2}{\omega}.\sin(\omega.t)$$

$$Io = -Is$$

$$Isint = \frac{G1}{\omega}.\sin(\omega.t) + \frac{G2}{\omega^{2.}}(1 - \cos(\omega.t))$$

$$Ioint = Isint$$

$$Pin(T4) = \frac{Ep.Ioint}{T4}$$

$$Vb1 = Ub1 - \frac{Isint}{Cb1}$$

$$Vs = Us$$

In the computer program, these formulae will be stored in a subroutine called sub4.

Program structure

The modelling program can be written around the four subroutines. The central part of the program will make successive calls to the appropriate subroutine. The calculated values of current and voltage will be used to determine when the circuit moves form one mode to the next. The final values of Io, Is, Vb1 and Vs will be used as the initial values, Jo, Js, Ub1 and Us, for the next mode. The actual sequence of the modes depends upon the operating frequency and load condition. Under full load condition when Ep is not close to zero, the sequence of modes will be as shown in Table 7.

One cycle of operation ends when Io falls below Ioref. This would result in S1 being turned ON, putting the circuit in to mode I and starting the cycle once more. At the end of each cycle, the input power can be compared with a reference value (Pref) and Ioref can be adjusted until the powers are equal. It is then possible to read various important values

S1-D1	B1	Mode	End Condition
ON	ON	I	Is>0
ON	OFF	II	Vs<-Eo
ON	ON	I	Is<0
ON	OFF	II	Isw=Io+Is<0
OFF	OFF	III	Vs>Eo
OFF	ON	IV	Io<Ioref

Table 7 PRPS Operating Sequence

such as the initial conditions for Io, Is, Vb1, Vs, the cycle time, output power, RMS values of Io and Is, DC and AC fluxes in the ferrite cores, etc.

Writing a program like this is well within the capabilities of anyone with some experience of programming. The calculations involved are so simple that there will be little difficulty in using almost any programming language. A model produced in this way will be faster and more accurate than could be produced with any of the standard modelling programs.

Conclusions

The PRPS configuration is well suited to the needs of the pre-converter application. It can boost the low mains voltages, near zero crossing, to high levels so that some power is delivered to the load throughout all of the mains cycle. This helps the PRPS appear as a resistive load to the mains.

A PRPS pre-converter can deliver a DC output voltage with low levels of mains ripple using only moderately sized output smoothing capacitors. The addition of a high frequency transformer gives mains isolation and the ability to have a wide range of output voltages.

The transformer need not be a major additional cost. The high operating frequency means the transformer uses ferrite core and is relatively small (5% of the size of copper / iron transformer). A side by side arrangement of the windings means the transformer is easy to wind, easy to insulate and can have the right leakage inductance to replace the resonant network inductor.

The resonant action of the PRPS circuit allows the main semiconductor switching device to be turned off at zero current. This reduces, considerably, the switching loss of this device allowing a smaller device to be used in higher power / frequency circuits than it could normally resulting in a significant cost saving.

Unfortunately an overall analysis of the performance of a PRPS pre-converter is difficult. However, by breaking the cycle of operation into its logical modes, it becomes easy to generate the time functions for all the currents and voltages. It is simple to incorporate these equations into a computer program to produce an accurate, detailed and fast running model of the system.

The use of pre-converters is become increasingly necessary and the characteristics of PRPS circuits mean that there are well suited to this function. It is easy to overcome the apparent complexity of resonant systems to produce PRPS pre-converters which are elegant, efficient and cost effective.

Acknowledgments

We are grateful for all the contributions from our colleagues within Philips and to the Application Laboratories in Eindhoven and Hamburg.

We would also like to thank Dr.P.H.Mellor of the University of Sheffield for contributing the application note of section 3.1.5.

The authors thank Mrs.R.Hayes for her considerable help in the preparation of this book.

The authors also thank Mr.D.F.Haslam for his assistance in the formatting and printing of the manuscripts.

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Preface

This book was prepared by the Power Semiconductor Applications Laboratory of the Philips Semiconductors product division, Hazel Grove. The book is intended as a guide to using power semiconductors both efficiently and reliably in power conversion applications. It is made up of eight main chapters each of which contains a number of application notes aimed at making it easier to select and use power semiconductors.

CHAPTER 1 forms an introduction to power semiconductors concentrating particularly on the two major power transistor technologies, Power MOSFETs and High Voltage Bipolar Transistors.

CHAPTER 2 is devoted to Switched Mode Power Supplies. It begins with a basic description of the most commonly used topologies and discusses the major issues surrounding the use of power semiconductors including rectifiers. Specific design examples are given as well as a look at designing the magnetic components. The end of this chapter describes resonant power supply technology.

CHAPTER 3 describes motion control in terms of ac, dc and stepper motor operation and control. This chapter looks only at transistor controls, phase control using thyristors and triacs is discussed separately in chapter 6.

CHAPTER 4 looks at television and monitor applications. A description of the operation of horizontal deflection circuits is given followed by transistor selection guides for both deflection and power supply applications. Deflection and power supply circuit examples are also given based on circuits designed by the Product Concept and Application Laboratories (Eindhoven).

CHAPTER 5 concentrates on automotive electronics looking in detail at the requirements for the electronic switches taking into consideration the harsh environment in which they must operate.

CHAPTER 6 reviews thyristor and triac applications from the basics of device technology and operation to the simple design rules which should be followed to achieve maximum reliability. Specific examples are given in this chapter for a number of the common applications.

CHAPTER 7 looks at the thermal considerations for power semiconductors in terms of power dissipation and junction temperature limits. Part of this chapter is devoted to worked examples showing how junction temperatures can be calculated to ensure the limits are not exceeded. Heatsink requirements and designs are also discussed in the second half of this chapter.

CHAPTER 8 is an introduction to the use of high voltage bipolar transistors in electronic lighting ballasts. Many of the possible topologies are described.

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