APPLICATION NOTE

Demonstration Board
TZA3004HL
SDH/SONET Data&Clock Recovery

June 1997

Philips
Semiconductors

PHILIPS

SDH/SONET Data&Clock Recovery TZA3004HL

FEATURES

- Full functional testing capability, including loop mode
- 4-Layer Epoxy FR4 PCB
- SMA RF Connectors
- Differential microstrip lines with 50 Ω odd mode impedance
- Single-ended and differential operation possible
- Assembly Instructions
- Full extended ground and supply voltage layers

APPLICATIONS

- Functional Verification
- Performance Evaluation
- Application Tests

GENERAL DESCRIPTION

The demonstration board for the TZA3004HL data & clock recovery IC can be supplied assembled or non assembled. This board can be used to evaluate the TZA3004HL, alone, and allows the application designer to do extensive testing without having to worry about other external factors. For maximum reliability the IC is soldered to the board. This application note describes the schematic and the layout of the board and contains assembly instructions. A functional test is described in detail.

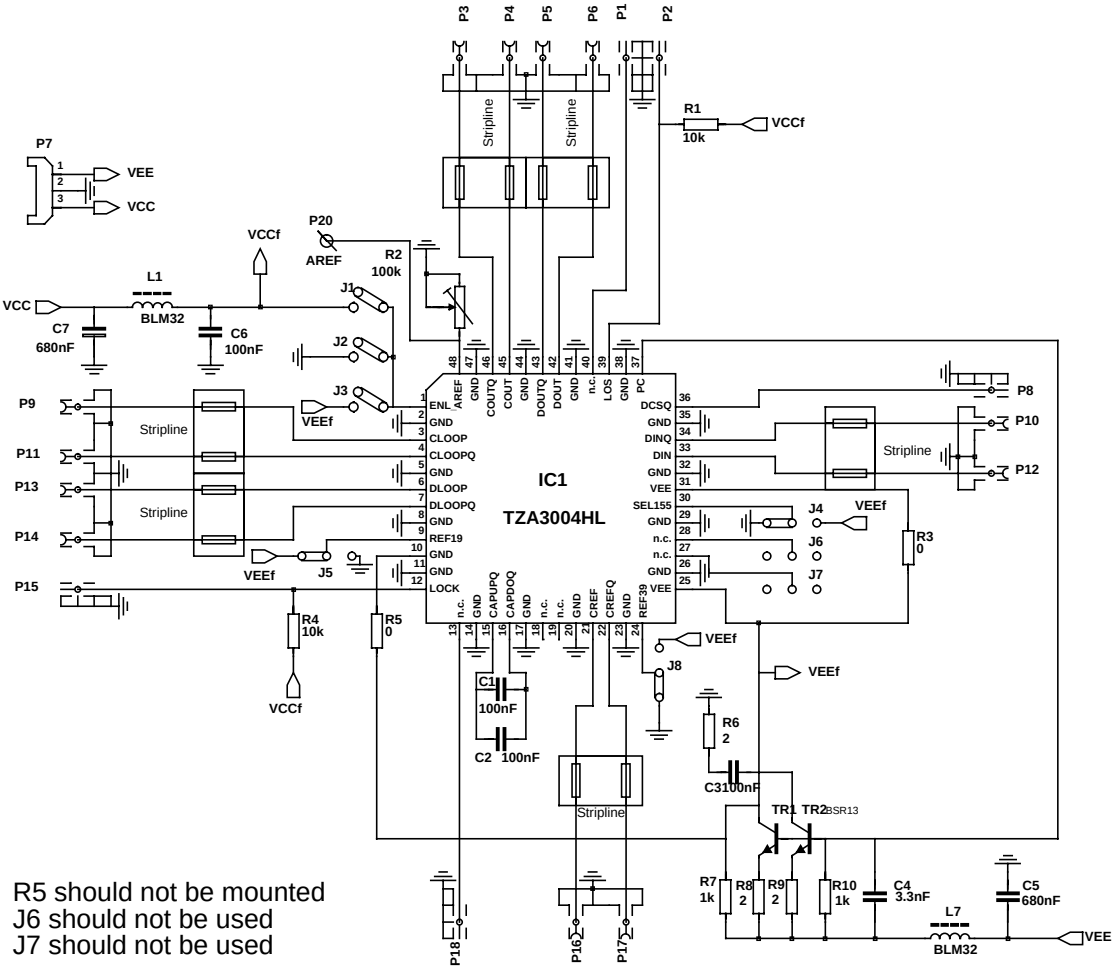
A data sheet for the IC is available: “Data Sheet TZA3004HL, Objective specification, December 1996”

ORDERING INFORMATION

To order demonstration boards, write to:

Philips Semiconductors C&M-N
Marketing Department
Gerstweg 2
6534 AE Nijmegen
The Netherlands

DEMO BOARD SCHEMATIC

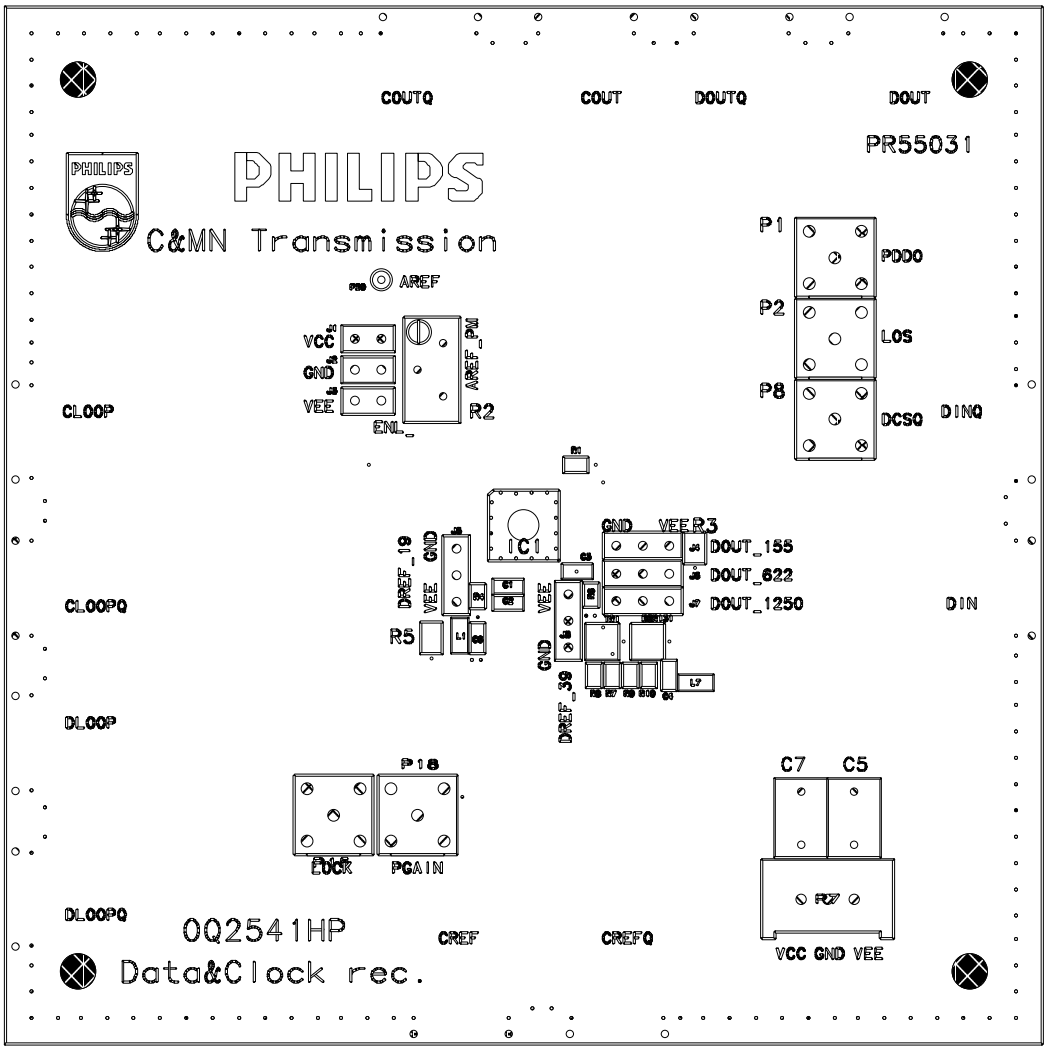


R5 should not be mounted
J6 should not be used
J7 should not be used

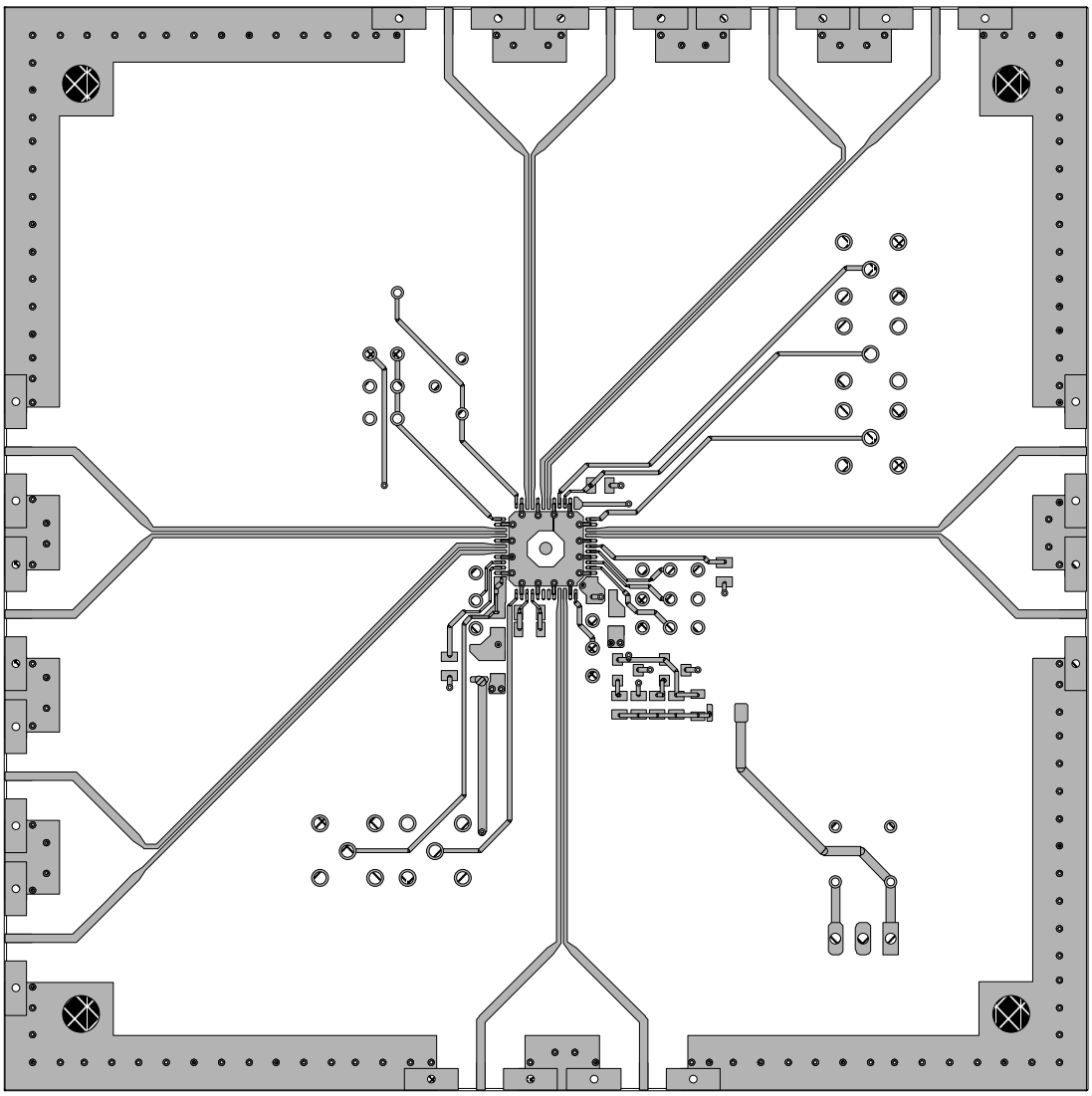
BILL OF MATERIALS

item no	count	company part no	component	series	vendor	tolerance	rating	geometry	reference
1	1	8222-411-55031	Board						
2	5	R144426	SMB CLICK str	COAX	Radiall			SMB_straight	P1,P2,P8, P15,P18
3	1	MKS3733-1-0-303	MKS3730_3p	MKS3730	Stocko			MKS3730_3p	P7
4	2		BSR13	Switching	Philips			SOT23	TR1, TR2
5	1	2422-034-15068	Solder Pin Small		Philips			Solder Pin Small	P20
6	5	2422-024-04008	Jumper_3p	print switch	Philips			Jumper_3p	J4,J5,J6,J7, J8
7	3	2422-024-04008	Jumper_2p	print switch	Philips			Jumper_2p	J1,J2,J3
8	2	2322-734-92002	0	RC11	Philips	1%	0.1 W	R0805	R3,R5
9	3	2322-730-61204	2	RC11	Philips	5%	0.1 W	R0805_hf	R6,R8,R9
10	2	2322-730-61103	10k	RC11	Philips	5%	0.1 W	R0805_hf	R1,R4
11	2	2322-730-61102	1k	RC11	Philips	5%	0.1 W	R0805_hf	R7,R10
12	4	2222-910-16649	100 nF	C910-X7R	Philips	10%	25 V	C0805_hf	C1,C2,C3, C6
13	1	2222-590-16621	3.3 nF	C590-X7R	Philips	10%	63 V	C0805_hf	C4
14	2	2222-370-11684	680 nF	MKT 370	Philips	10%	63 V	C370_C	C5, C7
15	1	2122-362-00729	100k	3296Y	Bourns	10%	0.5 W	BO3296Y	R2
16	1	PN-TZA3004HL	TZA3004HL	IC_Universal	Philips			SOT313	IC1
17	2	BLM32A07	BLM32	CBD	Murata			BLM32	L1, L7
18	12	142-0801-811	SMA Launcher	COAX	EF Johnson			SMA	P3,P4,P5, P6,P9,P10, P11,P12, P13,014, P16,P17

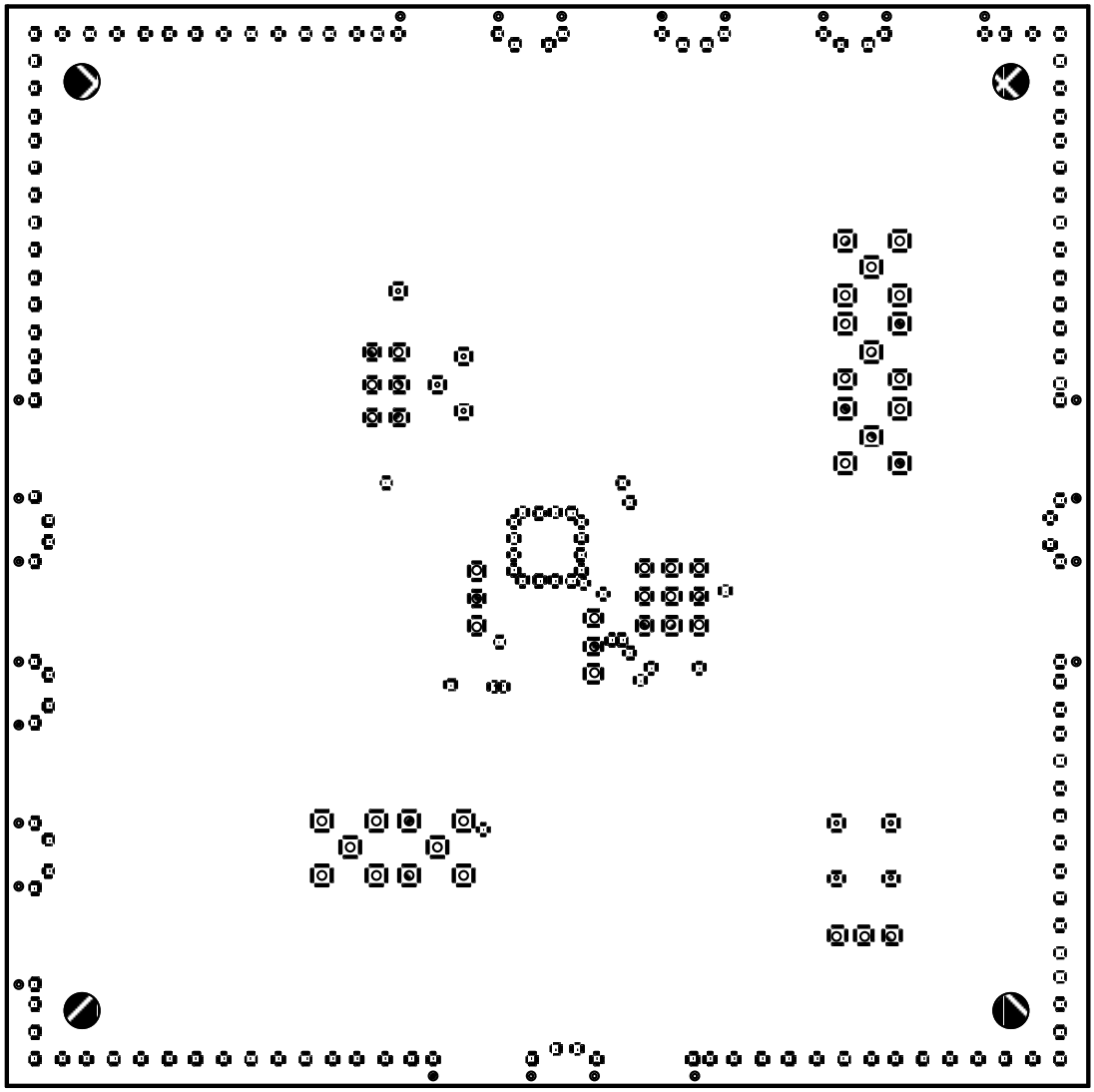
DEMO BOARD ASSEMBLY DRAWING



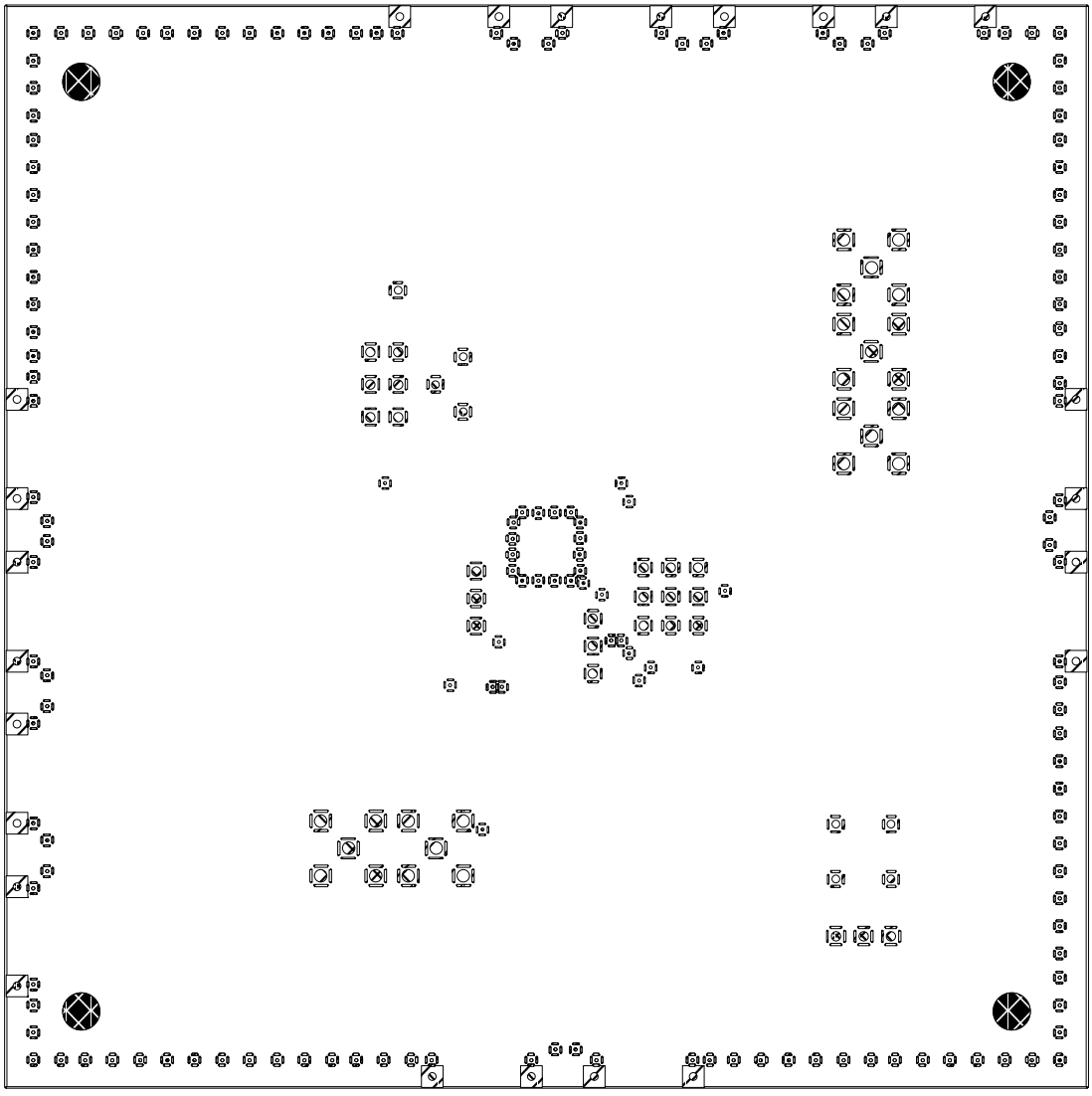
LAYOUT: TOP LAYER, SIGNAL LAYER



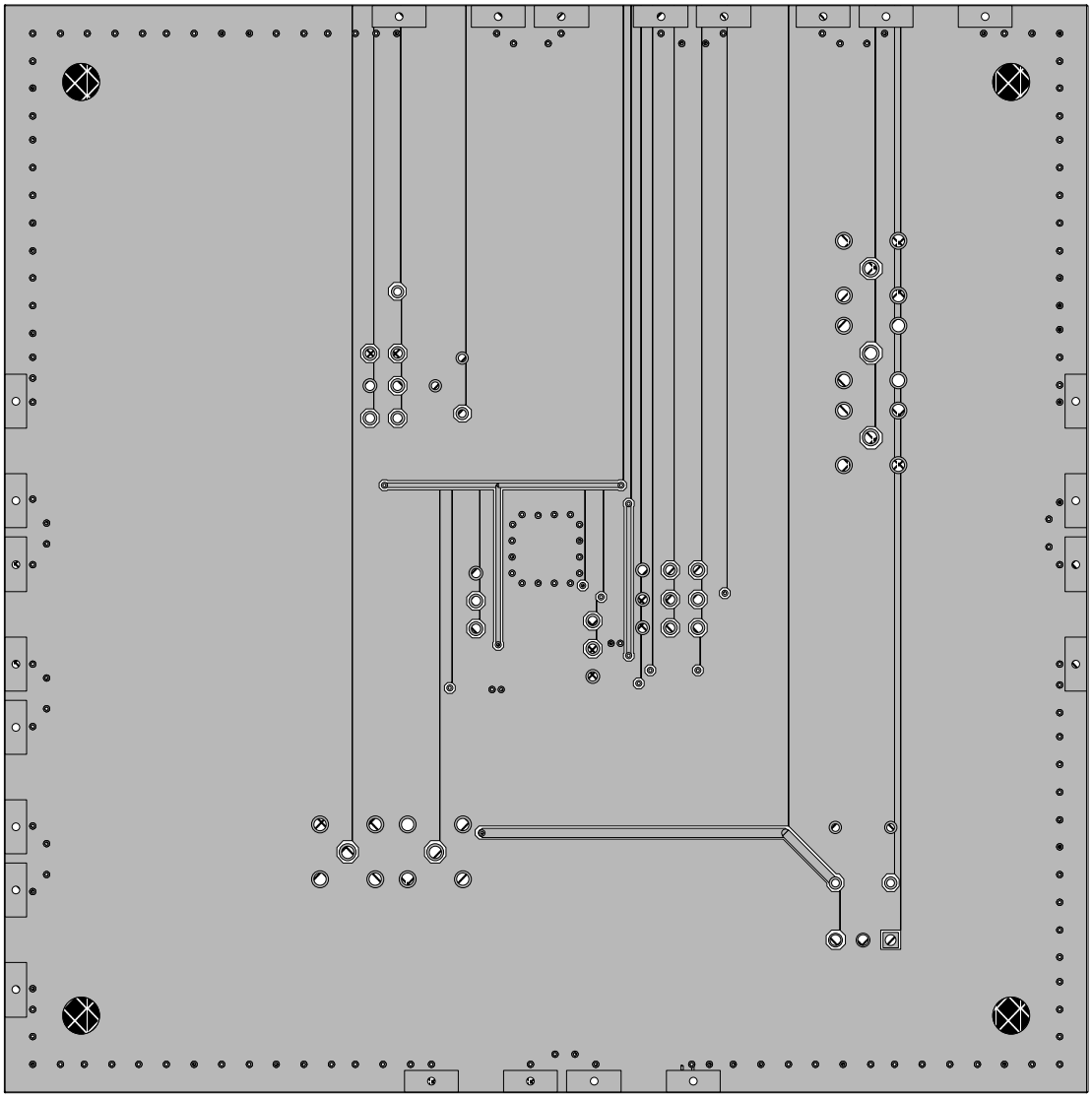
LAYOUT: 2ND LAYER, GROUND LAYER (NEGATIVE PROJECTION)



LAYOUT: 3RD LAYER, SUPPLY LAYER (NEGATIVE PROJECTION)



LAYOUT: BOTTOM LAYER, GND & SIGNAL LAYER



PINNING

SYMBOL	PIN	DESCRIPTION
$\overline{ENL}$	1	enable loop mode; active LOW
GND	2	ground
CLOOP	3	clock output in loop mode
CLOOPQ	4	inverted clock output in loop mode
GND	5	ground
DLOOP	6	data output in loop mode
DLOOPQ	7	inverted data output in loop mode
GND	8	ground
REF19	9	enable frequency divider 2; f_{ref}=19 MHz
GND	10	ground
GND	11	ground
LOCK	12	lock detect
n.c	13	not connected
GND	14	ground
CAPUPQ	15	external loop filter capacitor
CAPDOQ	16	external loop filter capacitor return
GND	17	ground
n.c.	18	not connected
n.c.	19	not connected
GND	20	ground
CREF	21	reference clock input
CREFQ	22	inverted reference clock input
GND	23	ground
REF39	24	enable frequency divider 2; fref=39 MHz
VEE	25	negative supply voltage
GND	26	ground
n.c.	27	not connected
n.c.	28	not connected
GND	29	ground
SEL155	30	enable frequency divider 1; f_{out}=155 MHz
VEE	31	negative supply voltage
GND	32	ground
DIN	33	data input
DINQ	34	inverted data input
GND	35	ground
DCSQ	36	DC sense for offset control
PC	37	power control
GND	38	ground
LOS	39	loss of signal
n.c.	40	not connected

SYMBOL	PIN	DESCRIPTION
GND	41	ground
DOUT	42	data output in normal mode
DOUTQ	43	inverted data output in normal mode
GND	44	ground
COUT	45	clock output in normal mode
COUTQ	46	inverted clock output in normal mode
GND	47	ground
AREF	48	output amplitude adjustment

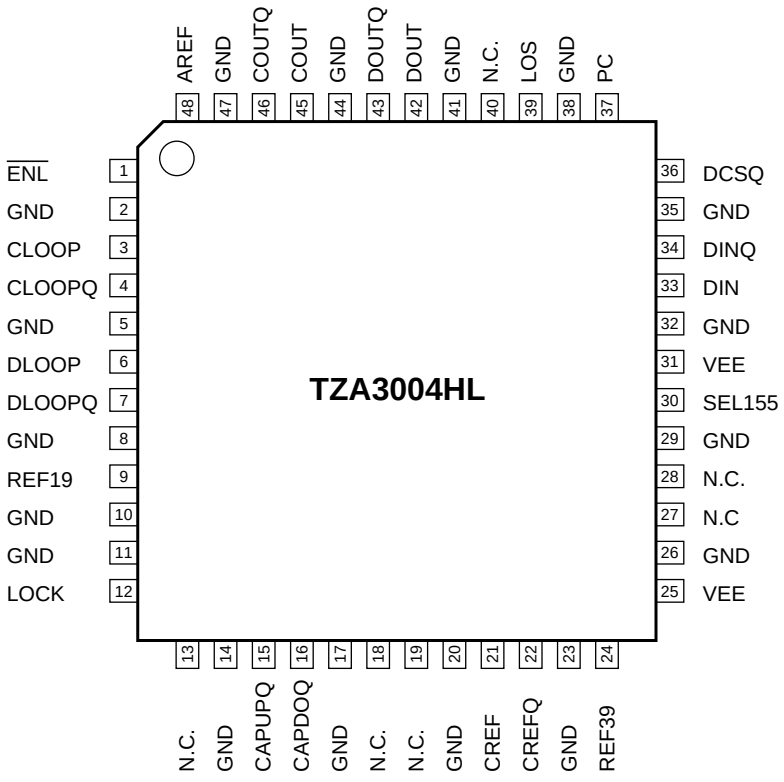


Fig.1 Pin configuration.

PREPARING THE DEMO BOARD FOR OPERATION

!! WARNING: ALL RF INPUT AND OUTPUT IC PINS ARE **NOT ESD PROTECTED**. HANDLE THE DEMONSTRATION BOARD ACCORDING TO STANDARD ESD HANDLING PROCEDURES!

!! WARNING: R5 SHOULD NOT BE MOUNTED. THIS CAN DAMAGE THE IC!

Adjust the supply voltages to their nominal values before connecting the power cable to the board, i.e. V_{EE} = -4.5V and V_{CC} = +5V.

Unless mentioned otherwise, all RF connections have to be terminated with 50Ω.

JUMPER TABLES

Several IC settings can be selected by means of jumpers, according to the tables below, where '0' indicates an open jumper and '1' indicates a closed jumper.

Normal mode vs. loop mode

FUNCTIONAL MODE	J1(VCC)	J2(GND)	J3(VEE)	DOUT(Q)	COUT(Q)	DLOOP(Q)	CLOOP(Q)
DCR	1	0	0	ENabled	ENabled	DISabled	DISabled
DCR	0	1	0	DISabled	DISabled	ENabled	ENabled
DCR	0	0	1	ENabled	ENabled	ENabled	ENabled

Division factor of frequency divider 1, DCR bit rate selection STM1/OC3 or STM4/OC12

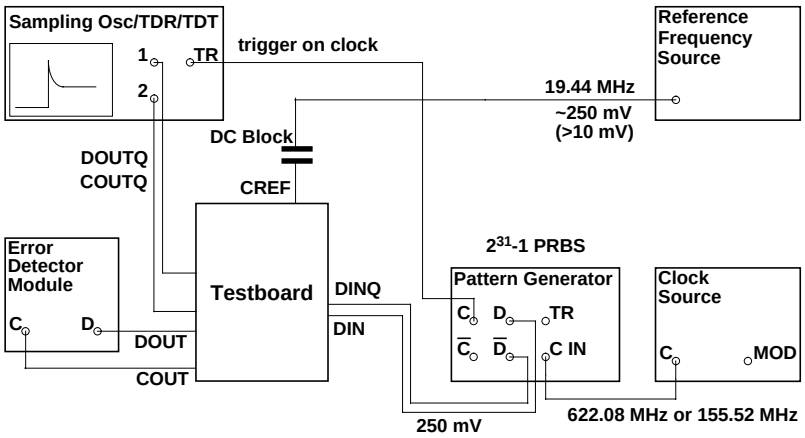
DIVISION FACTOR	BIT RATE	SEL155 (J4)
4	STM4	GND
16	STM1	V_{EE}

Division factor of frequency divider 2, reference frequency selection

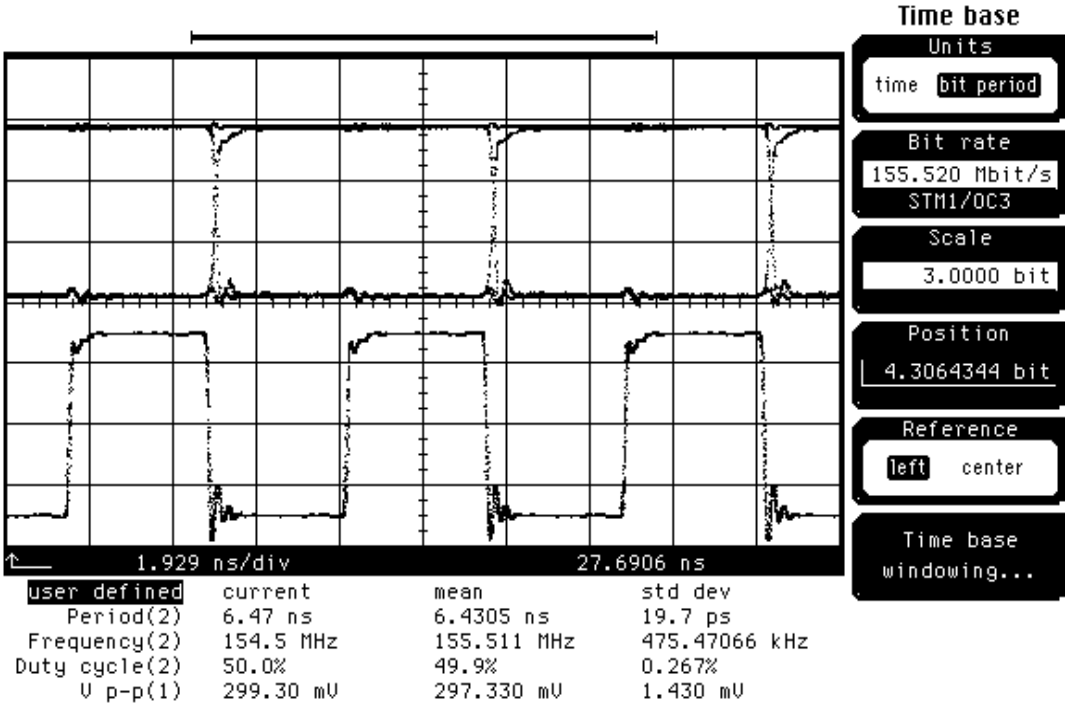
DIVISION FACTOR	REF19 (J5)	REF39 (J8)
64	GND	V_{EE}
128	V_{EE}	V_{EE}

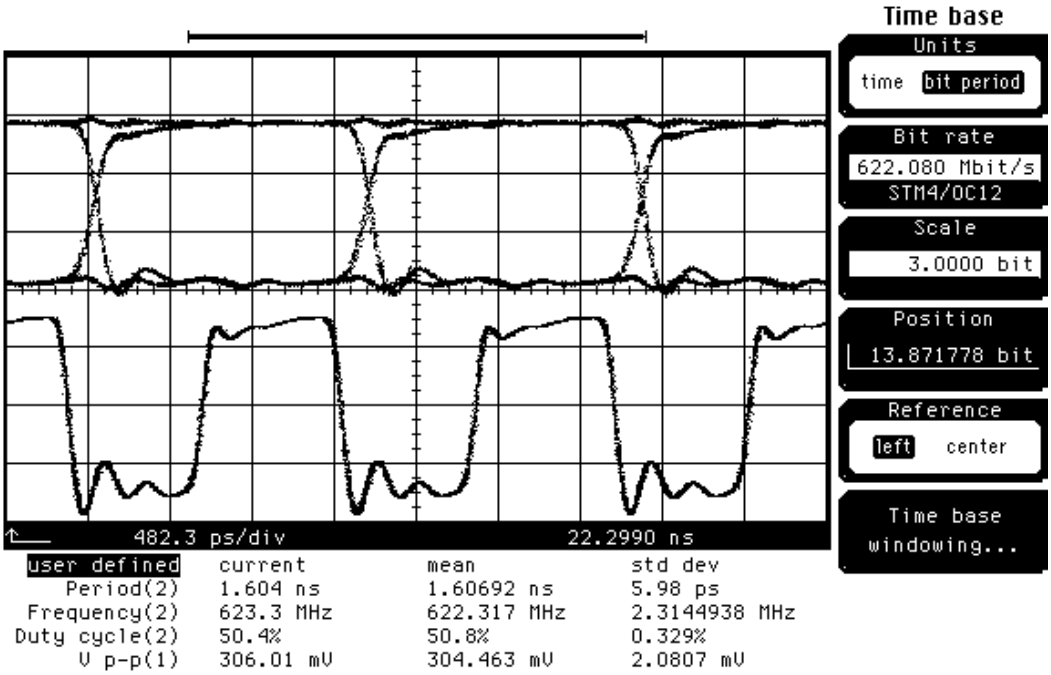
FUNCTIONAL TEST OF TZA3004HL DATA & CLOCK RECOVERY

.



Above:Functional test setup: Data &Clock Recovery mode
Below: Data eye diagram (upper) and recovered clock (lower) in a STM1/OC3 (155.52 Mbit/s) application
Next Page: Recovered data and clock in a STM4/OC12 (622.08 Mbit/s) application




Time base
Units
time
bit period
Bit rate
622.080 Mbit/s
STM4/OC12
Scale
3.0000 bit
Position
13.871778 bit
Reference
left
center
Time base
windowing...
482.3 ps/div
22.2990 ns
user defined
current
mean
std dev
Period(2)
1.604 ns
1.60692 ns
5.98 ps
Frequency(2)
623.3 MHz
622.317 MHz
2.3144938 MHz
Duty cycle(2)
50.4%
50.8%
0.329%
V p-p(1)
306.01 mV
304.463 mV
2.0807 mV