PLA Devices

INTRODUCTION

Philips Semiconductors PLAs are particularly useful in the design of wide address decoders and random logic replacement. The primary advantage Philips Semiconductors brings to these applications with their PLA devices is product term sharing, which is made possible via the two programmable arrays graphically shown in Figure 1. The familiar PAL® architecture supports a programmable AND array, followed by a fixed OR array. Better than 90% of the PAL devices that are available today are limited to 8 input wide OR gates. When pursuing a solution to a complex address decoding scheme, this restriction is prohibitive. The Philips Semiconductors PLA devices support 100% connection of all product terms to one or more OR gates. Once a term is created, it can be shared with any or all of the output functions. No duplication of resources is incurred. The popular PLXX153 family support 32-input wide OR gates which are ideal for memory or I/O decoders. The addition of programmable output polarity also enhances design efficiency and logic minimization.

The two programmable array concept dominates the Philips PLD product line. With the exception of the PAL-type devices which have been geared for ultimate performance, all Philips PLDs have been architected with efficient and flexible PLA structures. With the largest breadth programmable product line in the industry, Philips believes the designer can truly fill his requirements from the several product lines – PLA, PAL and PLS. Two combinatorial logic PLA device descriptions follow. For information on PLA devices with registers please refer to the sequencer section of this manual.

PHILIPS SEMICONDUCTORS PLUS153

Figure 2 depicts the Philips PLUS153. This bipolar PLA is pin and functionally equivalent to the Philips PLS153, however is available with a maximum propagation delay time of 10ns from input to output.

The PLUS153 has eight dedicated inputs and 10 bidirectional pins. The bidirectional pins may be adapted to suite the user's specific needs. 20-pin DIP or PLCC packages are available.

The output structure of the PLUS153 includes programmable polarity control on each output. Either active HIGH (non-inverting) or active LOW (inverting) outputs are configurable via the EX-OR gate associated with each I/O. Individual 3-State control of the I/O is also supported with the ten direction control AND terms (D1-D9).

Other benefits to the PLUS153 include full pin compatibility with most 20-pin combinational PAL parts. The natural product term sharing capabilities of the PLA architecture yield complete freedom of configuration should the engineer implement a particularly creative decode configuration.

PHILIPS SEMICONDUCTORS PLUS173

Figure 3 depicts the Philips Semiconductors PLUS173. This bipolar PLA is functionally equivalent to the Philips PLS173. The 24-pin PLUS173 has four more inputs pins than the PLUS153. The user may adapt the bidirectional pins to suit particular decoding needs, but the propagation delay time is still no more than 10ns from stabilized input to stable output for a PLUS173-10 device.

By having more inputs than the 153 part, the 173 can either resolve more input lines or generate more outputs functions for the same number of inputs. Distinct 3-State control over each output may be useful for controlling chip enables where contention (i.e., multiple access) may exist.

For speed and input width, the PLUS173 is probably the best single PLS available today for both memory and I/O decoding. Combining the 10ns T_{PD} with the distinguishable range of 12 to 21 inputs, the designer can easily decode say 16 input addresses as well as read/write qualifiers or encoded status signals. Output polarity control (Active-High or Active-Low) is achieved by programming the Exclusive-OR gate associated with each output.

The flexibility achieved with a PLA structure can be quickly appreciated by the designer who has experienced the frustration of the dedicated "OR" structures in PAL ICs. Currently, the only time penalty for the freedom granted by a PLA is a few nanoseconds!

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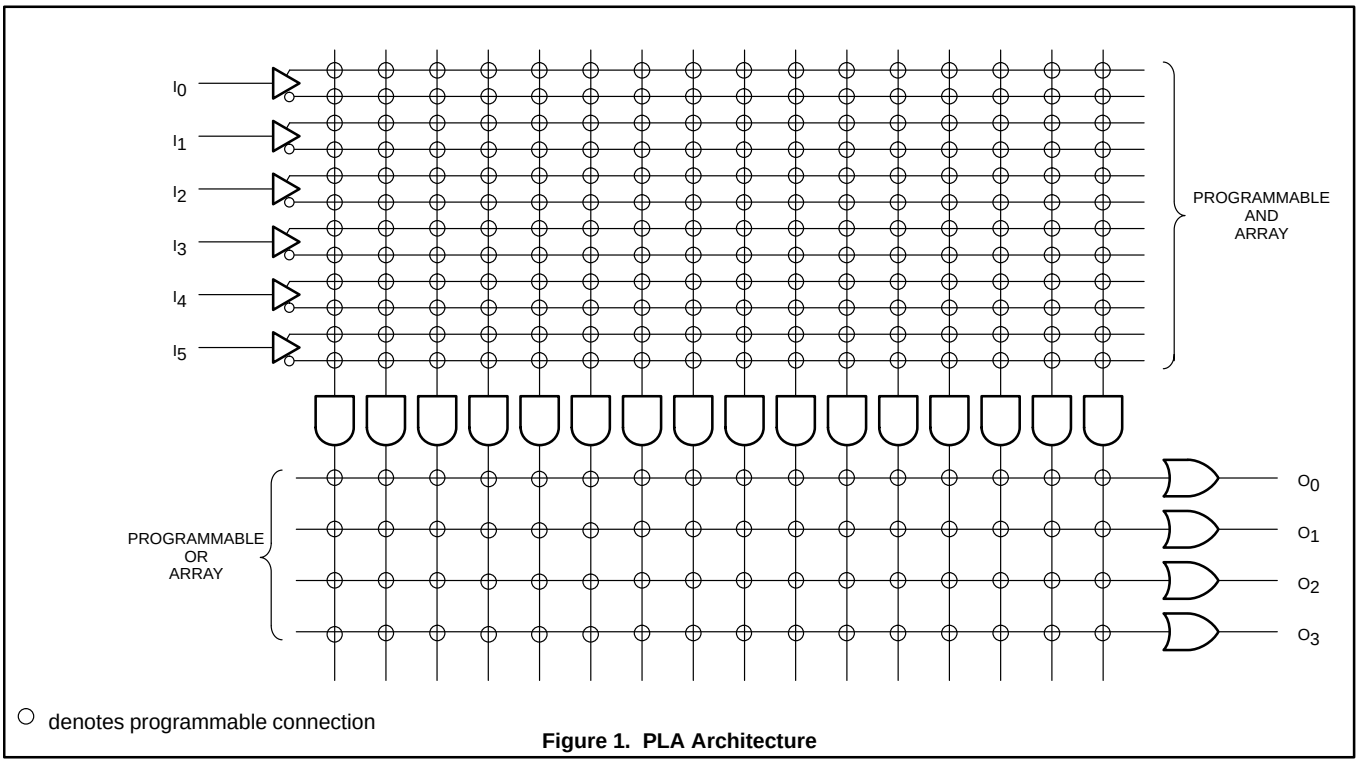

Figure 1. PLA Architecture

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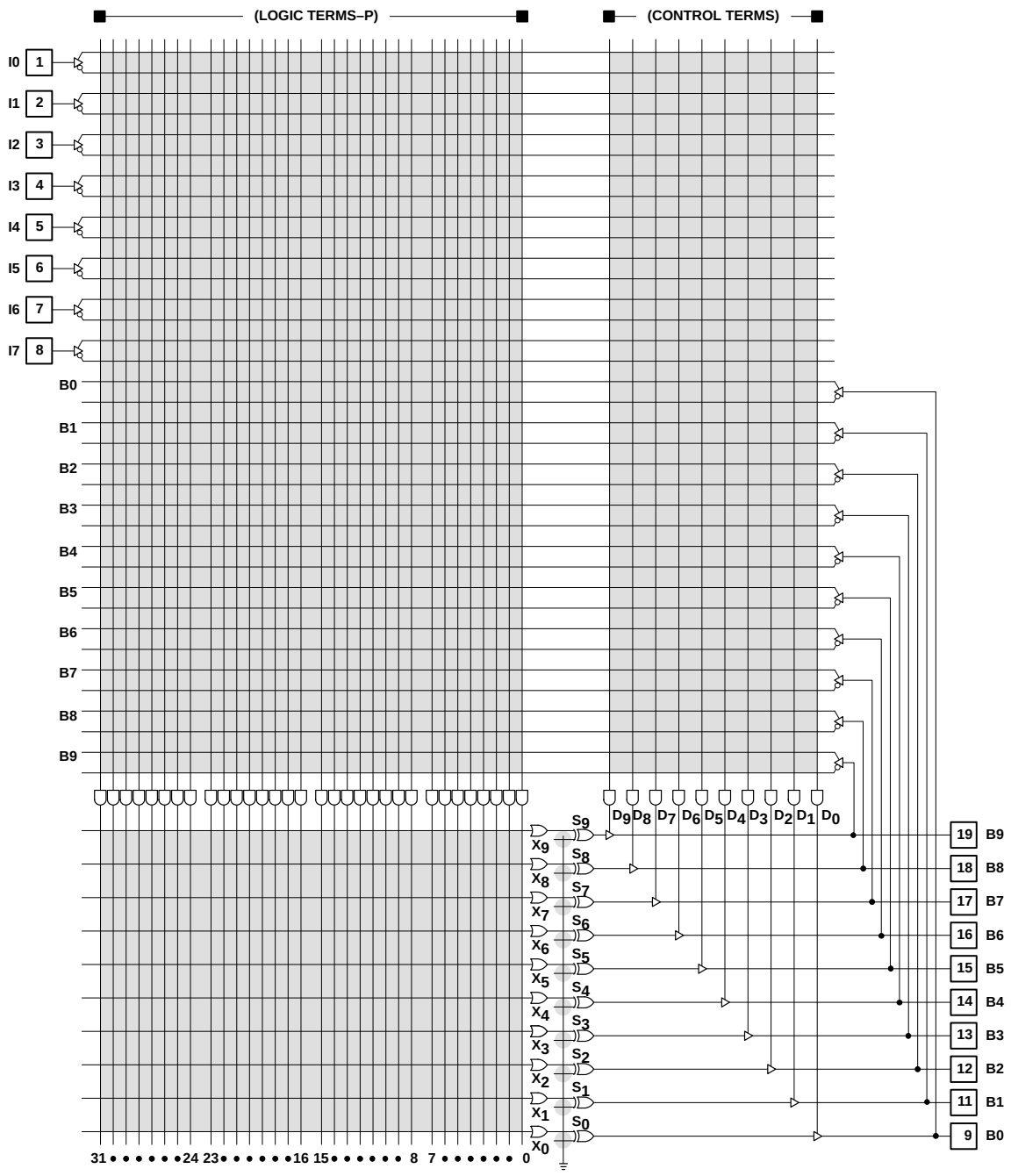

Figure 2. PLUS153

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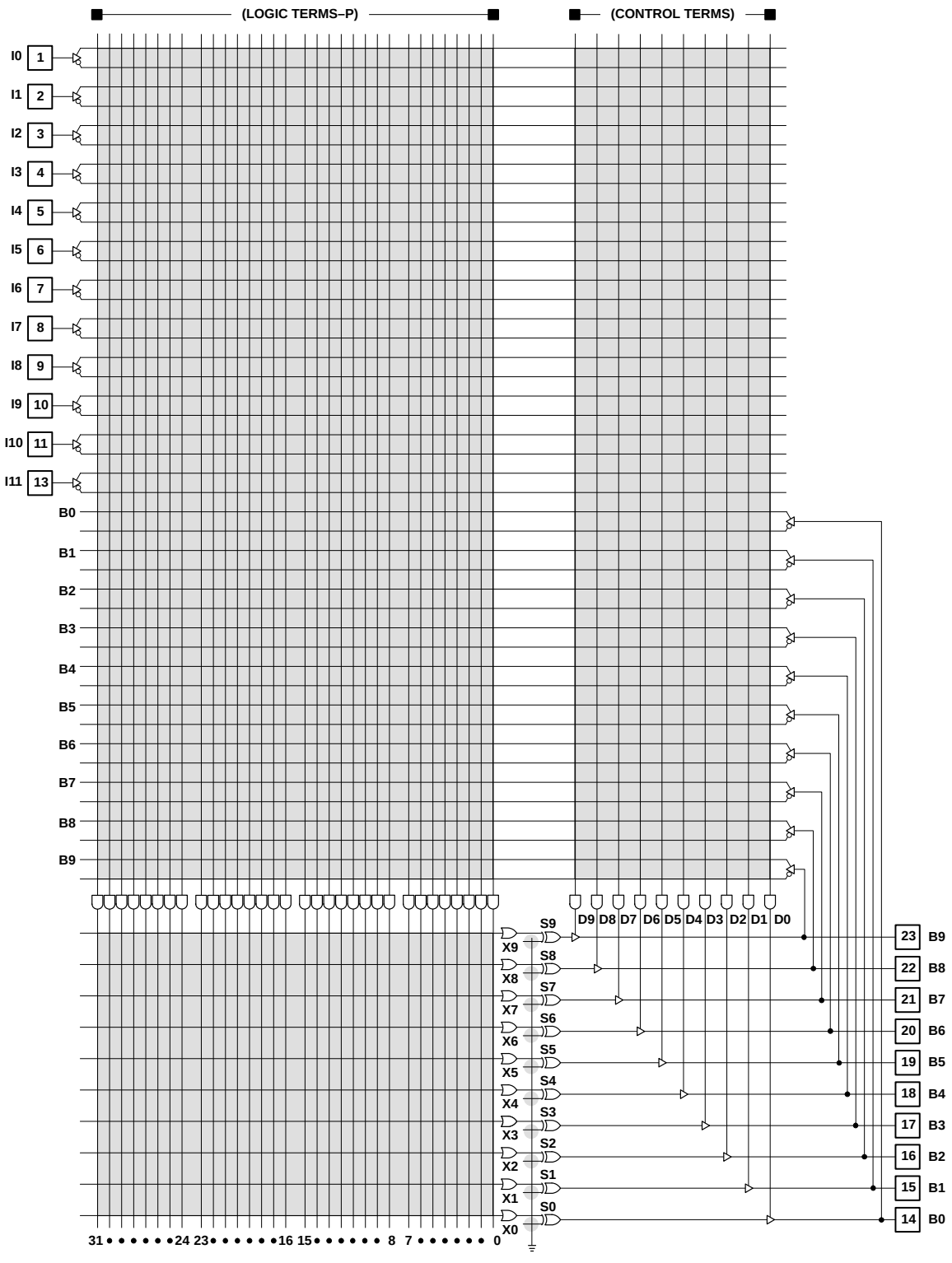

Figure 3. PLUS173