AN996
APPLICATION NOTE

Emulating the Unification of Flash and EEPROM: A Glossary

Many microcontroller applications need both Flash memory and EEPROM. This document summarises the relevant issues and terminology involved in designing efficient systems with the two types of memory.

The subjects are arranged in alphabetical order, in the form of a glossary. Cross-references are shown in **bold face**.

The aim of this document is to highlight the advantages of the M39432: a new memory device that is fabricated by ST using a new dual memory technology called FLASH+™. This device contains 4 Mb of single-voltage Flash memory, and 256 Kb of parallel-access EEPROM, fabricated together on a single chip.

ACCESS TIME

The access time depends on the value of Vcc. Presently, the M39432 is available with a voltage range of 3.0 V to 3.6 V, and an access time of 120 ns at Vcc = 3.0 V. Later versions of the M39432 will have a voltage range of 2.7 to 3.6 V, and an expected access time of 150 ns at 2.7 V.

APPLICATIONS

With FLASH+, dual memories (one Flash memory and one EEPROM) can be fabricated together, thereby reducing the number of memory packages on the PCB, and also reducing the system **Power Consumption**. The technology is, therefore, ideally suited for use in the portable applications market, notably for:

- mobile telephones
- cordless telephones
- electronic notebooks
- hand held meters
- electronic personal assistants
- portable PCs with very long periods away from the mains.

CONCURRENT OPERATION

Write and erase operations in the EEPROM area are managed internally. Although this requires a few milliseconds, the Flash memory remains accessible during this time. In particular, instruction fetches from the Flash memory can continue uninterrupted while the EEPROM area is still updating itself.

EMULATION OF EEPROM

There are three main techniques, as described more fully in *AN931*, for emulating EEPROM in an area of flash memory.

The first method is to use a single bank of flash memory, and to write software that traps addresses aimed at some of the memory sectors, and makes them behave like EEPROM memory. This **External Software Emulation of EEPROM (ESE)** technique, though, suffers from a number of disadvantages. At run-time, accesses to the memory are slowed down enormously by the need to execute the emulation software. The development-time, too, is greatly extended by the need to fine-tune the application software to work with the emulation software.

The second method is to use a device with two banks of flash memory: one to be accessed as flash memory, the other to be accessed as if it were EEPROM. This avoids the need for much, but not all, of the emulation software, and also allows **Read While Write (RWW)** operations, thereby reducing access latency. However, these devices still require some emulation software, for the management of the linked list that allows byte-wise write operations to be emulated in flash memory, and for managing the flash memory sector-erase operation.

The third method is to integrate all of the necessary hardware logic on the chip, and to perform **on-chip hardware emulation of EEPROM (OHE)**. This is the technique that is used in FLASH+ technology, as used for implementing the M39432. The emulated EEPROM, in the Flash memory block, can be accessed as a true EEPROM, with a byte or page write cycle of less than 10 ms.

ERASING THE FLASH MEMORY

The M39432 has a bulk-erase function, to erase the entire 4 Mb of Flash memory in one go. It also has a sector-erase function, to erase selected sectors (of which there are eight, each one 64 Kbytes in size).

EXTERNAL SOFTWARE EMULATION OF EEPROM (ESE)

Flash memory and EEPROM can both be read in a bytewise fashion. Flash memory, though, only allows bytewise writing to bytes that have previously been erased, with the erase operation only being able to be performed in a sectorwise (or devicewise) fashion.

To emulate the bytewise update capability of EEPROM in flash memory, each emulated byte is represented as a linked list within a newly erased sector of flash memory. A second sector is reserved for taking over when the first sector becomes full, and is erased in readiness. Each data byte is accompanied by a two-byte address pointer whose initial value is ‘null’ (erased). Each write operation involves adding an element on to the end of the linked-list of the byte that is being addressed.

ESE is costly in terms of performance. Each read operation in the emulated EEPROM involves finding the first entry for the byte that is being addressed, and then tracing down through the linked-list until the end of the list is reached. The read operation, therefore, can involve a very long sequence of read cycles. The access time of any one byte is proportional to the number of elements in the linked list, and hence to the number of times that the particular byte has been updated.

ESE is also costly in terms of memory. If the linked lists are to be allowed to grow to an average length of five elements between sector erases, and given that every data byte is accompanied by a two-byte pointer, two 16 Kbyte sectors of flash memory can only emulate an EEPROM of a thirtieth of that capacity (just over 1 Kbyte). A further 16 Kbyte of flash memory is occupied by the emulation software. Moreover, around 4 Kbyte of external RAM must also be provided, for caching some of the emulation software.

IDENTIFIERS

The M39432 supports three different identifiers:

- The manufacturer identifier (1 byte, whose value is 20h)
- The Flash memory block identifier (1 byte, whose value is 0E3h)
- The EEPROM block identifier (64 bytes, whose contents are user defined).

A further 64 byte **One-Time-Programmable Row (OTP)** is provided, as described on page 3.

ON-CHIP HARDWARE EMULATION OF EEPROM (OHE)

ST's FLASH+ technology has been developed expressly to support the on-chip hardware **Emulation of EEPROM**. It is used to implement the functionality of multiple memory: two memory devices, one Flash memory and one EEPROM, within a single package.

ONE-TIME-PROGRAMMABLE ROW (OTP)

The M39432 contains a 64 byte OTP row, distinct from the EEPROM block **Identifier** that is described on page 2. The OTP row can be *written once*, using a dedicated multi-byte instruction (see the application note *AN999*, or Table 4 of the M39432 data sheet). This row can be used for any user-defined purpose (such as for the holding of serial numbers, fabrication parameters, and other tags for identification and traceability). The first write operation (whether it be a byte or page write) to the OTP row will freeze the whole row against any further writes.

PACKAGE

The M39432 is packaged in a TSOP40 (10x20 mm) format. The 40-pin arrangement is forward-compatible with (that is, an extended form of) that of the 32-pin M29F040 Flash memory.

The footprint of the M39432 allows significant savings in circuit board space when compared to the alternative of using two discrete packages. An M39432 in a single TSOP40 occupies about 40% less area of PCB than a standard 4 Mb TSOP32 Flash memory device and a 256 Kb TSOP28 EEPROM device.

POWER CONSUMPTION

The M39432 is particularly well suited for portable equipment applications where the power consumption in both operating and stand-by modes are critical parameters. The stand-by current can be as low as 5 µA over the full voltage and temperature ranges when the device is set in the Deep Power-Down mode.

Because the stand-by current is so small, it is largely negligible in calculations of the typical energy consumption of the system. These calculations are dominated by the size of the operating current. For the M39432, though, the operating current is required only during the processor's read and write cycles. For **ESE**, each read or write operation is composed of a very long sequence of microprocessor read and write cycles (possibly several hundred of them in each sequence). The full operating current is therefore required for shorter periods using the M39432 than it is for the ESE technique, and so its energy consumption is proportionately much lower.

PROGRAMMING THE MEMORY

See **Writing to the device**.

PROTECTION

The whole EEPROM area and each Flash sector can be protected against spurious writes. (See **Software Data Protection (SDP)** and **Sector Protection**).

READY/$\overline{\text{BUSY}}$ (R/$\overline{\text{B}}$)

The Ready/$\overline{\text{Busy}}$ output pin (R/$\overline{\text{B}}$) indicates the status of the EEPROM, and operates completely independently of the status of the Flash memory. It is normally held high, and only goes low to indicate when the EEPROM is performing an internal write operation.

READ WHILE WRITE (RWW)

Read While Write is a type of **Concurrent Operation.** It is a feature of the technique for the **Emulation of EEPROM** using a dual-bank of flash memory.

SOFTWARE DATA PROTECTION (SDP)

The EEPROM area of the M39432 can be protected from inadvertent writes. Two specific multi-byte instructions are provided (see the application note *AN999*, or Table 4 of the M39432 data sheet) for protecting and un-protecting the EEPROM. By being composed of a specific sequence of bytes, the probability is reduced of the instruction being issued inadvertently.

The Flash memory area can also be protected, as described for **Sector Protection**.

SECOND SOURCE

The M39432 is compatible with an other competitor devices announced as available on the market for early 1997.

SECTOR PROTECTION

Each Flash sector of the M39432 can be protected separately against programming or erasure. Flash sector protection is programmed with a specific sequence (see Figure 8 and Table 8 of the M39432 data sheet). Any attempt to program or erase a protected Flash sector will be ignored by the device. Reading the Flash protection status allows the user to know which sectors of the Flash area are protected or not protected. Flash sectors can only be unprotected together by using a specific sequence (see Figure 9 and Table 9 of the M39432 data sheet).

The EEPROM area can also be protected, as described under the **Software Data Protection (SDP)** heading.

TECHNOLOGY

FLASH+ technology is implemented using a standard 0.6 micron Flash memory process.

WRITING TO THE DEVICE

The EEPROM area can be written to in a bytewise or pagewise fashion (64 bytes at a time). In either case, two successive operations are performed (internally and automatically): a byte-erase or a page-erase cycle followed by a byte-write or a page-write cycle. This takes less than 10 ms to complete for a page write, and significantly less for a byte write.

The Flash memory area can only be written in a bytewise fashion. This operation uses a dedicated multi-byte instruction (see the application note *AN999*, or Table 4 of the M39432 data sheet), and takes less than 10 µs for each byte.

FURTHER READING

Table 1 lists all the application notes that describe FLASH+ technology and the M39432 memory device.

Table 1. Bibliography of the Application Notes on FLASH+ Technology

Application Note	Content	Title
AN997	Introduction	M39432: a FLASH+™ Multiple Memory Device
AN931	Greater detail	On-Chip Hardware EEPROM Emulation versus Flash Memory Software Solutions
AN996	Glossary	Emulating the Unification of Flash and EEPROM: a Glossary
AN998	Technology	FLASH+™ Multiple Memory Technology
AN999	Drivers	Software Drivers for the M39432 FLASH+™ Multiple Memory

If you have any questions or suggestions concerning the matters raised in this document, please send them to the following electronic mail address:

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Please remember to include your name, company, location, telephone number and fax number.