APPLICATION NOTE

- TDA8752B PLL CALCULATOR - METHOD & SOFTWARE

AN/99057

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SUMMARY

The **TDA8752B** is a triple high-speed 8-bit Analog-to Digital converter with controllable amplifiers and clamps. The **TDA8752B** includes a Phase Locked Loop, controlled via the serial I²c bus, that can be locked on the horizontal line frequency and generates the ADC clock.

This **A**pplication **N**ote describes the method to calculate the **TDA8752B** PLL parameters and describe the using of the **PLL calculator** program, given with this **A**pplication **N**ote, allowing the user to find rapidly the PLL parameters.

1. METHOD TO FIND THE PLL PARAMETERS:

To compute the PLL parameters, you need only two data: the pixel frequency and the clock frequency (corresponding to the horizontal line frequency). Then you must follow the steps in the order: *divider ratio*, *VCO gain* and *loop filter resistance & charge-pump current*.

1.1 DIVIDER RATIO:

To compute the divider ratio, you need the pixel frequency and the horizontal clock frequency. The divider ratio is given by:

$$DR = \frac{FPix}{HSync},$$

where:

Fpix: reference pixel frequency,
Hsync: reference clock frequency.

The divider ratio is programmed on an 11-bit word in VCO, PHASEA and DIVIDER registers. You can see the representative registers in **Table 1**.

REGISTER	BIT DEFINITION							
	MSB							LSB
VCO						Di11	Di10	Di9
PHASEA		Di0						
DIVIDER	Di8	Di7	Di6	Di5	Di4	Di3	Di2	Di1

- Table 1. DR divider ratio programmed in VCO, PHASE A and DIVIDER registers -

To program the divider ratio, you must first program the VCO register, the PHASEA register and finally the DIVIDER register.

1.2 VCO GAIN:

To choose the VCO gain, you need the pixel clock frequency value and refer to the VCO gain control table in the datasheet. The VCO is programmed in the VCO register that you can see in **Table 2**.

REGISTER	BIT DEFINITION							
	MSB							LSB
VCO				Vco1	Vco0			

- Table 2. Vco gain programmed in VCO register -

1.3 LOOP FILTER RESISTANCE & CHARGE-PUMP CURRENT:

The internal resistance for the VCO filter and the charge-pump current are computed together. From the equations of the natural PLL frequency (Fn) and the damping factor(x) given in the datasheet, you can find the relation of the frequency where the gain loop is unitary, according to the internal resistance and the charge-pump current:

$$Fo = \frac{R.Ko.Ip}{2.\pi.DR}.\frac{Cz}{Cp + Cz},$$

where:

R : internal resistance for the filter,
Ko : VCO gain (choosen before),
Ip : charge-pump current,
DR : divider ration (computed before),
Cz, Cp : capacitor of the PLL filter.

To simplify the Fo relation, you can make an approximation given by:

$$Cz \rangle\rangle Cp,$$

hence:

$$\frac{Cz}{Cp + Cz} \approx 1,$$

and:

$$Fo \approx \frac{R.Ko.Ip}{2.\pi.DR}.$$

On the other way (given in the datasheet):

$$Fo \leq 0.15.HSync ,$$

hence:

$$R.Ip \leq \frac{2.\pi.DR.0.15.HSync}{Ko} = LIM .$$

In order to get an optimum setting of the PLL parameters, you must be inferior and as close as possible to LIM. With the charge-pump current and the internal resistance for the VCO filter tables given in the datasheet, you can find the best R.Ip couple inferior and close to LIM.
In the case where there are several couples that are inferior and close to LIM, you must choose the couple that have the damping factor closest to 1. The damping factor, is given by:

$$\xi = \frac{1}{2}.\frac{fn}{fz} ,$$

where:

fn :natural PLL frequency,
fz :loop filter zero frequency,

or:

$$\xi = \pi.R.\sqrt{\frac{Ko.Ip.Cz}{DR}} ,$$

with:

$$fn = \frac{1}{2.\pi}.\sqrt{\frac{Ko.Ip}{(Cz + Cp).N}} ,$$

and:

$$fz = \frac{1}{2.p.R.Cz} .$$

The charge-pump current and the internal resistance is programmed in the CONTROL and VCO registers that you can see on **Table 3**.

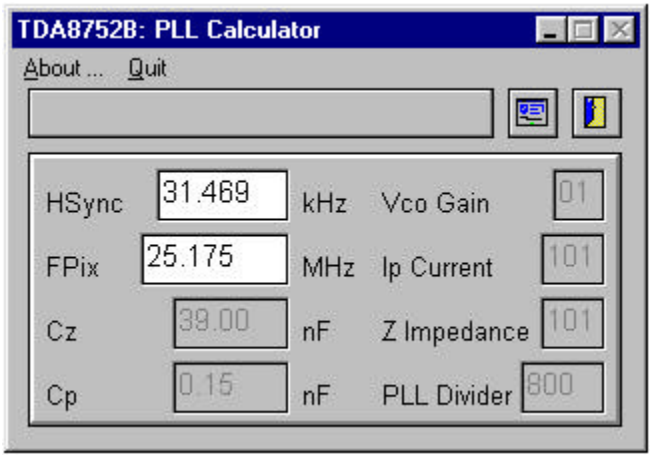
REGISTER	BIT DEFINITION							
	MSB							LSB
CONTROL						Lp2	Lp1	Lp0
VCO	Z2	Z1	Z0					

- Table 3. Charge pump current & internal resistance programmed in CONTROL and VCO registers -

2. PLL CALCULATOR SOFTWARE:

2.1 INSTALLATION:

To install the PLL Calculator software, you need a PC with Windows™ 3.11 or 95. To use this software, you must double click on the **Pllcalc.exe** file and you must have the window represented on **Figure 1** on your computer screen.



- Figure 1. Typical window -

2.2 DESCRIPTION:

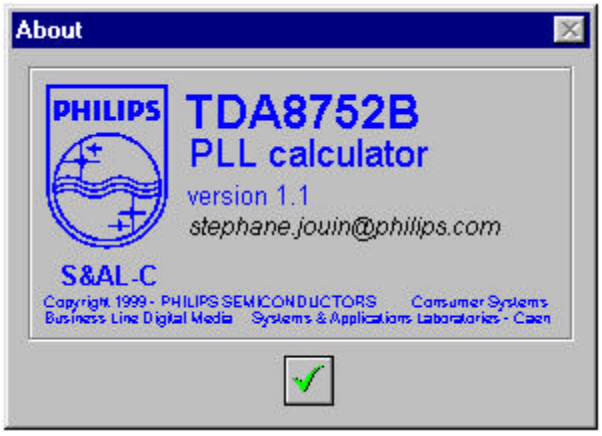
Only two edit windows (25.175) are used to compute all PLL registers. These edit windows allow to enter the Hsync value, corresponding to the horizontal line frequency, and the Fpix value corresponding to the pixel clock frequency.

In grey edit windows(101), you can see the Vco gain, the Ip current and the Z impedance (R) values in binary word, the PLL divider(DR) computed from Hsync and Fpix values and the values of Cz and Cp capacitors used.

This software, indicating the Cz and Cp capacitor values, is valid for the TDA8752B device only.

2.3 GENERAL USE:

The **About …** menu gives some information about the program and the program support. A view of this window is given on **Figure 2**.



- Figure 2. About window -

The **Quit** menu allows to quit the program.

2.4 SPEED BUTTON:

In the window, two speed buttons are available to access rapidly to some functions:

 accesses to the about window.

 allows to quit the program.