APPLICATION NOTE

Application of the UBA2050(A)/51(A;C) One-Chip Telephone ICs

AN99047

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Abstract

The UBA2050, UBA2050A, UBA2051, UBA2051A and UBA2051C are telephony ICs for application in line powered electronic telephone sets. They offer all line interface functions, speech functions, dialling and ringer functions. They perform the interface between the telephone line and transducers such as microphone capsule, earpiece and buzzers. The transmission part is in the range of the TEA106x- and TEA111x-family. The ICs contain also a dialler circuit for DTMF and pulse dialling. An integrated supply V_{DD} with internal voltage regulator supplies the dialler and is available as supply point for external use.

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Summary

This report provides application support for designing electronic telephone sets with the One-chip telephone ICs UBA2050(A) and UBA2051(A;C) with speech, dialling and ringer functions. A V_{DD} supply point with internal voltage stabilizer is integrated in these ICs.

A detailed description of the several circuit blocks of these ICs as well as the possible settings to adjust the DC, transmission characteristics and dialler/ringer arrangements are given. EMC aspects and protection are discussed also. Furthermore an application example of UBA2050(A)/51(A;C) is given and some measurement results of this application are presented.

Two demonstration boards, one prepared for UBA2050(A) and one prepared for UBA2051(A), can also be used for a basic telephone. The advantage is one printed circuit board for several types of telephones to meet PTT requirements in several countries.

APPENDIX 1 gives a list of abbreviations and definitions used in this report, APPENDIX 2 the diagrams of an application example and APPENDIX 3 the dialling procedures of the UBA2050(A)/51(A;C).

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1. INTRODUCTION

The UBA2050, UBA2050A, UBA2051, UBA2051A and UBA2051C (called in general: UBA2050(A)/51(A;C)) offer all speech and line interface functions, dialling and ringer functions required in electronic telephone sets. They perform the interface between the telephone line and transducers such as microphone capsule, earpiece and buzzers. The transmission part is in the range of the TEA106x- and TEA111x-family. The ICs contain also a dialler circuit for DTMF and pulse dialling. An integrated supply V_{DD} with internal voltage regulator supplies the dialler and is available as supply point for external use.

This report gives a detailed description of the UBA2050(A)/51(A;C) which starts by the block diagram for these ICs and by discussing every detail of the sub-blocks in chapters 2 and 3. Chapter 4 describes an application example with its measurement results e.g. start-up and line disconnect behaviour. Also EMC behaviour is taken into account as described in chapter 5. Hints for printed circuit diagram are given in chapter 6. The application cookbook in chapter 7 helps the developer to adjust the application.

The UBA2051(A) is focused on in this report. This IC contains extra features compared to the UBA2050(A). Also some parts supported by the UBA2050(A) will be described.

NOTE: The values of parameters given in this application note are as accurate as possible, but please, refer to the latest product specification for the latest ones.

2. BLOCK DIAGRAM

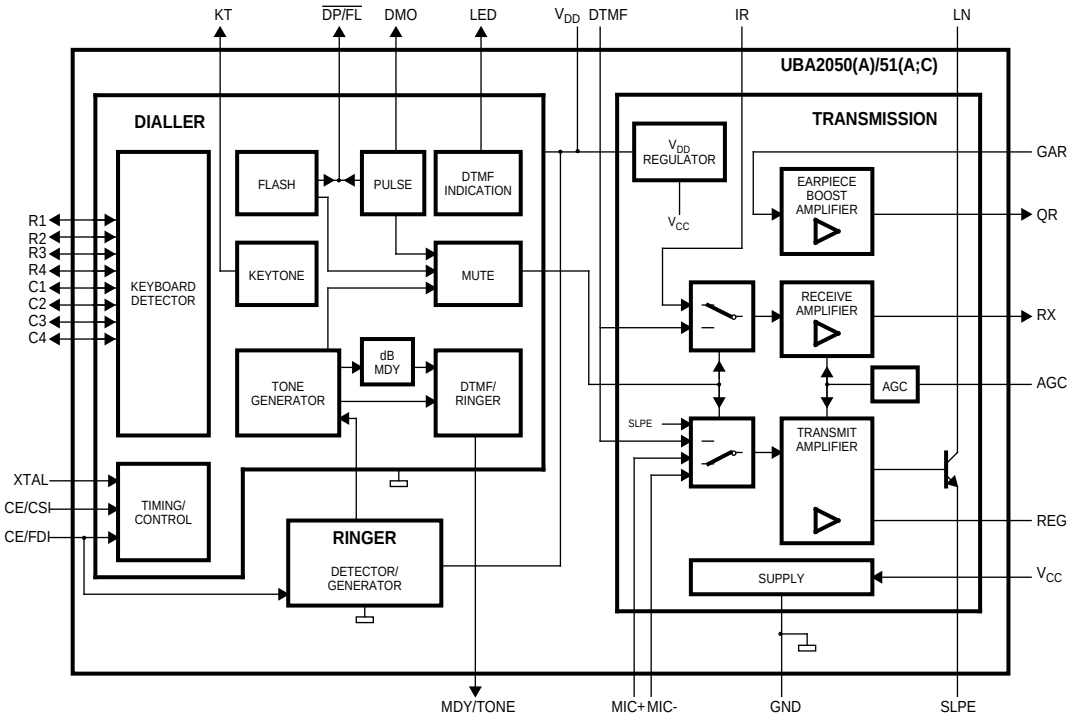

Fig.1 Block diagram of UBA2050(A)/51(A;C)

Refer to Fig.2 and TABLE 1 concerning pinning of the UBA2050(A) and UBA2051(A;C)

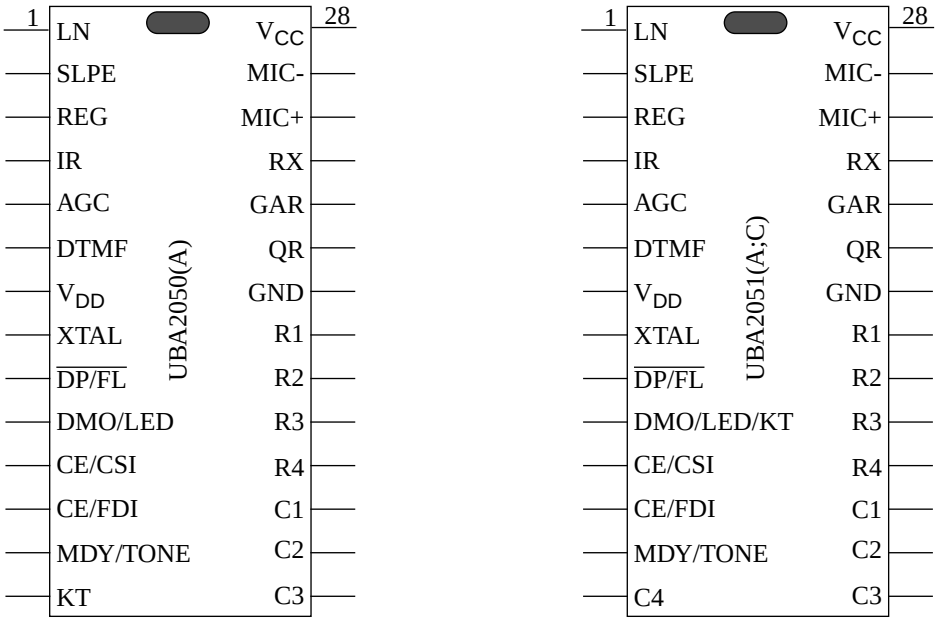

Fig.2 UBA2050(A)/51(A;C) pinning

TABLE 1 Pinning of UBA2050(A)/51(A;C)

Pin	Name	Description
1	LN	positive line terminal
2	SLPE	slope (DC resistance) adjustment
3	REG	line voltage regulator decoupling
4	IR	receiving amplifier input
5	AGC	automatic gain control / line-loss compensation
6	DTMF	DTMF transmit input
7	V_{DD}	stabilized dialler/ringer part supply
8	XTAL	oscillator input
9	$\overline{DP/FL}$	dial pulse / flash output (active LOW)
10	DMO	dial mode output (UBA2050/51)
	LED	DTMF mode indication output (active HIGH) (UBA2050A/51A)
	KT	keytone output (UBA2051C)
11	CE/CSI	chip enable / cradle switch input
12	CE/FDI	chip enable / frequency discrimination input
13	MDY/TONE	melody (ringer) output / DTMF generator output
14	KT	keytone output (UBA2050(A))
	C4	keyboard input / output (UBA2051(A;C))

Pin	Name	Description
15	C3	keyboard input / output
16	C2	keyboard input / output
17	C1	keyboard input / output
18	R4	keyboard input / output
19	R3	keyboard input / output
20	R2	keyboard input / output
21	R1	keyboard input / output
22	GND	negative line terminal
23	QR	earpiece amplifier output
24	GAR	gain adjustment earpiece amplifier
25	RX	receive amplifier output
26	MIC+	non-inverting microphone amplifier input
27	MIC–	inverting microphone amplifier input
28	V_{CC}	supply for transmission part and peripherals

The three main functions of Fig.1, transmission, dialler and ringer, are briefly described. The given values are typical values at nominal conditions. The gain factors of the transmit and receive amplifier are internally fixed.

Consult data sheet [1] if necessary.

TRANSMISSION PART

The transmission part contains the V_{DD} regulator, receive amplifier, earpiece boost amplifier, transmit amplifier combined with the LN-SLPE voltage stabilizer, AGC circuit, DTMF input attenuator and supply part.

V_{DD} regulator: Delivers a stabilized voltage for the dialler in transmission mode as well as in ringer mode. It consumes a fixed current of 4.5 mA from pin LN. Output V_{DD} follows the DC voltage at pin LN up to V_{DD} = 3.3 V.

The V_{DD} stabilizer functions as a shunt stabilizer in ringer mode to keep V_{DD} at 3.3 V. The input current into pin V_{DD} is delivered by the ringing signal via the ringer stage. The voltage stabilizer (LN-SLPE) is not supplied in this mode; V_{LN} is about 0 V.

Receive amplifier: Transfers the receive signal from input IR to output RX with a voltage gain of 33.4 dB. Output RX drives the earpiece boost amplifier. The input impedance is 20 kΩ.

The DTMF tones applied to the DTMF amplifier input are attenuated and coupled into the receive amplifier during DTMF dialling.

Earpiece boost amplifier: The receive signal from the receive amplifier is coupled into the earpiece boost amplifier which drives the earpiece. The (initial) gain from RX output to QR output may be set between 0 dB and −14 dB by means of the resistors between RX and GAR and between GAR and QR. By adaptating the resistor network the amplifier offers a gain boost from 0 dB to +12 dB, relative to the initial gain.

Transmit amplifier: Inputs are MIC+ and MIC- with an input impedance of 64 kΩ (2 x 32 kΩ). The outputs of the transmit amplifier are LN and SLPE which modulate the line current, flowing from LN to SLPE. The DTMF signal is coupled into the transmit amplifier during DTMF dialling while the MIC+ and MIC− inputs are disabled.

The microphone gain from the MIC inputs to LN is 44.2 dB at R_{SLPE} = 20 Ω and $Z_{SET} = Z_{line}$ = 600 Ω. The microphone gain is controlled by the AGC block. The DTMF gain from DTMF to LN is 26 dB.

LN-SLPE voltage stabilizer: Stabilizes $V_{ref} = V_{LN\text{-}SLPE}$ at 4.15 V. V_{ref} can be increased by means of a resistor R_{VA} connected between REG and SLPE and V_{ref} can be decreased by means of a resistor R_{VA} connected between REG and LN. The stabilizer is decoupled by C_{REG}. An electronic coil function is realised between LN and GND which has an equivalent inductance value of $L_{EQ} = C_{REG} \times R_{SLPE} \times R_P$. The internal resistance R_P is ≥17.5 kΩ.

The preferred value of R_{SLPE} = 20 Ω. Changing R_{SLPE} will affect DC settings, AGC characteristics, transmit, receive and sidetone characteristics and BRL at lower audio frequencies.

In the audio frequency range the impedance of the IC between LN and GND is much more than 600 Ω. The set impedance Z_{SET}, defined as the impedance between the line terminals A/B and B/A, has to be made by means of an external network R_{CC} (resistor or complex network) connected between LN and capacitively connected to GND.

AGC: The AGC function controls the gain of the receive and transmit amplifier as a function of line current when the AGC pin is connected to GND (directly or via an external R_{AGC} resistor) to compensate the line losses.

DTMF input attenuator: Is required to adapt DTMF levels to different country requirements. The DTMF gain from DTMF to LN measures 26 dB.

V_{CC} supply: Provides a supply for the internal circuitry of the transmission part from pin V_{CC}. This voltage supply is derived from the LN voltage by means of a low pass filter. This supply point may also be used to supply external circuits e.g. electret microphone. Internal current consumption is 1.25 mA.

DIALLER PART

The dialler part takes care of the system control, system settings and the generation and detection of various signals. The dialler offers a 32-digit Last Number Redial (LNR). Only UBA2051(A;C) supports 13 repertory numbers (3 direct + 10 indirect) of 21 digits.

Timing/control: Consists of a resonator-controlled on-chip oscillator, internal reset circuit and state determinator. A 3.579545 MHz quartz-crystal or ceramic resonator has to be connected to pin XTAL. The oscillator starts when V_{DD} reaches the operation voltage level with CE/CSI = HIGH or CE/FDI = HIGH.

The reset circuit monitors the power supply for low voltage level and determines whether an internal reset signal will be generated to avoid unknown state of the circuit.

Depending on the status of pins CE/CSI and CE/FDI any state will be entered or left:
STAND-BY (on-hook), ON-LINE (off-hook) or RINGER state. When both CE/CSI and CE/FDI are LOW, an internal reset signal will be generated.

Keyboard detector: Scans the keyboard of max. 20 keys. The keyboard is connected to pins C1-C4 and R1-R4. Pin C4 is only available with the UBA2051(A;C). A detected key-press results in a key operation. Multiple pressed keys at the same time will not be detected. The resistors options will be read from pins C1-C3 and R1-R4 at start-up by the keyboard detector.

Keytone generator: Produces a keytone of 597 Hz with a duration of 30 ms when a key entry becomes valid. A keytone is available with the UBA2050(A) and the UBA2051C on the KT output.

Pulse dialler: Generates a number of pulses corresponding with the pressed key ([0] to [9]), except for key [0] which is characterized by 10 pulses, to drive the external line current interrupter. Pulses are present on $\overline{\text{DP/FL}}$ output.

The DMO output is activated during pulse dialling to enable external hardware to decrease the DC voltage over the telephone line during the ‘make periods’. This output is only intended for the UBA205x and not for the UBA205x(A;C).

Flash generator: Makes the $\overline{\text{DP/FL}}$ output LOW for a specific time during flash operation. The flash time can be set by the resistor options.

Mute controller: Mutes the transmit and receive amplifiers of the transmission part during pulse or DTMF dialling as well as flash operation.

DTMF indication (LED driver): Indicates the DTMF dialling mode by making the LED output HIGH. In pulse dialling mode and during access pause operation the output remains LOW. Only UBA205xA offers this feature.

Tone generator: Generates two kind of signals: DTMF (Tone) signals during DTMF dialling or programmable melody (MDY) in RINGER state which are transmitted by the DTMF/Ringer multiplexer and available on the MDY/TONE output.

During DTMF dialling, two simultaneously tones are generated. The MDY/TONE output has to be connected to the DTMF input of the transmission part via an external attenuation network.

In RINGER state, a (square-wave) ringer melody will be produced. The ringer melody has to be supplied to the ringer output stage. Melodies can be selected using keys [1] to [4].

DTMF/Ringer multiplexer: Selects one of two generated signals to the MDY/TONE output (melody signal (MDY) or tone signal (TONE)). It depends on following states: RINGER state (using MDY signal) and ON-LINE state (using TONE signal).

dB MDY attenuator: Attenuates the generated melody from the tone generator. Four ringer volume levels are supported when using keys [5] to [8]. They correspond to the attenuation values of: -18 dB, -12 dB, -6 dB and 0 dB.

RINGER PART

The ringer part contains the ringer detector, also named ringer discriminator, and melody generator. The ringer will only be activated when CE/CSI = LOW, CE/FDI is provided with ringer signal and the dialler is in STAND-BY state. The frequency discriminator evaluates and checks the frequency (≥13 Hz) of the incoming ringer signal. A ringer melody with 3 tones in sequence will be generated after detection and validation of the ringer signal.

3. DESCRIPTION OF THE IC

Basic Application of the UBA2051(A)

The basic application of the UBA2051(A) is shown in Fig.3. All the components names refer to the basic application of the IC shown in Fig.51 and Fig.52. The circuit diagram of a demonstration board OM5840[3] is considered as the basic application. It contains all features except keytone that the UBA2050(A)and UBA2051C can offer.

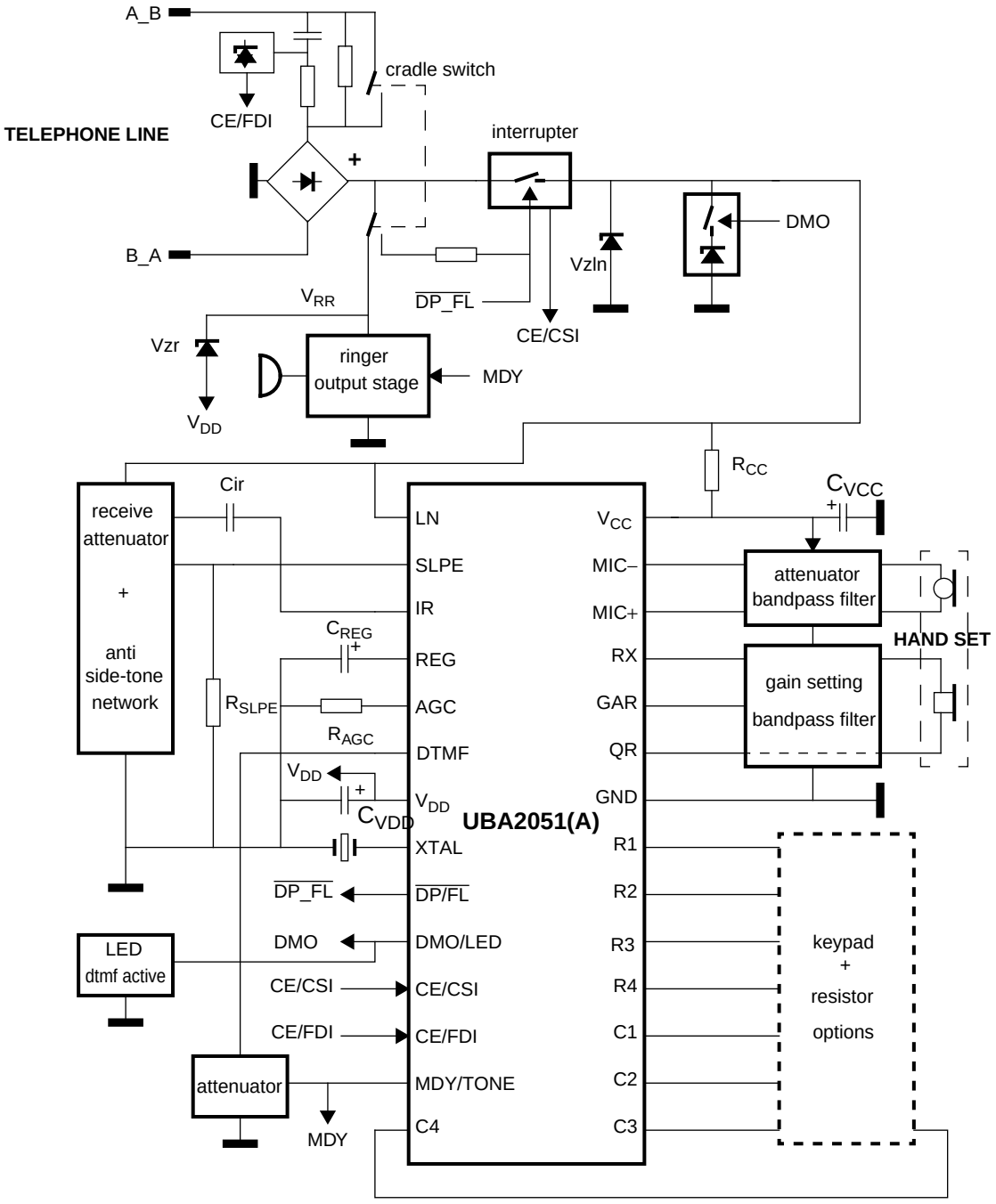

Fig.3 Principle of basic application of Fig.51 and Fig.52

3.1 TRANSMISSION PART

All the curves shown in this section result from measurement of typical samples using the schematic shown in Fig.3.

3.1.1 DC characteristics and supply blocks

Principle of operation

The UBA2050(A)/51(A;C) generates a stabilized voltage (called V_{ref}) between pins LN and SLPE. This reference voltage, typically 4.15 V, is temperature compensated. The voltage at pin REG is used by the internal regulator to generate the stabilized V_{ref} voltage and is decoupled by a capacitor C_{REG} connected to GND.

For transmission, the UBA2050(A)/51(A;C) must have a low resistance to the DC current and a high impedance to speech signals. The C_{REG} capacitor in combination with R_P and R_{SLPE} realizes an equivalent (internal) inductance between LN and GND resulting in a set impedance of R_{SLPE} at DC up to an approximation of the external network between LN and V_{CC} (R_{CC} of Fig.4) at audio frequencies.

The DC voltage at pin SLPE is proportional to the line current with an offset due to the V_{DD} supply current.

This general configuration is shown in Fig.4.

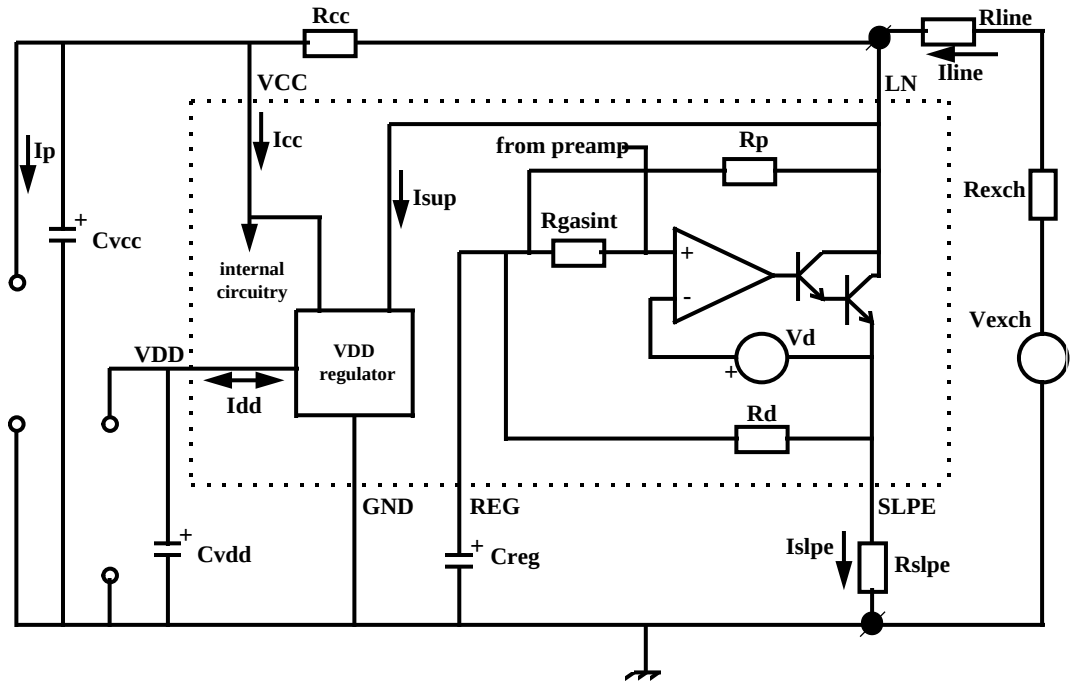

Fig.4 Supply configuration

The IC regulates the line voltage between pins LN and SLPE. The voltage on pin LN can be calculated as:

$V_{LN} = V_{ref} + R_{SLPE} \times I_{SLPE}$

$I_{SLPE} = I_{line} - I_{SUP} - I_{CC} - I_P$

I_{line} = line current

I_{CC}= current consumption of the IC

I_P = supply current for peripherals connected on V_{CC}

I_{SUP} = current consumed by the V_{DD} regulator

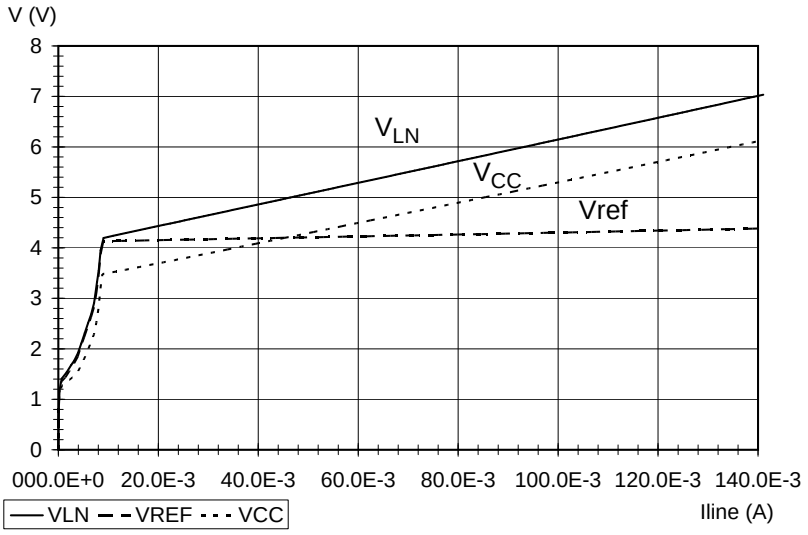

Fig.5 V_{LN}, V_{CC} and V_{ref} versus line current

The DC line current I_{line} flowing into the telephone set is determined by V_{exch}, R_{exch}, R_{line} and the voltage across the telephone set including diode bridge. The voltages V_{LN}, V_{CC} and the V_{ref} versus the line current are shown in Fig.5.

Below a threshold of the line current I_{th} (typically 8 mA), V_{ref} is automatically adjusted to a lower value (down to an absolute minimum voltage of 1.45 V). This means that more sets can operate in parallel.

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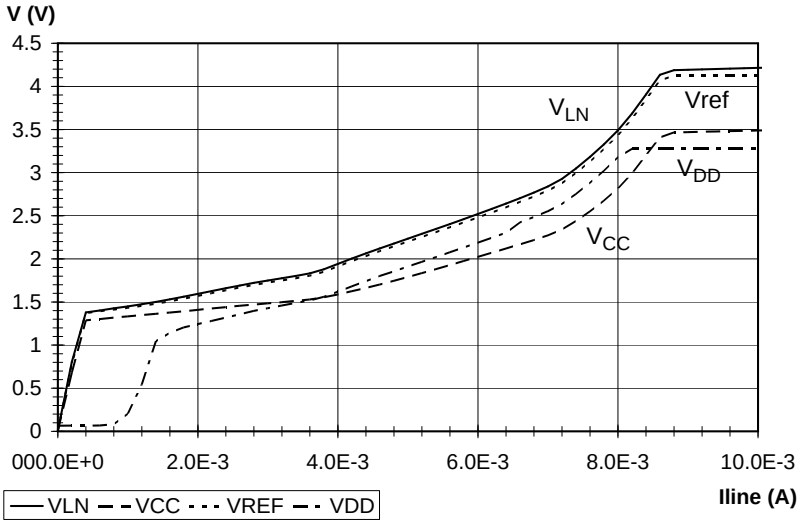

Fig.6 Low voltage behaviour

For line currents below this threshold current, the UBA2050(A)/51(A;C) has reduced sending and receiving performances, moreover the voltage of V_{DD} and the current I_{SUP} are reduced. This is called the low voltage area as indicated in Fig.6

The internal circuitry of the UBA2050(A)/51(A;C) is supplied from pin V_{CC} which is derived from the line voltage by means of a resistor (R_{CC}). Due to the transmission and receive signals on LN, this supply point V_{CC} must be decoupled by a capacitor (C_{VCC}). Fig.7 shows the IC current consumption (I_{CC}) as a function of the V_{CC} supply voltage.

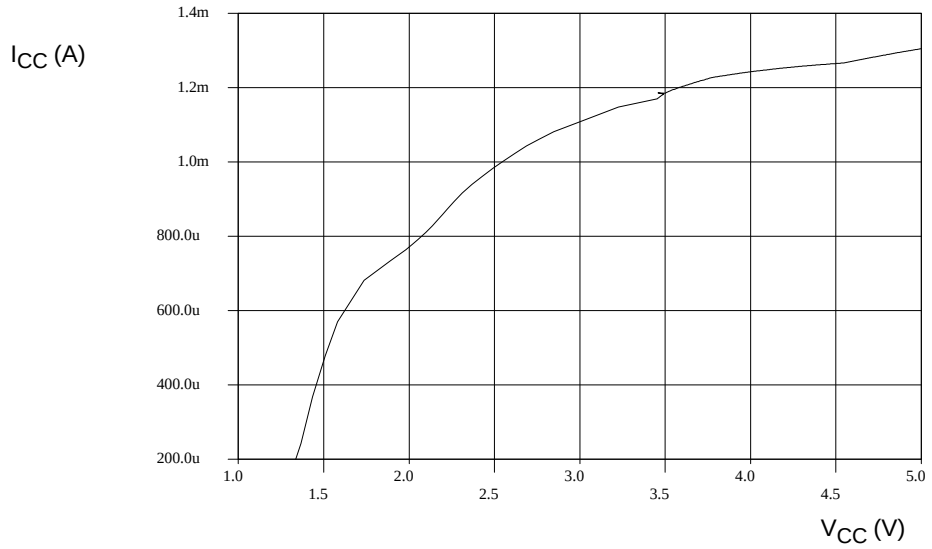

Fig.7 Current consumption I_{CC} of the transmission part versus V_{CC}

Adjustments and performances

The reference voltage, V_{ref}, can be adjusted by means of an external resistor Rva. It can be increased by connecting the Rva resistor between pins REG and SLPE, or decreased by connecting the Rva resistor between pins REG and LN (see Fig.8). Reduction of the line voltage by Rva reduces the peripheral supply capabilities: V_{LN} must be at least 0.35 V higher than V_{DD} (V_{DD} = 3.3 V typically). To ensure correct operation, it is not advised to adjust V_{ref} to a value lower than 3 V or higher than 7 V (the maximum operating voltage of 12 V must be guaranteed by the application as well as the safe operating temperature of the IC). These adjustments will slightly affect a few parameters: there will be a small change in the temperature coefficient of V_{ref} and a slight increase in the spread of this voltage reference due to matching between internal and external resistors. Furthermore, the Rva resistor connected between REG and LN will slightly affect the set impedance (see section “set impedance”).

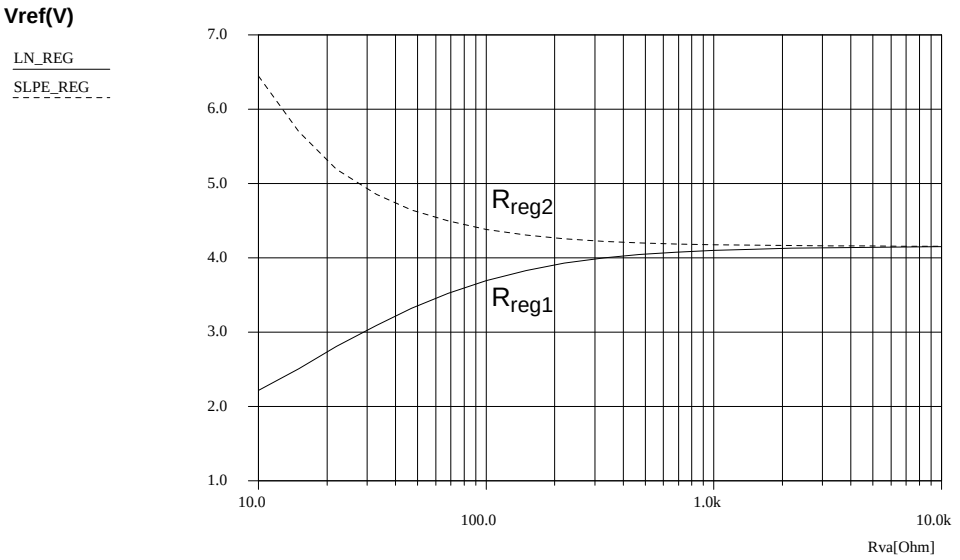

Fig.8 Adjustment of V_{ref} by means of R_{reg2} and R_{reg1}

The DC slope of the voltage on pin LN is influenced by the R_{SLPE} resistor. The preferred value of R_{SLPE} is 20 Ω. Any change of R_{SLPE} will affect more than the DC characteristics, it also influences the gains, the AGC characteristics, the maximum output swing on the line and the low voltage area threshold I_{th}.

3.1.2 Supply V_{CC}

Fig.9 indicates the V_{CC} supply, the current switch and the V_{DD} voltage stabilizer.

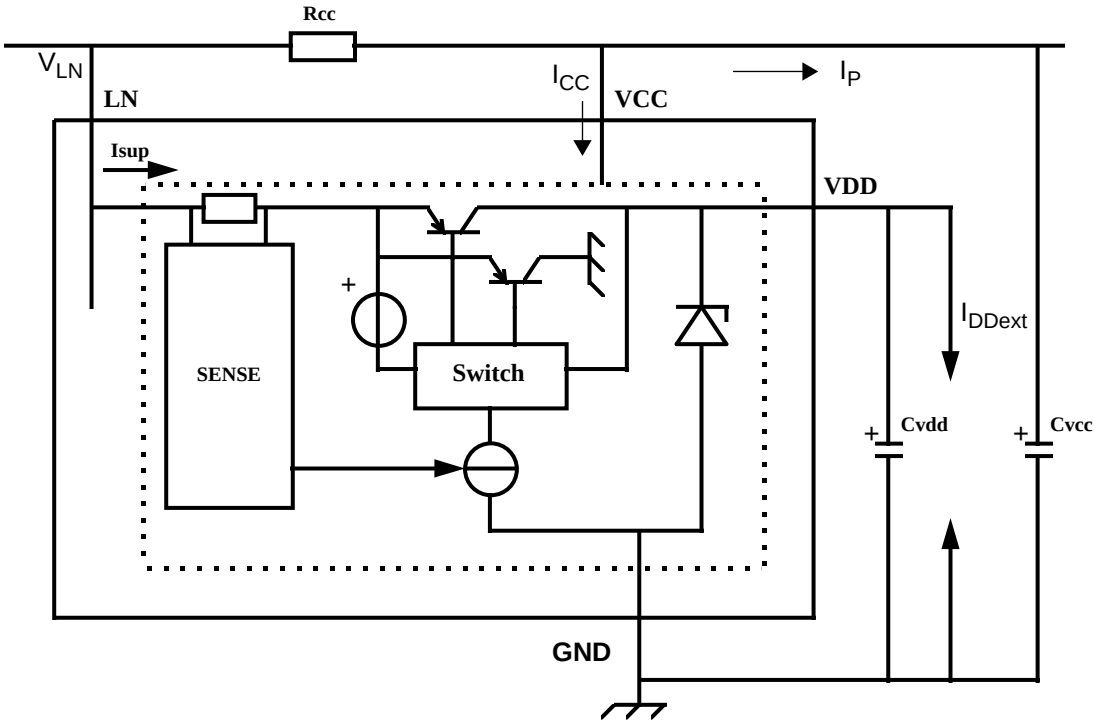

Fig.9 Supply configuration

Principle of operation

The voltage at pin V_{CC}, with GND as reference, is the supply voltage of the internal circuitry of the UBA2050(A)/51(A). V_{CC} is derivated from V_{LN}, which contains the line signal, and is (low pass) filtered by R_{CC} and C_{VCC}. As mall current can be drawn from V_{CC} to supply peripheral circuits. However, due to the high internal resistance of this supply point the supply possibilities are rather limited.

The internal current consumption of the UBA2050(A)/51(A) depends on a static part I_{CC}, as shown in Fig.7, and a dynamic part I_{rec} consumed by the earpiece amplifier to drive the earpiece. I_{rec} depends on the signal swing across the earpiece and the impedance of the earpiece mainly.

Depending on the setting of V_{LN} and the resistance of R_{CC}, a small current I_P is available for external use, taking into account a V_{CC} minimum of 2 V and a minimum voltage difference between V_{CC} and SLPE of 1.7 V. Both values are minimum working voltages of the IC.

The available current I_P can be approximated as follows:

$V_{CC} = V_{LN} - (I_{CC} + I_P + I_{rec}) \times R_{CC}$

with $I_{rec} = vqr / (pi \times R_L)$

V_{LN} : DC voltage at LN, adjustable by means of Vref; see Fig.8. Think about country requirements (DC mask)
R_{CC} : DC resistance of the network between LN and V_{CC} to justify the set impedance

vqr : peak voltage across the earpiece
R_L : impedance of the earpiece

$I_{P(max)} = [V_{LN} - V_{CC(min)} - (I_{CC} + I_{rec(max)}) \times R_{CC}] / R_{CC}$

At nominal settings (Vref = 4.15 V):

V_{LN} = 4.35 V at I_{line} = 15 mA and 6.2 V at I_{line} = 100 mA
$V_{CC(min)}$ = 2 V at I_{line} = 15 mA and 3.7 V at I_{line} = 100 mA
$I_{rec(max)}$ is 1.1 mA at vqr = 537 mV-peak across an earpiece (R_L) of 150 Ω.
vqr is based on the specified $V_{QR(max)}$ at 150 Ω load and a continuously signal across the earpiece

The maximum available current I_P = 1.3 mA using a fixed value of 1.4 mA for I_{CC}.
Advised is a maximum load current from V_{CC}, for external use, of 1 mA.

Adjustments and performances

As the impedance connected between LN and V_{CC} also determines the set impedance, the easiest way to increase the current capability of the supply point V_{CC} is to increase the reference voltage V_{ref}, and V_{LN}, by connecting a resistor Rva between pins REG and SLPE (see 3.1.1). However, refer to country requirements (DC masks) about the possibility to increase V_{LN} and, please, take into account that:

- V_{CC} is a weak supply point for load currents of less than 1 mA
- the minimum V_{CC} supply level is about 2.0 V and
- the difference between V_{CC} and V_{SLPE} has to be more than 1.7 V over the whole line current range

3.1.3 Supply V_{DD}

Principle of operation

V_{DD} is a 3.3 V regulated supply for the internal dialler and may be used to supply external circuitry. The dependency of V_{DD} from the line voltage V_{LN}, as a function of line current, is as follow, see also Fig.10:

- $V_{LN} < 1.5$ V :$V_{DD} = 0$ V
- 1.5 V $< V_{LN} < 3.6$ V :$V_{DD} = V_{LN} - 0.35$ V
- $V_{LN} > 3.6$ V :$V_{DD} = 3.3$ V

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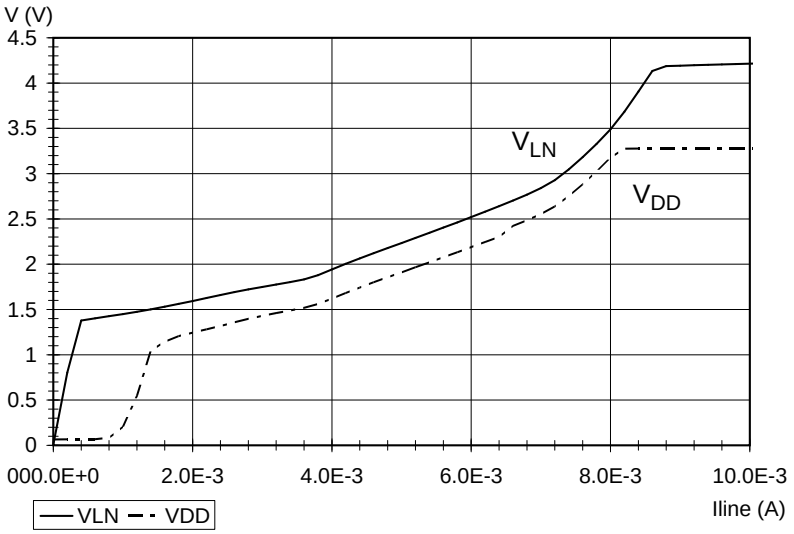


Fig.10 V_{DD} and V_{LN} versus line current

As indicated in Fig.9, two PNP transistors conduct the line current either to V_{DD} or to GND: when the voltage on LN is higher than V_{DD} + 0.2 V the current supplies V_{DD}, when the voltage on LN is lower than V_{DD} the line current is rerouted to GND and when the voltage on LN is between V_{DD} and V_{DD} + 0.2 V both transistors are conducting in order to minimize distortion.

When V_{DD} equals 3.3 V, a constant current I_{SUP} (4.5 mA typically at $I_{line} > 11$ mA) is sunk from LN. This constant current doesn't affect the return loss and its value is taken into account for the AGC characteristic.

The maximum current I_{DD} drawn from V_{DD}, to supply external circuitry, depends on the operation mode. In speech mode the maximum current is available (2.6 mA maximum) while in DTMF mode less current is available (1.9 mA maximum) because of the enlarged current consumption of the dialler.
In pulse dialling mode the maximum output current is reduced because of the interrupted input current I_{SUP} in correlation with V_{LN}.

In ringer mode, V_{DD} works as a shunt regulator at 3.3 V; the shunt regulator is able to sink up to 75 mA between V_{DD} and GND as shown in Fig.11.

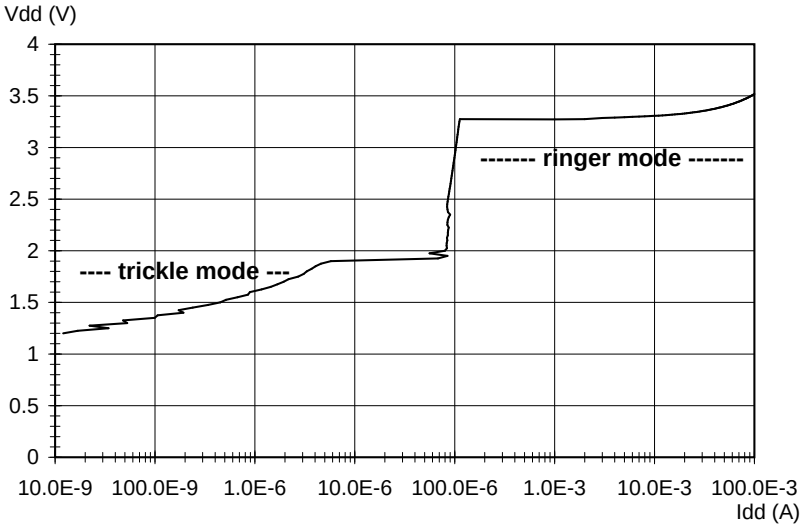


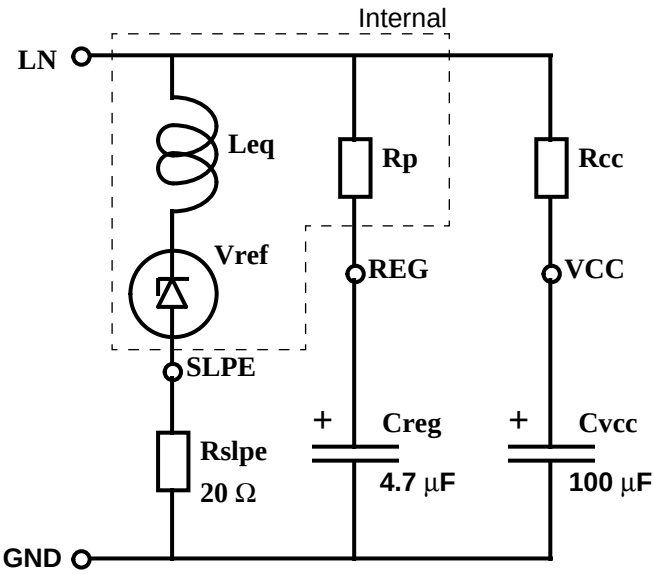
Fig.11 V_{DD} versus input current in trickle mode as well as in ringer mode

In trickle mode (on-hook condition) the IC has to be supplied from the line via a high ohmic resistor to save memory contents. In this mode the current consumption of the shunt regulator has to be reduced to a minimum. The maximum (specified) current consumption at V_{DD} = 1.2 V is 300 nA. The current consumption of the shunt stabilizer in trickle mode (V_{DD} < 2V) is also shown in Fig.11.

3.1.4 Set impedance

Principle of operation

The UBA2050(A)/51(A;C) behaves like an equivalent inductance that presents a low impedance to DC (R_{SLPE}) and a high impedance (R_P) to speech signals. R_P is an integrated resistance in the order of 17.5 kΩ +/-15%. It is in parallel with the external RC realized by R_{CC} and C_{VCC}. Thus, in the audio frequency range, the set impedance (between LN and GND) is mainly determined by the R_{CC} resistor. Fig.12 shows an equivalent schematic for the set impedance.



Leq = Cregx Rslpe x Rp
Rp = internal resistor

Fig.12 Equivalent set impedance

Adjustments and performances

When decreasing the reference voltage V_{ref} by a resistor connected between LN and REG, this resistor is in parallel with R_P (see Fig.12) so, slightly modifying the impedance.

If complex set impedance is required, the R_{CC} resistor has to be replaced by a complex network (see Fig.52: $R_{set1} + R_{set2} // C_{set}$). The DC resistance, which influences the value of V_{CC}, becomes $R_{set1} + R_{set2}$.

3.1.5 Microphone amplifier

Principle of operation

Fig.13 shows the block diagram of the microphone amplifier.

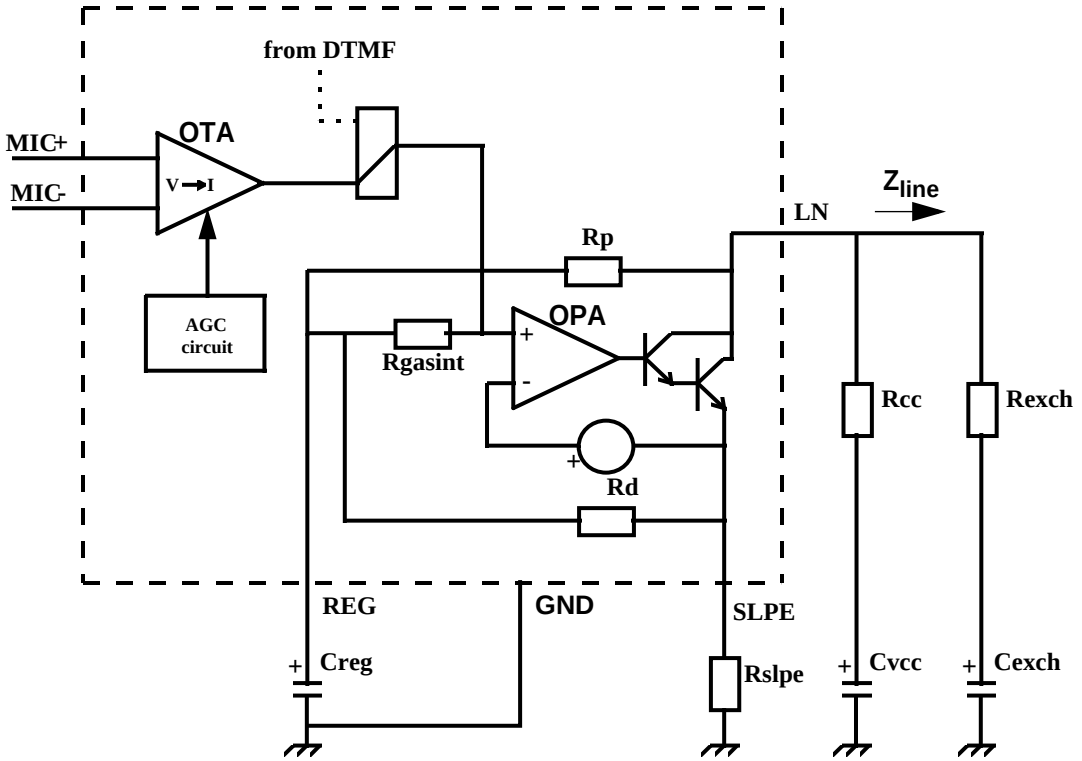


Fig.13 Microphone channel

The microphone amplifier has symmetrical high input impedances (typically 64 kΩ between MIC+ and MIC–). The input of this microphone amplifier is able to handle AC signals up to 18 mV_{rms} with less than 2% total harmonic distortion.

As can be seen from Fig.13, the microphone amplifier itself is built up out of two parts: a preamplifier which realizes a voltage to current conversion, and an end-amplifier which realizes the current to voltage conversion. The overall gain (Gvtx) of the microphone amplifier from inputs MIC+/MIC– to output LN is given by the following equation:

$$Gvtx = 20 \times \log Avtx$$

$$Avtx = 2.65 \times (Rgasint / Rrefint) \times ((Ri // |Z_{line}|) / R_{SLPE}) \times \alpha$$

with:

Rgasint = internal resistor realizing the current to voltage conversion (typically 29.5 kΩ with a spread of +/- 15%)

Rrefint = internal resistor determining the value of an internal PTAT tail current source (typically 7.25 kΩ with a spread of +/- 15% matched with Rgasint)

Ri = set impedance fixed by the network between LN and V_{CC} (R_{CC} for this example) in parallel with R_P (typically 17.5 kΩ)

Z_{line} = load impedance of the line during the measurement

α = gain control (AGC) factor varying from 1 at I_{line} = 15 mA to 0.5 at I_{line} = 75 mA when AGC function is applied (see chapter 3.1.7 for details)

Using these typical values in the equation at Z_{line} = 600 Ω and R_{CC} = 620 Ω, we find a gain equal to:

Gvtx = 20 × log Avtx = 44.2 dB at I_{line} = 15 mA

The microphone input stage will be disabled during DTMF or pulse dialling.

Adjustments and performances

Fig.14 shows the frequency response of the microphone amplifier at a microphone signal of 3 mV_{rms} and different ambient temperatures. General conditions are: I_{line} = 15 mA, R_{CC} = 620 Ω and Z_{line} = 600 Ω.

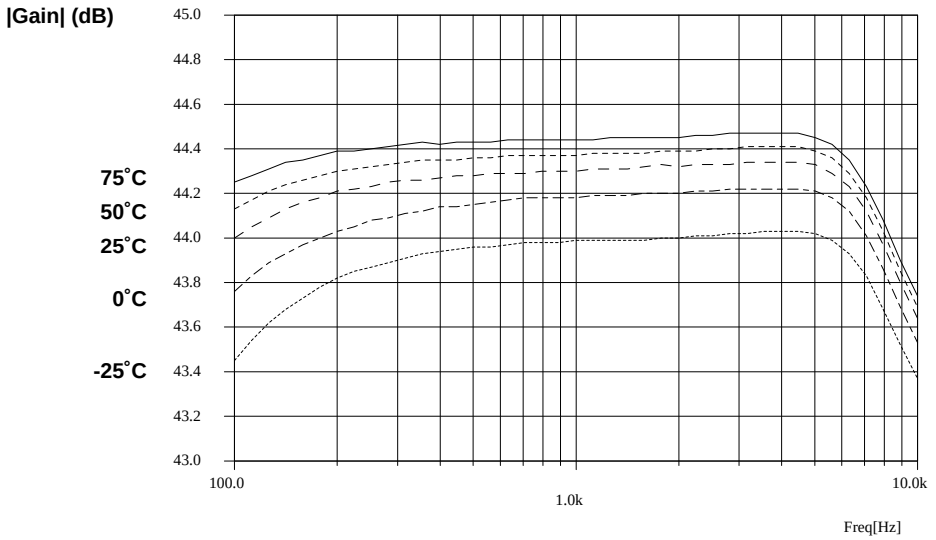


Fig.14 Frequency response of the microphone amplifier at different temperatures

Fig.15 shows the distortion of the line signal versus signal swing on LN at 4 mA, 15 mA and 70 mA line currents. The increase of the distortion at 4 mA and 15 mA is caused by the clipping of the output stage (between LN - SLPE) while at 70 mA the increase of the distortion, up to about 2.4 V_{rms}, is caused by the microphone input stage.

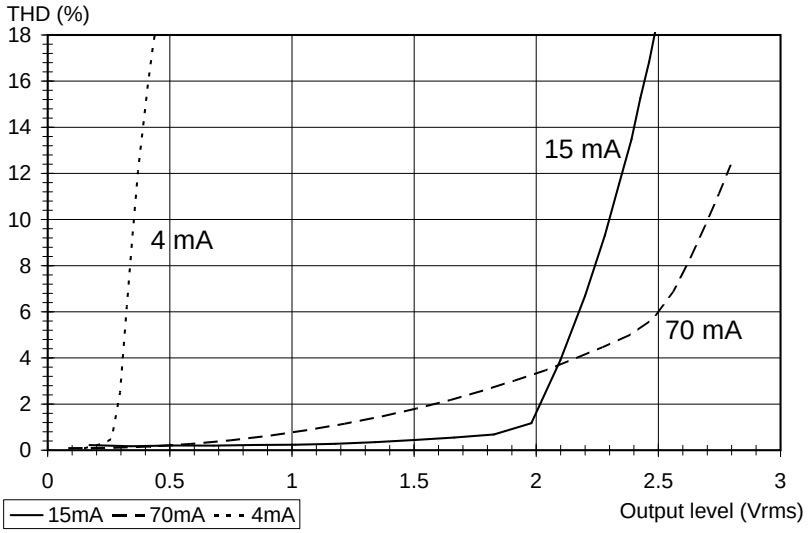


Fig.15 Distortion of the line signal

Fig.16 shows the noise level on the line (psophometrically weighted: P53 curve) versus line current at nominal gain when a 200 Ω resistor is connected between the inputs MIC+ and MIC-.

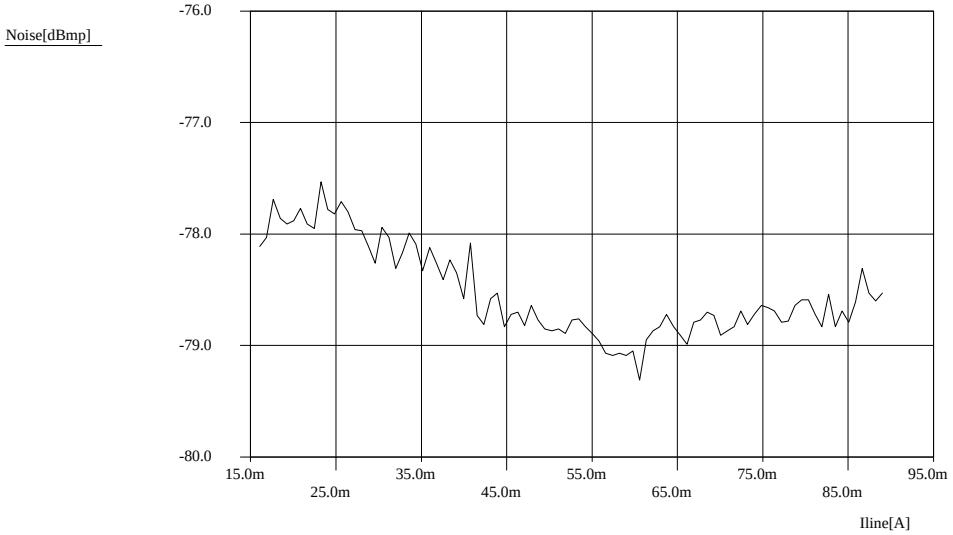


Fig.16 Microphone noise versus line current

Fig.17 shows the common mode rejection ratio at 15 mA and microphone signals of 1 kHz. Two curves are presented. One shows the spectrum of the signal on pin LN when a (differential) microphone signal is applied on pin MIC– while pin MIC+ is short circuited to GND, the other shows the spectrum when a (common) microphone signal is applied on pins MIC- and MIC+ connected together. A CMRR of more than 80 dB is shown by means of the difference of the two curves at 1 kHz.

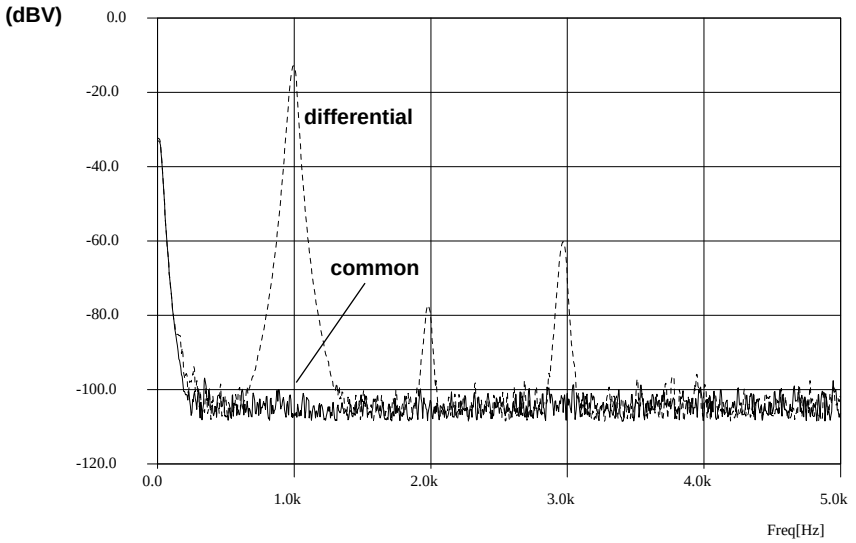


Fig.17 Common mode rejection ratio on microphone

3.1.6 Receive amplifier block

Principle of operation

Fig.18 shows the block diagram of the receive channel.

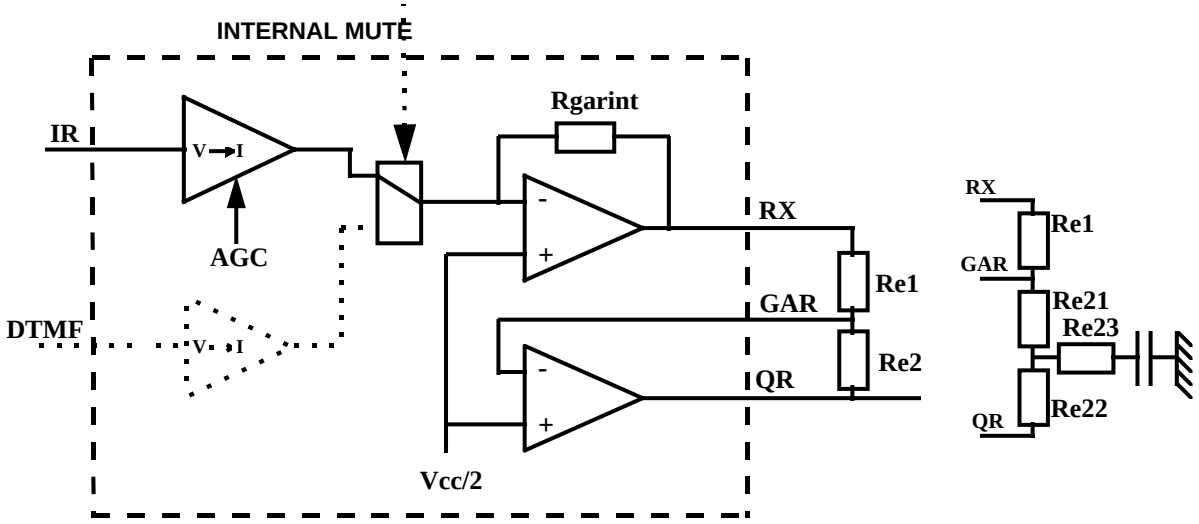


Fig.18 Receive channel

As can be seen from Fig.18, the receive amplifier block is built up out of three parts: a preamplifier which realizes a voltage to current conversion followed by an end-amplifier which realizes the current to voltage conversion at output RX and the earpiece amplifier with output QR. The gain from IR to RX is internally fixed while the gain from RX to QR can be externally determined. The preamplifier has an a-symmetrical high input impedance (typically 20 kΩ) between pins IR and GND. The earpiece amplifier of the UBA2050(A)/51(A;C) is able to drive loads down to an impedance of 150 Ω at QR while the receive amplifier can only drive loads down to 10 kΩ. The output capability is suitable for several kind of earpieces and can drive either dynamic, magnetic or piezo-electric earpieces. In case of magnetic or dynamic earpieces, a capacitor in series is required for decoupling. The overall gain Gvrx of the receive amplifier from input IR to output RX is given by the equation:

$Gvrx = 20 \times \log Avrx$

$Avrx = 2.53 \times Rgarint/Rrefint \times \alpha$

with:

Rgarint = internal resistor realizing the current to voltage conversion (typically 134 kΩ with a spread of +/-15%)

Rrefint = internal resistor determining the value of an internal PTAT current source (typically 7.25 kΩ with a spread of +/- 15% matched with Rgarint)

α = gain control factor varying from 1 at I_{line} = 15 mA to 0.5 at I_{line} = 75 mA when AGC function is applied (see chapter 3.1.7 for details)

Using these typical values in the equation, we find a gain equal to:

$Gvrx = 20 \times \log Avrx$ = 33.4 dB at I_{line} = 15 mA

The receive channel will be disabled during DTMF or pulse dialling.

Adjustments and performances

The gain of the earpiece amplifier (from RX to QR) can be adjusted between −14 and +12 dB. For this purpose, Fig.18 shows two ways of setting this gain. A gain of 33.4 dB from IR to RX compensates the attenuation approximately provided by the anti-sidetone network resulting in an overall gain of about 0 dB from LN to QR.

Two external capacitors C_{GAR} (connected between GAR and QR) and C_{GARS} (connected between GAR and GND) ensure stability of the earpiece amplifier when the relationship $C_{GARS} = 10 \times C_{GAR}$ is fulfilled. The capacitor C_{GAR} provides a first order low pass filter, which cut-off frequency is determined with R_{E2}. Furthermore, if a high-pass filter is required a capacitor can be inserted in series with R_{E1}. Fig.19 shows the frequency response and the typical gain of the receive amplifier from IR to RX at different temperatures.

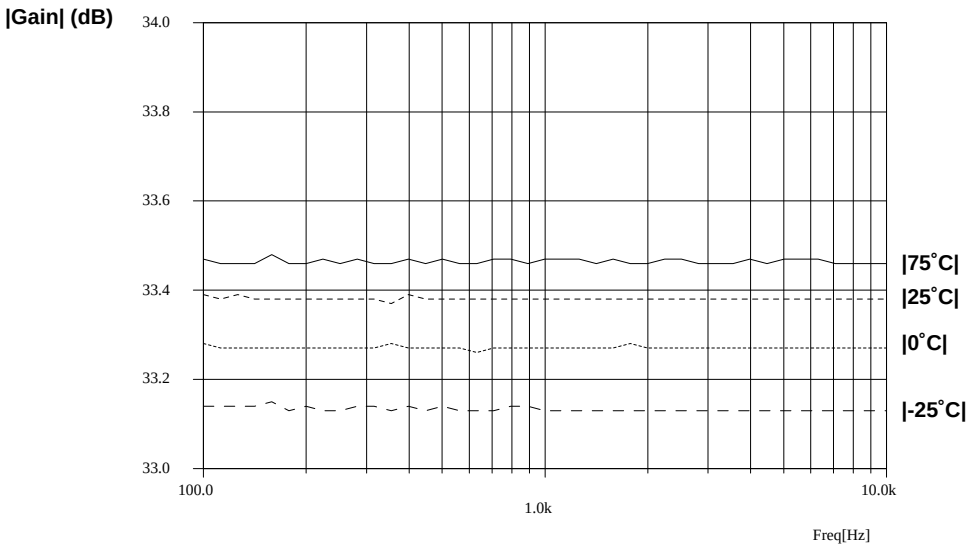


Fig.19 Receive gain versus frequency: influence of temperature

The maximum output swing versus distortion of output QR depends in general on the total gain from IR to QR. At low gain settings of the earpiece amplifier the output signal of QR will be clipped by the RX output stage. The maximum output swing on RX is about 280 mV_{rms} at THD = 2%, which corresponds to an input signal on IR of 12.5 mV_{rms} at maximum line current (max. AGC).

At higher gain settings the output signal will be clipped by the QR output stage at about 370 mV_{rms} at THD = 2% and an output load of 150 Ω. The gain of the earpiece amplifier (RX to QR) is not affected by AGC.

Fig.20 shows the distortion of the earpiece signal versus output swing at load of 150 Ω and 450 Ω, 15 mA line current and 0 dB gain setting.

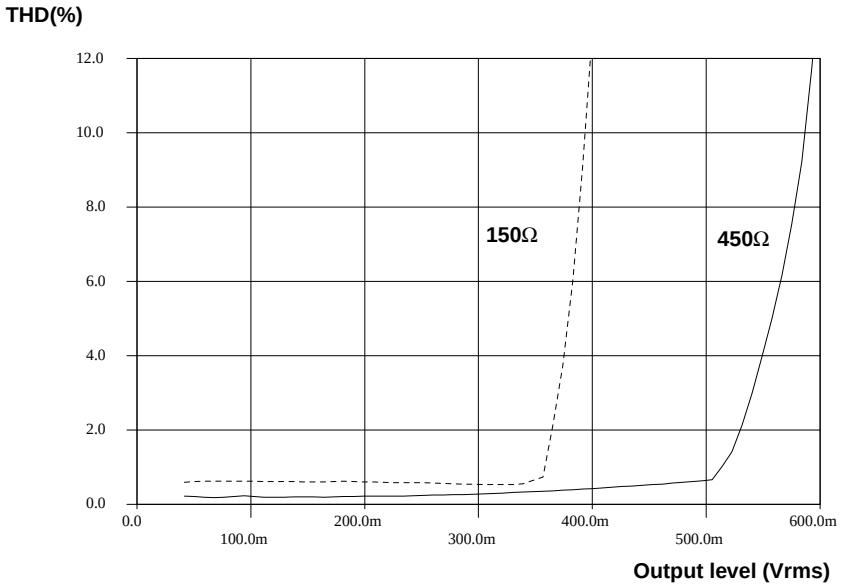


Fig.20 Distortion of the earpiece signal at 150 Ω and 450 Ω load

Fig.21 shows the noise on QR loaded with 150 Ω (psophometrically weighted: P53 curve) as a function of the line current with a gain of 0 dB of the earpiece amplifier measured with open input IR. Take into account that the noise on QR is proportional to the gain setting of the earpiece amplifier.

The noise contribution from the line, with the anti-sidetone network connected to input IR, can not be neglected.

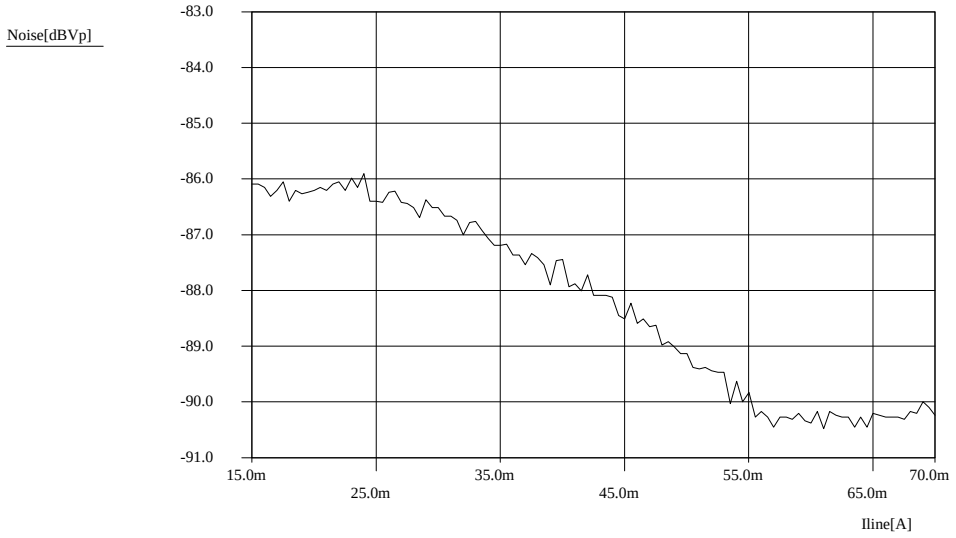


Fig.21 Noise level across earpiece at 0 dB gain setting at open IR input

3.1.7 Automatic gain control

Principle of operation

The UBA2050(A)/51(A;C) features automatic line loss compensation. The automatic gain control varies the gain of the microphone and receive amplifiers in accordance with the DC line current. To enable this AGC function, the pin AGC must be connected to the pin GND. For line currents below a current threshold, I_{start} (typically 23 mA), the gain control factor is equal to 1, giving the maximum value to the gains Gvtx and Gvrx. If this threshold current is exceeded, the gain control factor α is reduced and then the gains of the controlled microphone and receive amplifiers are also reduced. When the line current reaches an other threshold current, I_{stop} (typically 59 mA), the gain control factor α is limited to its minimum value equal to 0.5, giving the lower value to the microphone and receive controlled gains. The gain control range of both amplifiers is typically 6 dB, which corresponds approximately to a line length of 5 km (0.5 mm twisted pair copper) with an attenuation of 1.2 dB/km.

The attenuation is correlated to the current I_{AGC} sunk at pin AGC: when this current is lower than typically 4.5 µA the gains are maximum, when this current is higher than typically 14 µA the gains are minimum. This current is proportional to the voltage between pins SLPE and GND. The IC contains an internal resistor which sets I_{start} and I_{stop}. By adding a resistor externally in series (between pins AGC and GND) reduces I_{AGC} and increases the values of I_{start} and I_{stop}.

Adjustments and performances

The AGC of the UBA2050(A)/51(A;C) can be used with different exchange supply voltages and different feeding bridge resistances. For this purpose, a resistor R_{AGC}, can be inserted between pins AGC and GND. This R_{AGC} resistor increases both threshold currents I_{start} and I_{stop} proportionally. Fig.22 shows the control of the microphone gain versus the line current for different values of R_{AGC}. When no AGC function is required, the AGC pin must be left open, then the control factor α remains to 1 over the line current range.

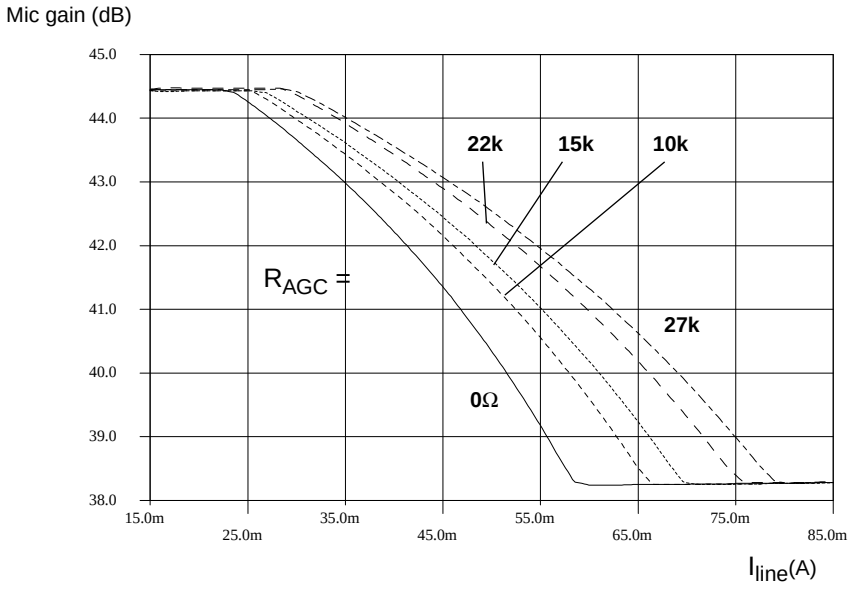


Fig.22 AGC on the microphone gain versus line current at different R_{AGC} values

3.1.8 DTMF amplifier

Principle of operation

Fig.23 shows the block diagram of the DTMF channel.

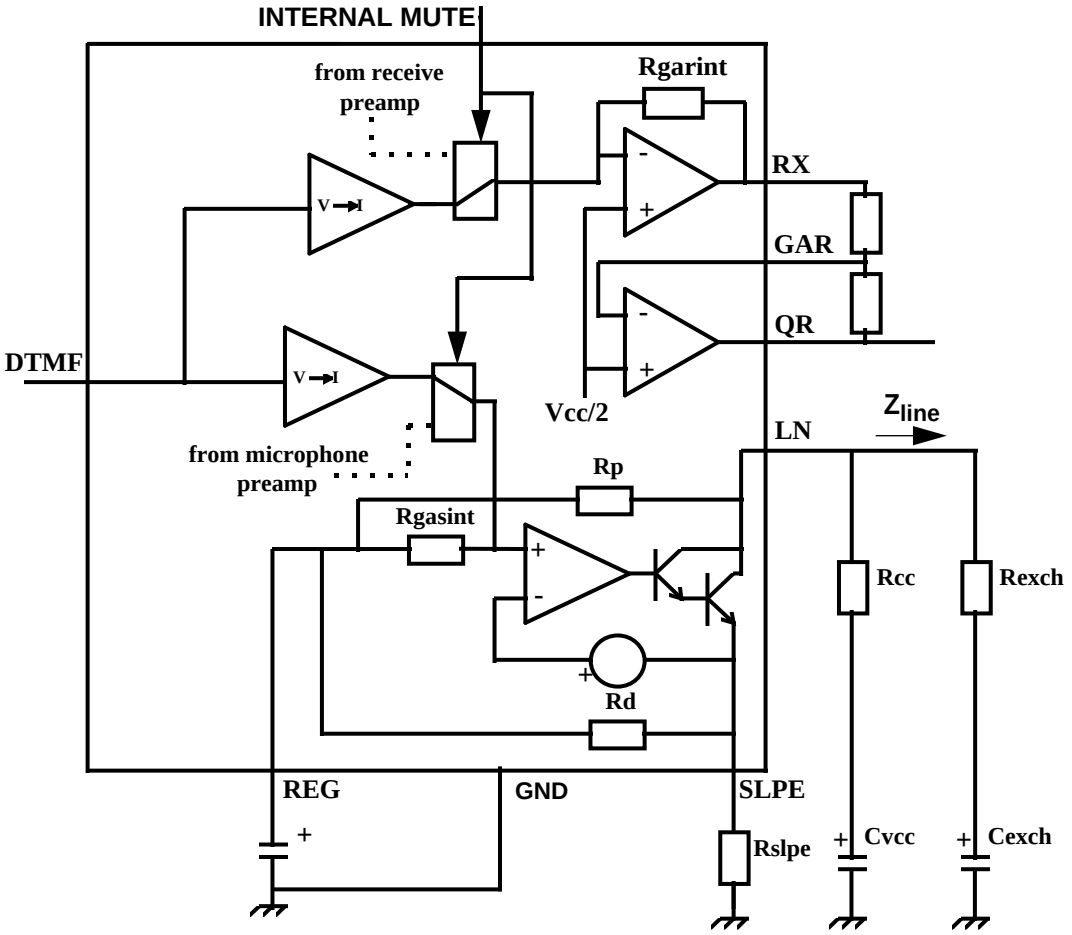


Fig.23 DTMF channel of the UBA2050(A)/51(A;C)

The DTMF amplifier has an asymmetrical high input impedance of 20 kΩ typically between pins DTMF and GND. The input is biased at GND, so when the input DTMF signal is polarized at GND, a decoupling capacitor is not necessary. The DTMF amplifier is built up out of two parts: a preamplifier which realizes the voltage to current conversion and the same end-amplifier as the microphone amplifier. No AGC is applied to the DTMF channel. The overall gain (Gvmf) of the DTMF amplifier from input DTMF to output LN is given by the following equation:

$Gvmf = 20 \times \log Avmf$

$Avmf = 0.246 \times (Rgasint / Rrefint) \times ((Ri // |Z_{line}|) / R_{SLPE})$

with:

Rgasint = internal resistor realizing the current to voltage conversion (typically 29.5 kΩ with a spread of +/- 15%)

Rrefint = internal resistor determining the current of an internal current stabilizer (typically 7.25 kΩ with a spread of +/- 15% matched with Rgasint)

Ri = set impedance fixed by the network between LN and V_{CC} (R_{CC} for this example) in parallel with R_P (typically 17.5 kΩ)

Z_{line} = load impedance of the line during the measurement

Using these typical values in the equation at Z_{line} = 600 Ω and R_{CC} = 620 Ω, we find a gain equal to:

Gvmf = 20 × log Avmf = 26 dB

Furthermore, the DTMF signal is attenuated and transferred to the receive amplifiers as confidence tone.

Fig.24 shows the frequency response of the DTMF amplifier at 15 mA and different ambient temperatures.

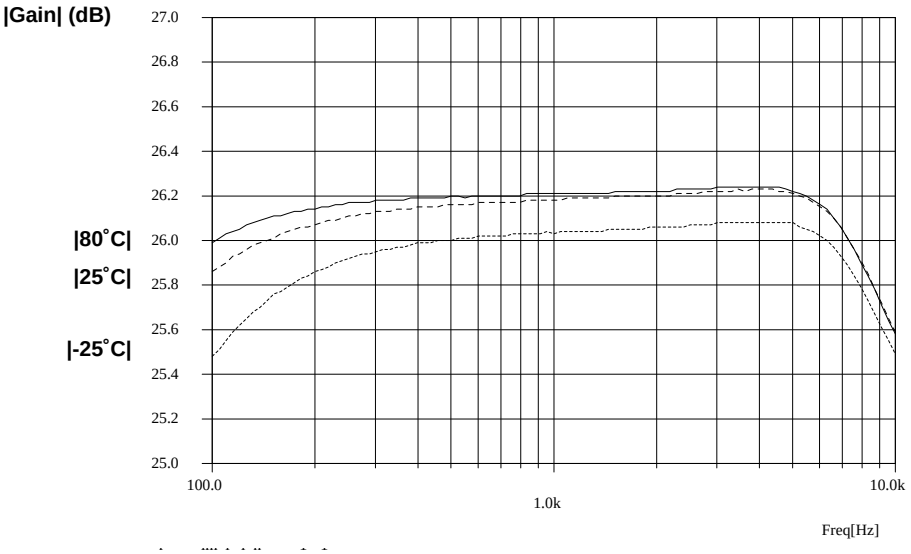


Fig.24 DTMF gain versus frequency: influence of temperature

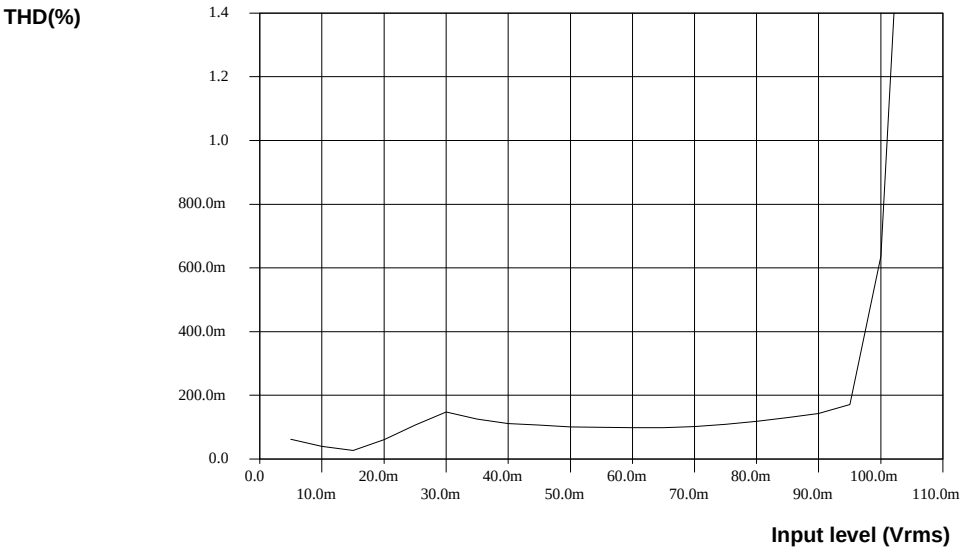


Fig.25 Distortion of the DTMF line signal versus input signal on DTMF

The input of the DTMF amplifier can handle signals up to 110 mV_{rms} with less than 2% THD. Fig.25 shows the distortion on line versus the input signal at I_{line} = 15 mA. The DTMF signal generated by the dialler part (MDY/TONE output) has to be attenuated before it can be offered to the DTMF input.

3.1.9 Internal MUTE

The internal MUTE function of the UBA2050(A)/51(A;C) realizes electronic switching between speech mode and the dialling mode. In dialling mode, both microphone and the receive channels are disabled while the DTMF channel is enabled. In speech mode the microphone and the receive channels are enabled while the DTMF channel is disabled.

3.1.10 Anti-sidetone networks

Principle of operation

To avoid the microphone signal to return back with a too high level in the receive channel, the anti-sidetone circuit uses the microphone signal from pin SLPE (which is in opposite phase) to cancel the microphone signal at the IR input of the receive amplifier. The anti-sidetone bridge already used for the TEA111x (or TEA106x) families or a conventional Wheatstone bridge as shown in Fig.26 may be used for the design of the anti-sidetone network.

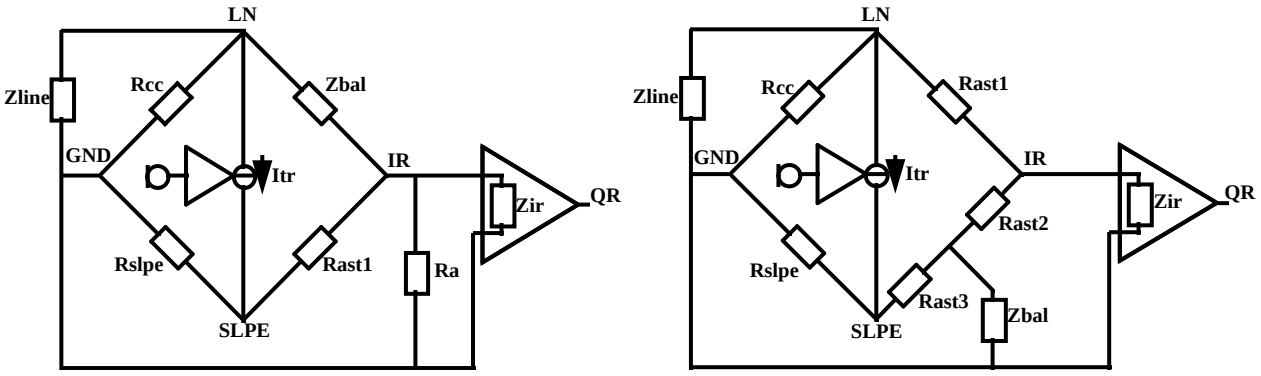


Fig.26 Wheatstone bridge (left) and TEA111x family anti-sidetone bridge (right)

The TEA111x (or TEA106x) family anti-sidetone bridge has the advantage of a relative flat transfer function in the audio frequency range between the input IR and the output RX, both with real and complex set impedances. Furthermore, the attenuation of the bridge for the receive signal (between pins LN and IR) is independent of the value chosen for Z_{bal} after the set impedance has been fixed and the condition shown in equation (a) is fulfilled. Therefore, re-adjustment of the overall receive gain is not necessary in many cases.

Compared to the previous one, the Wheatstone bridge has the advantages of needing one resistor less and a smaller capacitor in Z_{bal}. But the disadvantages include the dependence of the attenuation of the bridge on the value chosen for Z_{bal} and the frequency dependence of that attenuation. Moreover, the input stage may introduce some distortion at high signal levels. This requires some readjustment of the overall receive gain.

TEA111X family bridge

The anti-sidetone circuit is composed of: R_{CC} //Z_{line}, R_{ast1}, R_{ast2}, R_{ast3}, R_{SLPE} and Z_{bal}. Maximum compensation is obtained when the following conditions are fulfilled:

$$R_{SLPE} \times R_{ast1} = R_{CC} \times (R_{ast2} + R_{ast3}) \quad \text{(a)}$$

$$k = [R_{ast2} \times (R_{ast3} + R_{SLPE})] / (R_{ast1} \times R_{SLPE})$$

$$Z_{bal} = k \times Z_{line}$$

The scale factor k is chosen to meet the compatibility with a standard value of capacitor for Z_{bal}.

In practice, Z_{line} varies strongly with line length and line parameters. Consequently, the value for Z_{bal} has to be chosen to fit with an average line length giving acceptable sidetone suppression for short and long lines. The suppression further depends on the accuracy with which Z_{bal} equals this average line impedance.

Example

A theoretical equivalent average line impedance shown in Fig.27.

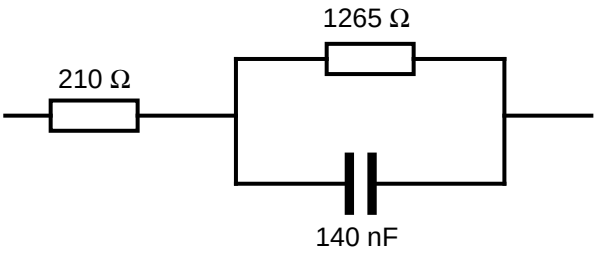


Fig.27 Equivalent average line impedance

For compatibility of the capacitor value in Z_{bal} with a standard capacitor value from the E12 series (220 nF):

$k = 140 / 220 = 0.636$

For R_{ast2}, a value of 3.92 kΩ has been chosen. So, using the previous equations, we can calculate Z_{bal}, R_{ast1}, R_{ast3}. We find R_{ast1} = 130 kΩ, R_{ast3} = 390 Ω, and for Z_{bal} 130 Ω in series with 220 nF // 820 Ω.

The attenuation of the receive line signal between LN and IR can be derived from the following equation:

$$V_{IR} / V_{LN} = (Z_{IR} // R_{ast2}) / [R_{ast1} + (Z_{IR} // R_{ast2})]$$

If $R_{ast2} >> (R_{ast3} // Z_{bal})$.

With the values used in this example, it gives 32 dB at 1 kHz.

Z_{IR} is the receive amplifier input impedance, typically 20 kΩ.

Wheatstone bridge

The conditions for optimum suppression are given by:

$$Z_{bal} = (R_{ast1} / R_{SLPE}) \times (R_{CC} // Z_{line})$$

Also, for this bridge type, a value for Z_{bal} has to be chosen that corresponds with an average line length.

The attenuation of the received line signal between LN and IR is given by:

$$V_{IR} / V_{LN} = (Z_{IR} // R_{ast1} // Ra) / [Z_{bal} + (Z_{IR} // R_{ast1} // Ra)]$$

R_a is used to adjust the bridge attenuation; its value has no influence on the balance of the bridge.

3.2 DIALLER PART

See also Fig.1

3.2.1 Timing/Control

The behaviour of the Timing/Control function depends on the conditions of the XTAL, CE/CSI and CE/FDI pins during start-up (off-hook action) and line disconnect (on-hook action, flash and unexpected line breaks). It handles also several states to be entered or left: STAND-BY, ON-LINE and RINGER state. A reset delay time of 280 ms will also be processed by the Timing/Control function for detecting line breaks. A complete handshake protocol between Timing/Control function and the remaining of the circuitry avoids RAM contents loss when the IC is disabled again by CE/FSI= LOW and CE/FDI= LOW.

An external 3.579545 MHz quartz-crystal or ceramic resonator has to be connected between XTAL and GND. Depending on the CE/CSI and CE/FDI pins any operating state can be entered. After determining the state and reaching the operating voltage level for V_{DD}, the oscillator starts. Actions such as ringer generation, dialling, programming, line disconnect can be executed depending on the ringer signal, line break, cradle switch and/or key entry.

One-pin oscillator

The time base of the UBA2050(A) and UBA2051(A;C) is provided by an on-chip oscillator which consists of an oscillator circuit with build-in load capacitance, amplitude control, a schmitt-trigger circuit and an output buffer. The oscillator is completed by connecting a quartz-crystal or ceramic resonator between XTAL and GND. Generating the correct DTMF tones, the crystal has to be a 3.579545 MHz type while for a ceramic resonator the types from Murata CSA 3.58 MG or AVX Kyocera KBR 3.58 MSA are preferred. The oscillator starts when V_{DD} reaches the operating level with CE/FDI = HIGH or CE/CSI = HIGH.

Start-up after off-hook

The telephone set starts up as follows (see Fig.51 and Fig.52; see [1] for functionality of CE/CSI and CE/FDI):

1. Cradle switch S1 is switched on (e.g. handset is lifted), it makes the CE/CSI input HIGH via R_{CSI}.
2. Line voltage is offered to the base of TR3 via this switch and R3. TR3 conducts and activates TR1. The line current will then flow through TR1 providing the supply power for the whole application.
3. The dialler is initialized by the internal reset signal.
4. After reset and reaching the minimum operating voltage of 2.0 V for V_{DD} the oscillator is running and the Timing/Control function monitors the status of CE/CSI and CE/FDI for determining which state will be entered: ON-LINE or RINGER. In this case only CE/CSI input is HIGH so that ON-LINE state is entered.
5. The dialler performs a memory integrity check. In case of failing check, the whole memory is cleared.
6. Before resistor option read, the dialler waits for “pins C1-C4 and R1-R4 are HIGH”. Moreover, the resistor options read cycle is performed in parallel with memory integrity check.
7. The telephone set is operational and can be used for conversation or dialling.

Fig.28 shows the start-up of the dialler after switching on the cradle switch S1 at I_{line} = 20 mA. All supply capacitors C_{VCC}, C_{feed}, C_{VDD}, C_{REG} and C_{VRR} are *discharged* before start-up. Take into account that V_{LN} is clamped at about 10 V by Z1 immediately after start-up.

During normal use of a telephone set with UBA2050(A)/51(A;C) the C_{VDD} capacitor will be continuously charged (trickle current) and therefore even faster start-up of the dialler can be achieved.

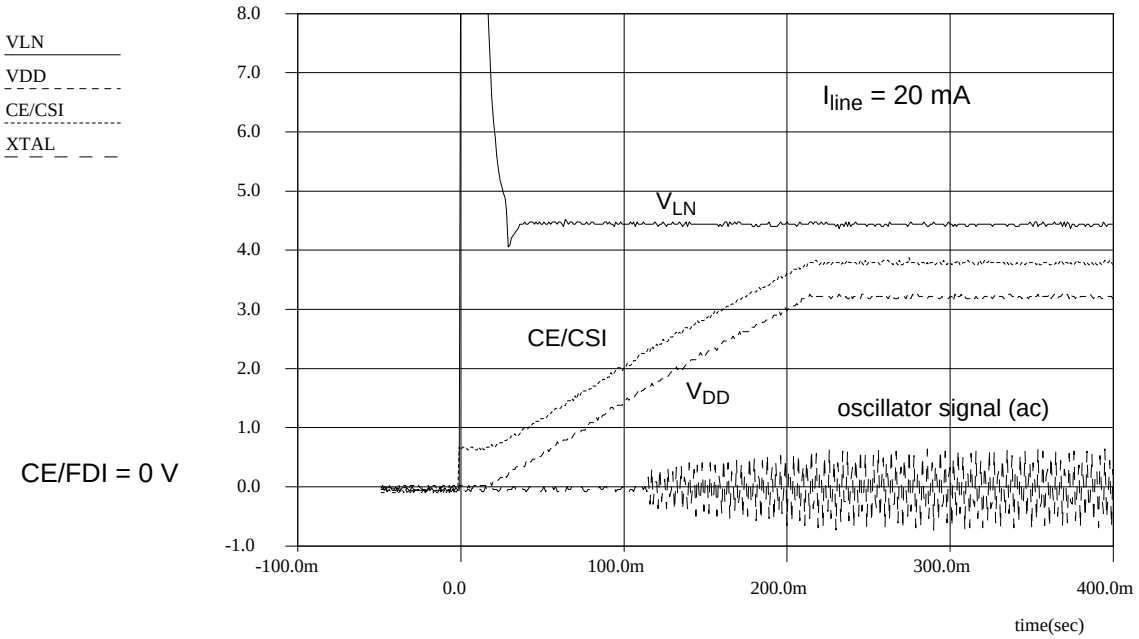


Fig.28 Dialler start-up after off-hook

Start-up at incoming ringer signal

The telephone set performs the following procedure when an incoming ringer signal is applied to CE/FDI input:

1. The current into V_{DD} is delivered by the ringing signal. The V_{DD} regulator acts as a shunt stabilizer to keep V_{DD} at 3.3 V_{typ}. It provides the supply power to the dialler part.
2. The dialler is initialized by the internal reset signal.
3. After reset and reaching the minimum operating voltage of 2.0 V for V_{DD} the oscillator is running and the Timing/Control function monitors the status of CE/CSI and CE/FDI for determining which state will be entered: ON-LINE or RINGER. In this case CE/CSI input is LOW and CE/FDI is provided with pulses of the ringer signal. RINGER state is entered after evaluating this signal.
4. The dialler performs a memory integrity check. In case of failing check, the whole memory is cleared.
5. Before resistor option read, the dialler waits for “pins C1-C4 and R1-R4 are HIGH”. Moreover, the resistor options read cycle is performed in parallel with memory integrity check.
6. In parallel with resistor options read cycle and memory integrity check, the ringer detector checks the validation of the ringer signal conforming the ringer specification before a ringer melody will be generated. This to detect a valid ringer signal as soon as possible

Fig.29 and Fig.30 show the start-up of the dialler after t = 0 when a first ringer signal (35 V_{rms} / 50 Hz) is offered at the A/B terminals. V_{DD} was already charged to approx. 1.5 V by means of the $R_{trickle}$ from V_{exch} = 48 V. Take into account that V_{DD} will be charged to 3.3 V when V_{RR} node becomes stabilised; see Fig.50. The oscillator starts after about 75 ms while the MDY signal for the ringer stage is available after 120 ms. The supply voltage V_{DD} (V_{DD} > POR trip level) determines the start-up of the ringer in this case. The supply capacitor C_{VRR} was discharged before start-up.

Ringer sound is produced after receiving ringer signal of at least 1.5 ringer periods, after V_{DD}-minimum is reached, due to ringer frequency evaluation.

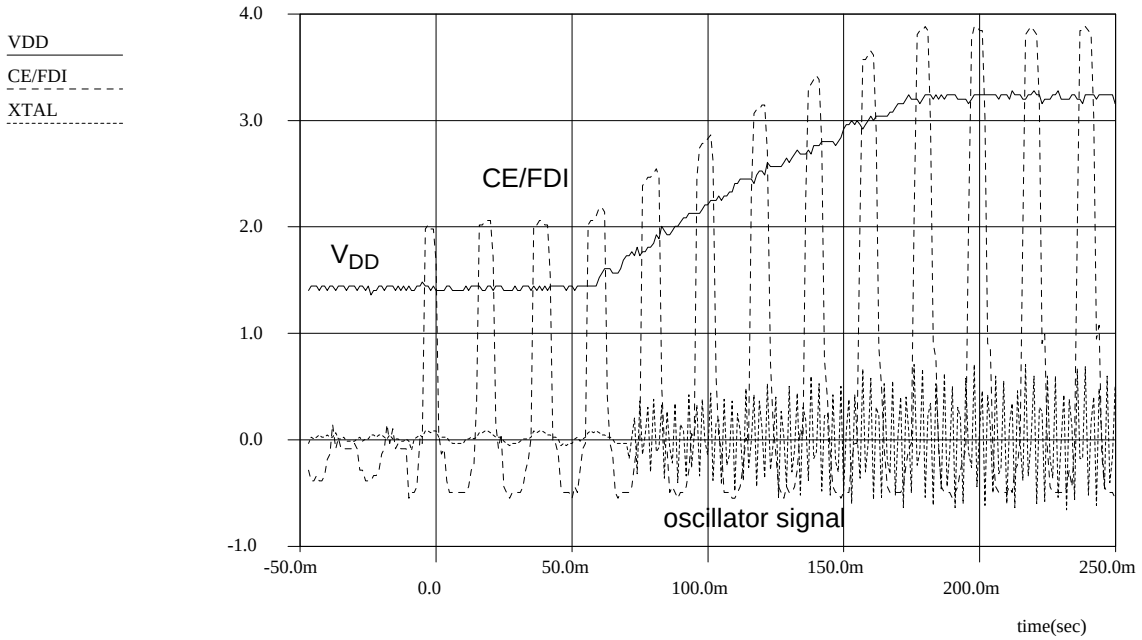


Fig.29 Dialler start-up for incoming ringer signal; V_{DD}, CE/FDI and oscillator signal

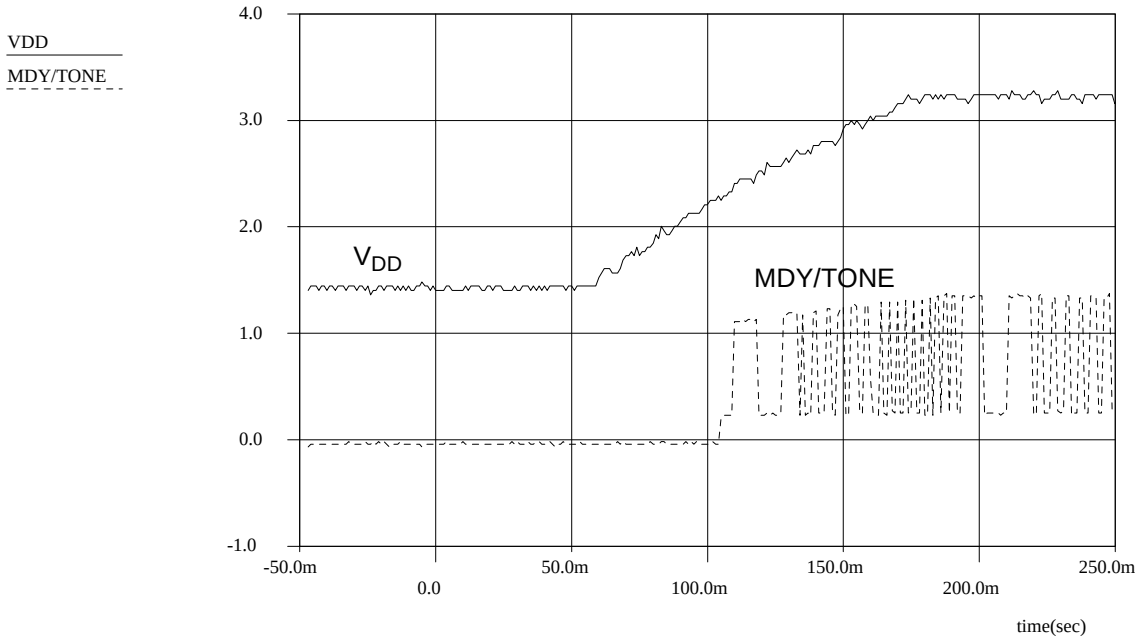


Fig.30 Dialler start-up for incoming ringer signal; V_{DD} and MDY signal

Line disconnect

If the inputs CE/CSI and CE/FDI are LOW for more than the reset delay time (typ. 280 ms) an internal reset pulse will be generated and the dialler will go into STAND-BY state again. It will occur when there is a line-break or the handset is back on the cradle and there is no ringer signal. The current for RAM retention is delivered by the telephone line via the high ohmic resistor $R_{trickle}$ (see Fig.51). The RAM retention current will be smaller than 300 nA at the specified V_{DD} of 1.2 V. All blocks inside the UBA2050(A)/51(A;C) including the oscillator are stopped and require no power supply. Only the RAM and the supply voltage monitor are using current.

The task of the line-break detector is monitoring the line voltage. When the line-break occurs the dialler will interrupt the current task after reset delay time. All necessary actions will be completed before entering into STAND-BY state, to avoid damaging the contents of internal RAM by abruptly stopping the dialler. Only when the supply capacitor C_{VDD} goes below POR trip level all actions are stopped immediately.

Fig.31 shows line disconnect of the dialler when the handset goes on-hook. The oscillator stops 280 ms after CE/CSI went LOW.

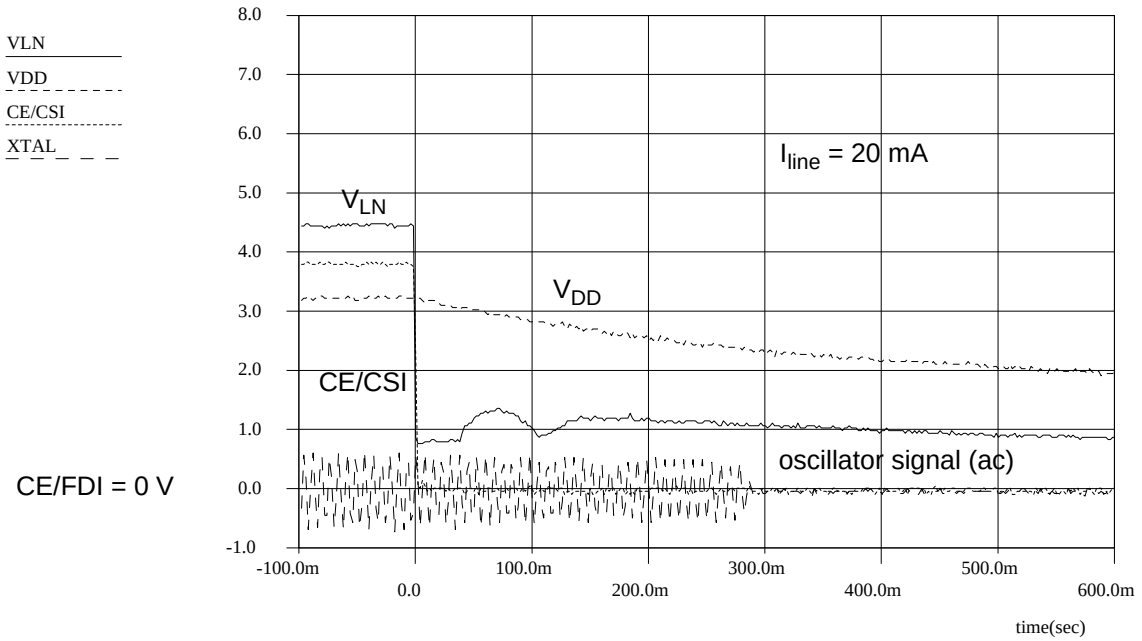


Fig.31 Dialler line disconnect

Changing to STAND-BY state is prevented when a flash is activated. The detector will be suppressed because the duration of 2 selectable flash times (300 and 600 ms) are longer than the reset delay time. After flash period the timer will start again. Keep in mind that the supply capacitors in this case have to supply the dialler and the peripherals for at least 880 ms (flash of 600 ms + reset delay time of 280 ms).

3.2.2 Pulse dialler

The pins $\overline{DP/FL}$ and DMO are responsible for the pulse dialling and flash function. These are connected to a line interrupter respectively a DMO stage. Flash function will be realised using the same interrupter. Several break/make ratios and flash times can be selected by means of resistor options.

Pulse dialler

The pulse dialling system uses line current interruptions to signal the digits dialled to the exchange. The number of line current interruptions corresponds to the digit dialled except for the digit [0] which is characterized by 10 interruptions.

Digits such as [0] to [9] entered via the keyboard are converted into pulses which are available on the $\overline{\text{DP/FL}}$ output. Pulse sequences start with a pre-digit pause followed by a sequence of pulses corresponding to the present digit and then an inter-digit pause of 800 ms duration at 10pps.

The pulse dialler is activated when the pulse mode is selected by means of the resistor option PTS. At dialling, the transmission part is muted and only confidence clicks are audible in the earpiece. By application it is possible to feed the generated keytones (UBA2050(A)/51C) into the earpiece via pin GAR (See Fig.43).

Flash generator

The flash function, when key [R] is pressed results in a calibrated pulse which drives the electronic line current interrupter via pin $\overline{\text{DP/FL}}$. This pin is also used by the pulse dialler. It is not possible to use the flash generator and the pulse dialler at the same time. They depend on the digit sequence.

DMO

The DMO pin of the UBA2051 is used to enable external hardware which decreases the DC voltage over the telephone line during pulse dialling. Several countries require this feature. It will also be activated during a flash period.

Timing selection

Each pulse starts with a line break (mark) followed by line make (space). Selection can be made for make/break ratio and the number of pulses per second: 1:2/2:3 resp. 10/20 pps. See TABLE 3 for the selection.

Flash interruption times depend on the resistor options (see TABLE 3). Four times are possible: 80, 98, 300 and 600 ms. After every flash an interflash pause of 800 ms is inserted to recover the power supply for the dialler part (e.g. in case of multiple flashes).

3.2.3 Tone generator

The pin MDY/TONE has 2 operating states:

RINGER state

At valid incoming ringer signal a ringer melody (square-wave) with four different volumes will be generated via this pin. See next sections for more information about.

ON-LINE state

In ON-LINE state, the dialler converts keyboard inputs such as digits [0] to [9], [*] and [#] into data for the on-chip DTMF generator. See Fig.32. Tones are transmitted via MDY/TONE output. Each digit corresponds to a combination of two tones, out of four possible LOW resp. three HIGH group frequencies. On the output 2 simultaneous tones are generated at levels of typical -12.6 dBm for the HIGH group and -14.7 dBm for the LOW groups. The harmonic contents fulfil the CEPT CS 203 recommendations. Generation of tones is only possible when tone dialling mode in ON-LINE state is selected.

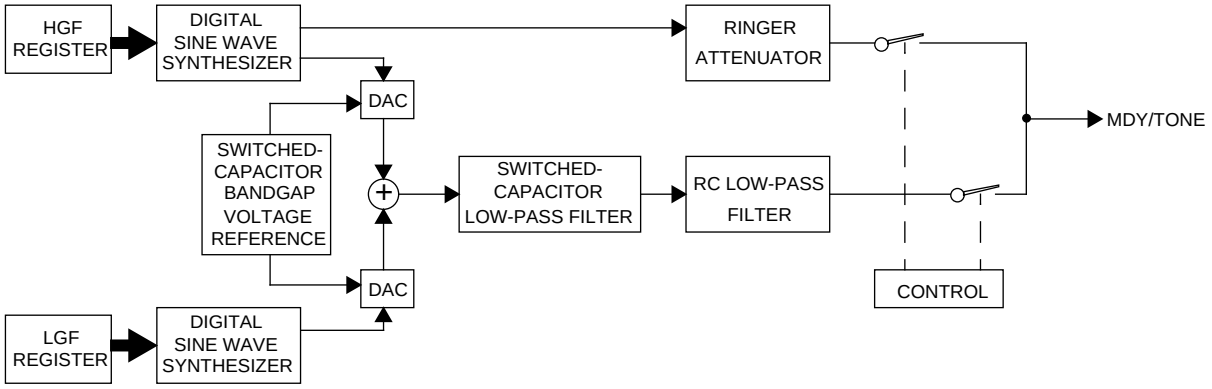


Fig.32 Block diagram of the DTMF generator

3.2.4 LED output

UBA2051A is able to drive a LED when connected to pin LED. The output becomes active HIGH in two cases:

1. in pulse dialling mode (set with resistor option R_{PTS}) when the first DTMF code is sent after switching by key [P->T] or key [*/T].
2. in tone dialling mode (resistor option R_{PTS} removed) when a key is pressed and the first DTMF code is sent.

The output will remain LOW during and directly after reset. The LED output is able to source from V_{DD} up to 1.9 mA when sufficient supply current is available from V_{DD}.

3.2.5 Keyboard

Pins C1-C4 and R1-R4 connect the keyboard in which 20 keys are mounted. In the matrix, 4 keys are connected to ground (GND). The advantage of this arrangement compared to a traditional keyboard is the pin reduction that can be obtained for the same amount of keys. Furthermore the settings called resistor options can be read via these pins C1-C3, R1-R4 without an additional pin for enabling the read operation. This is possible thanks to special I/O port functionality.

For UBA2050(A), the pin C4 is not available because the dialler has no memory for repertory numbers.

Keyboard structure

The UBA2051(A;C) supports the keyboard structure as shown in Fig.33. For UBA2050(A), all repertory-related keys are not supported. At the left side in this figure, 7 resistors are placed to select resistor options. It will be explained in the following sections.

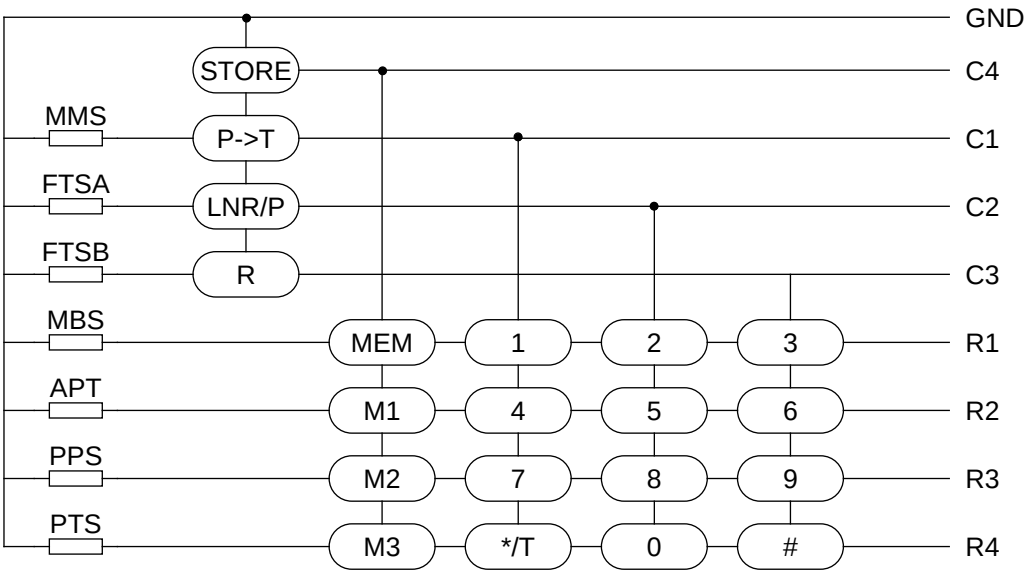


Fig.33 Keyboard structure

The keys [*/T] and [P->T] have the same function during pulse mode (no R_{MMS}). It allows the set-maker to make a choice which keys will be used during design-in phase.

Functional keys

The meaning of each key is described in TABLE 2.

TABLE 2 Key definitions

Keys	Definition
[0-9], [*/T], [#]	Digits
[*/T], [P->T]	Switch over to DTMF dialling (mixed mode dialling)
[LNR/P]	Last Number Redial if this key is the first key pressed after going off-hook
[LNR/P]	Access Pause if this key is not the first key pressed after going off-hook
[M1-M3]	Direct repertory numbers
[MEM]	Indirect repertory numbers
[R]	Recall (flash function)
[STORE]	Memory programming

Keyboard scanning principle

In order to fulfil the requirements for some countries the choice for this IC is a matrix keyboard which detects a double key pressed and in this case inhibiting the DTMF signal on the line. On the other hand the keyboard supports the roll-over feature. For example, a second key entry will reject the first key entry and the next key entry becomes valid when all other keys are released again.

A key entry becomes valid after specified debounce time to avoid a wrong key entry interpretation due to the behaviour of mechanical switches. In principle the keyboard debounce procedure consists out of 2 parts, first the debounce detection time and second the real key detection. Approximately 20 ms is required for this procedure. The debounce procedure for release keys is vice versa.

The keyboard controller takes care of several cases: when no key, single key or multiple keys are pressed. Special attention is paid to keys connected to GND because they are different from the remaining keys in the keyboard with relation to scanning and detection procedure.

Keytone generator

A keytone is generated each time a valid key is pressed. The keytone has a frequency of 597 Hz and a duration of 30 ms. This feature is only offered for the UBA2050(A) and UBA2051C. The KT output is a push-pull output. A buzzer can be connected between this output and GND taking into account a from V_{DD} point max. sourced output current up to 1.9 mA when sufficient supply current is available from V_{DD}

3.2.6 Resistor options

User options can be selected by means of resistors which can be externally connected between the pins R1-R4, C1-C3 and GND. The options are read via these pins without an additional pin for enabling the read operation. Special I/O port functionality makes this possible.

Resistor options settings

According to TABLE 3 a number of 7 options can be selected. Each resistor has the value of 1 MΩ and is connected to GND.

TABLE 3 Resistor options

Resistor	To Pin	Function	Condition	ON(1)	OFF(1)
FTSA	C2(2)	flash time select	FTSB = off	300 ms	98 ms
FTSA	C2(2)	flash time select	FTSB = on	80 ms	600 ms
MMS	C1	[*/T] definition		[*/T] => [*]	[*/T] => [P->T]
MBS	R1	make/break ratio select		33/66	40/60
APT	R2	access pause time select		3.6 seconds	2.0 seconds
PPS	R3	pulses per second		20 pps	10 pps
PTS	R4	pulse/tone select		pulse mode	DTMF mode

Note:
1. **on** = option resistor present; **off** = option resistor not present
2. pin C3 belongs to resistor option FTSB.

The options can only be scanned if no keys are pressed on the keyboard. After each reset of the dialler it scans the keyboard repeatedly until all keys are released. Next, it reads and translates the resistor options into system parameters which will be maintained during the whole off-hook period. So changing the resistor options in this period has no influence on the dialler.

Scanning principle

During and directly after reset the scanning procedure for the keyboard and option resistors will not be performed. In this state pins C1-C4, R1-R4 are set to LOW. After reset the dialler starts to monitor the two pins CE/CSI and CE/FDI before entering any of the different operating states as described in datasheet [1].

Next, the keyboard pins become HIGH ant the dialler waits for releasing of possible pressed keys before scanning of resistor options can be started.

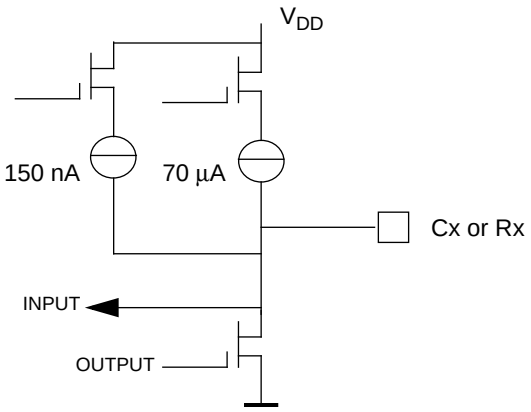


Fig.34 C1-C4, R1-R4 Input/Output stage configuration

The pins R1-R4 and C1-C4 are connected internally to one of two port pull-up source currents: typically 150 nA (I_{OH2}) or 70 µA (I_{OH1}). The current source of 150 nA is selected during the resistor options read to achieve a low voltage drop across the high ohmic resistor, when applied, with respect to the thresholds of the logic levels. A low level means that a resistor option is present. The resistor options are scanned and translated into system parameters which are stored.
The 70 µA (I_{OH1}) is used for keyboard scanning during the whole off-hook period to suppress the presence of option resistors in relation with the voltage at the keyboard pins. This voltage will reach nearly the V_{DD} voltage. A pressed key will force this level to zero in this case.

3.2.7 Dialling procedures

APPENDIX 3 gives a description of the dialling procedures. They are categorized into:

- Dialling with LNR
- Store in repertory
- Dialling from repertory

All actions and dial outputs use the same symbols which are described in the beginning of this appendix.

3.3 RINGER PART

The pins CE/CSI, CE/FDI and MDY/TONE take care of the generation of a ringer signal to the ringer stage.

3.3.1 Ringer input frequency measurement

The ringer signal is offered to CE/FDI input of the UBA2050(A)/51(A;C). It is half-wave rectified so that the dialler can easily detect zero-crossing, especially at high frequencies and square wave shaped ringer signals. The ringer circuitry becomes active for all incoming ringer frequencies of more than the 13 Hz frequency threshold. This frequency threshold can not be adjusted externally. The ringer signal is valid when the following conditions are met:

- $f_{ring} \geq 13$ Hz
- CE/CSI = LOW
- ringer signal duration > 1.5 frequency cycles (max. 150 ms at 13 Hz)
- threshold levels: $0.2 \times V_{DD}$ for low level and $0.8 \times V_{DD}$ for high level

The CE/FDI input is used to activate and initialize the dialler part of the IC. It is notified that the CE/CSI input has to be LOW for the evaluation of the ringer signal otherwise the dialler will enter the ON-LINE state.

Before the dialler circuit can evaluate and check the ringer signal, it has to be powered out of the ringer signal, available at the A/B terminals, via pin V_{DD}. The V_{DD} regulator functions as a shunt stabilizer to keep V_{DD} at 3.3 V. The capacitor C_{VDD} should be able to keep the V_{DD} voltage at level when the ringer voltage drops between the signal bursts.

3.3.2 Melody and Volume

When the ringer signal is valid, the MDY/TONE output delivers a melody. This melody follows the cadence of the ringer signal. The signal at pin MDY/TONE is a square wave. Four different melodies are available which can be selected using keys [1] to [4] (*only during ringing*). The melody frequency and duration are given in table 2 “Ringer melodies” in datasheet [1]. Only the basic DTMF frequencies are used.

The signal level of the ringer melody at output MDY/TONE can be controlled using keys [5] to [8]. These (peak to peak) levels are 3.2 V, 2.0 V, 1.4 V and 1.1 V corresponding to voltage levels across the buzzer with an attenuation of respectively 0 dB, −6 dB, −12 dB and −18 dB typically.

The last selected melody (keys [1] to [4]) and ringer volume (keys [5] to [8]) will be stored in RAM and used again when the dialler enters the RINGER state again. It is important that the V_{DD} voltage level remains above 1.2 V even when the dialler has been in the STAND-BY state. Otherwise the previous stored settings are lost.

4. APPLICATION EXAMPLE

An application example is also described in this report. This example is a general purpose application for exchanges with voltage regulation. For exchanges with current regulation (European TBR21 requirement) see [4]. All possible hardware stages such as DTMF indication (LED driver), DMO stage and gain boost are drawn in the application diagram. The set-maker can develop a user-specified telephone set quickly by composing the UBA2050(A)/51(A;C) with one or more stages. Only some fine tuning is required to fulfil specific country requirements.

Demonstration board OM5840 [3] is a good example for this application. In this chapter the functionality of this board is explained and evaluated.

The UBA2050(A)/51(A;C) denotes the types UBA2050, UBA2050A, UBA2051, UBA2051A, UBA2051C. Unless specified, these types will hereafter be referred as UBA2051. In case that a hardware stage is described in this chapter the appropriate type should be used for proper connection.

4.1 Description of the application

The application example for a low-cost basic telephone set is shown in Fig.51 and Fig.52. It is build up with the UBA2051 transmission/dialler/ringer IC and a discrete ringer output stage with PXE buzzer. The interconnections between both figures are indicated. The application offers the following features:

- High performance line interrupter (or low-cost line interrupter)
- Transmission functions with adjustable parameters as described for the transmission part in chapter 3.
- Pulse, DTMF and mixed mode dialling, redial, 13-number repertory dialling as specified in ref. [1]
- Ringer signal detection and melody generation
- DMO function
- LED output for DTMF dialling indication
- Gain boost
- Keytone generation (not shown but separately explained)

The application is build up around the UBA2051. The individual settings of the UBA2051 are for 600 Ω set impedance and 2.0 V minimum operating voltage (V_{DD}) for the dialler part at dialling. The several blocks of the application are briefly described in this chapter. Details concerning the performances are given in section 4.2.

Polarity guard and protection

One diode bridge D2 to D5 is applied for the transmission part as well as for the ringer stage to ensure proper functioning independently of the polarity of the line voltage respectively to rectify the ringer signal. Protection against excessive current surges is achieved by a break-over diode D1 (BR211_220) between the A-B/B-A terminals. The current limiter R_{prot} and TR2 provides protection against current surges exceeding about 150 mA. It is not designed for continuous limitation of the line current.

According to the UBA2050(A)/51(A;C) specification, the voltage on most of the pins of the transmission part may not exceed about 12 V. To prevent this a voltage regulator diode Z1 (BZD23C_10 V) is connected between LN and GND. Z1 limits also this voltage during start-up at higher line currents (> 40 mA).

The voltage across the ringer output stage is limited at about 20 V by means of the zener diode Z5, diode D6 and 3.3 V_{typ} via the V_{DD} pin of the UBA2051. V_{DD} is limited by the shunt stabilizer of the UBA2051 at 3.3 V_{typ}.

High performance line interrupter

In view of lowest DC-mask, a high performance line interrupter is applied in this application. The interrupter is directly controlled by the $\overline{DP/FL}$ output of the UBA2051. The $\overline{DP/FL}$ output from the dialler is an open drain output and is high-impedance when the reset of the dialler is active.

When the set goes off-hook using the cradle switch (S1), line current flows through resistor R_{prot} and P-MOST FET TR1. In this situation the gate-source voltage of TR1 is negative and the P-MOST conducts. TABLE 4 shows the properties of the interrupter.

TABLE 4 P-MOST line interrupter properties

Advantages (+)	Disadvantages (-)
powerless switching	MOS handling required
low ohmic on-resistance	higher cost than bipolar
lowest DC-mask	few vendors
adjustable over-current protection	
no influence on set impedance	
no base current loss	

The voltage drop across the interrupter is shown in Fig.35. It can be calculated by the line current times the on-resistance of the interrupter measuring about 14 Ω including the 3.9 Ω protection resistor. This voltage drop increases the total DC slope-resistance of the set (R_{SLPE} = 20 Ω) to about 40 Ω. The interrupter has no influence on the set impedance due to the relative low ohmic on-resistance from LINE to LN and the relative high ohmic control circuitry between LINE and VEE.

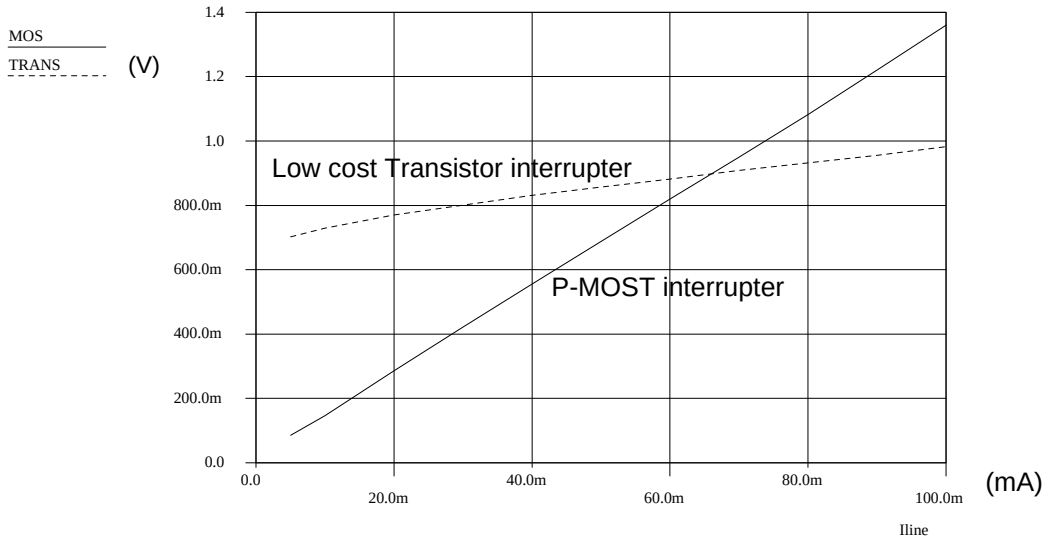


Fig.35 Voltage drop across interrupters, including 3.9 Ω R_{prot} resistor

Low-cost line interrupter

A low-cost line interrupter can be made according to Fig.36. It is a transistor-driven line interrupter consisting of 3 transistors TR1, TR2, TR3 and 3 resistors R1, R2 and R3.

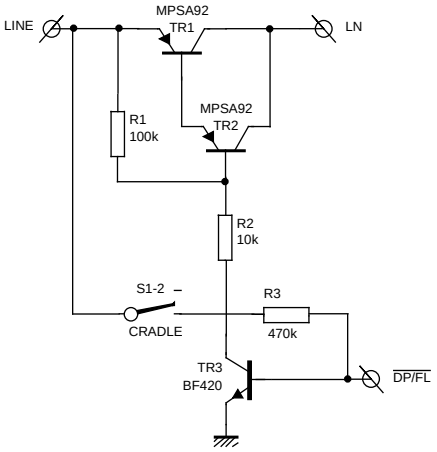


Fig.36 Low-cost line interrupter

At off-hook a small current will flow through R1 and R2 to GND via TR3 when the $\overline{DP/FL}$ is HIGH. Consequently, TR1 and TR2 conduct. The set impedance will be affected by the low ohmic value of R2; its value has to be as high as possible. However, R2 has to be low enough to keep TR1 and TR2 into saturation over the whole line current range. R1 decreases the switch-off time off the interrupter.
TABLE 5 shows the properties of the interrupter.

TABLE 5 Low-cost line interrupter properties

Advantages (+)	Disadvantages (-)
low cost	high voltage drop at low line currents
many vendors	R2 affects AC impedance
	1 transistor extra

Line current interruption is achieved by a LOW level on pin $\overline{DP/FL}$. The $\overline{DP/FL}$ output from the dialler is an open drain output and is high-impedance when the reset of the dialler is active.

The voltage drop across this type of interrupter as a function of line current is also shown in Fig.35.

Speech / transmission

The transmission part of the UBA2051 stabilizes the DC voltage between LN and SLPE. It delivers the supply voltage V_{CC} for internal use and for the connected electret microphone. Also the integrated V_{DD}-regulator supplied from V_{LN} delivers supply for the dialler part and possible connected peripherals. V_{CC} is buffered by C_{VCC} while V_{DD} is buffered by C_{VDD}. The set impedance will be mainly determined by the impedance of the network between LN and V_{CC}. This application has a set impedance of about 600 Ω realised by R_{set1} = 620 Ω,

R_{set2} = 0 Ω and not applied C_{set}. A complex set impedance can be realised by means of the complex network R_{set1}, R_{set2} and C_{set}. Take into account the increased DC resistance between LN and V_{CC} at complex networks which decreases the supply performance of V_{CC}.

The application is intended for use with an electret microphone and dynamic earpiece. Use of another electret microphone requires a modification of the application. The attenuation between microphone and IC has to be adapted by the network: Rtx1, Rtx2, Rtx3, Ctx1 and Ctx2. Earpiece gain is adjustable by the gain boost network: R_{GAR1}, R_{GAR2}, C_{gb}, R_{gb1}, R_{gb2} and R_{gb3}. Microphone and earpiece arrangements are detailed described in ref. [1].

Buffer capacitor C_{VCC} is discharged rapidly during the break periods at pulse dialling with the result that the V_{DD} buffer capacitor C_{VDD} will not be charged during these periods.

One Pin Oscillator

All UBA205x types have a one pin oscillator with an integrated load capacitance of typ. 18pF (Cosc) and a typical negative resistance of -6kΩ (Rosc). The resonator (crystal or ceramic) has to be connected between XTAL and GND. For generating the correct DTMF tones, the resonator should be a 3.579545 MHz type. Connecting a ceramic type will give more frequency deviation, but can still fulfil the requirements (Murata CSA 3.58 MG or AVX Kyocera KBR 3.58 MSA). When using a ceramic resonator, additional components may be required depending upon the ceramic resonator specifications (refer to product type specification). By connecting a few pico-farad in parallel with the resonator the oscillation frequency can be decreased. By connecting a few ten pico-farad in series with the resonator, the oscillation frequency can be increased.

For a specified ceramic resonator the following formulas can be used to calculate the oscillation frequency (see Fig.37):

$$f_{osc} = \frac{1}{2\pi \cdot \sqrt{L_s \cdot C_{tot}}}$$

$$C_{tot} = \frac{C_s \cdot (C_p + C_{osc})}{C_s + C_p + C_{osc}}$$

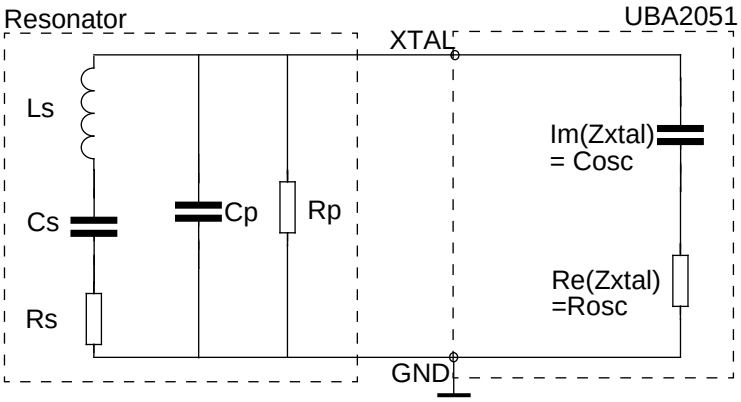


Fig.37 Resonator equivalent circuit connected to one pin oscillator.

Oscillation will only occur when the sum of Rosc and the series resistance of the resonator Rs is negative. However this internal Rosc is affected by Cp and Rp of the resonator. To calculate the remaining Rosc the following procedure must be used.

The series circuit Xosc, Rosc is transformed into a parallel circuit X_x and R_x

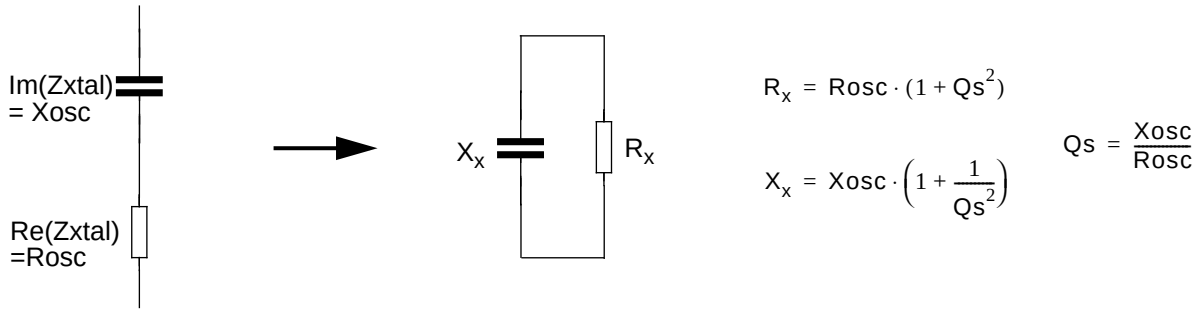


Fig.38 Series to parallel transformation

The influence of the resonator parallel resistance Rp and capacitance Cp (=Xp) is added to X_x and R_x. Suppose that the resonator manufacturer guarantees a minimum value of Rp (not relevant for a quartz-crystal) and a maximum value for Cp.

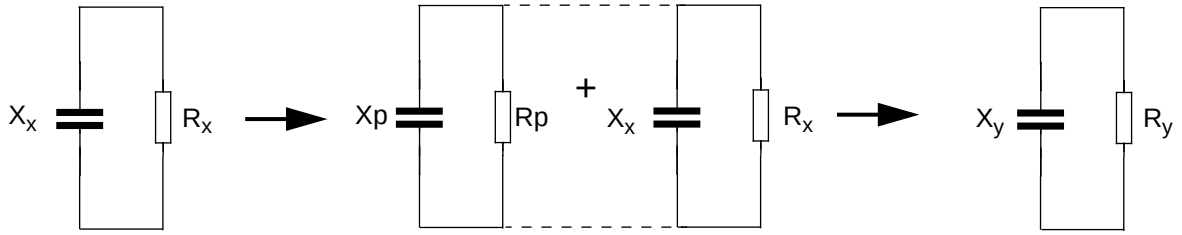


Fig.39 Correction for Rp and Cp

The corrected parallel circuit is transformed back into a series circuit X_z and R_z

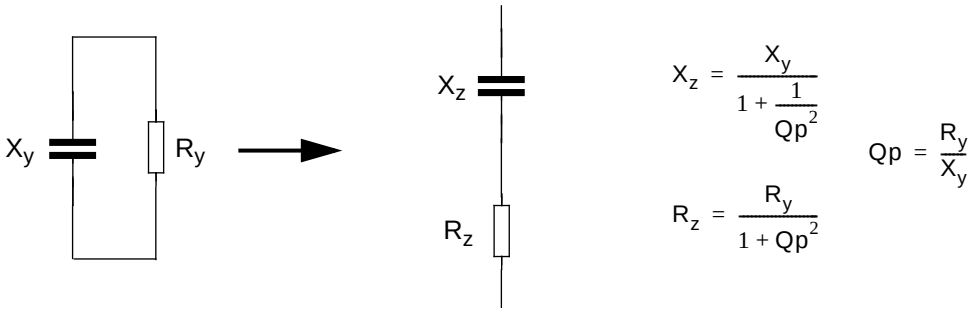


Fig.40 Parallel to series transformation

For oscillation the sum of R_z and Rs should be negative.

EXAMPLE:

UBA2051:
Cosc = 18 pF;
Rosc = -6 kΩ

Resonator: (Murata CSA3.58MG see [9])
Ls = 360.6 µH Cp = 40.32 pF
Cs = 5.99 pF Rp = 500 MΩ
Rs = 6.7 Ω

f_{osc} = 3.596039 MHz : Δf = +0.46% => Xosc = - j2459; Xp = - j1098
X_z = - j1010
R_z = - 149 Ω => Rz + Rs = - 149Ω + 6.7Ω = -142.3Ω <= The sum is negative therefore oscillation will occur.

Dialler/Ringer

The dial parameters of the dialler part of the UBA2051 can be set by resistor options to specific-country requirements. A single contact keyboard is connected to the I/Os named R1-R4, C1-C4. Without repertory facility the UBA2050(A) can be used. Consequently, all repertory-related keys (STORE, MEM, M1, M2 and M3) have to be removed.

Reset is performed by the internal reset of the UBA2051. Output $\overline{DP/FL}$ drives the interrupter to perform pulse dialling (set with resistor option R_{PTS}) and flash function. The position of cradle switch S1 determines the CE/CSI level during STAND-BY state (CE/CSI = LOW) and ON-LINE state (CE/CSI = HIGH).

Input CE/FDI is connected to A/B line via the network C_{ring}, Z4 and R_{FDI} to detect the operation state of the UBA2051 in combination with CE/CSI. Frequency discriminator network Z4, R_{FDI} and R4 in combination with threshold of the CE/FDI input detects a ringer signal from the A/B line with minimum frequency of 13 Hz at a minimum ringer voltage of 18 V_{rms}.

Output MDY/TONE delivers the melody for the ringer circuit (in ringer mode) and the DTMF dialling signal to the DTMF input of the transmission part (in conversation mode) via attenuator C_{dtmf}, R_{dtmf1} and R_{dtmf2} as shown in Fig.41. The capacitor blocks the DC component. The calculated attenuation is 19.4 dB to which the input impedance on pin DTMF is also taken into account. The load of the external attenuator at output MDY/TONE is very large with respect to the output impedance (at MDY/TONE) of the tone generator.

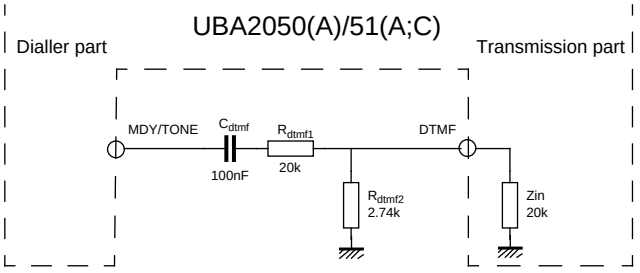


Fig.41 DTMF attenuation network

Ringer circuit

The ringer signal from the line is available on the CE/FDI input of the UBA2051 via capacitor C_{ring}, zener diode Z4 and resistors R_{FDI} and R4. Only the positive swing of the ringer signal is offered to this pin.
The minimum ringer voltage depends on the network and the threshold of the CE/FDI input and is approximately 18 V_{rms}. The voltage discriminator (Z4, R_{FDI} and R4) takes care for this voltage.

When CE/FDI is provided with valid ringer pulses (frequency and level) and CE/CSI is kept LOW the dialler part enters the RINGER state immediately. For this, the V_{DD} capacitor should be kept charged during STAND-BY state to speed-up initialization of the dialler part at incoming ringer signals. Supply of the ringer stage is delivered by the ringer signal from the exchange via the diode-bridge D2 to D5 and the series network C_{ring}-R_{ring}. The supply voltage for the ringer stage is limited by the zenerdiode Z5. This diode is cascaded with diode D6 and the V_{DD} regulator resulting in V_{RR}-max = 20 V. The energy is stored into supply capacitor C_{VRR}.

The ringer buzzer is driven by the three transistors TR4 to TR6. Due to capacitive behaviour of the buzzer, it will be charged and discharged repeatedly by means of transistors TR4 resp. TR5. The volume of the ringer sound is controlled by means of the keys [5] to [8] via amplitude control of the MDY/TONE signal. The basic adjustment of the ringer sound can be done by resistor R_{VOL}. Resistor R_{MDY} limits the current from pin MDY/TONE. Furthermore, the ringer melody can be changed by means of the keys [1] to [4].

DMO stage

UBA2050 and UBA2051 (not UBA2051(A;C)) supports the DMO (dial mode output) function in pulse dialling mode. In DMO mode the DC resistance respectively the voltage between A/B terminals is reduced. The DMO stage is shown in Fig.51 and consists of zener diode Z3, MOSFET (TR7) and resistor R_{DMO}.
By changing zener diode Z3 by an other voltage type, the voltage between the A/B lines during the pulsed digit can be adjusted.

The DMO circuitry is driven by the DMO output of the dialler. This output is a push-pull output and is LOW when the reset of the dialler is activated. TR7 conducts when DMO output is HIGH. The voltage between the A/B terminals will be about 6.0 V when DMO stage is activated.

LED arrangements

Two LED connection arrangements are shown in Fig.42 which can be applied with the A-version only of the UBA205XA family.

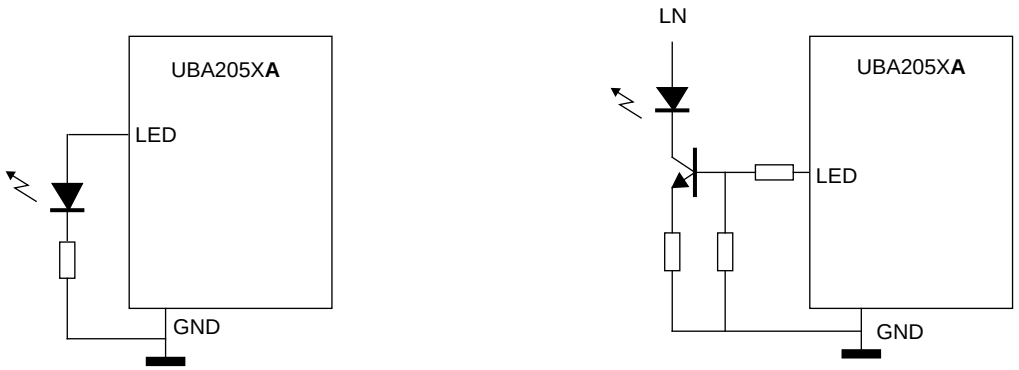


Fig.42 LED arrangements

The LED (low current type) can be supplied directly from the LED output when sufficient supply current is available from V_{DD} (max.1.9 mA). In the other case, LN can be used to supply the LED by means of a current source as shown in the right hand diagram of Fig.42. This circuit has no influence on the set impedance. Both circuits are available in the application of Fig.51 and Fig.52, selectable by jumpers.

Gain boost selection

As described in datasheet [1], the earpiece gain from RX to QR can be set between −14 dB and +12 dB (see Fig.18). Resistor R_{E2} adjusts the gain from −14 to 0 dB while a network of R_{E21}, R_{E22} and R_{E23} replaces this resistor to boost the gain from 0 to 12 dB. Resistor R_{E1} has a preferred value of 100 kΩ. The gain between IR and RX is fixed at 33.4 dB. Take into account that the sidetone network attenuates the receive signal from LN to input IR with 32 dB.

The gain boost network as shown in Fig.52 can boost or attenuate the earpiece gain using the jumpers J8 to J10. TABLE 6 shows the gain boost selection. The overall voltage gain is in the range from −6 to +6 dB. Refer to [1] for more information about gain boost calculation.

TABLE 6 Gain boost selection

Jumper placed	R_{gb}	Gain (RX to QR)	Gain (LN to QR)
None	-	–7 dB	–5.6 dB
Only J8	18.2 kΩ	–3 dB	–1.6 dB
Only J9	7.15 kΩ	+1 dB	+2.4 dB
Only J10	3.65 kΩ	+5 dB	+6.4 dB

The dynamic earpiece of the handset is connected between the terminals EAR+ and EAR–.

Keytone buzzer

The keytone output is only available with the UBA2050(A) and UBA2051C. The keytone signal can be made audible in two ways as shown in Fig.43 which are not supported by the application of Fig.51 and Fig.52.

According to Fig.43, a keytone buzzer can be connected directly to the KT output or the keytone signal can be coupled into the receive path to make it audible by the earpiece.

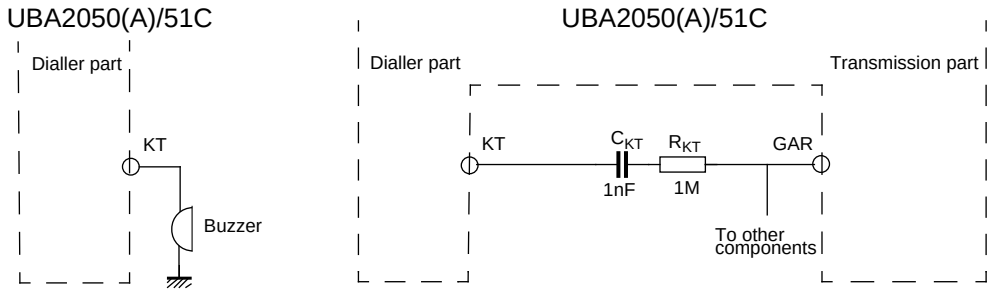


Fig.43 Keytone arrangements

For the left handed option, max. 1.9 mA can be delivered to the buzzer when sufficient supply current is available from V_{DD}. Buzzer KPE-167 from Kingstate or PKM34EW from Murata can be applied.

The right handed solution is the cheapest one that uses only two components. Components values of 1 nF and 1 MΩ are based on a cut-off frequency of 160 Hz. It is important to use a high value for the resistor R_{KT} otherwise the gain of the receive path will be affected.

4.2 Settings and performance of the application

4.2.1 DC behaviour

DC settings

The DC voltage at the A/B-B/A terminals is a result of the voltage drop across the UBA2051, the line interrupter and diode bridge. The voltage drop across the UBA2051 depends on the setting of the reference voltage (V_{ref}) between LN and SLPE and the voltage drop across R_{SLPE} which depends on the line current.

Important for the minimum line voltage (A/B-B/A) is the minimum supply voltage V_{DD} required by the dialler. V_{DD} is supplied by V_{LN} which depends on the resistors R_{reg1} or R_{reg2}. Both resistors are not placed in the application to change V_{ref}; resulting in a default value of V_{ref} = 4.15 V.

The A-B/B-A voltage measures 6.2 V at 20 mA line current, while V_{CC} = 3.6 V and V_{DD} is stabilized at 3.3 V. DTMF as well as pulse dialling can be achieved. The V_{DD} level will be below the stabilised level of 3.3 V at break-periods during pulse dialling and flash.

Fig.44 shows the line voltage $V_{A/B}$ across the A/B-B/A terminals as a function of line current I_{line} with R_{reg2} is not placed as well as with R_{reg2} = 40 kΩ.

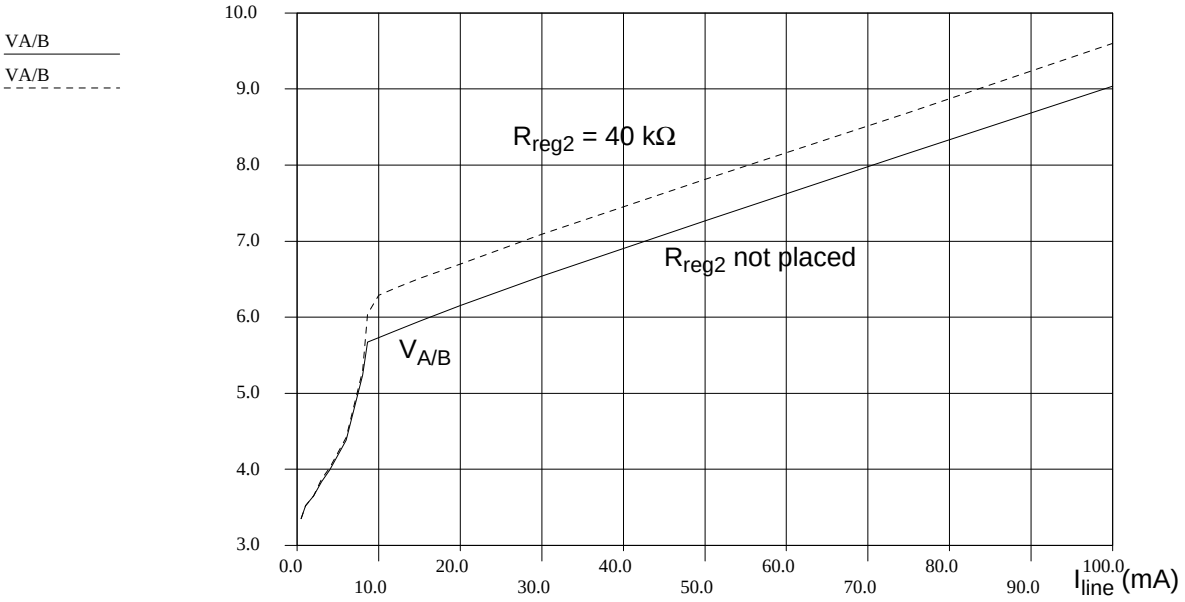


Fig.44 Line voltage across the set as a function of line current

Supply possibilities

V_{CC} can be used to supply peripherals e.g an electret microphone. The possibilities are rather limited and depend in general of the LN-SLPE setting, the DC resistance of the network between LN and V_{CC} and the total current consumption from V_{CC}. It is also possible to supply peripherals by V_{DD}. Max. output current is 1.9 mA because the dialler part is also supplied from V_{DD} and requires current when generating DTMF tones. The dialling functions, DTMF and pulse dialling, are operational according the specification down to I_{line} is about 6 mA, while transmit and receive are possible down to about 3 mA.

In STAND-BY state (on-hook) the repertory numbers have to be stored. A minimum of 300 nA at V_{DD} = 1.2 V is specified for memory retention. Consult Fig.11 for the internal current consumption at low V_{DD} levels. Providing supply to V_{DD} pin is achieved by the series network: $R_{trickle}$, D3, S1-2, R6 and D6. It is adjusted for exchange with voltage of 48 V. Depending on PTT requirements the resistor $R_{trickle}$ can be modified to provide less or more current I_{DD} from the line in on-hook state.
Remark: during on-hook, peripherals on V_{DD} can influence the memory retention! Therefore during on-hook peripherals should not drain any current from V_{DD}.

4.2.2 Transmission

Set impedance and BRL

A set impedance of 600 Ω is realised with R_{set1} = 620 Ω, while for complex set impedance a complex network between LN and V_{CC} has to be realised.

Fig.45 shows the BRL (dB) of a '600 Ω set' measured with 600 Ω reference. In the same graph is given the BRL (dB) of a 'complex set' consisting of R_{set1} = 825 Ω, C_{set} = 115 nF and R_{set2} = 220 Ω measured with a reference impedance of 825 Ω // 115 nF + 220 Ω. In this case, the value of C_{REG} is increased up to 6.8 µF to reach a BRL of > 18 dB at 300 Hz

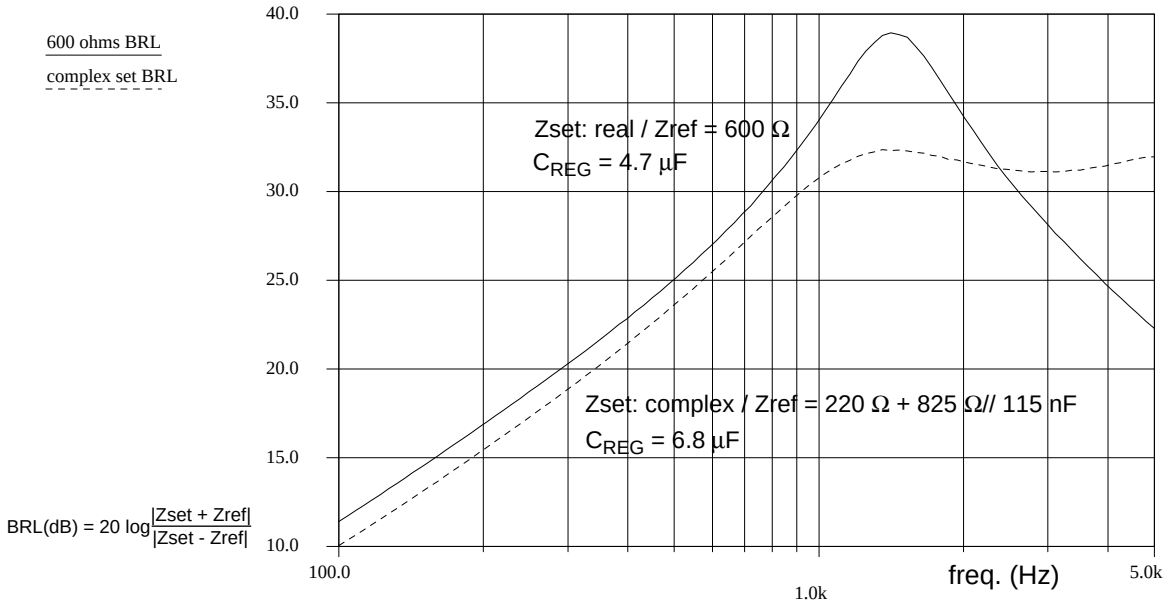


Fig.45 BRL of application example at 'real' and 'complex' termination

Send and receive

This application is intended for use with an electret microphone. The total gain from microphone terminals to the line measures 26 dB at 600 Ω set impedance and 600 Ω line load without activated AGC function. The internal gain setting is 44.2 dB typical, while an attenuation of about 18 dB is achieved by network (Ctx1, Ctx2, Rtx1, Rtx2, Rtx3), input impedance (Zi(MIC)) and EMC components (C103 and C104).

The maximum swing of the line signal measures 8.4 dBm at THD = 2% (10 dBm at 10%) over the frequency range 300 Hz - 3400 Hz, at 600 Ω set impedance, 600 Ω line load and 20 mA line current. A capacitor of 1 nF (Cint) is placed between the gate-source of TR1 to keep TR1 conducting at negative swings of the line signal. It improves the maximum swing of the line signal at lower frequencies.

The overall receive gain from line to earpiece is about −6 dB at an earpiece impedance of 150 Ω. This is due to the attenuation of 32 dB from line to IR input, the internally determined gain of the receive stage of 33.4 dB typically and the (externally adjustable) gain of the earpiece amplifier of -6.4 dB. The gain values are given without activated AGC function and without gain boost.

Depending on jumpers J8 to J10 (shown in Fig.52), the overall receive gain can be determined. See "Gain boost selection" on page 52.

Side tone / AGC

Reproduction of the (electrical) microphone signal in the earpiece is reduced by the anti-sidetone circuit consisting of the components R_{ast1}, R_{ast2}, R_{ast3}, R_{bal1}, R_{bal2} and C_{bal}. The principle of the applied TEA111x (or TEA106x) family bridge is given in chapter 3.1.10 and fully described in [6].

In case AGC is not applied (pin AGC open) the anti-sidetone circuit has to be re-calculated for a mean cable length of < 5 km. Re-adjustment of the balance circuit is necessary for other cable types, different line length, etc.

4.2.3 Dialling

DTMF dialling

The DTMF signal from the MDY/TONE output of the dialler part is attenuated by the network R_{dtmf1}, R_{dtmf2} and C_{dtmf} and applied to the DTMF input of the transmission part. During dialling the signal is amplified by the DTMF stage and transferred to the line resulting in a total level of approx. –4 dBm at 600 Ω set impedance and 600 Ω line load. The gain of the DTMF stage is 26 dB typical.

Pulse dialling / Flash

The line current will be interrupted by the electronic interrupter (TR1) under control of the $\overline{DP/FL}$ signal. During the break-periods of the dialled digit (or flash) the UBA2051 has to be supplied by the stored energy of C_{VCC} and C_{VDD} because they will not be charged during these periods. The value of buffer capacitors C_{VCC} and C_{VDD} have a value of 100 µF resp. 220 µF to keep the V_{DD} supply level at > 2.0 V.

Fig.46 shows the voltage at the A/B-B/A terminals, supply voltages V_{CC} and V_{DD} and the line current during dialling of a digit [8]; V_{exch} = 48 V.

Fig.47 shows V_{DD} and V_{CC} during the maximum selectable FLASH time of 600 ms. The V_{DD} voltage is reduced to about 2.1 V.

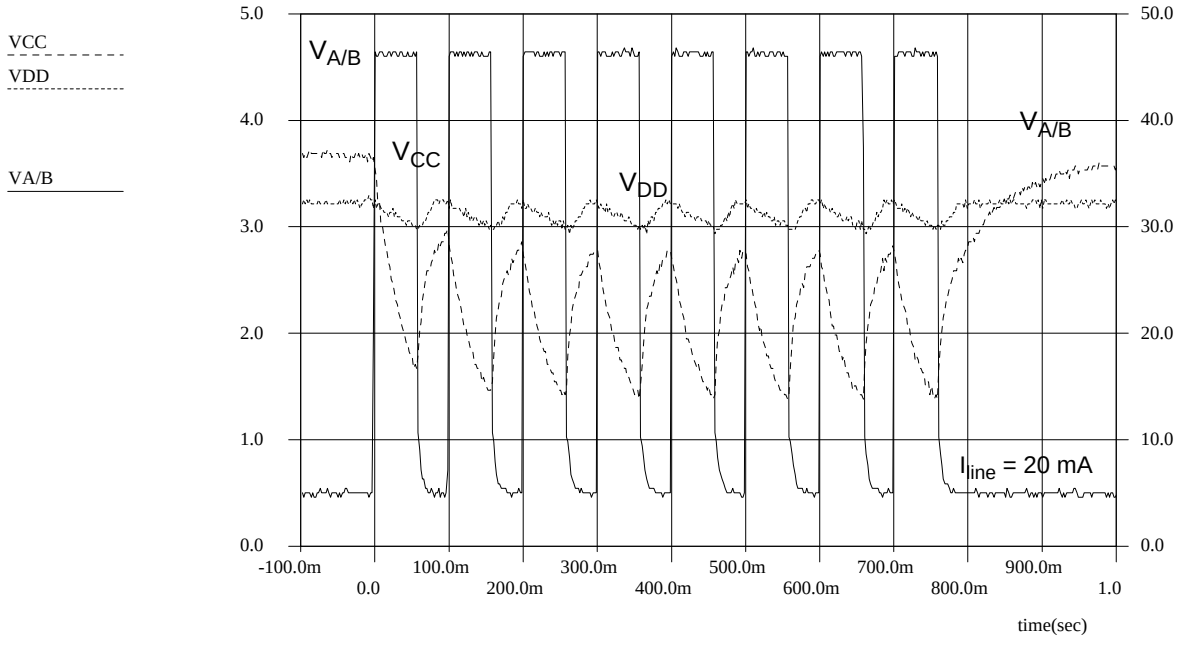


Fig.46 Behaviour of V_{CC} and V_{DD} during pulse dialling of digit [8]

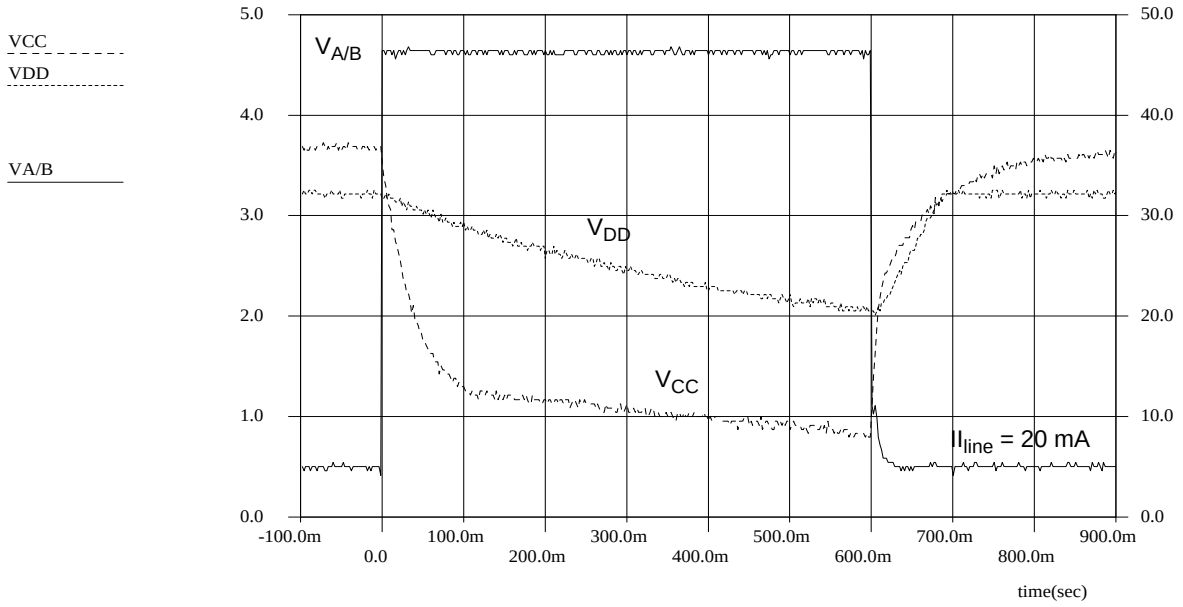


Fig.47 Behaviour of V_{CC} and V_{DD} during a flash of 600 ms

4.2.4 Start-up and Disconnect

Off-hook start-up

Fig.48 (V_{LN}, V_{CC}, V_{DD} and $V_{A/B}$ as function of time) shows the start-up behaviour after off-hook (outgoing call) at I_{line} = 20 mA. At t < 0 the line current I_{line} = 0 mA while all supply capacitors and C_{REG} have been discharged. When I_{line} starts flowing, the voltage at LN will be clamped by the protection zener Z1 at about 10 V. When V_{CC} is about 2.2 V the line voltage stabilizer becomes operational. See datasheet [1] for more information.

After connecting the application with the line supply the very first time, the handset has to be lifted to charge the supply capacitors C_{VDD}. The set is operational within 200 ms at 20 mA line current. In STAND-BY state the V_{DD} capacitor C_{VDD} is kept charged by $R_{trickle}$. The DC current in this state has to be more than 300 nA.

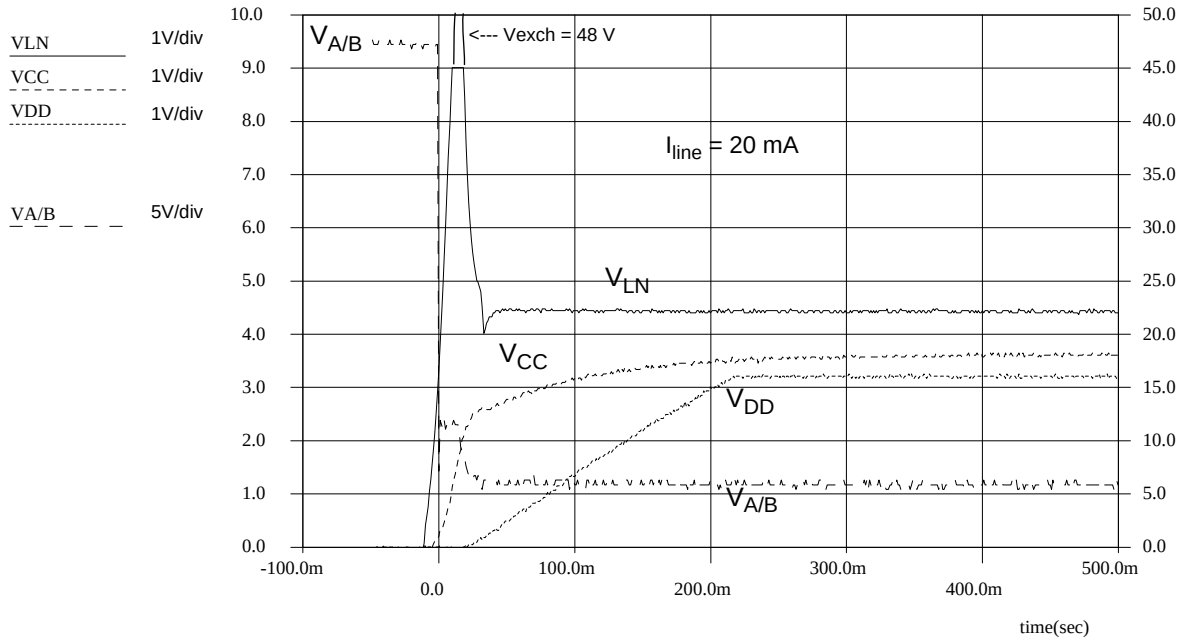


Fig.48 Start-up after off-hook; IC-voltages and line voltage $V_{A/B}$

Line disconnect

When the handset is placed on the cradle (on-hook) and the dialler is ON-LINE state or RINGER state at t = 0, the dialler will detect a line break. After a waiting time (the reset delay time) of 280 ms the dialler goes into STAND-BY state. The V_{DD} will decrease slowly to an end-level of about 1.5 V.

Ringer start-up

Fig.49 and Fig.50 shows the start-up behaviour after a ringing burst (incoming call) at a discharged C_{VDD} capacitor respectively charged C_{VDD} (V_{DD} ~ 1.5 V) and at a AC ringer voltage of 35 V_{rms} and f = 50 Hz. C_{VRR} was discharged in both cases. When the ringer voltage goes high, the capacitor C_{VRR} starts charging via capacitor C_{ring}, resistor R_{ring} and diode bridge D2-D5. Also the voltage of capacitor C_{VDD} rises from 1.5 V to 3.3 V via zener diode Z5 and diode D6. As soon as V_{DD} reaches 2.0 V (V_{POR}; Power On Reset level) the dialler starts and monitors the pin CE/FDI (see Fig.29 and Fig.30) whether the ringer signal is still present.

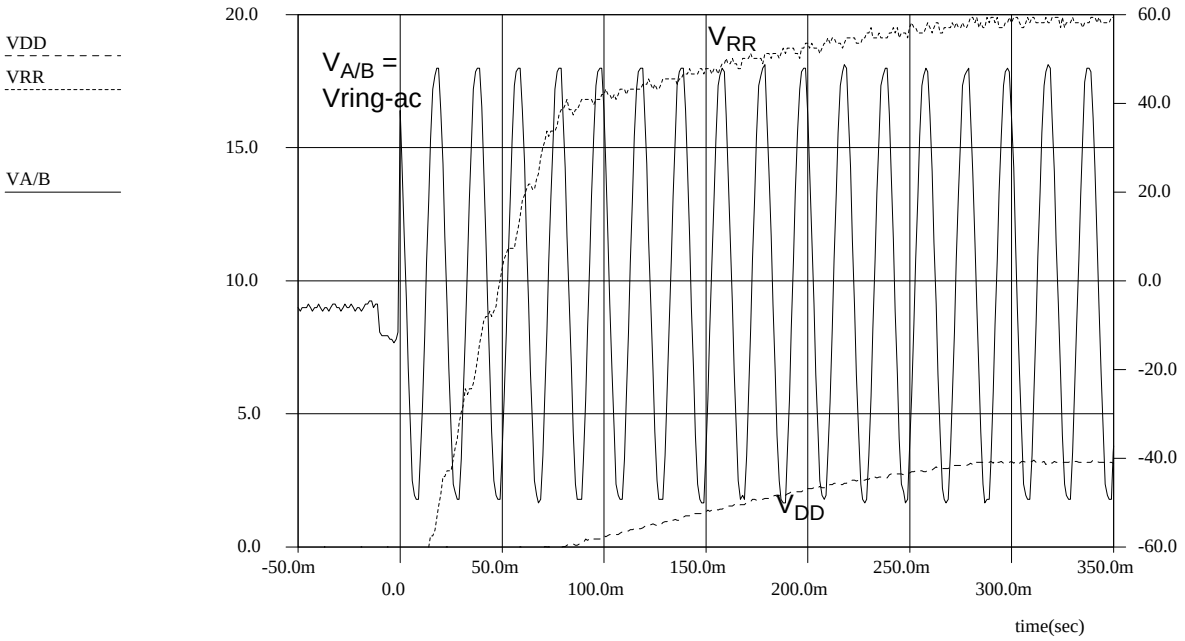


Fig.49 Ringer start-up; V_{DD} capacitor discharged before start-up

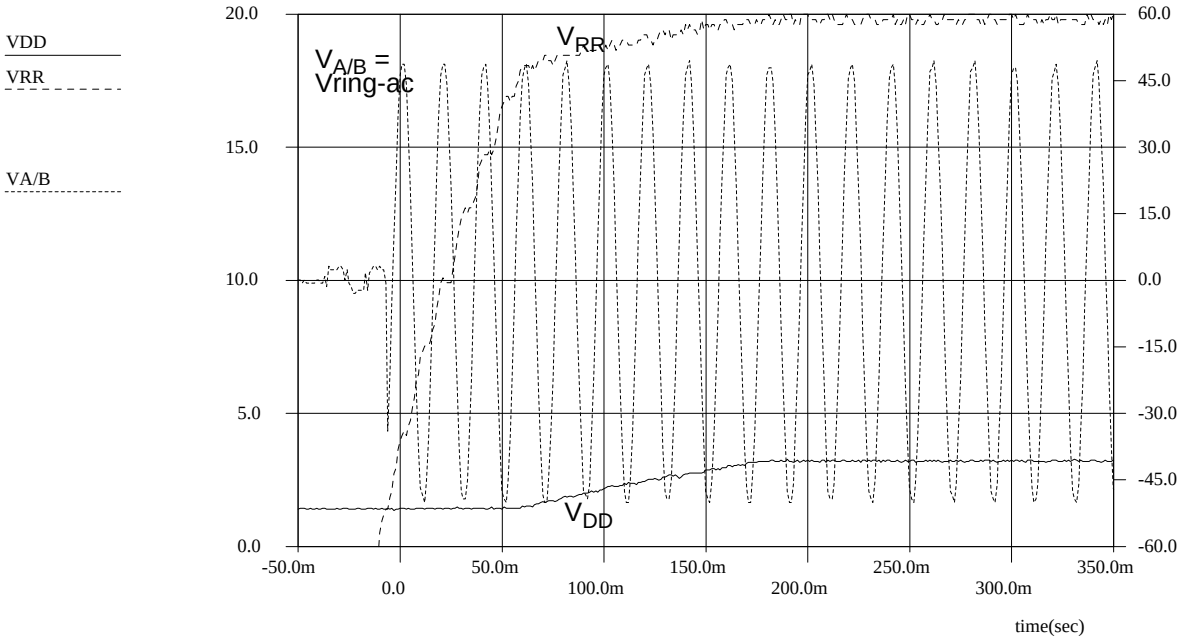


Fig.50 Ringer start-up; V_{DD} capacitor charged before start-up by means of $R_{trickle}$

5. ELECTROMAGNETIC COMPATIBILITY

The UBA2050(A)/51(A;C) has been designed with on-chip measures to keep RF disturbances away from sensitive circuit parts at higher RF frequencies (> 80 MHz). For the lower frequency range (from 150 kHz upwards) the coupling into the IC occurs mainly via the A/B-lines and the handset cord. Improvement of the immunity at those frequencies can be realised by filtering at the PCB connectors and IC pins and a PCB layout which is designed with respect to EMC.

The demonstration boards (OM5839 and OM5840, see [2] resp. [3]) have a single-sided wiring with filled ground plane between the interconnections. The EMC measures on the PCB are:

- Filtering from A/B-B/A terminals to line input LN of the UBA2050(A)/51(A;C) by means of C100 at the line terminals, C101 from pin LN to GND.
- Filtering from the PCB terminals MIC-/MIC+ to the MIC inputs of the IC by C105 and C107 at the PCB terminals, series resistors Rtx1 and Rtx2 and decoupling at the MIC pins by means of C103 and C104.
- Filtering from the PCB terminal TEL to QR output of the IC by C106 at the PCB terminal.
- Filtering of the receiver channel at input IR by C102. Furthermore is the bandwidth of the receiver amplifier limited by C_{GAR} and stability guaranteed by means of the combination of C_{GAR} and C_{GARS}.
- Decoupling capacitor C_{VDD} via short connection to pin V_{DD} **AND** GND.

General recommendations of EMC measures to design the PCB are:

- Use a filled ground between the wires in case of a single-sided PCB or a ground plane when a double-sided PCB is applied.
- Place line and handset connectors close to each other on the same side of the PCB and decouple the connections by means of EMC capacitors.
- Place EMC capacitors as close as possible to the corresponding IC pins. Use small size ceramic capacitors.
- Make interconnection-wires as short as possible. Use wire-bridges instead of a clever design with long wires.
- Design a symmetrical microphone entry from connector to MIC inputs of the IC.

6. HINTS FOR PRINTED CIRCUIT BOARD LAYOUT

Care must be taken to avoid that the large line current flows into common ground tracks to which sensitive points (such as amplifier inputs) are connected. For this reason special attention should be paid to the pins LN and SLPE of the UBA2050(A)/51(A;C) which conduct almost the complete line current. The copper tracks connecting the external components to the corresponding IC-pins should be kept as short as possible.

The ground connection of all RFI-capacitors should be realized by means of as large as possible copper planes or grids. RFI-capacitors must be connected as close as possible to the pins that have to be decoupled.

The ground plane on the circuit board must be kept as large as possible where every copper area must be connected to the ground-plane (or grid) on at least two points.

An “RF-guard” as described in chapter 5 can be realised. An example of a printed circuit board layout for the UBA2050(A)/51(A;C) can be found in [2] and [3].

7. APPLICATION COOKBOOK

This chapter gives the adjustment steps to realise a basic application with the UBA2050(A)/51(A;C). Referring to Fig.51 and Fig.52, the design flow is given as a number of steps which should be made. As far as possible for every step, the components involved and their influence on every step are given.

Step	Adjustment
DC setting: Adjust the DC setting of the UBA2050(A)/51(A;C) to the local PTT requirements.	
Voltage LN-GND	This voltage can be adjusted by changing V_{ref}: increased up to 7 V with the R_{reg2} resistor between pins REG and SLPE (or decreased down to 3 V with the R_{reg1} resistor between REG and LN).
DC slope	The DC slope might be modified by changing the value of R_{SLPE} (this is not advised: a lot of parameters are changed too). A relative small increase of the DC slope can be realised with a resistor in series with LN
Supply point V_{CC}	Depends on the values of V_{ref} and the resistive part of the network between LN and V_{CC} (R_{set1} + R_{set2}).
Artificial inductor	Its value can be adjusted by changing the value of C_{REG}: BRL at the lower frequencies can be improved by a higher value in case of complex set impedance; it has, however, a negative effect on start-up behaviour.
Microphone supply	The current through the electret microphone is adjusted by means of the resistors R_{micp} and R_{micm}. Extra supply decoupling is advised by means of R_{feed} and C_{feed}.
Impedance and sidetone: After setting the required set impedance, the sidetone has to be optimized using the sidetone network in order to minimize the loop gain in all line conditions. AGC can be adjusted at that step.	
Set impedance	The BRL is adjusted with the impedance network connected between LN and V_{CC} (R_{set1} + R_{set2}//C_{set}). Take into account the total DC resistance between LN and V_{CC}.
Sidetone	Adjust Z_{bal} (R_{bal1}, R_{bal2}, C_{bal}) according to the line characteristics.
AGC	Internally defined, the characteristics (I_{start} and I_{stop}) can be shifted to higher line currents with an external R_{AGC} resistor connected between AGC and GND. In case it is necessary to shift I_{start} and I_{stop} to lower current values, the value of R_{SLPE} must be increased proportionally (see section 3.2.5; a lot of other parameters are changed too).
DTMF gain	
DTMF	The network C_{dtmf}, R_{dtmf1} and R_{dtmf2} determines the attenuation before entering the DTMF pin. The internal DTMF gain is fixed.

Step	Adjustment
Microphone and receive gains	
Microphone gain	The microphone gain of the application has to be adjusted before entering pins MIC+/MIC- of the UBA2050(A)/51(A;C). It can be reduced by using the resistor Rtx3 which forms a bridge attenuator with Rtx1 and Rtx2. Ctx1, Ctx2 form a high-pass filter with Rtx1, Rtx2 in series with the input impedance at MIC+/MIC-. A capacitor Cmic (connected between MIC- and MIC+ terminals) forms a low-pass filter with the impedance of the microphone and the resistors R_{micp}/R_{micm}.
Earpiece gain	The earpiece gain of the application has to be adjusted by means of the resistors R_{E1} and $R_{GAR1} + R_{GAR2}$ without gain boost. A capacitor in parallel with $R_{GAR1} + R_{GAR2}$ forms a low-pass filter, stability is ensured with capacitor $C_{GARS} = 10 \times C_{GAR}$ between pins $_{GAR}$ and GND.
Ringer stage	
Ringer voltage	The ringer voltage can be adjusted by means of the zener diode Z5.
Sound level	The level is adjusted by the resistor R_{VOL}. The ratio between R5 and R_{VOL} determines the gain. Maximum swing across the buzzer depends on the ringer voltage, the gain and the amplitude of the MDY/TONE signal (volume control).
DMO stage	
A/B voltage	The A/B voltage is in DMO mode adjustable with the zener diode Z3.

8. REFERENCES

[1] Philips Semiconductors DATA sheet UBA2050(A);51(A;C) “One-Chip telephone ICs with speech, dialler and ringer functions”.

[2] Philips Semiconductors User Manual ETT/UM99014, ‘User manual for OM5839: Demonstration board UBA2050(A)’, G. Knubben.

[3] Philips Semiconductors User Manual ETT/UM99001, ‘User manual for OM5840: Demonstration board UBA2051(A)’, G. Knubben.

[4] Philips Semiconductors Application Note AN96140, ‘TEA1112 for France’, J. Soree.

[5] Philips Semiconductors Data Handbook IC03a. “Semiconductors for Wired Telecom Systems”. Order number: 9397 750 00839

[6] Philips Semiconductors Data Handbook IC03b. “Semiconductors for Wired Telecom Systems”. Order number: 9397 750 00811

[7] IEC Publication DIS 1000-4-6 (formerly 801-6). Electromagnetic compatibility for electrical and electronic equipment. Part6: Immunity to conducted disturbances, induced by radio frequency fields above 9 kHz.

[8] IEC 1000-4-3 Draft International Standard (Annex B). Immunity to radiated, radio frequency, electromagnetic fields (formerly IEC 801-3).

[9] Murata Application Manual “Ceramic resonator (CERALOCK^{R})”, 30 May 1997 (P17E10.pdf)

APPENDIX 1 LIST OF ABBREVIATIONS AND DEFINITIONS

A/B-B/A	Line terminals of application example
AGC	Automatic Gain Control; line loss compensation facility
APT	Access Pause Time selection
BRL	Balance Return Loss
CE/FDI	Chip Enable / Frequency Discriminator Input
CE/CSI	Chip Enable / Cradle Switch Input
$\overline{DP/FL}$	(Inverted) Dial Pulse / FLash output
DTMF	Dual Tone Multi Frequency
EMC	Electro Magnetic Compatibility
Electret	Electret microphone with amplifier
GND	Ground reference
Gvrx	Gain factor of receive stage
Gvtx	Gain factor of transmit stage
I_{CC}	Current consumption (from V_{CC})
I_{led}	Current through the LED connected between LN and LED
I_{line}	Line current
I_{rec}	Current consumption of receive amplifier
I_p	Current consumption of the peripheral devices connected to V_{CC}
Ish	Excess of line current from LN to SLPE
I_{start}, I_{stop}	Start and stop currents of the AGC function
I_{th}	Threshold current of low voltage function
k	Scale factor of balance network
LED	Light Emitting Diode
L_{EQ}	Artificial inductor of voltage stabilizer
MBS	Make Break ratio Selection
[M1]-[M3]	Direct memory recall keys
MIC+/-	Microphone input
[MEM]	Indirect memory recall key
OM5839	Demonstration board for the UBA2050(A)
OM5840	Demonstration board for the UBA2051(A)
PCB	Printed Circuit Board
PTS	Pulse Tone Selection
PXE	Piezo Ceramic Buzzer Element
R_a	Resistor to adjust the sidetone bridge attenuation
R_{ast}	Anti sidetone resistor
RF	Radio Frequency
R_{exch}	Bridge resistance of exchange
Rgarint	Internal resistance (134 kΩ) to define receive gain
R_{GAR}	External resistance to reduce receive gain
R_P	Internal resistance (17.5kΩ) between LN and REG
[STORE]	Programming mode key

THD	Total Harmonic Distortion (%)
TONE	Tone generator output
$V_{A/B}$	Voltage across the A-B/B-A line terminals
V_{CC}	Supply for Transmission part and peripherals
V_{DD}	Stabilized supply for Dialler and Ringer part
V_{LN}	DC level at LN (with respect to GND)
V_{ref}	Stabilized reference voltage between LN and SLPE
V_{RR}	Supply node of the ringer stage
V_{SLPE}	DC level at SLPE
V_{exch}	Exchange voltage
XTAL	Oscillator input
Z_{IR}	Input impedance of receive amplifier
Zmic	Symmetrical input impedance of microphone amplifier
Z_{bal}	Balance network to reduce side tone
Zset	Set impedance between A/B-B/A terminals
α	Gain control factor of AGC function; $0.5 < \alpha <= 1$
[x]	Reference to REFERENCE chapter
(x)	Reference to equation (x)

APPENDIX 2 APPLICATION WITH UBA2051

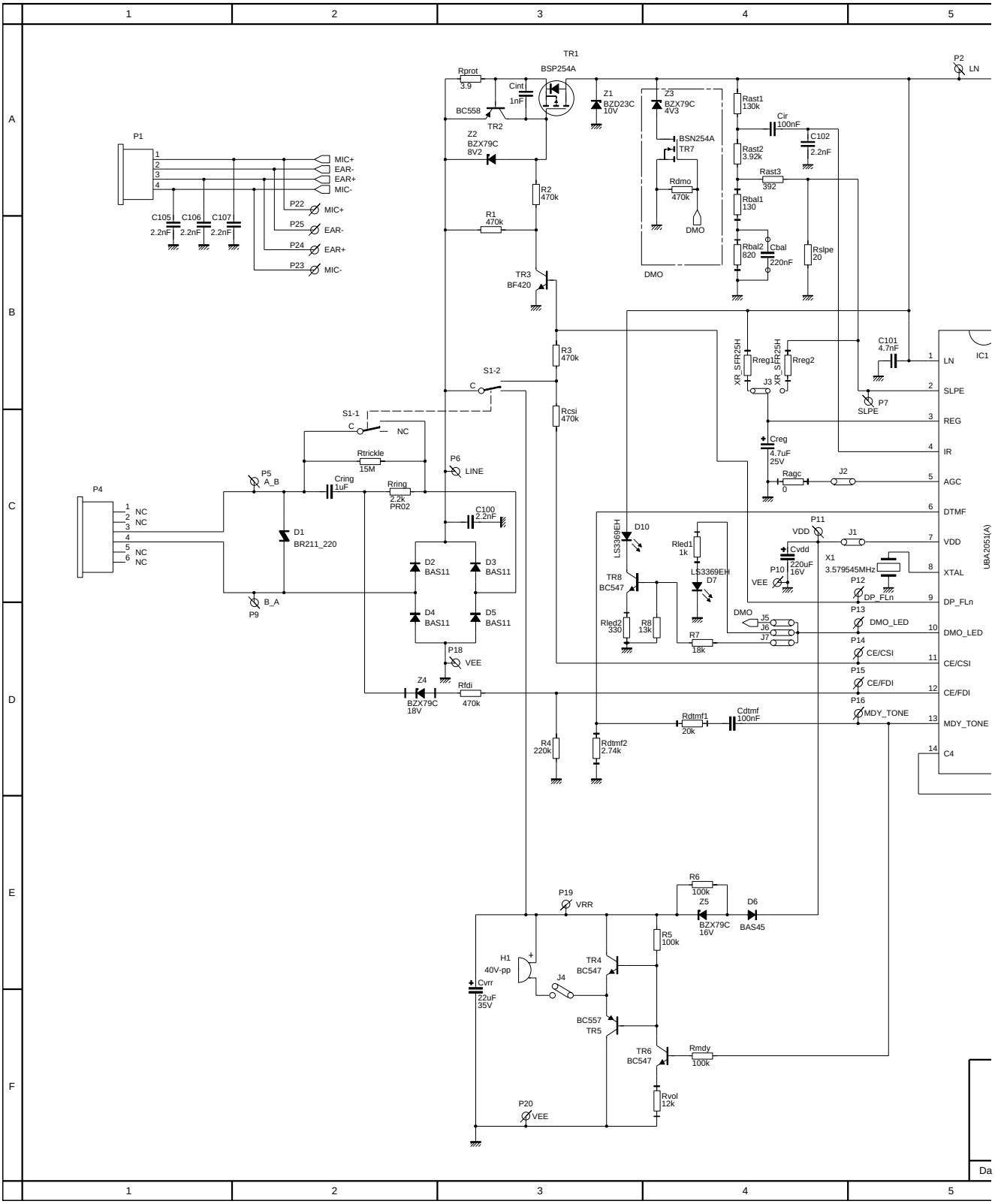


Fig.51 Application example; UBA2051, left part

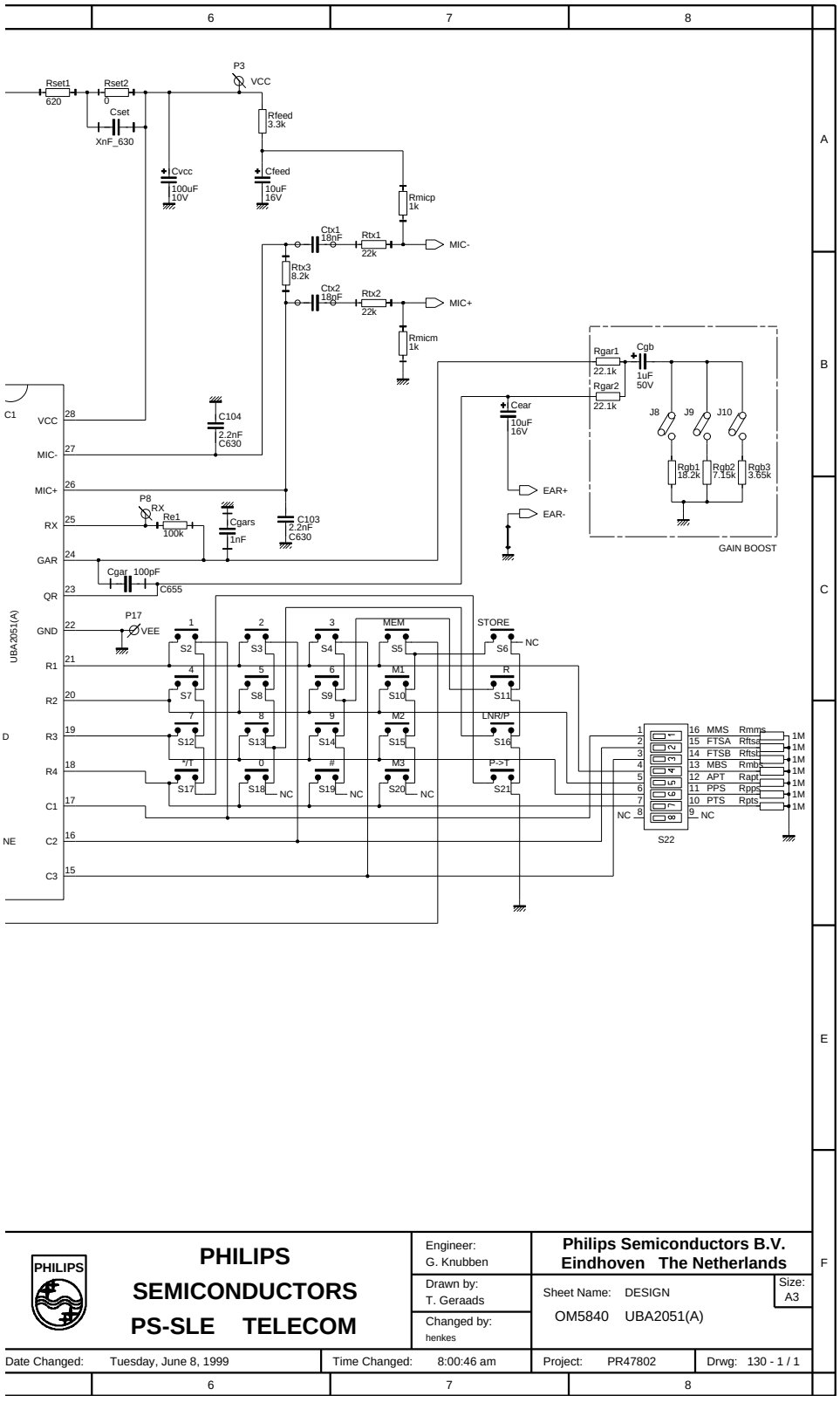


Fig.52 Application example; UBA2051, right part

APPENDIX 3 DIALLING PROCEDURES FOR UBA2050/51

1 SYMBOLS

⇑	OFF-HOOK operation
⇓	ON-HOOK operation
D1...Dn	digit key: [1], [2], [3], [4], [5], [6], [7], [8], [9], [0], [*], [#]
Dp1...Dpn	output pulse digit: 1, 2, 3, 4, 5, 6, 7, 8, 9, 0
Dt1...Dtn	output DTMF digit: 1, 2, 3, 4, 5, 6, 7, 8, 9, 0, *, #
R	Flash key
tfl	Flash output
P	Pause digit
tap	Access pause
LNR/P	Last Number Redial / Pause key
M1..Mn	Direct access memory
MEM	Indirect memory access key
ST	[Store] key
P->T	Pulse to Tone mode key
*/T	* / Pulse to Tone key ⇒ * in DTMF or P->T from Pulse mode
Characters	1, 2, 3, 4, 5, 6, 7, 8, 9, 0, *, #, P, P->T, R
(pulse mode)	PTS selection is pulse mode
(DTMF mode)	PTS selection is DTMF mode

Note: One keytone is generated when a key pressed is successfully processed exept if this key is a DTMF digit.

2 DIALLING WITH LNR

Actions:	⇑ D1, D2,...Dn	⇓	n<33
Dial out pulse:	Dp1, Dp2,...Dpn		
Dial out tone:	Dt1, Dt2,...Dtn		
Actions:	⇑ LNR/P	⇓	n<33
Dial out pulse:	Dp1, Dp2,...Dpn		
Dial out tone:	Dt1, Dt2,...Dtn		
Actions:	⇑ D1, D2,..., D32, D33,...Dn	⇓	n>32
Dial out pulse:	Dp1, Dp2,..., Dp32, Dp33,...Dpn		
Dial out tone:	Dt1, Dt2,..., Dt32, Dt33,...Dtn		
Actions:	⇑ LNR/P	⇓	n>32
Dial out pulse:	nothing		
Dial out tone:	nothing		
Actions:	⇑ D1, D2,..., LNR/P,..Dn	⇓	n<33
Dial out pulse:	Dp1, Dp2,...,tap,..Dpn		
Dial out tone:	Dt1, Dt2,...,tap,..Dtn		
Actions:	⇑ LNR/P	⇓	n<33
Dial out pulse:	Dp1, Dp2,...,tap,..Dpn		
Dial out tone:	Dt1, Dt2,...,tap,..Dtn		
Actions:	⇑ D1, D2,..., */T, Dx, Dy,..Dn	⇓	*/T ⇒ P->T ; n <33
Dial out pulse:	Dp1, Dp2,...,tap, Dtx, Dty,..Dtn		
Dial out tone:	Dt1, Dt2,..., *, Dtx, Dty,..Dtn		
Actions:	⇑ LNR/P	⇓	*/T ⇒ P->T ; n <33
Dial out pulse:	Dp1, Dp2,...,tap, Dtx, Dty,..Dtn		
Dial out tone:	Dt1, Dt2,..., *, Dtx, Dty,..Dtn		
Actions:	⇑ D1, D2,..., P->T, Dx,.., #, */T,..Dn	⇓	n <33
Dial out pulse:	Dp1, Dp2,...,tap, Dtx,.., #, *,..Dtn		
Dial out tone:	Dt1, Dt2,...,tap, Dtx,.., #, *,.. Dtn		
Actions:	⇑ LNR/P	⇓	n <33
Dial out pulse:	Dp1, Dp2,...,tap, Dtx,.., #, *,..Dtn		
Dial out tone:	Dt1, Dt2,...,tap, Dtx,.., #, *,.. Dtn		
Actions:	⇑ D1, D2,...Dn, R	⇓	n<32
Dial out pulse:	Dp1, Dp2,...Dpn, tfl		
Dial out tone:	Dt1, Dt2,...Dtn, tfl		
Actions:	⇑ LNR/P	⇓	n<32
Dial out pulse:	Dp1, Dp2,...Dpn		
Dial out tone:	Dt1, Dt2,...Dtn		

Actions:	⇑ D1, D2,...Dn, R	⇓		n>31
Dial out pulse:	Dp1, Dp2,...Dpn, tfl			
Dial out tone:	Dt1, Dt2,...Dtn, tfl			
Actions:	⇑ LNR/P	⇓		n>31
Dial out pulse:	nothing			
Dial out tone:	nothing			
Actions:	⇑ D1, D2,...Dn, R,	LNR/P, Dy	⇓	n<31
Dial out pulse:	Dp1, Dp2,...Dpn, tfl,	tap, Dpy		
Dial out tone:	Dt1, Dt2,...Dtn, tfl,	tap, Dty		
Actions:	⇑ LNR/P	⇓		n<31
Dial out pulse:	tap, Dpy			
Dial out tone:	tap, Dty			
Actions:	⇑ D1, D2,...Dn, R, Dx, LNR/P, Dy		⇓	n+4>32
Dial out pulse:	Dp1, Dp2,...Dpn, tfl, Dpx, tap, Dpy			
Dial out tone:	Dt1, Dt2,...Dtn, tfl, Dtx, tap, Dty			
Actions:	⇑ LNR/P	⇓		n+4>32
Dial out pulse:	nothing			
Dial out tone:	nothing			
Actions:	⇑ D1, D2,..., D30, R,	Dx,..Dn	⇓	(n - x) <33
Dial out pulse:	Dp1, Dp2,..., Dp30, tfl,	Dpx,...Dpn		
Dial out tone:	Dt1, Dt2,..., Dt30, tfl,	Dtx,...Dtn		
Actions:	⇑ LNR/P	⇓		(n - x) <33
Dial out pulse:	Dpx,...Dpn			
Dial out tone:	Dtx,...Dtn			
Actions:	⇑ D1, D2, */T, D4,*/T, D6, R, Dz,..Dn		⇓	*/T ⇒ P->T ; ((n - z)+7) <33
Dial out pulse:	Dp1, Dp2,. tap, Dt4, *,. Dt6, tfl, Dpz,...Dpn			
Dial out tone:	Dt1, Dt2, *, Dt4, *,Dt6, tfl, Dtz,...Dtn			
Actions:	⇑ LNR/P	⇓		*/T ⇒ P->T ; ((n - z)+7) <33
Dial out pulse:	Dpz,...Dpn			
Dial out tone:	Dtz,...Dtn			
Actions:	⇑ D1, D2, P->T, D4,*/T, D6, R, Dz,..Dn		⇓	((n - z)+7) <33
Dial out pulse:	Dp1, Dp2,. tap, Dt4, *,. Dt6, tfl, Dpz,...Dpn			
Dial out tone:	Dt1, Dt2, tap, Dt4, *,Dt6, tfl, Dtz,...Dtn			
Actions:	⇑ LNR/P	⇓		((n - z)+7) <33
Dial out pulse:	Dpz,...Dpn			
Dial out tone:	Dtz,...Dtn			

Actions:	⇑ D1, D2,..., */T, #, Dx,. Dy, R, Dz,..Dn	⇓	*/T ⇒ * ; ((n - z)+y+1) <33
Dial out pulse:	Dp1, Dp2,..., Dpx, Dpy, tfl, Dpz,...Dpn		
Dial out tone:	Dt1, Dt2,..., *, #,Dtx, Dty, tfl, Dtz,...Dtn		
Actions:	⇑ LNR/P	⇓	
Dial out pulse:	Dpz,...Dpn		*/T ⇒ * ; ((n - z)+y-1) <33
Dial out tone:	Dtz,...Dtn		*/T ⇒ * ; ((n - z)+y+1) <33
Actions:	⇑ D1, D2,.*/T, Dv, R, Dx..,*/T, Dy,..,,*/T, Dz,..Dn	⇓	*/T ⇒ P->T ; ((n - x)+5) <33
Dial out pulse:	Dp1, Dp2,. tap, Dtv, tfl, Dpx,.., tap, Dty,.. , *,Dtz,...Dtn		
Dial out tone:	Dt1, Dt2, *, Dtv, tfl, Dtx,.., *,Dty,.., *, Dtz...Dtn		
Actions:	⇑ LNR/P	⇓	*/T ⇒ P->T ; ((n - x)+5) <33
Dial out pulse:	Dpx,.., tap, Dty,.. , *, Dtz,...Dtn		
Dial out tone:	Dtx,.., *, Dty,.., *, Dtz...Dtn		
Actions:	⇑ D1, D2,... ,*/T, Dv, R, Dx..,*/T, Dy,.., */T, Dz,..Dn	⇓	*/T ⇒ * ; ((n - x)+v+1) >32
Dial out pulse:	Dp1, Dp2,..., Dpv, tfl, Dpx,.., Dpy,.., Dpz,...Dpn		
Dial out tone:	Dt1, Dt2,..., *, Dtv, tfl, Dtx,.., *, Dty,.., *, Dtz...Dtn		
Actions:	⇑ LNR/P	⇓	*/T ⇒ * ; ((n - x)+v+1) >32
Dial out pulse:	nothing		
Dial out tone:	nothing		

2 STORE IN REPERTORY

2.1 SINGLE PROGRAMMATION

Actions:	⇑ ST, D1, D2,...Dn, M1	⇓	n<22
Dial out:	nothing		
M1 content:	D1, D2,...Dn		
Actions:	⇑ LNR/P	⇓	
Dial out	nothing		
Actions:	⇑ ST, D1, D2,...Dn, M1	⇓	n>21
Dial out:	nothing		
M1 content:	Previous one	⇒ no programmation	
Actions:	⇑ LNR/P	⇓	
Dial out:	nothing		

Actions:	⇑ ST, D1, D2,..., P->T, Dx,.., #, */T, LNR/P,Dy,..Dn, M1	⇓	n<22
Dial out:	nothing		
M1 content:	D1, D2,..., P->T, Dx,.., #, *, P, Dy,..Dn	(Pulse mode)	
M1 content:	D1, D2,..., P->T, Dx,.., #, *, P, Dy,..Dn	(DTMF mode)	

Actions:	⇑ LNR/P	⇓
Dial out	nothing	

Actions:	⇑ ST, D1, D2,..., */T, Dx,.., #, */T,..Dn, M1	⇓	*/T ⇒ P->T ; n<22
Dial out:	nothing		
M1 content:	D1, D2,..., P->T, Dx,.., #, *,..Dn	(Pulse mode)	
M1 content:	D1, D2,..., *, Dx,.., #, *,..Dn	(DTMF mode)	

Actions:	⇑ LNR/P	⇓
Dial out	nothing	

Actions:	⇑ ST, D1, D2,..., */T, Dx,.., #, */T,..Dn, M1	⇓	*/T ⇒ * ; n<22
Dial out:	nothing		
M1 content:	D1, D2,..., Dx,.., Dn	(Pulse mode)	
M1 content:	D1, D2,..., *, Dx,.., #, *,..Dn	(DTMF mode)	

Actions:	⇑ LNR/P	⇓
Dial out	nothing	

Actions:	⇑ ST, D1, D2,..., P->T, Dx,.., #, */T,..Dn, MEM, 4	⇓	n<22
Dial out:	nothing		
MEM4 content:	D1, D2,..., P->T, Dx,.., #, *,..Dn	(Pulse mode)	
MEM4 content:	D1, D2,..., P->T, Dx,.., #, *,..Dn	(DTMF mode)	

Actions:	⇑ LNR/P	⇓
Dial out	nothing	

Actions:	⇑ ST, D1, D2,..., P->T, Dx, R, Dy,.., P->T, Dz,..., Dn, M1	⇓	n<22
Dial out:	nothing		
M1 content:	D1, D2,..., P->T, Dx, R, Dy,.., P->T, Dz,..., Dn	(Pulse mode)	
M1 content:	D1, D2,..., P->T, Dx, R, Dy,.., P->T, Dz,..., Dn	(DTMF mode)	

Actions:	⇑ LNR/P	⇓
Dial out	nothing	

2.2 CASCADE PROGRAMMATION

Actions:	⇑ ST, D1, D2, M1, ST, D3, D4, D5, M2, ST, D6, D7, MEM, 4, ST, M3	⇓
Dial out:	nothing	
M1 content:	D1, D2	
M2 content:	D3, D4, D5	
MEM4 content:	D6, D7	
M3 content:	empty	

Actions: ⇑ LNR/P ⇓
Dial out: nothing

Actions: ⇑ D1, D2, P->T, Dx, ..,Dz, ST, D1, D2, M1, ST, D3, D4, D5, M2 ⇓(Pulse mode)
Dial out: Dp1, Dp2, tap, Dtx, ..Dtz
M1 content: D1, D2
M2 content: D3, D4, D5

Actions: ⇑ LNR/P ⇓
Dial out nothing

Actions: ⇑ M1 ⇓
Dial out: Dp1, Dp2

Actions: ⇑ ST, D1, D2,..., P->T, Dx, ..., Dn, M1, D5, D6 ⇓ (Pulse mode) n<22
Dial out: Dp5, Dp6
M1 content: D1, D2,..., P->T, Dx, ..., Dn

Actions: ⇑ LNR/P ⇓
Dial out: Dp5, Dp6

2.4 NOTEPAD

Actions: ⇑ conversation ... ST, D1, D2,...Dn, ⇓ n<22
Dial out: nothing
LNR content: D1, D2,...Dn

Actions: ⇑ LNR/P ⇓
Dial out pulse: Dp1, Dp2,...Dpn
Dial out DTMF: Dt1, Dt2,...Dtn

3 DIALLING FROM REPERTORY

3.1 SINGLE DIALLING

M1 content: D1, D2,...Dn
Actions: ⇑ M1 ⇓
Dial out pulse: Dp1, Dp2,...Dpn
Dial out tone: Dt1, Dt2,...Dtn

Actions: ⇑ LNR/P ⇓
Dial out pulse: Dp1, Dp2,...Dpn
Dial out tone: Dt1, Dt2,...Dtn

MEM2 content: D1, D2,...Dn
Actions: ⇑ MEM, 2 ⇓
Dial out pulse: Dp1, Dp2,...Dpn
Dial out tone: Dt1, Dt2,...Dtn

Actions: ⇑ LNR/P ⇓
Dial out pulse: Dp1, Dp2,...Dpn
Dial out tone: Dt1, Dt2,...Dtn

M1 content: D1, D2,..., P->T, Dx, R, Dy,.., P->T, Dz,..., Dn
Actions: ⇑ M1 ⇓
Dial out pulse: Dp1, Dp2,.., tap, Dtx, tfl, Dpy,.., tap, Dtz,..., Dtn
Dial out DTMF: Dt1, Dt2,..., tap, Dtx, tfl, Dty,.., tap, Dtz,..., Dtn

Actions: ⇑ LNR/P ⇓
Dial out pulse: Dpy,.., tap, Dtz,..., Dtn
Dial out DTMF: Dty,.., tap, Dtz,..., Dtn

M1 content: D1, D2,..., *, Dx,.., #, *,..Dn
Actions: ⇑ M1 ⇓
Dial out pulse: Dp1, Dp2,..., Dpx,....Dpn
Dial out tone: Dt1, Dt2,..., *, Dtx,.., #, *,..Dtn

Actions: ⇑ LNR/P ⇓
Dial out pulse: Dp1, Dp2,..., Dpx,....Dpn
Dial out tone: Dt1, Dt2,..., *, Dtx,.., #, *,..Dtn

3.2 CASCADE DIALLING

Any cascade dialling is possible as soon as the previous dialling request is elapsed. If not elapsed, the new request is ignored.

M1 content: D1, D2,...Dn
MEM2 content: Dv, Dx,...Dz

Actions:	⇑ M1	Dr, Ds,	MEM, 2	⇓
Dial out pulse:	Dp1, Dp2,...Dpn	Dpr, Dps	Dpv, Dpx,...Dpz	
Dial out tone:	Dt1, Dt2,...Dtn	Dtr, Dts	Dtv, Dtx,...Dtz	

Actions: ⇑ LNR/P ⇓
Dial out pulse: Dp1, Dp2,...Dpn, Dpr, Dps, Dpv, Dpx,...Dpz (n + (z-v) +2) <33
Dial out tone: Dt1, Dt2,...Dtn, Dtr, Dts, Dtv, Dtx,...Dtz

M1 content:	D1, D2, D3, ...Dn			
MEM2 content:	Dv, Dx,...Dz			
Actions:	⇑ M1	MEM, 2	⇓	
Dial out pulse:	Dp1, Dp2, Dp3, ...Dpn			
Dial out tone:	Dt1, Dt2,Dt3, ...Dtn			
Actions:	⇑ LNR/P	MEM, 2		⇓
Dial out pulse:	Dp1, Dp2, Dp3, ...Dpn		Dpv, Dpx, ..Dpz	
Dial out tone:	Dt1, Dt2, Dt 3,...Dtn		Dtv, Dtx, ..Dtz	
Actions:	⇑ LNR/P		⇓	
Dial out pulse:	Dp1, Dp2, Dp3, ...Dpn, Dpv, Dpx, ..Dpz			(n + (z-v)) <33
Dial out tone:	Dt1, Dt2, Dt3,...Dtn, Dtv, Dtx, ..Dtz			

M1 content:	D1, D2, D3, R, D4,.., P->T, Dm, Dn			
MEM2 content:	Dv, Dx,...Dz			
Actions:	⇑ M1	MEM, 2		⇓
Dial out pulse:	Dp1, Dp2, Dp3, tfl, Dp4,.., tap, Dtm, Dtn		Dtv, Dtx, ..Dtz	
Dial out DTMF:	Dt1, Dt2, Dt3, tfl, Dt4,.., tap, Dtm, Dtn		Dtv, Dtx, ..Dtz	
Actions:	⇑ LNR/P		⇓	
Dial out pulse:	Dp4,.., tap, Dtm, Dtn, Dtv, Dtx, ..Dtz			(n + (z-v) -3) <33
Dial out DTMF:	Dt4,.., tap, Dtm, Dtn, Dtv, Dtx, ..Dtz			

M1 content:	D1, D2,.., D15, R, D16,.., D20			
MEM2 content:	Dv, Dx,...Dz			
Actions:	⇑ M1	MEM, 2		⇓
Dial out pulse:	Dp1, Dp2,.., Dp15, tfl, Dp16,.., Dp20		Dtv, Dtx, ..Dtz	
Dial out DTMF:	Dt1, Dt2,.., Dt15, tfl, Dt16,.., Dt20		Dtv, Dtx, ..Dtz	
Actions:	⇑ LNR/P		⇓	
Dial out pulse:	Dp16,.., Dt20, Dtv, Dtx, ..Dtz			(5 + (z-v)) <33
Dial out DTMF:	Dt16,.., Dt20, Dtv, Dtx, ..Dtz			

M1 content:	Dv, Dx,...Dz			
MEM2 content:	D1, D2,.., D15, R, D16,.., D20			
Actions:	⇑ M1	MEM, 2		⇓
Dial out pulse:	Dtv, Dtx, ..Dtz		Dp1, Dp2,.., Dp15, tfl, Dp16,.., Dp20	
Dial out DTMF:	Dtv, Dtx, ..Dtz		Dt1, Dt2,.., Dt15, tfl, Dt16,.., Dt20	
Actions:	⇑ LNR/P		⇓	
Dial out	nothing			((z-v)+21) >32