APPLICATION NOTE

Application of the TEA1111A

Speech circuit with dialler interface, regulated supply and earpiece volume control

AN99036

Philips Semiconductors

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Application Note

Abstract

The TEA1111A is a bipolar transmission circuit for use in telephone sets. It is part of TEA111x family.

A detailed description of the circuit blocks of the TEA1111A and advices on adjustments are contained in this report.

APPLICATION NOTE

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Speech circuit with dialler interface, regulated supply and earpiece volume control

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Summary

A detailed description of the blocks of the TEA1111A is given. The possible settings to adjust the DC and transmission characteristics are explained.

The TEA1111A incorporates a microphone amplifier, a DTMF amplifier, an earpiece amplifier with a 4 step digital volume control and a LED control output. It provides supplies for peripherals including a 3.25 V regulated one.

The evaluation board OM5889 for the TEA1111A is available.

CONTENTS

LIST OF FIGURES

1. INTRODUCTION

The TEA1111A offers all the microphone, receive and line interface functions required in telephone sets. It performs the interface between the line and the transducers of the handset.

The TEA1111A includes also a DTMF amplifier for dialling. The selection between the microphone amplifier and the DTMF amplifier is made with a “MUTE” function. The MUTE/ input switches-off both the microphone and the receive amplifiers and switches-on the DTMF amplifier.

A 4 step digital volume control is available on the earpiece amplifier.

The TEA1111A provides a LED control output .

Furthermore, a regulated 3.25 V supply is provided for the dialler or microcontroller.

The report is divided into two parts: the first part, up to chapter 3, gives a detailed description of the different circuit blocks of the TEA1111A including operating principles, settings of DC and transmission characteristics and performances of the different functions; the second part describes the consecutive steps to design and adjust applications using the TEA1111A and introduces the demoboard.

Note: the values of parameters given in this application note are as accurate as possible, but please, refer to the last product specification for final ones.

2. BLOCK DIAGRAM AND PINNING

Fig. 1 shows the block diagram of the TEA1111A, the pinning is shown in fig. 2.

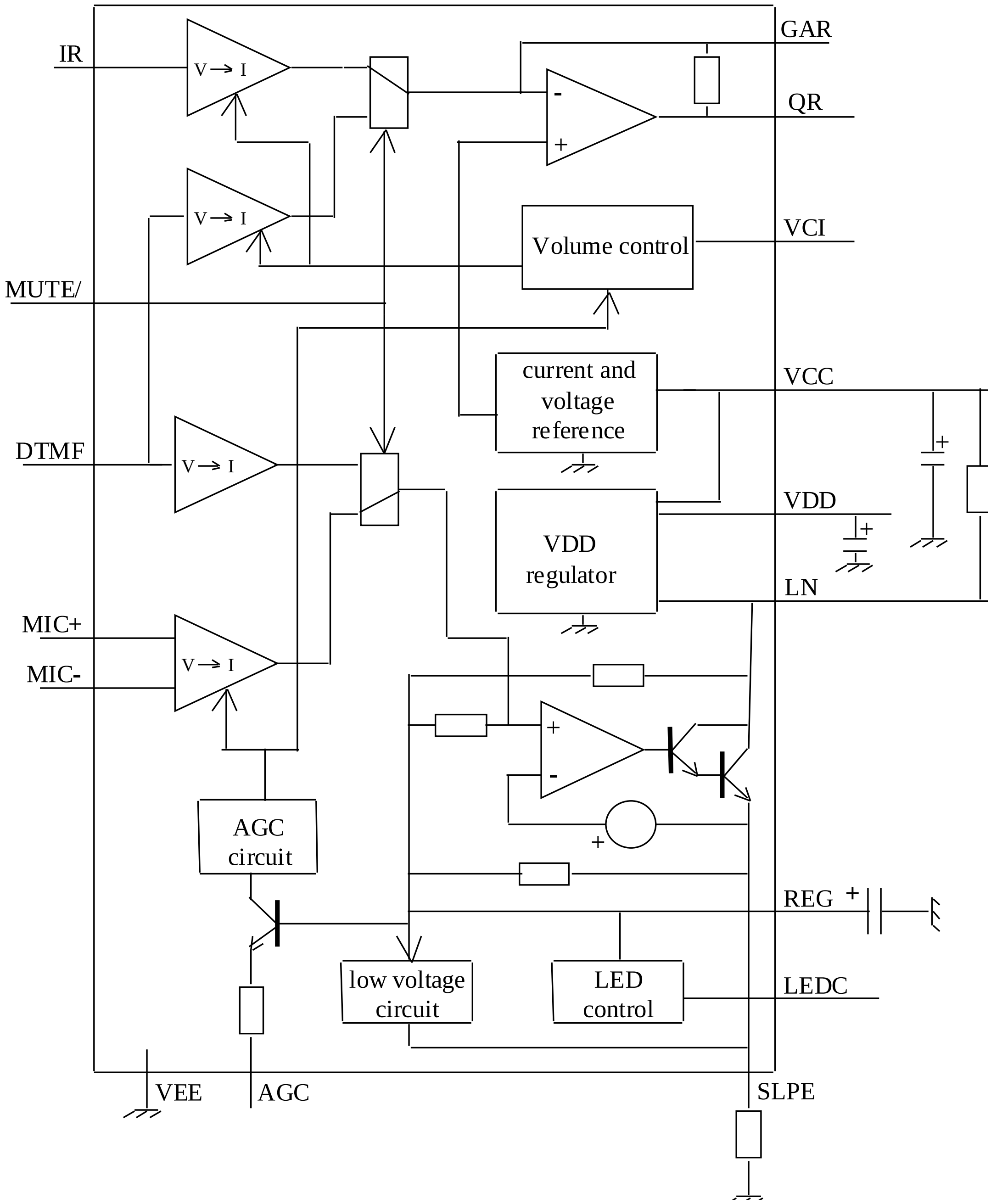


Fig. 1 TEA1111A block diagram

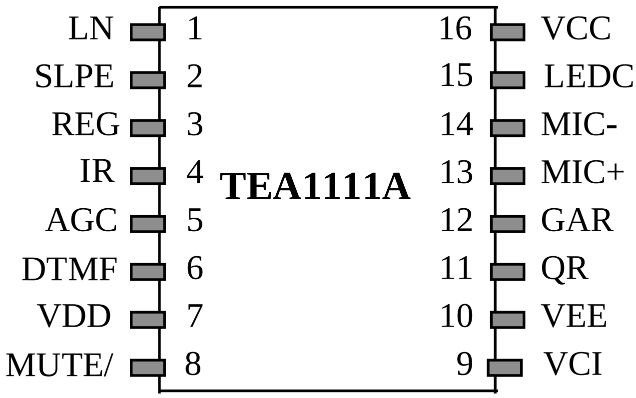


Fig. 2 TEA1111A pinning

TEA1111A PIN	NAME	DESCRIPTION
1	LN	Positive line terminal
2	SLPE	Slope adjustment
3	REG	Line voltage regulator decoupling
4	IR	Receive amplifier input
5	AGC	Automatic gain control
6	DTMF	DTMF input
7	V_{DD}	Regulated supply for peripherals
8	MUTE/	MUTE/ input
9	VCI	Earpiece volume control input
10	V_{EE}	Negative line terminal
11	QR	Receive amplifier output
12	GAR	Earpiece amplifier inverting input
13	MIC+	Non inverting microphone input
14	MIC-	Inverting microphone input
15	LEDC	LED control output
16	V_{CC}	Supply voltage for internal circuit

3. DESCRIPTION OF THE TEA1111A

All the curves shown in this section result from measurement of typical samples using the schematic shown in fig. 3.

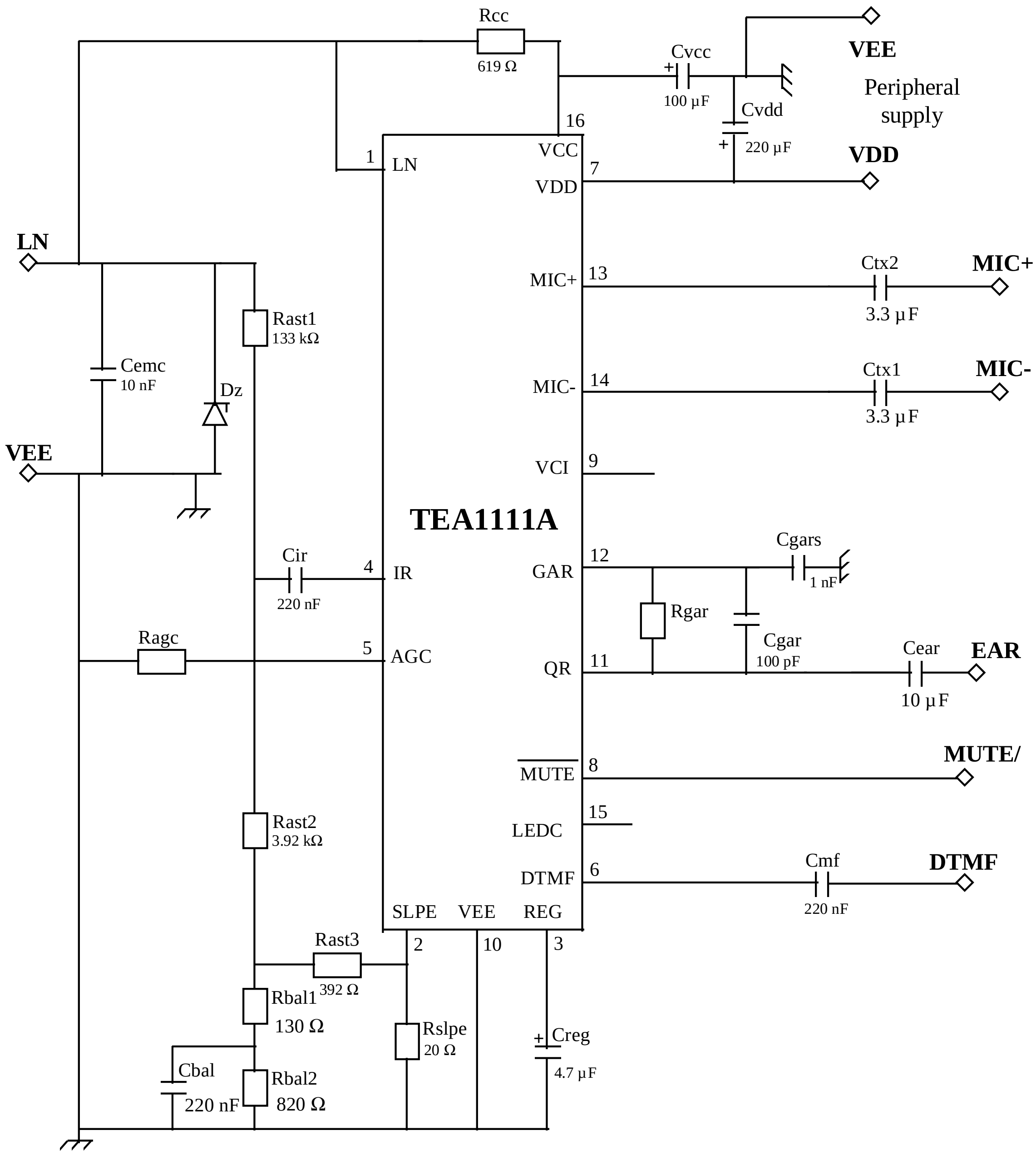


Fig. 3 Basic application for measurements

3.1 DC characteristics and supply block

3.1.1 DC characteristics

Principle of operation

The TEA1111A generates a stabilized voltage (called Vref) between pins LN and SLPE. This reference voltage, typically 3.8 V, is temperature compensated. The voltage at pin REG is used by the internal regulator to generate the stabilized Vref voltage and is decoupled by a capacitor Creg connected to VEE.

For effective operation of the apparatus, the TEA1111A must have a low resistance to the DC current and a high impedance to speech signals. The Creg capacitor, converted into an equivalent inductance (see “set impedance” section), realizes this impedance conversion from its DC value (Rslpe) to its AC value (Rcc +Rz//Cz in the audio frequency range). The DC voltage at pin SLPE is proportional to the line current with an offset due to the VDD and VCC supply currents (Isup and Icc).

This general configuration is shown in fig. 4.

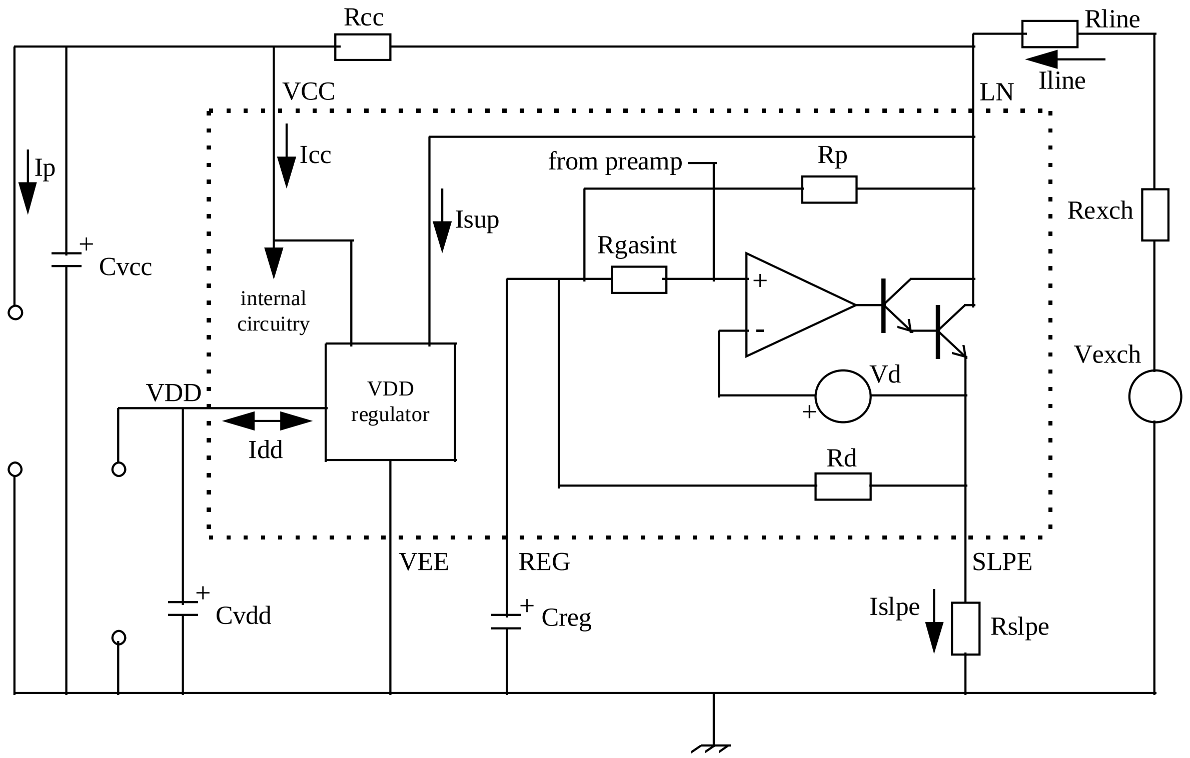


Fig. 4 DC characteristics configuration

The IC regulates the line voltage between pins LN and SLPE. the voltage on pin LN can be calculated as:

Vln = Vref + Rslpe × Islpe

Islpe = Iline - Isup - Icc - Ip

Iline = line current

Icc = current consumption of the IC

Ip = supply current for peripherals connected on VCC

Isup = Current consumed between LN and VEE by the Vdd regulator

The DC line current Iline flowing into the apparatus is determined by the exchange supply voltage Vexch, the feeding bridge resistance Rexch, the DC resistance of the telephone line Rline and the voltage across the telephone set including diode bridge.

Below a threshold line current Ith (typically equal to 9 mA) the internal reference voltage (generating Vref) is automatically adjusted to a lower value (down to an absolute minimum voltage of 1.45 V). This means that more sets can operate in parallel or that for a very low voltage feeding bridge the line current has a higher value. For line currents below this threshold current, the TEA1111A has reduced sending and receiving performances, moreover the Vdd value and the current Isup are reduced. This is called the low voltage area.

The internal circuitry of the TEA1111A is supplied from pin VCC. In line powered application, this voltage is derived from the line voltage by means of a resistor (Rcc) and must be decoupled by a capacitor (Cvcc). Fig. 5 shows the IC current consumption (Icc) as a function of the VCC supply voltage in different conditions.

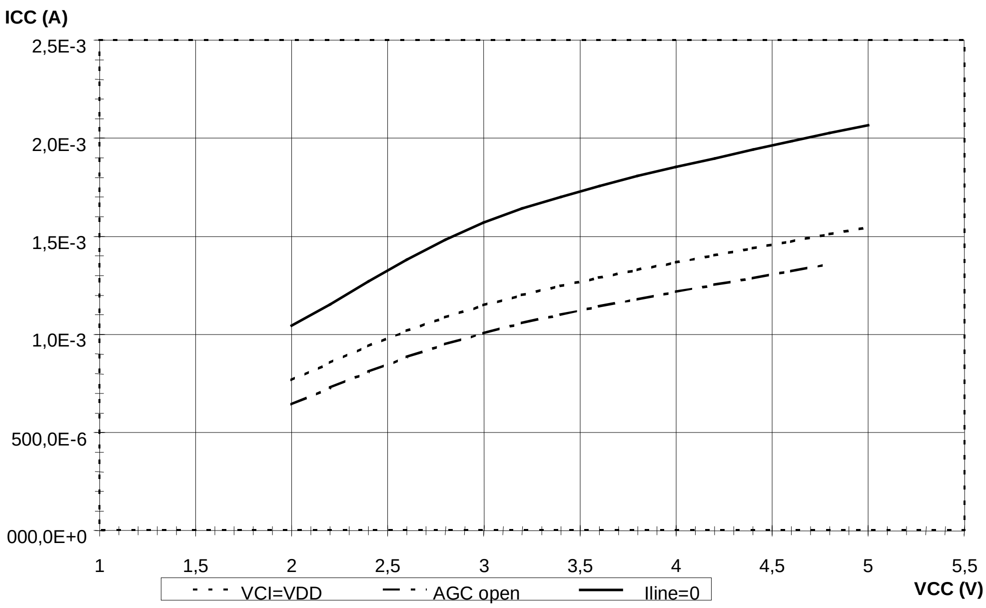


Fig. 5 Icc versus VCC

Fig. 6 shows the main voltages as a function of the line current.

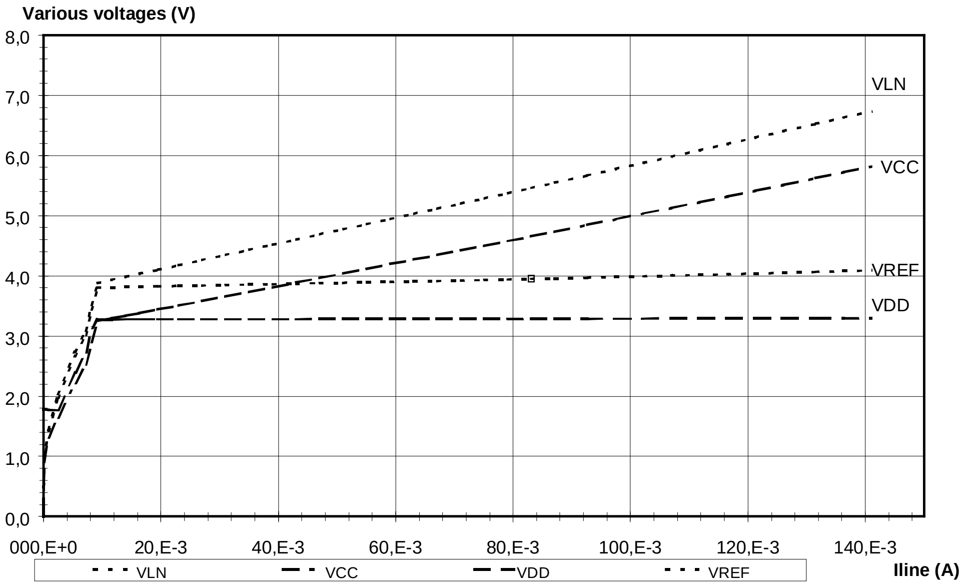


Fig. 6 Main voltages versus line current

Fig. 7 shows the behavior in the low voltage area in line powered condition.

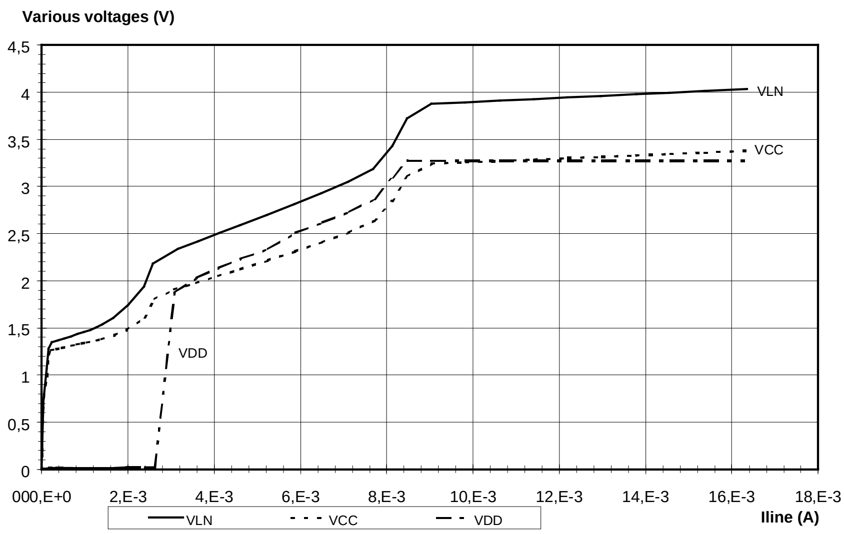


Fig. 7 Low voltage behavior in line powered condition

Adjustments and performances

The reference voltage, Vref, can be adjusted by means of an external resistor Rva. It can be increased by connecting the Rva resistor between pins REG and SLPE, or decreased by connecting the Rva resistor between pins REG and LN (see fig. 8). In line powered application, using the voltage reduction reduces the peripheral and the earpiece amplifier supply capabilities: Vln must be at least 0.35 V higher than Vdd. To ensure correct operation, it is not advised to adjust Vref at a value lower than 3 V or higher than 7 V (the maximum operating voltage of 12 V must be guaranteed by the application as well as the safe die operating temperature). These adjustments will slightly affect a few parameters: there will be a small change in the temperature coefficient of Vref and a slight increase in the spread of this voltage reference due to matching between internal and external resistors. Furthermore, the Rva resistor connected between REG and LN will slightly affect the apparatus impedance (see section “set impedance”).

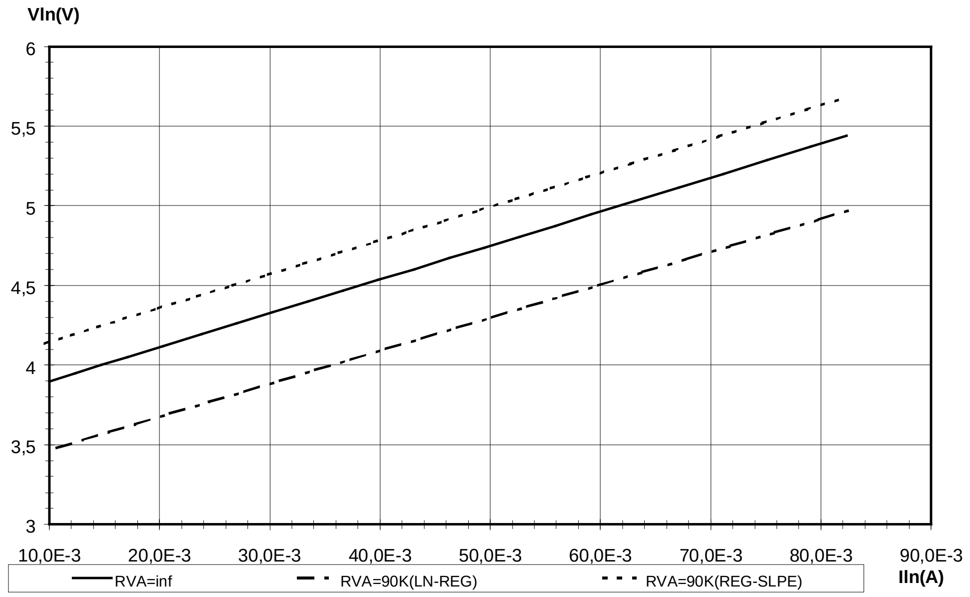


Fig. 8 Influence of the Rva resistor between REG and SLPE or between REG and LN

The DC slope of the voltage on pin LN is influenced by the Rslpe resistor as shown in fig. 9. The value of Rslpe may be slightly modified even if the preferred one is 20 Ω. Changing this value will affect more than the DC characteristics, it also influences the gains, the AGC characteristics, the maximum output swing on the line and the low voltage threshold Ith.

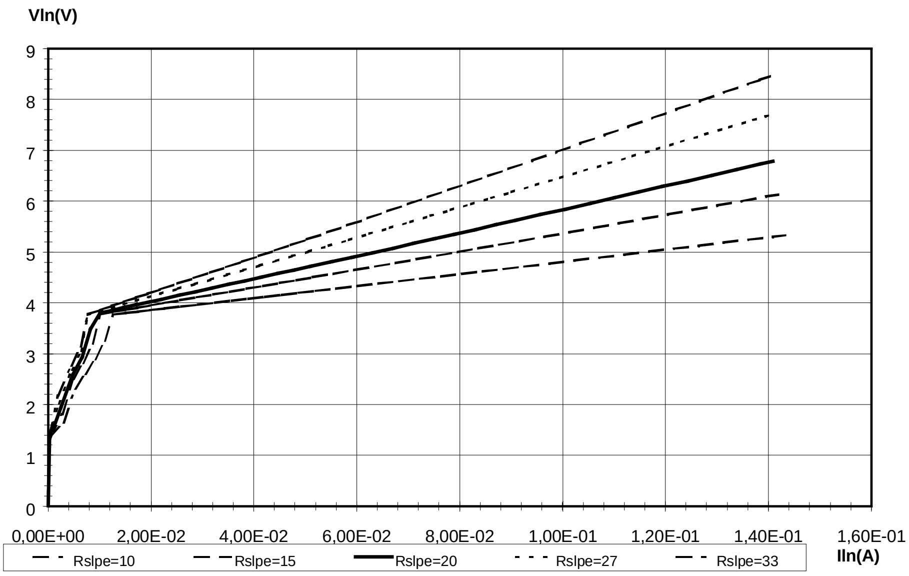


Fig. 9 Influence of Rslpe on the DC characteristics

3.1.2 Supplies for peripherals

Fig. 10 shows the architecture of the supply block.

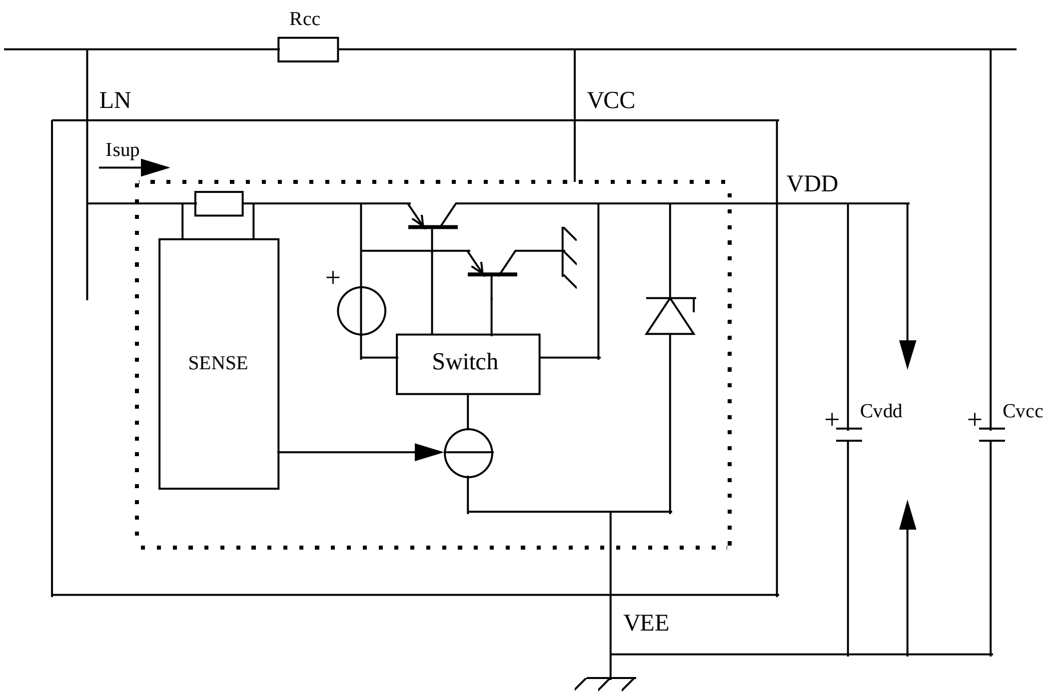


Fig. 10 Supply configuration

Supply VCC

Principle of operation

The supply voltage at pin VCC is normally used to supply the internal circuitry of the TEA1111A. However, a small current can be drawn to supply peripheral circuits having VEE as ground reference. The VCC supply voltage depends on the current consumed by the IC and the peripheral circuits as shown by the following formula:

$$VCC = VCC0 - Rccint \times (Irec + Ip)$$

$$VCC0 = Vln - Rcc \times Icc$$

Irec = internal current necessary to supply the receive output amplifier to realize an AC peak voltage Vqr across the earpiece impedance Rl

$$Irec = Vqr / (\pi \times Rl)$$

Rccint = Rcc // internal equivalent impedance between VCC and VEE

Rccint is the output impedance of the voltage supply point. As can be seen from fig.5, the internal supply current Icc depends on the voltage on pin VCC, it means that the impedance of the internal circuitry connected between VCC and VEE is not infinite. While supplying a peripheral circuit on VCC, the Ip supply current flowing through the Rcc resistor decreases the value of the voltage on pin VCC and then reduces the Icc consumption. So, the impedance to use in combination with Ip and Irec is not Rcc but Rccint which includes in parallel the impedance of the internal circuitry connected between VCC and VEE. For a line current equal to 15 mA and Rcc equal to 620 Ω, this Rccint impedance is approximately 540 Ω.

As VCC is limited to a minimum value to ensure correct operation, Ip will be limited to a maximum value. The limit is imposed by the requirement to maintain a minimum permitted voltage between VCC and SLPE which is called Vmin. So the maximum current available depends on the DC settings of the IC: Vref, Rcc(+Rz), Rslpe and the required AC signal level at the line and receive outputs. To simplify the calculation, we will use the worst case for Rccint, which is Rcc, it gives:

$$VCC = Vln - Rcc\ (Icc + Irec)$$

$$VCC = Vref + Rslpe\ (Iline - Icc - Irec - Isup) - Rcc\ (Icc + Irec)$$

$$VCCmin = Vmin + Rslpe\ (Iline - Icc - Irec - Ip - Isup)$$

$$Ipmax = (VCC - VCCmin) / Rcc$$

$$Ipmax = (Vref - Vmin) / (Rcc - Rslpe) - [Rcc\ (Icc + Irec)] / (Rcc - Rslpe)$$

$$Vmin = 1.7\ V + Vln\ [Rslpe / (Zline // Rcc)]$$

Adjustments and performances

As the impedance connected between LN and VCC also determines the set impedance, the easiest way to increase the current capability of the supply point VCC is to increase the reference voltage Vref by connecting a resistor Rva between pins REG and SLPE (see 3.1.1).

Supply VDD

Principle of operation

VDD is a 3.25 V regulated supply for dialler or microcontroller. In speech mode, VDD is line powered while in trickle mode or in ringer mode it can be externally powered.

When VDD is line powered, it can provide at least 3 mA when VDD equals 3.25 V but its value is typically correlated with the value of the line voltage as follow:

- Vln < 2V : VDD = 0
- 2 V < Vln < 3.65 V : VDD ≅ Vln - 0.35 V
- Vln > 3.6 V and VCC > 2 V : VDD = 3.25 V

Fig. 6 and 7 show VDD and Vln versus line current.

The correlation between line voltage and VDD is done in order to get a voltage difference between Vln and VDD of at least 0.3 V. On the block diagram, two PNP transistors drive the line current either to VDD or to VEE: when the voltage on LN is higher than VDD + 0.2 V the current is driven to VDD, when the voltage on LN is lower than VDD the line current is driven to VEE, when the voltage on LN is between VDD and VDD + 0.2 V both transistors are conducting in order to minimize distortion.

When VDD equals 3.25 V, a constant courant Isup (4.3 mA typically) is sunk from LN. This constant current doesn’t affect the return loss and its value is taken into account for the AGC characteristic. In this condition, the current Idd available at the output VDD is at least 3 mA. When VDD is lower than 3.25 V, both currents Isup and Idd are reduced accordingly.

In trickle mode or in ringer mode, VDD works as a shunt regulator at 3.25 V. In trickle mode the current consumption of the shunt regulator is dramatically reduced in order to have typically 100 nA when VDD is lower than 1.2 V. In ringer mode, the shunt regulator is able to sink up to 75 mA between VDD and VEE. Fig. 11 shows the current consumptions on VDD.

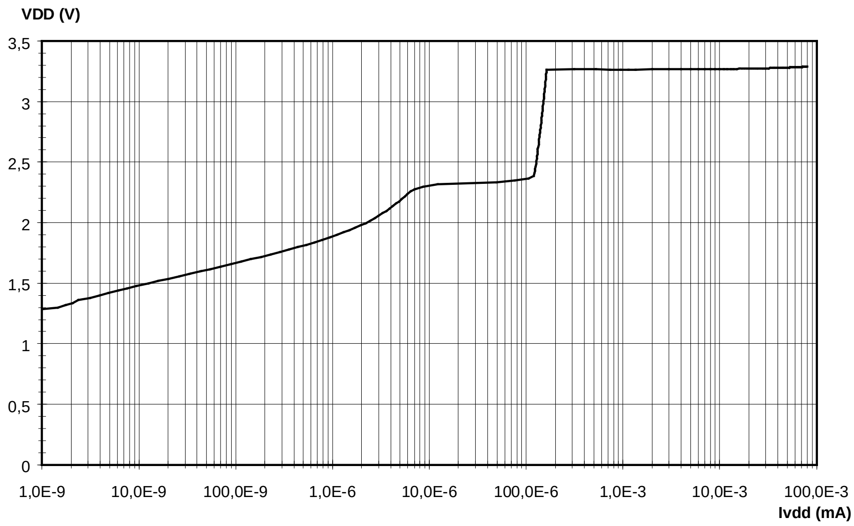


Fig. 11 Current consumption on VDD

NB: Due to this supply structure, the TEA1111A cannot be used in combination with the TEA1081, TEA1083/A, TEA1085/A, TEA1093 or OM5153. In this configuration, the stability may not be possible.

3.2 LED control output

Principle of operation

The TEA1111A provides an on-hook / off-hook status indication. This is done by a DC current available at pin LEDC that can be used by a simple buffer circuit to drive a LED. The LED current flows between pins LN and SLPE. In low line current condition, below 12 mA, no DC current is available at pin LEDC. For line currents between 12 and 82 mA, the DC current at pin LEDC is (Iline - 12 mA) / 150. For line currents larger than 82 mA, the current at LEDC output hardly increases.

Adjustments and performances

The value of the current flowing in the LED is also proportional to the gain of the buffer, on the demoboard, this gain is $(100 \times \beta / (100 + \beta))$, this current should stay compatible with the line current and all the other current consumptions. If this condition is met, as the LED current flows into SLPE, the AGC characteristic is not modified and the distortion is not affected.

Fig. 12 shows the LEDC output current versus line current.

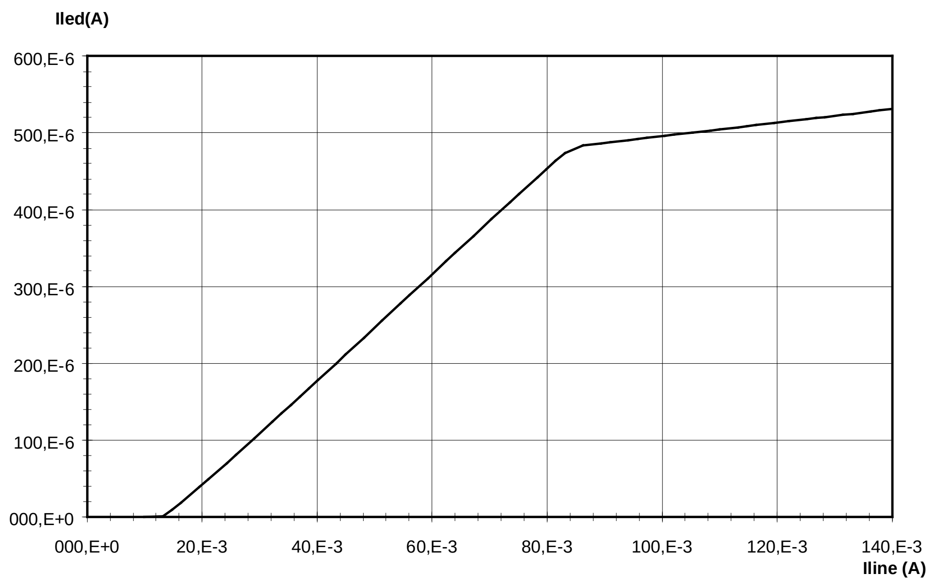


Fig. 12 LEDC output current versus line current

3.3 Set impedance

Principle of operation

The TEA1111A behaves like an equivalent inductance that presents a low impedance to DC (Rslpe) and a high impedance (Rp) to speech signals. Rp is an integrated resistance in the order of 17.5 kΩ +/-15%. It is in parallel with the external RC realized by Rcc and Cvcc. Thus, in the audio frequency range, the apparatus impedance (called set impedance) is mainly determined by the Rcc resistor. Fig. 13 shows an equivalent schematic for the set impedance.

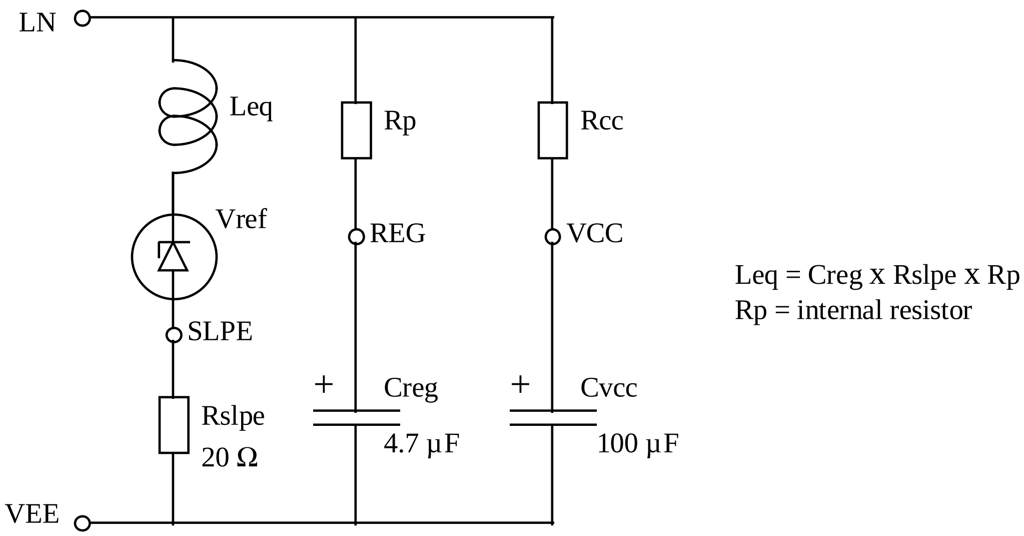


Fig. 13 Equivalent set impedance

Adjustments and performances

When decreasing the reference voltage Vref, a resistor is connected between LN and REG in parallel of Rp (see fig. 13) so, slightly modifying the impedance.

If complex set impedance is required, the Rcc resistor is replaced by a complex network (see fig. 32 :Rcc + Rz // Cz). The DC resistance which influences the value of VCC becomes Rcc + Rz.

3.4 Microphone amplifier

Principle of operation

In fig. 14, the block diagram of the microphone amplifier of the TEA1111A is depicted.

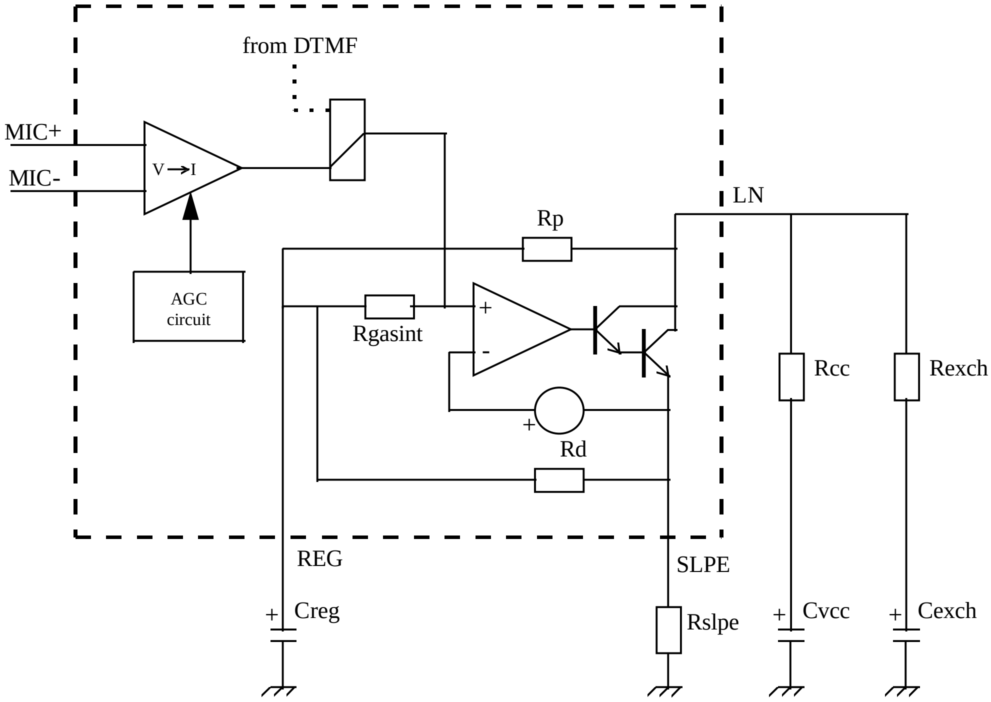


Fig. 14 Microphone channel

The microphone amplifier has symmetrical high input impedances (typically 68 kΩ -2 times 34 kΩ- between pins MIC+ and MIC- with maximum tolerances of +/- 15%). The input of this microphone amplifier is able to handle AC signals up 18 mVrms with less than 2% total harmonic distortion.

As can be seen from fig. 14, the microphone amplifier itself is built up out of two parts: a preamplifier which realizes a voltage to current conversion, and an end-amplifier which realizes the current to voltage conversion. The overall gain Gv(mic-ln) of the microphone amplifier from inputs MIC+/MIC- to output LN is given by the following equation:

$$Gv(mic\text{-}ln) = 20 \times \log Av(mic\text{-}ln)$$

$$Av(mic\text{-}ln) = 2.6 \times (Rgasint / Rrefint) \times (Ri//Zline / Rslpe) \times \alpha$$

with:

Ri = the AC apparatus impedance, Rcc//Rp (typically 620 Ω // 17.5 kΩ)

Rgasint = internal resistor realizing the current to voltage conversion (typically 29.5 kΩ with a spread of +/-15%)

Rrefint = internal resistor determining the current of an internal current stabilizer (typically 7.25 kΩ with a spread of +/- 15% correlated to the spread of Rgasint)

Zline = load impedance of the line during the measurement

α = gain control factor varying from 1 at Iline = 15 mA to 0.5 at Iline = 75 mA when AGC function is applied (see chapter 3.5 for details)

Using these typical values in the equation and assuming Zline = 600 Ω, we find a gain equal to:

$$Gv(mic\text{-}ln) = 20 \times \log Avtx = 44\ dB \qquad \text{at } Iline = 15\ mA$$

The different gain controls (AGC; MUTE/) act on the microphone preamplifier stage, modifying its transconductance.

Adjustments and performances

Fig 15 shows the typical frequency response and gain of the microphone amplifier of the TEA1111A.

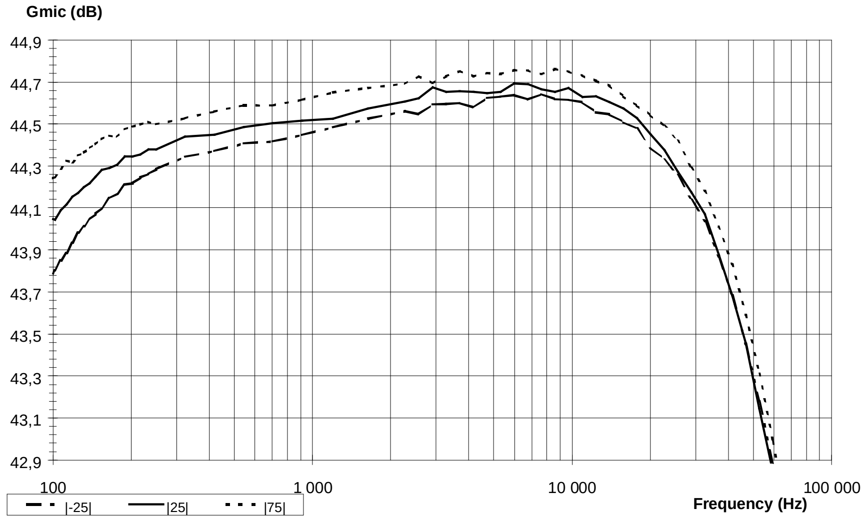
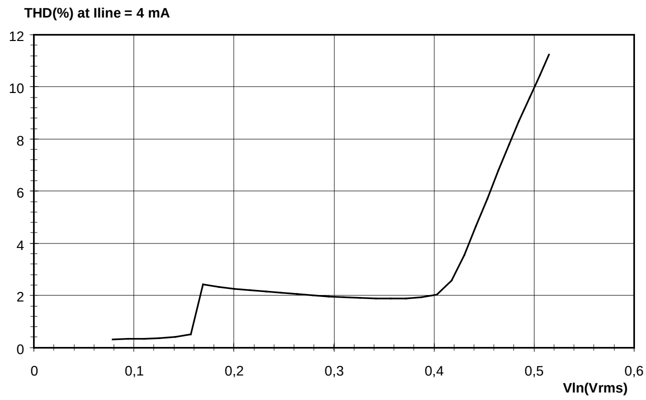


Fig. 15 Microphone gain versus frequency: influence of temperature

Fig 16 shows the distortion of the signal on the line as a function of the line signal at 4 mA, 15 mA and 75 mA.



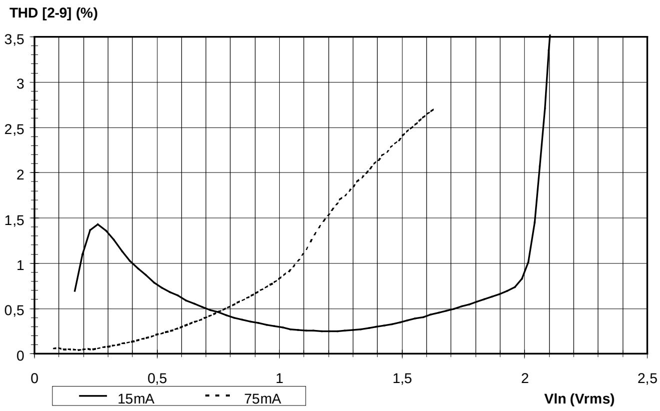


Fig. 16 Distortion on line versus line signal on TEA1111A

Fig. 17 shows the microphone noise (psophometrically weighted: P53 curve) versus line current at nominal gain when a 200 Ω resistor is connected between the inputs MIC+ and MIC-.

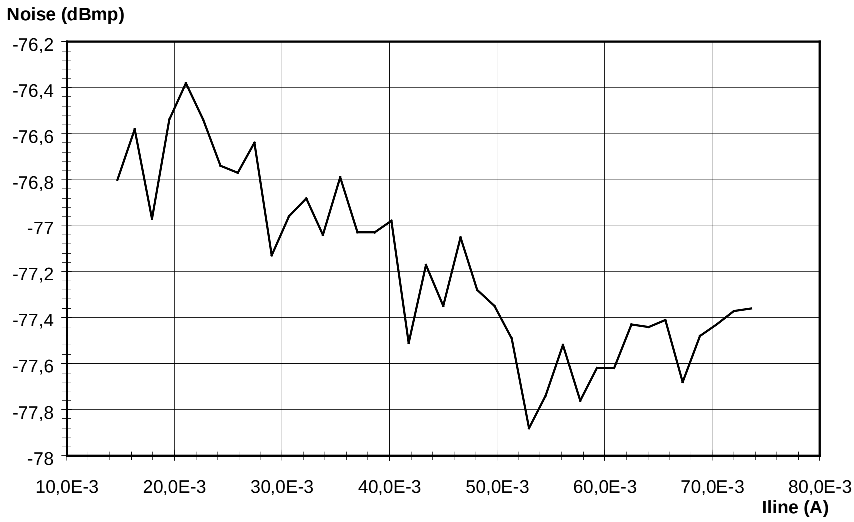


Fig. 17 Microphone noise versus line current

Fig. 18 shows the common mode rejection ratio at 15 mA. Two curves are present in this fig. 19, the first one is the spectrum of the signal on pin LN when a microphone signal is applied on pin MIC- while pin MIC+ is shorted to VEE, the second one is the spectrum of the signal on pin LN when a microphone signal is applied on pins MIC- and MIC+ shorted together. Both signals are at 1 kHz, the difference between the two curves gives the CMRR.

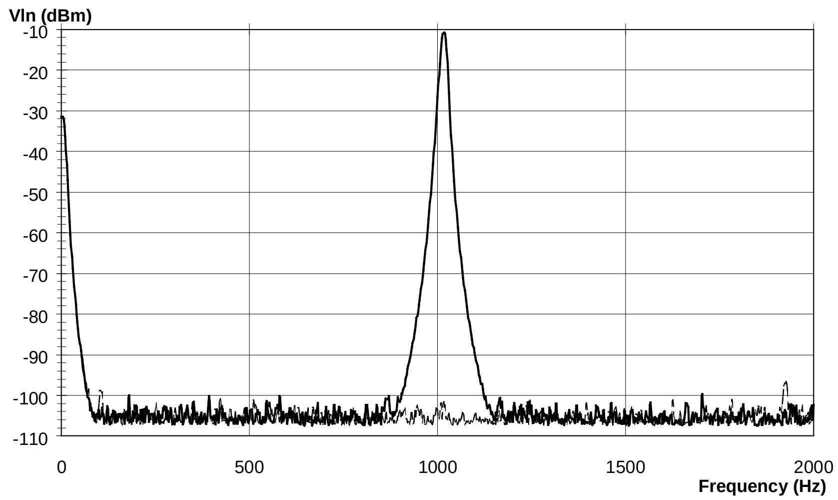


Fig. 18 Common mode rejection ratio on microphone

3.5 Earpiece amplifier block

Principle of operation

In fig. 19, the block diagram of the earpiece amplifier is depicted.

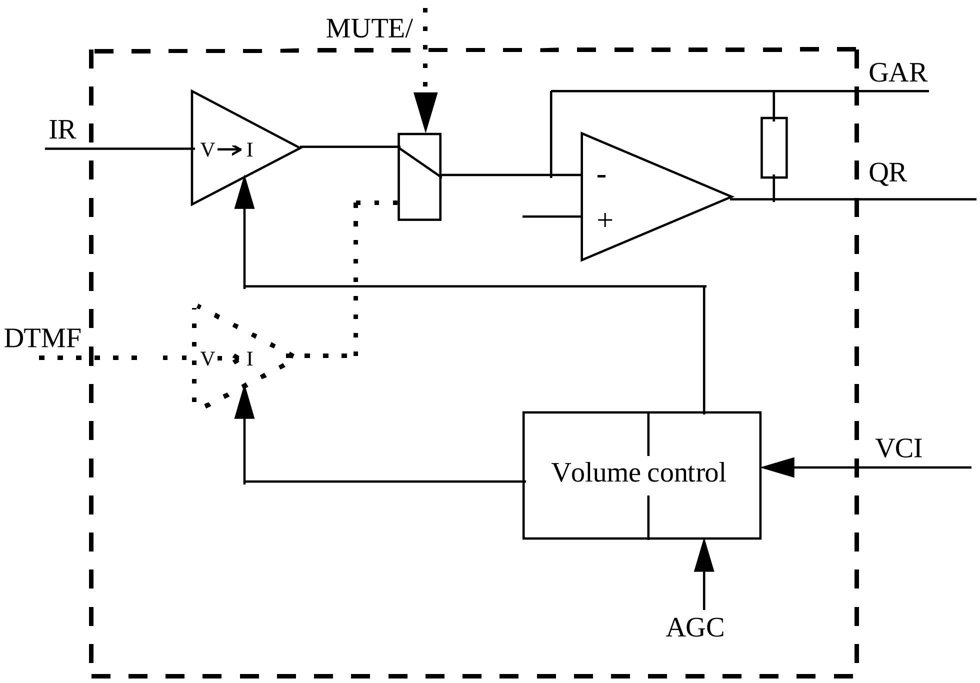


Fig. 19 Receive channel

As can be seen from fig. 19, the receive amplifier block is built up out of three parts: a preamplifier which realizes a voltage to current conversion followed by an end-amplifier which realizes the current to voltage conversion at QR and a volume control block that sets the convertion gain of the preamplifier. The preamplifier has an asymmetrical high input impedance between pins IR and VEE. It is equal to 22 kΩ with a maximum tolerance of +/-15%. The volume control provides 4 steps of gain with a typical step amplitude of 4.85 dB giving in total typically 14.5 dB.

The end-amplifier of the TEA1111A has a rail to rail output structure and can drive loads down to an impedance of 150 Ω at QR, the output capability is suitable for several kind of earpieces and can drive either dynamic, magnetic or piezo-electric earpieces. In case of magnetic or dynamic earpieces, a capacitor in series is required for decoupling. At minimum gain setting, the overall gain Gv(ir-qr) of the receive amplifier from input IR to output QR is given by the equation:

$$Gv(ir\text{-}qr)min = 20 \times \log Av(ir\text{-}qr)$$

$$Av(ir\text{-}qr)min = 1.35 \times Rgarint/Rrefint \times \alpha$$

with:

Rgarint = internal resistor realizing the current to voltage conversion (typically 123 kΩ with a spread of +/-15%)

Rrefint = internal resistor determining the current of an internal current stabilizer (typically 7.25 kΩ with a spread of +/- 15% correlated to the spread of Rgarint)

α = gain control factor varying from 1 at Iline = 15 mA to 0.5 at Iline = 75 mA when AGC function is applied (see chapter 3.5 for details)

Using these typical values in the equation, we find a gain equal to:

Gv(ir-qr)min = 20 $\times$ log Av(ir-qr) = 27.2 dB at Iline = 15 mA

The different gain controls (AGC; MUTE/) act on the receive preamplifier stage, modifying its transconductance.

Adjustments and performances

The gain of the earpiece amplifier can be externally reduced by 0 to -6 dB with a resistor Rgar connected between pins GAR and QR, however, this gain adjustment slightly increases the gain spread and affects the temperature coefficient due to matching between internal and external resistors.

The 4 steps of gain are generated by a voltage decoding of the voltage control input pin VCI. The gain versus VCI voltage is typically as follow:

0 V < VCI < 0.25 VDD:	Gmin (27.2 dB)
0.27 VDD < VCI < 0.54 VDD:	Gmin + 4.85 dB
0.56 VDD < VCI < 0.79 VDD:	Gmin + 9.7 dB
0.82 VDD < VCI < VDD:	Gmin + 14.5 dB = Gmax

Two external capacitors Cgar (connected between GAR and QR) and Cgars (connected between GAR and VEE) ensure stability of the earpiece amplifier when the relationship Cgars = 10 $\times$ Cgar is fulfilled. The capacitor Cgar provides a first order low pass filter, which cut-off frequency is determined with Rgar // Rgarint. Fig. 20 shows the frequency response and the typicall gains of the receive amplifier from IR to QR at different temperatures.

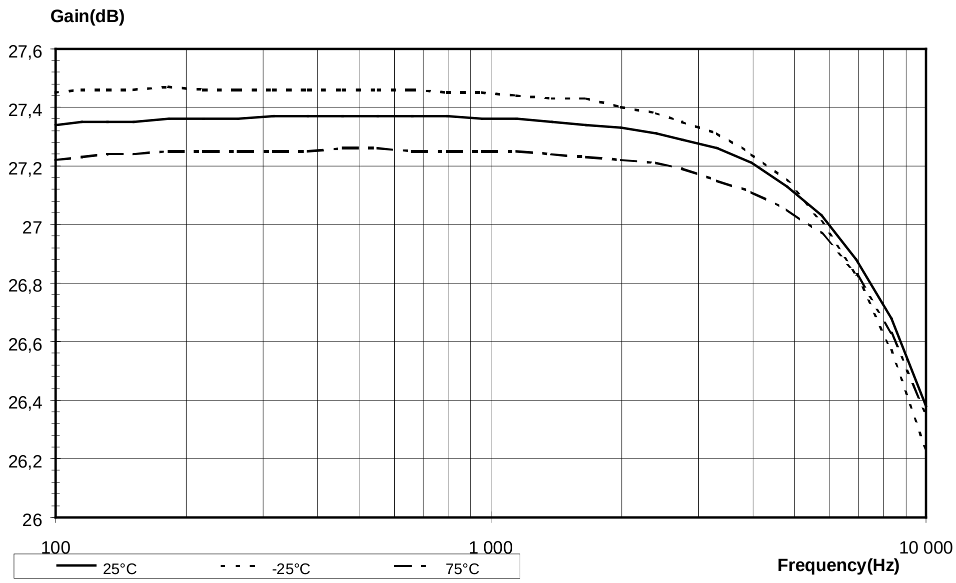


Fig. 20 Receive gains versus frequency: influence of temperature

The maximum output swing on QR depends on the DC line voltage, the Rcc resistor, the Icc current consumption of the circuit, the Ip current consumption of the peripheral circuits and the load impedance on QR.

The receiving input IR can handle signals up to 18 mVrms with less than 2% THD. Fig. 21 shows the distortion on QR for a line current equal to 15 mA with a gain setting at minimum and maximum on this amplifier. Fig. 22 shows the distortion for a line current of 15 mA with 150 and 450 Ω loads.

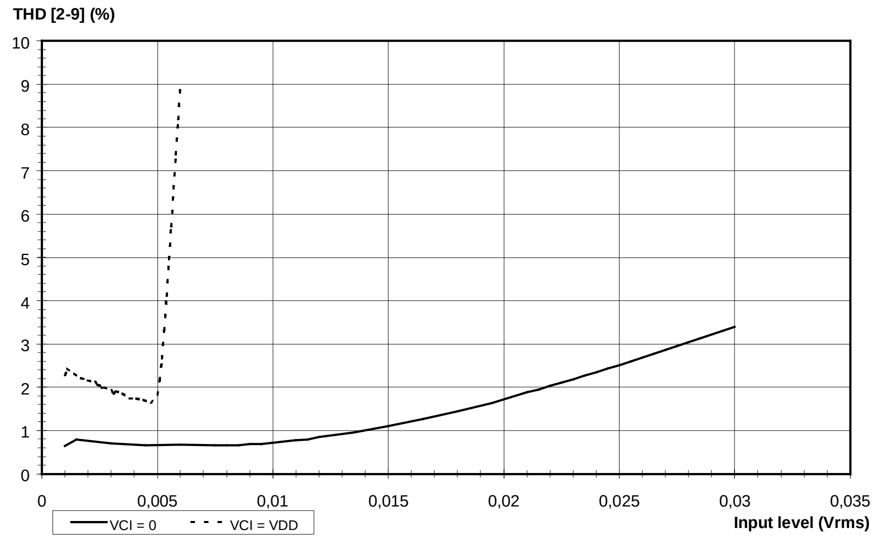


Fig. 21 Distortion on QR versus input signal on IR

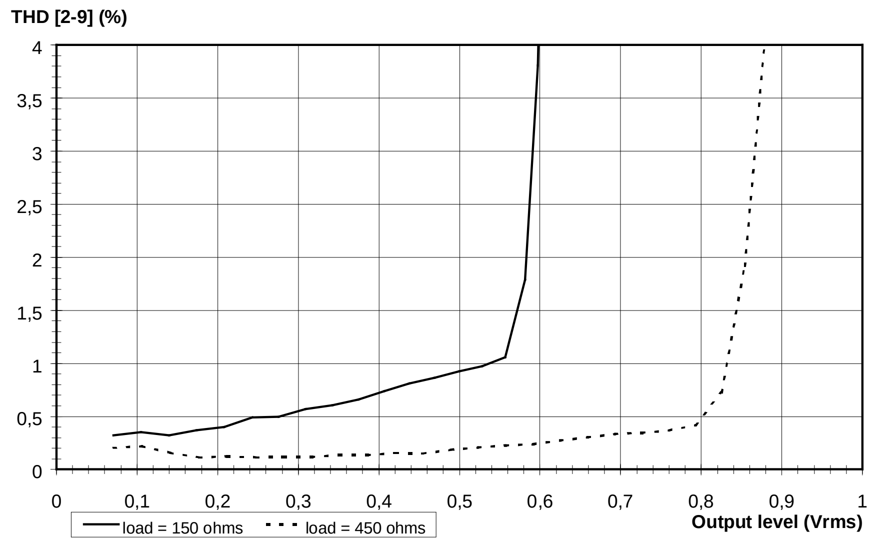


Fig. 22 Distortion on QR versus load

Fig. 23 shows the noise on QR loaded with 150 Ω (psophometrically weighted: P53 curve) as a function of the line current at different gains setting of this amplifier. This curve has been done with an open input IR. With the antisidetone network connected to the input IR, part of the microphone noise generated on the line will be added.

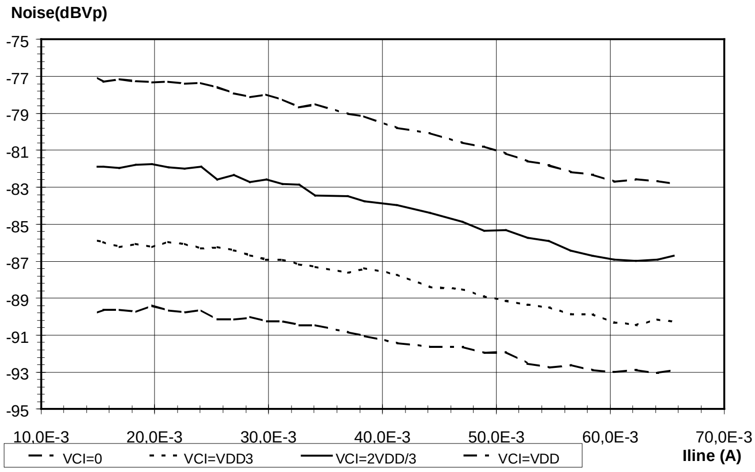


Fig. 23 Noise on QR

3.6 Automatic gain control

Principle of operation

The TEA1111A performs automatic line loss compensation. The automatic gain control varies the gain of the microphone and receive amplifiers in accordance with the DC line current. To enable this AGC function, the pin AGC must be connected to the pin VEE. For line currents below a current threshold, Istart (typically 23 mA), the gain control factor α is equal to 1, giving the maximum value to the gains Gv(mic-ln) and Gv(ir-qr). If this threshold current is exceeded, the gain control factor α is reduced and then the gains of the controlled microphone and receive amplifiers are also reduced. When the line current reaches an other threshold current, Istop (typically 59 mA), the gain control factor α is limited to its minimum value equal to 0.5, giving the lower value to the microphone and receive controlled gains. The gain control range of both amplifiers is typically 6 dB, which corresponds approximately to a line length of 5 km (0.5 mm twisted pair copper) with an attenuation of 1.2 dB/km.

The attenuation is correlated to the current Iagc sunk at pin AGC: when this current is lower than typically 4.6 µA the gains are maximum, when this current is higher than typically 14 µA the gains are minimum. This current is proportional to the voltage between pins SLPE and VEE. There is an internal resistor which sets Istart and Istop, adding one externally in series (between pins AGC and VEE) reduces Iagc and therefore increases the values of Istart and Istop.

Adjustments and performances

The AGC of the TEA1111A can be used with different exchange supply voltages and different feeding bridge resistances. For this purpose, a resistor Ragc, can be inserted between pins AGC and VEE. This Ragc resistor increases both threshold currents Istart and Istop proportionally. Fig. 24 shows the control of the microphone gain versus the line current for different values of Ragc. When no AGC function is required, the AGC pin must be left open, then the control factor α equals to 1 and both controlled gains are at their maximum values.

When Ragc = 0 and the value of Istart is too high, increasing the value of Rslpe reduces proportionally Istart and shifts the AGC to lower currents. In this case, the value of Istop is also reduced and the gains are modified. If the value of Rslpe has to be increased a lot, it is possible to restore the typical gains by connecting in parallel an RC series network which makes a total AC impedance of 20 Ω.

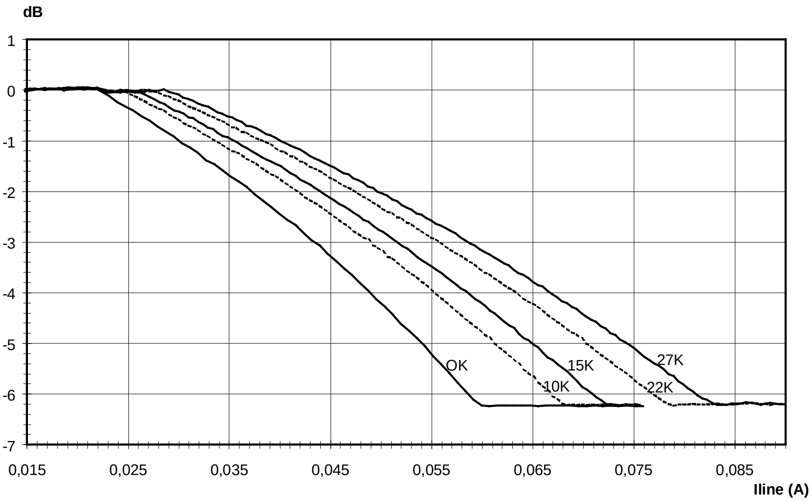


Fig. 24 AGC on the microphone gain versus line current and Ragc

3.7 DTMF amplifier

principle of operation

In fig.24, the block diagram of the DTMF channel of the TEA1111A is depicted.

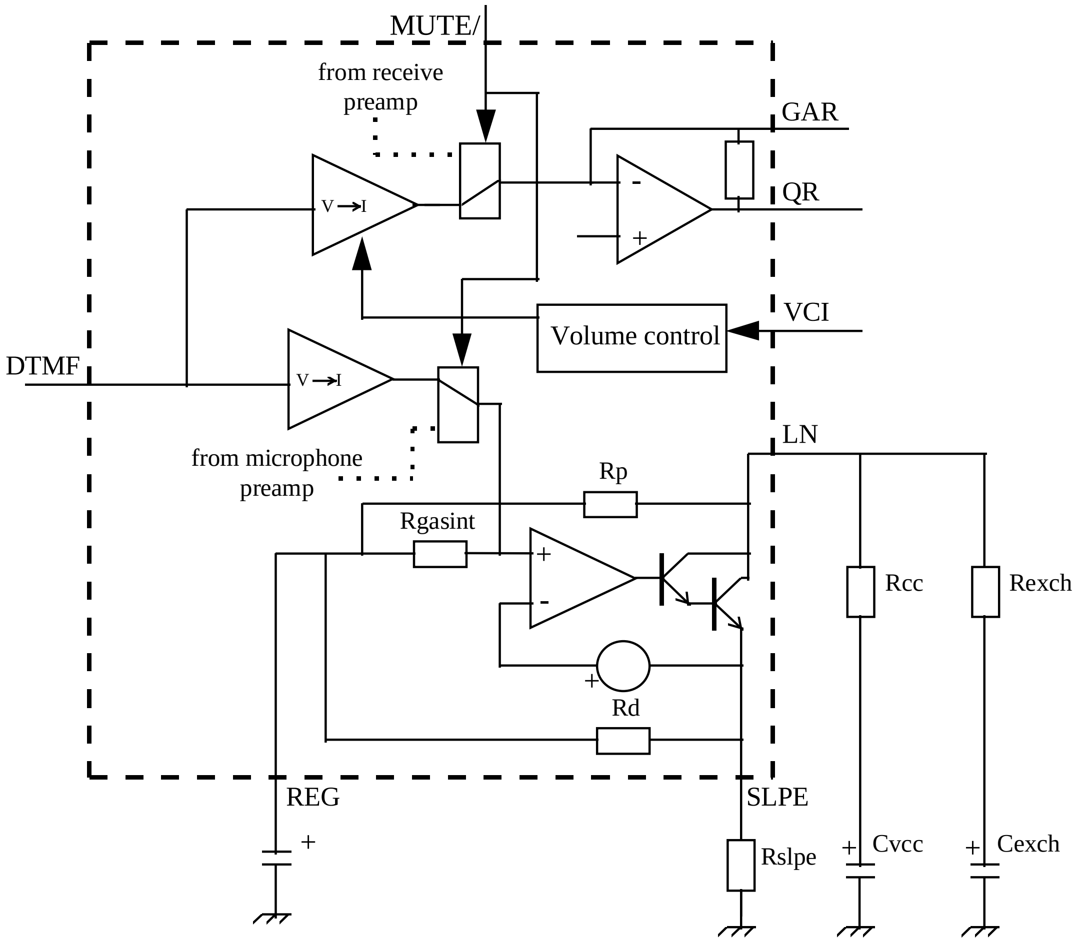


Fig. 25 DTMF channel of the TEA1111A

The DTMF amplifier has an asymmetrical high input impedance of 20 kΩ between pins DTMF and VEE with a maximum spread of +/-15%. The input is biased at VEE, so when the input DTMF signal is polarized at VEE, the decoupling capacitor is not necessary. The DTMF amplifier is built up out of two parts: a preamplifier which realizes the voltage to current conversion and the same end-amplifier as the microphone amplifier. No AGC is applied to the DTMF channel. The overall gain Gv(mf-ln) of the DTMF amplifier from input DTMF to output LN is given by the following equation:

$$Gv(mf\text{-}ln) = 20 \times \log Av(mf\text{-}ln)$$

$$Av(mf\text{-}ln) = 0.244 \times (Rgasint / Rrefint) \times (Ri//Zline / Rslpe)$$

with:

Ri = the AC apparatus impedance, Rcc//Rp (typically 620 Ω // 17.5 kΩ)

Rgasint = internal resistor realizing the current to voltage conversion (typically 29.5 kΩ with a spread of +/-15%)

Rrefint = internal resistor determining the current of an internal current stabilizer (typically 7.25 kΩ with a spread of +/- 15% correlated to the spread of Rgasint)

Zline = load impedance of the line during the measurement

Using these typical values in the equation and assuming Zline = 600 Ω, we find a gain equal to:

Gv(mf-ln) = 20 × log Avmf = 25.9 dB

Furthermore, the DTMF signal is attenuated and sent to QR as confidence tone with the volume control providing 4 steps of gain with a typical step amplitude of 4.7 dB giving in total typically 14.2 dB.

Fig. 26 shows the frequency response of the DTMF amplifier at 15 mA and different temperatures.

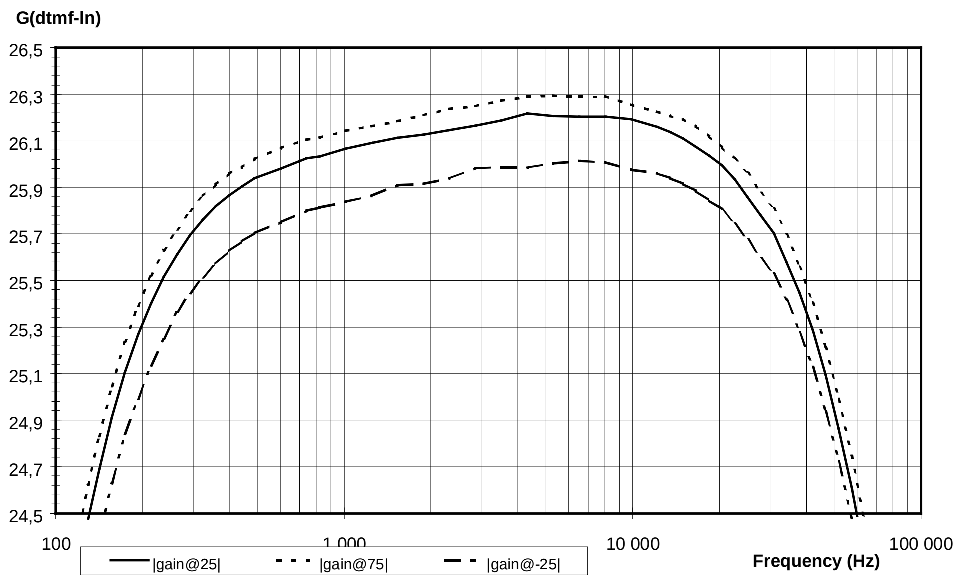


Fig. 26 DTMF gains versus frequency: influence of temperature

The input of the DTMF amplifier can handle signals up to 110 mVrms with less than 2% THD. Fig. 27 shows the distortion on line versus the rms input signal at Iline = 15 mA.

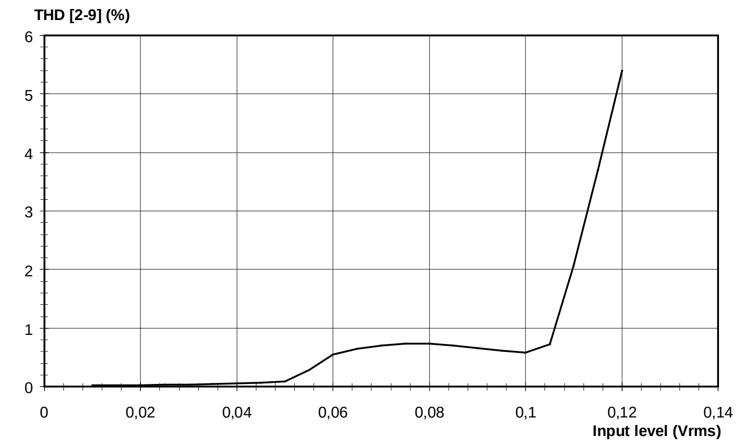


Fig. 27 Distortion of the DTMF signal on line versus input signal

3.8 "MUTE" function

Principle of operation

The "mute" realizes an electronic switching between the speech mode and the dialling mode. If a low level is applied to the MUTE/ input, both the microphone and the receive channels are disabled while the DTMF channel is enabled. By applying a high level or leaving pin MUTE/ open the microphone and the receive channels are enabled while the DTMF channel is disabled. The MUTE/ input has a pull-up structure to VCC, so it can be directly driven by an open drain output. Nevertheless, in case of I/O structure on the microcontroller side, a push-pull output structure is recommended to polarize properly the input of the microcontroller when VCC varies (no current will flow from VDD to VCC via this pin). The threshold voltage level is 0.65 V typically with a temperature coefficient of -2 mV/°C. Fig. 28 shows the MUTE/ input current versus MUTE/ input voltage.

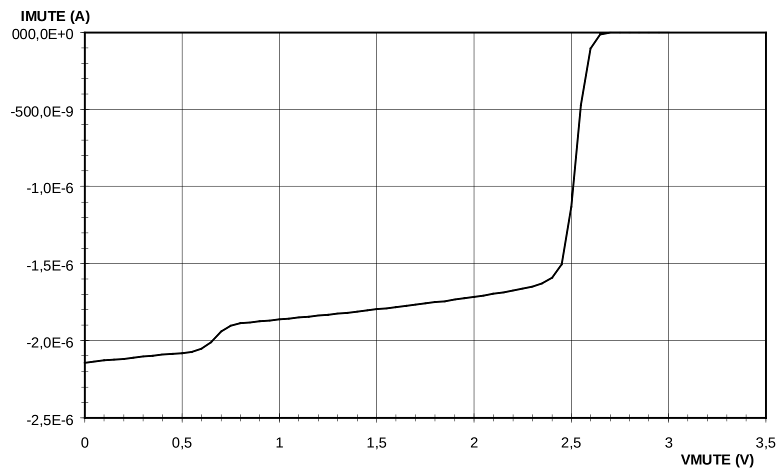


Fig. 28 MUTE/ input current versus MUTE/ input voltage

Adjustments and performances

Fig. 29 shows the microphone amplifier gain reduction at Iline = 15 mA for an input signal of 1 kHz versus the MUTE/ input voltage.

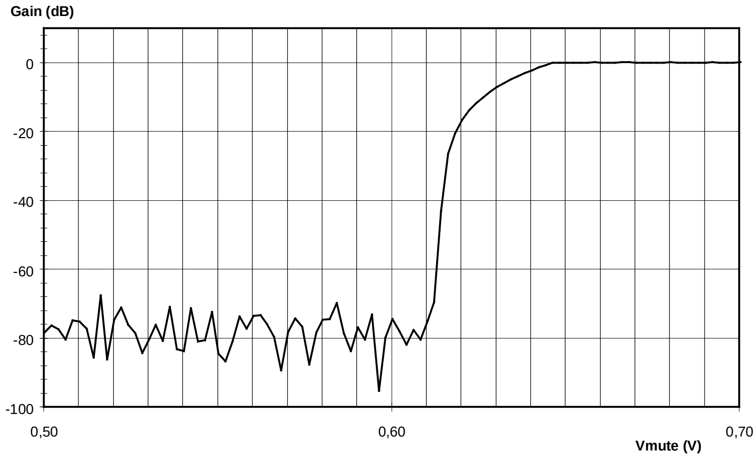


Fig. 29 Microphone gain reduction versus MUTE input voltage

The “mute” function works down to a voltage on VCC equal to about 1.7 V. Below this threshold, the microphone and receive amplifiers remain always enabled independently of the MUTE/ input level. The maximum voltage allowed at the MUTE/ input is VDD and the minimum is GND-0.4 V.

3.9 Anti-sidetone network

Principle of operation

To avoid the microphone signal to come back with a too high level in the receive channel, the anti-sidetone circuit uses the microphone signal from pin SLPE (which is in opposite phase) to cancel the microphone signal at the IR input of the receive amplifier. The anti-sidetone bridge already used for the TEA111x (or TEA106x) families or a conventional Wheatstone bridge as shown in fig. 30 may be used for the design of the anti-sidetone network.

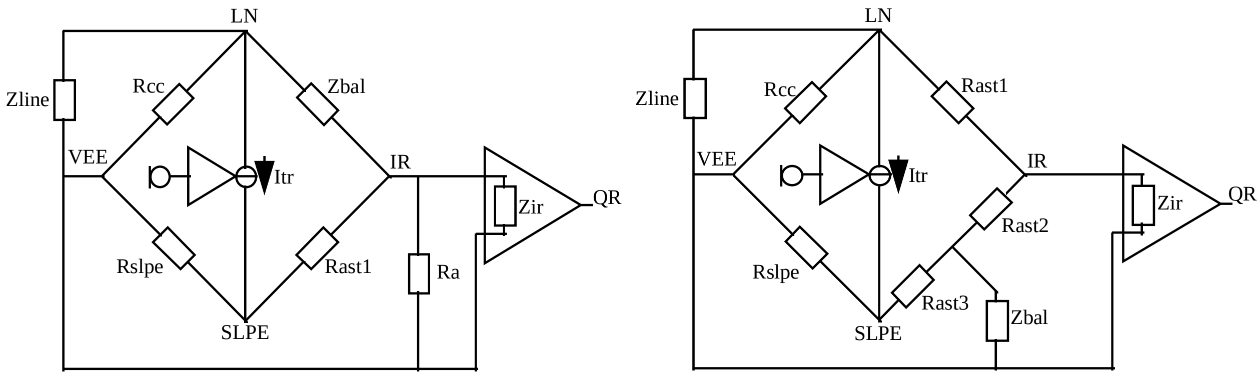


Fig. 30 Wheatstone bridge (left) and TEA111x family anti-sidetone bridge (right)

The TEA111x (or TEA106x) family anti-sidetone bridge has the advantage of a relative flat transfer function in the audio frequency range to the output QR, both with real and complex set impedances. Furthermore, the attenuation of the bridge for the receive signal (between pins LN and IR) is independent of the value chosen for Zbal after the set impedance has been fixed and the condition shown in equation (a) is fulfilled. Therefore, readjustment of the overall receive gain is not necessary in many cases.

Compare to the previous one, the Wheatstone bridge has the advantages of needing one resistor less and a smaller capacitor in Zbal. But the disadvantages include the dependence of the attenuation of the bridge on the value chosen for Zbal and the frequency dependence of that attenuation moreover, the input stage may introduce some distortion on high level signal. This requires some readjustment of the overall receive gain.

3.9.1 TEA111x family bridge

The anti-sidetone circuit is composed of: Rcc//Zline, Rast1, Rast2, Rast3, Rslpe and Zbal. Maximum compensation is obtained when the following conditions are fulfilled:

$$\text{Rslpe} \times \text{Rast1} = \text{Rcc} \times (\text{Rast2} + \text{Rast3}) \quad \text{(a)}$$

$$k = [\text{Rast2} \times (\text{Rast3} + \text{Rslpe})] / (\text{Rast1} \times \text{Rslpe})$$

$$\text{Zbal} = k \times \text{Zline}$$

The scale factor k is chosen to meet the compatibility with a standard value of capacitor for Zbal.

In practice, Zline varies strongly with the line length and line type. Consequently, the value for Zbal has to be chosen to fit with an average line length giving acceptable sidetone suppression with short and long lines. The suppression further depends on the accuracy with which Zbal equals this average line impedance.

Example

Let’s optimize for a theorical equivalent average line impedance shown in Fig. 31.

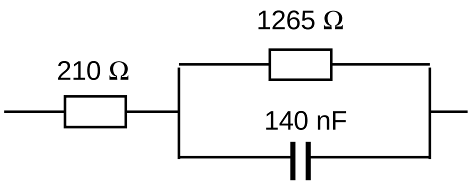


Fig. 31 Equivalent average line impedance

For compatibility of the capacitor value in Zbal with a standard capacitor value from the E6 series (220 nF):

$$k = 140 / 220 = \mathbf{0.636}$$

For Rast2, a value of 3.92 kΩ has been chosen. So, using the previous equations, we can calculate Zbal, Rast1, Rast3. We find Rast1 = 130 kΩ, Rast3 = 390 Ω, and for Zbal **130 Ω in series with 220 nF // 820 Ω.**

The attenuation of the receive line signal between LN and IR can be derived from the following equation:

$$\text{Vir} / \text{Vln} = (\text{Zir} // \text{Rast2}) / [\text{Rast1} + (\text{Zir} // \text{Rast2})]$$

If Rast2 >> (Rast3 // Zbal).

With the values used in this example, it gives 32 dB at 1 kHz.

Zir is the receive amplifier input impedance, typically 20 kΩ.

3.9.2 Wheatstone bridge

The conditions for optimum suppression are given by:

Zbal = (Rast1 / Rslpe) × (Rcc // Zline)

Also, for this bridge type, a value for Zbal has to be chosen that corresponds with an average line length.

The attenuation of the received line signal between LN and IR is given by:

Vir / Vln = (Zir // Rast1 // Ra) / [Zbal + (Zir // Rast1 // Ra)]

Ra is used to adjust the bridge attenuation; its value has no influence on the balance of the bridge.

4. APPLICATION COOKBOOK

In this chapter, the procedure for making a basic application is given. Refering to fig. 32, the design flow is given as a number of steps which should be made. As far as possible for every step, the components involved and their influence on every step are given.

Step	Adjustment
DC setting :	
Adjust the DC setting of the TEA1111A to the local PTT requirements.	
Voltage LN-VEE	This voltage can be adjusted by changing Vref: increased up to 7 V with the Rva resistor between pins REG and SLPE (or decreased down to 3 V with a resistor between REG and LN).
DC slope	The DC slope might be modified by changing the value of Rslpe (this is not advised: all gains are modified, AGC characteristic is modified).
Supply point VCC	In line powered applications, depends on the values of Vref and the resistive part of the impedance network (Rcc + Rz).
Artificial inductor	Its value can be adjusted by changing the value of Creg: a smaller value speeds-up the DC current shape during transients but decreases the value of the inductance and therefore affects the BRL at low frequencies.
Impedance and sidetone :	
After setting the required set impedance, the sidetone has to be optimized using the antisidetone network in order to minimize the loop gain in all line conditions. AGC can be adjusted at that step.	
Application impedance	The BRL is adjusted with the impedance network connected between LN and VCC (Rcc + Rz//Cz).
Sidetone	Adjust Zbal (Rbal1, Rbal2, Cbal) according to the line characteristics.
AGC	Internally defined, the characteristics (Istart and Istop) can be shifted to higher line currents with an external Ragc resistor connected between AGC and VEE. In case it is necessary to shift Istart and Istop to lower current values, the value of Rslpe must be increased proportionally (see §3.6).

Step	Adjustment
TEA1111A microphone and receive gains	
Microphone gain	The microphone gain of the application has to be adjusted before entering pins MIC+/MIC- of the TEA1111A. It can be reduced by using the resistor Rtx3 which forms a bridge attenuator with Rtx1 and Rtx2. Ctx1, Ctx2 form a high-pass filter with Rtx1, Rtx2 in series with the input impedance at MIC+/MIC-. A capacitor Cmic forms a low-pass filter with the impedance of the microphone and the resistors Rmicp/Rmicm.
Earpiece gain	The gain between IR and QR is fixed at 27.2 dB when VCI is 0 V and can be increased by steps of 4.85 dB. This gain can also be slightly reduced by means of a resistor Rgar. The VCI input thresholds are compatible with digital control on two digits via R-2R network (VCIL, VCIH). A capacitor Cgar in parallel with Rgar forms a low-pass filter, stability is ensured with capacitor Cgars ($10 \times$ Cgar) between pins GAR and VEE.
TEA1111A DTMF gain	
DTMF	The DTMF is selected with a low level on pin MUTE/. Its level on line must be adjusted before entering pin DTMF. The capacitor Cmf can be removed when the input signal is biased at VEE.

5. EXAMPLE OF APPLICATION

A demoboard (OM5889) is available. As the TEA1111A may be used in various applications, this demoboard includes only the TEA1111A with its basic environment.

Fig. 32 gives the schematic of the demoboard while fig. 33 gives its component placement diagram. On these schematics, the capacitors connected with dotted lines are indicated for RFI immunity purpose.

According to the application, it is possible to connect the electret microphone to VDD instead of VCC. In this case, the current capability of VDD would be reduced by the electret consumption and the current capability of VCC would be increased by the same value (which would allow a slight increase of the earphone amplifier capability), moreover, the electret microphone consumption would discharge the capacitor C_{VDD}.

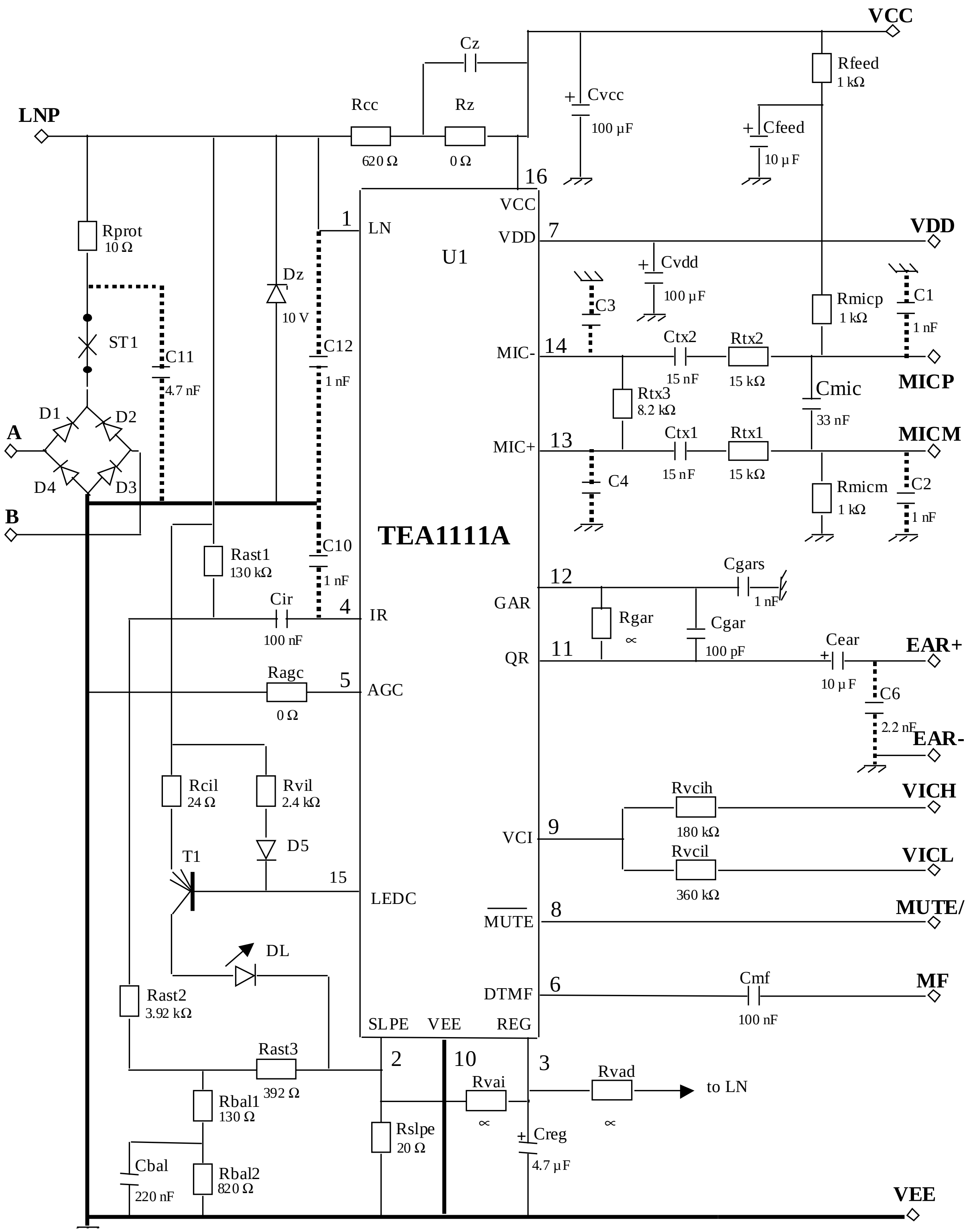


Fig. 32 Basic application of the TEA1111A

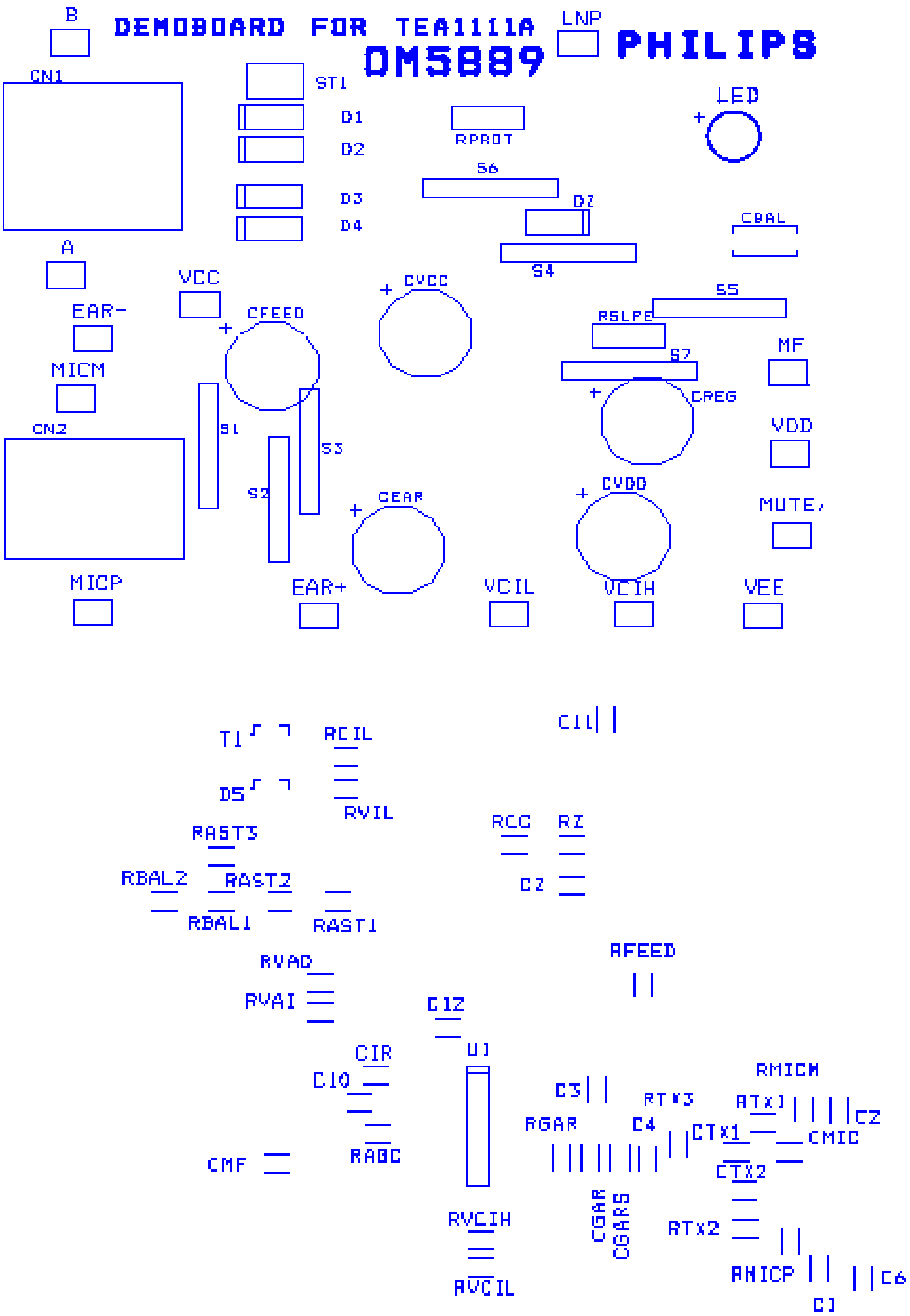


Fig. 33 Component placement diagram of the demoboard

6. ELECTROMAGNETIC COMPATIBILITY

As no common international specification exists for RFI immunity, and as different assembly methods may lead to different solutions, only some advices can be provided.

It is advisable to take care of the impedance of the Ground, the smallest is always the best. This means that the Ground (VEE) trace must always be as large as possible, the best is to have a second layer dedicated to this purpose.

MIC+/MIC- inputs may also be sensitive (RF signals entering these pins would be amplified). Care has to be taken with the lay-out of the microphone amplifier, which is also helpful for the noise, providing a good decoupling to VEE. Capacitor of a few hundred pF forming low-pass RC filters to VEE may be added at the input of the amplifier (C3, C4).

Low impedance capacitors in parallel with the electrolythic one between VCC and VEE as well as in parallel with the Creg capacitor may help.

Usually a low impedance capacitor connected between LN and VEE (C12) helps for the conducted interferences, but this capacitor is in parallel with the impedance network of the apparatus, so, its value must be small enough.

In general when connections come from external environment (e.g. MICP, MICM, A, B,EAR+ on the demoboard), it is better to filter the RFI signal before it influences the close environment of the TEA1111A (e.g. action of C1, C2, C11, C6 on the demoboard). When C6 has to be larger than 2.2 nF, a small resistor between QR and C6 may be necessary for stability.

NB: At very high frequencies (1 to 2 Ghz), the parasitic inductance of the RFI capacitors as well as the length of their connections (about 1 nH per mm) becomes a major concern and may inhibit the effect of these capacitors, at those frequencies, SMD capacitors are preferred.

7. REFERENCES

[1] TEA1111A Speech circuit with dialler interface, regulated supply and earpiece volume control
Device specification

[2] TEA1111A Line Interface Demonstration Board
User Manual of OM5889 TEA1111A Line Interface Demonstration Board

[3] Philips Semiconductors
Semiconductors for Wired Telecom Systems
Data Handbook -IC03a -

[4] Philips Semiconductors
Semiconductors for Wired Telecom Systems
Application Handbook -IC03b -

APPENDIX LIST OF ABBREVIATIONS AND DEFINITIONS

A-B	Line terminals of application example
AGC	Automatic Gain Control: line loss compensation
BRL	Balance Return Loss: matching between the apparatus impedance and a reference
DTMF	Dual Tone Multi Frequency
EMC	ElectroMagnetic Compatibility
GAR	Earpiece amplifier gain adjustment pin of the TEA1111A
Gv(mf-ln)	DTMF amplifier gain
Gv(ir-qr)	Earpiece gain
Gv(mic-ln)	Microphone gain
IC	Integrated circuit
Icc	Current consumption of the TEA1111A on VCC
Idd	Current in supply point VDD
Iline	Line current
Ip	Current consumption of the peripherals on VCC
Irec	Internal current consumption (from VCC) of the receive amplifier
IR	Receive amplifier input pin of the TEA1111A
Islpe	Part of the line current flowing through SLPE pin
Istart	Start current of the AGC function
Istop	Stop current of the AGC function
Isup	Supply current of the voltage regulator
Ith	Threshold current of the low voltage part
k	Scale factor of anti-sidetone network
Leq	Artificial inductor of the voltage stabilizer
MUTE/	MUTE/ input of the TEA1111A
OM5889	Demoboard of the TEA1111A
QR	Earpiece amplifier output pin of the TEA1111A
Ra	Resistor to adjust the sidetone bridge attenuation
Rast	Antisidetone resistor
REG	Filter capacitor of the equivalent inductor connection pin of the TEA1111A
Rexch	Bridge resistance of exchange
RFI	Radio Frequency Interference

Rgarint	Internal resistance (123 kΩ) which sets the receive gain
Rgasint	Internal resistance (29.5 kΩ) which sets the microphone gain
Rp	Internal resistance between LN and REG
Rva	Voltage adjustment resistor
SLPE	Slope input pin of the TEA1111A
THD	Total Harmonic Distortion (%)
MIC+/MIC-	Microphone amplifier input pins of the TEA1111A
VCC	Positive supply of the TEA1111A
VDD	Regulated supply
VEE	Ground reference of the TEA1111A
Vln	DC voltage between LN and VEE
Vref	Stabilized reference voltage between LN and SLPE
Vslpe	DC voltage level between SLPE and VEE
Zir	Input impedance of the receive amplifier of the TEA1111A
Zbal	Anti-sidetone network balance impedance
α	Gain control factor of the AGC