# AN987

# DRAM Refresh Modes

DRAMs offer the lowest cost per bit of any memory, and for that reason are enormously popular in a wide range of applications. This low cost per bit is achieved with a very simple bit cell design, among other things, but rooted in this simplicity are some inherent drawbacks. One major limitation is the need to refresh each memory bit at regular intervals. This note discusses what refresh is, the reasons refresh is required for DRAM operation, and the various types of refresh available on Motorola DRAMs. Refer to individual data sheets for information on specific devices.

The heart of any memory device is the bit cell. A 4M DRAM has 4,194,304 of these cells in the memory array. Each cell holds a single bit of information in the form of a high or low voltage, where high voltage = a binary “1”, and low voltage = a binary “0”. The DRAM bit cell consists of one transistor and one capacitor. The transistor acts as a switch, regulating when the capacitor will charge and discharge, while the capacitor stores a high or low voltage charge.

All capacitors leak over time, slowly losing the charge stored in them, regardless of how carefully they are constructed. Junction and dielectric leakage are two capacitor discharge paths that are characteristic of the DRAM bit cell, and both are affected by temperature. The capacitor in the bit cell can hold a small charge, on the order of 35 fF for 4M DRAM technology. As this charge dissipates through leakage paths, the small difference between a “1” and a “0” diminishes. If nothing is done to restore the charge for a “1” on the capacitor to its initial value, the sensing circuitry on the DRAM will eventually be unable to detect a charge difference and will read the cell as a “0”.

Thus, all the capacitors in the memory array must be periodically recharged, or refreshed. Refresh is accomplished by accessing each row in the array, one row at a time. When a row is addressed, the decoded wordline (row) is connected to the wordline driver which enables the transfer gates for all of the cells on the selected row. This connects the storage capacitors to the bitlines (columns) and the stored data states are detected and latched by the sense amplifiers. The sense amplifiers swing the bitlines to the rails, rewriting (refreshing) the stored data. The specified refresh time has improved with each new generation of DRAM; 2 ms for the 16K DRAM, 4 ms for the 256K DRAM, 8 ms for the 1M DRAM, 16 ms for the 4M DRAM, and 32 ms for the 16M DRAM. Longer refresh times mean more time available for access to memory, and less time required to refresh the device.

Design and operation of the DRAM allow only one row to be refreshed at a time. The actual number of refresh cycles required to refresh the entire array depend on the architecture and configuration of the DRAM, and can be found in the data sheet of the specific device. Motorola’s 4M x 1 DRAM, the MCM54100A-70, will be used to illustrate the various refresh modes available. In the case of the 4M x 1 DRAM, there are 1024 rows, with 4096 bits in each row.

Refresh can be performed in either a single burst of 1024 refresh cycles (one cycle per row) every 16 ms, or distributed over time, one refresh cycle every 15 μs (16 ms per 1024 rows = 15.6 μs per row) or some combination of these two extremes. As long as every row is refreshed within 16 ms, the actual method used is best determined by system use of the DRAM. The burst takes 133 μs to complete (130 ns per row x 1024 rows on a 70 ns device). Distributed refresh takes 130 ns per row, again taking 133 μs to refresh the entire array. No memory operations (reading or writing) can take place during the refresh period.

The 4M x 1 DRAM can be refreshed in three ways: $\overline{\text{RAS}}$-only refresh (ROR), $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh (CBR), and hidden refresh. In addition, any normal read or write operation refreshes the row accessed. In any case, the time required to refresh one row is the random read or write cycle time ($t_{RC}$) of the device (130 ns in the case of the MCM54100A-70). The device must be in normal random mode, not test mode, to utilize any of these specific refresh methods.

$\overline{\text{RAS}}$-only refresh requires external row counters, to ensure all rows are refreshed within the specified time, and externally supplied row addresses. These are typically supplied by a DRAM controller similar to the design shown in AN1063. ROR is performed by supplying row addresses and completing a $\overline{\text{RAS}}$ cycle; switching $\overline{\text{RAS}}$ from inactive (high) to active (low), holding $\overline{\text{RAS}}$ low for $t_{RAS}$, then switching back to high, and holding $\overline{\text{RAS}}$ high for $t_{RP}$. $\overline{\text{CAS}}$ must be held high throughout the ROR cycle, hence the name $\overline{\text{RAS}}$-only refresh. Figure 1 illustrates the $\overline{\text{RAS}}$-only refresh cycle of the 4M DRAM.

$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh relies on an internal refresh counter which generates the address of the next row to be refreshed. CBR is performed by switching $\overline{\text{CAS}}$ from high to low while $\overline{\text{RAS}}$ is high, then switching $\overline{\text{RAS}}$ low after $t_{CSR}$, and remaining low for $t_{RAS}$. The write enable pin (W), must be high during the $\overline{\text{RAS}}$ active transition in order to prevent entry into the 4M DRAMs test mode. This reversal of the usual clock order activates the internal refresh counter that generates the address of the row to be refreshed; external row addresses are ignored. $\overline{\text{CAS}}$ must be held low for $t_{CHR}$ after $\overline{\text{RAS}}$ goes low, then it becomes a don’t care. Figure 2 illustrates the $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle of the 4M DRAM.

Hidden refresh is a special case of CBR that maintains valid data at the output if $\overline{\text{CAS}}$ remains low after $t_{CHR}$, as shown in Figure 3. With $\overline{\text{CAS}}$ held low, $\overline{\text{RAS}}$ is switched high after $t_{RAS}$, held high for $t_{RP}$, and then switched low again, beginning another $\overline{\text{RAS}}$ cycle and refreshing the next row address generated by the internal refresh counter. As long as $\overline{\text{CAS}}$ is held low, data is valid at the output, resulting in a long read cycle. Since data can be read while the device is being refreshed, the refresh operation appears to be hidden by the read cycle. The same refresh can be performed after a write cycle is initiated, as long as $\overline{\text{W}}$ is held high during the $\overline{\text{RAS}}$

active transition, in order to prevent entry into the test mode. Apart from the initial write operation, additional write operations cannot be performed during the hidden refresh cycle, as shown in Figure 4.

In addition to these traditional refresh methods, many of the newer DRAM configurations, such as Motorola's MCM5V4800 512K x 8 DRAM, are incorporating a self refresh feature, removing the need to have the external counters and timers of the DRAM controller on a battery backup circuit. The self refresh operation is entered just as a normal $\overline{CAS}$ before $\overline{RAS}$ refresh, but $\overline{CAS}$ and $\overline{RAS}$ are both held low for a time greater than $t_{RASS}$ (> 100 μs), as shown in Figure 5. After this time, the DRAMs internal timer starts, and a new row address generated by the internal refresh counter is refreshed approximately every 130 μs. When the refresh pulse is generated by the internal timer, the $I_{CC}$ current may peak as high as 120 mA, but the average self refresh current $I_{CCS}$ is guaranteed to be less than 200 μA, as shown in Figure 6. The self-refresh mode is exited when either $\overline{RAS}$ or $\overline{CAS}$ goes high.

The importance of the internal refresh counter can be seen in many of the refresh methods discussed, and as such, some customers may wish to test its operation by using the $\overline{CAS}$ before $\overline{RAS}$ refresh counter test. This test is performed with a read-write operation. During the test, the internal refresh counter generates the row addresses, while the external address supplies the column address. The entire array is refreshed after 1024 cycles, as indicated by the check data written in each row. The test can be performed after the minimum of eight CBR initialization cycles. This test procedure is as follows and is illustrated in Figure 7.

1. Write the entire array with "0"s using the normal write mode.
2. Select a column address, read the "0" and write a "1" by performing the CBR counter test, read-write cycle. Repeat 1024 times. The array will now contain all "0"s, except for a single column of "1"s.
3. Read the entire column of "1"s using the normal read mode.
4. Using the same starting column address as in step 2, read the "1" and write a "0" by performing the CBR counter test, read-write cycle. Repeat 1024 times.
5. Read the entire column of "0"s using the normal read mode.
6. Repeat steps 1 through 5 using complement data.

Refresh is an integral and necessary part of DRAM operation. Substantial improvements have been made in increasing the time between refresh cycles, but as long as bit cell design utilizes a capacitor, periodic recharging will be required. The wide variety of refresh methods available in DRAMs offered by Motorola allow their use in virtually any system.

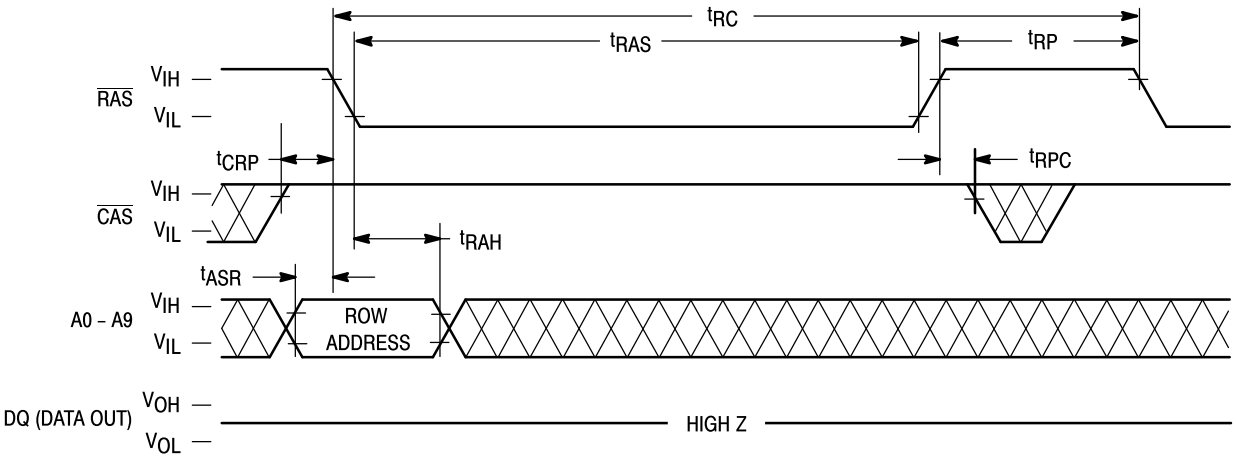


**Figure 1. $\overline{RAS}$-Only Refresh Cycle**
($\overline{W}$ and A10 are Don't Care)

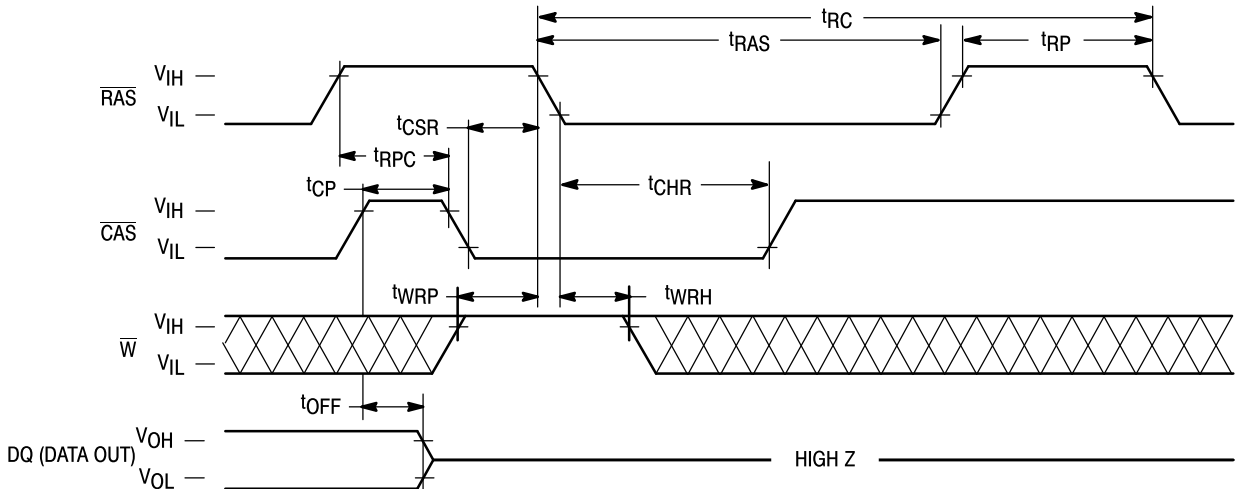


**Figure 2. $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle**

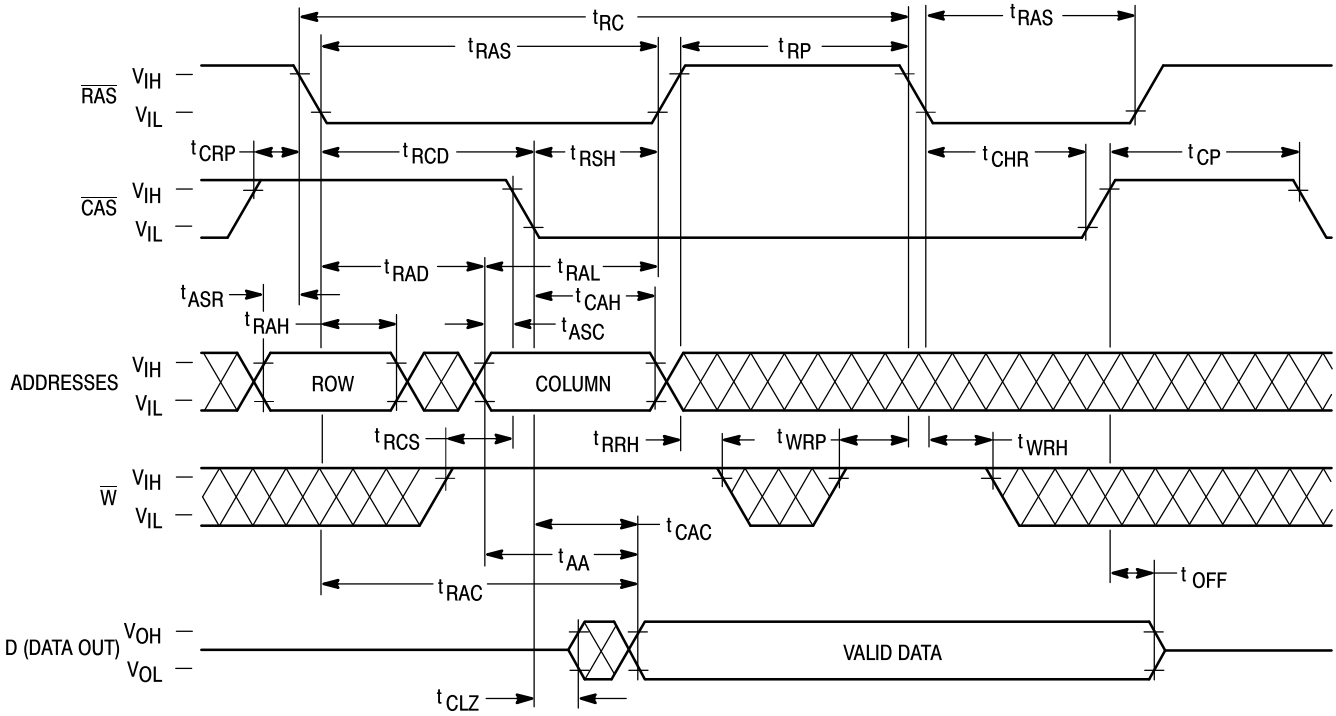


**Figure 3. Hidden Refresh Cycle (READ)**

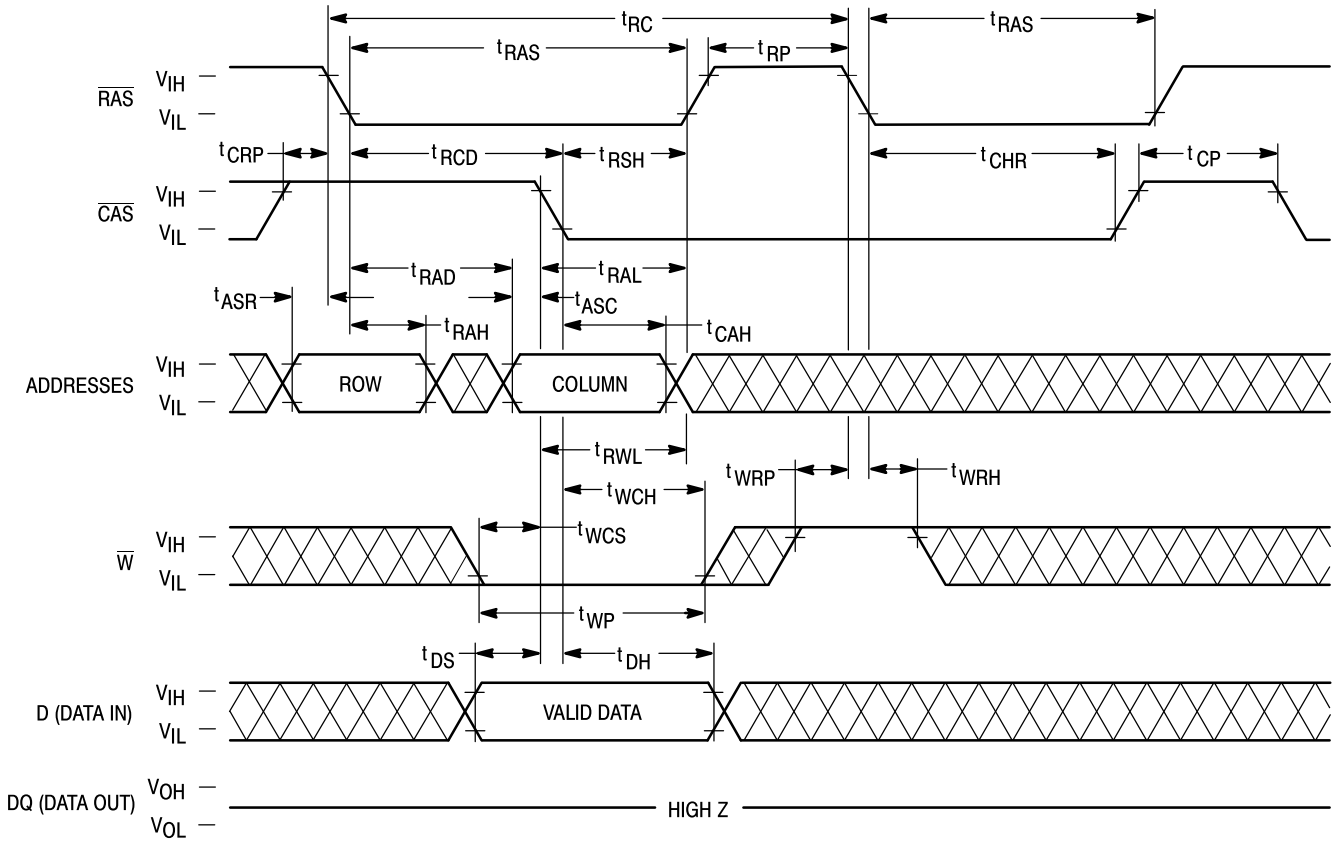


**Figure 4. Hidden Refresh Cycle (EARLY WRITE)**

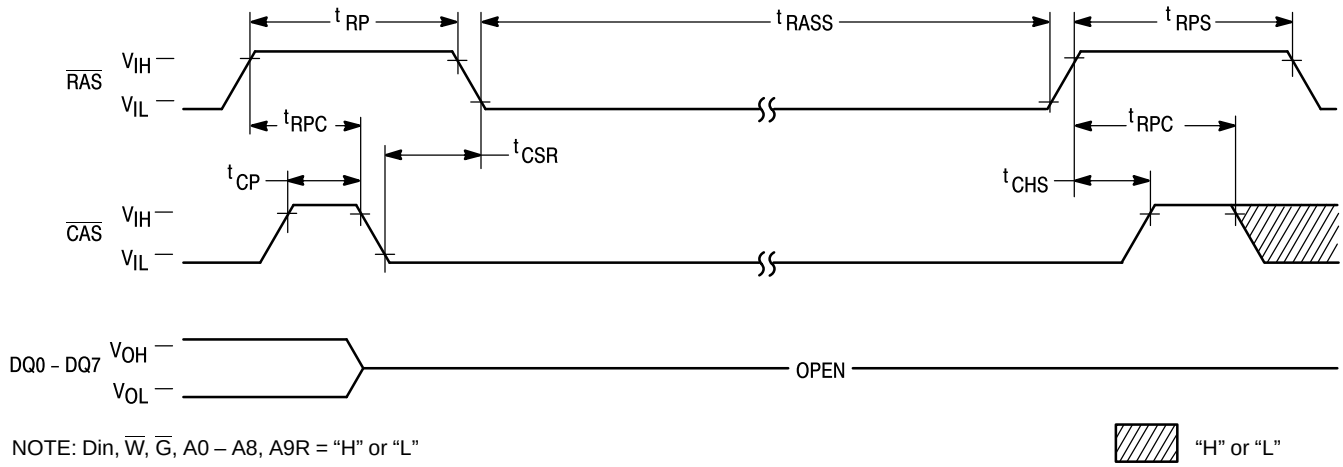


**Figure 5. CAS Before RAS Self-Refresh Cycle for the MCM5V4800A**

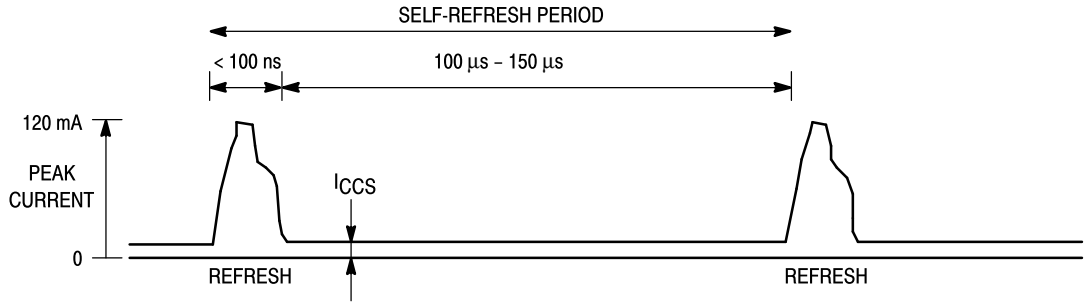


**Figure 6. Power Supply Current of the MCM5V4800A During Self-Refresh**

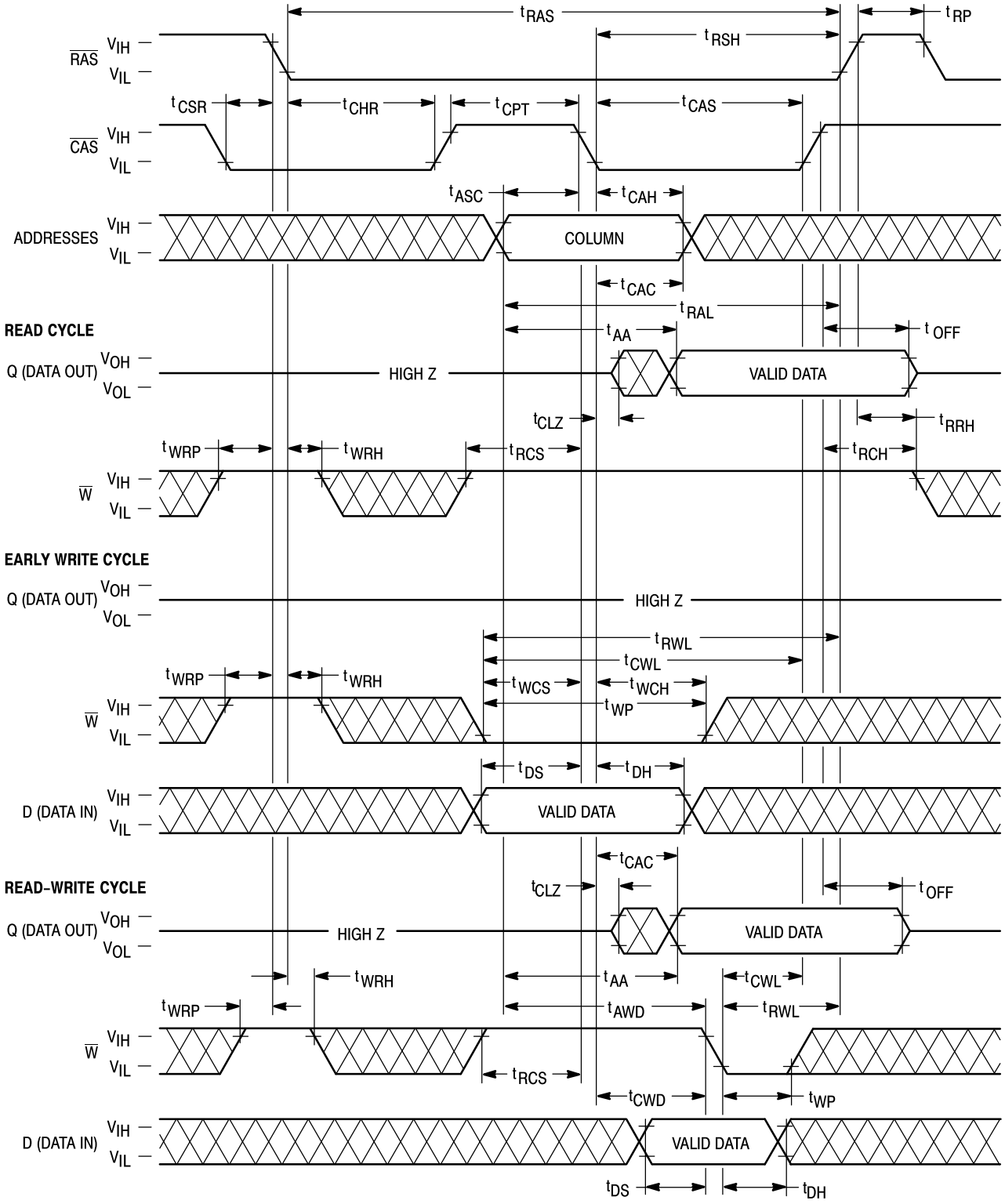


**Figure 7. $\overline{CAS}$ BEFORE $\overline{RAS}$ REFRESH COUNTER TEST CYCLE**

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