APPLICATION NOTE

UMA1022M
Low Voltage, Low Noise Dual Frequency Synthesiser

AN98102

Philips Semiconductors

PHILIPS

Abstract

The UMA1022M is a low voltage, low noise dual synthesiser. It is intended for radiocommunication systems like GSM, DCS1800, PCS1900, DECT, DAMPS, WLL, WLAN, ... where good noise performance and fast switching time are required.
A close in noise value of -86.5 dBc/Hz has been measured in the loop bandwidth of a typical GSM application.

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1 Introduction to the UMA1022M dual synthesiser

The UMA1022M is a low voltage, low noise single chip solution to a dual frequency synthesiser used in radiocommunications. Designed in a BICMOS process, it operates from 2.7 (3 NiCd cells) to 5.5V. The UMA1022M contains all necessary elements with the exception of the quartz, VCO and loop filter components to build two PLL frequency synthesisers.
It is intended that the RF synthesiser operates in the 300 to 2100 MHz range, and the IF synthesiser works between 50 to 550 MHz, up to 4V (50 to 400 MHz, up to 5.5V). The reference divider uses a common part and a separate subdivider section. For each synthesiser, fully programmable main and reference dividers are integrated on chip. Fast programming is possible via a three wire serial bus with clock speeds up to 10 MHz.
The common reference divider can be driven by a VTCXO or a simple quartz since a internal oscillator/buffer is designed in the UMA1022M.
Separate power and ground pins are provided to the analog (charge pump, bipolar part) and digital (CMOS) circuits. An independent supply for the crystal oscillator section allows maximum frequency stability.
The charge pump currents are fixed by internal resistances and controlled by the serial interface. Only a passive loop filter is necessary, the charge pumps function within a wide voltage compliance range to improve the overall system performance.

2 Programming

A simple three wire unidirectional serial bus is used to program the synthesiser. The three lines are DATA, CLK (Clock) and Enot (Enable). The data sent to the device is loaded in bursts framed by Enot. Programming clock edges are ignored until Enot goes active low. The programmed information is loaded into the addressed latch when Enot returns inactive high. Only the last 19 bits serially clocked into the device are retained within the programming register. Additional leading bits are ignored, and no check is made on the number of clock pulses. The NMOS-rich design uses virtually no current when the bus is inactive; power-up is initiated when Enable is taken LOW and power-down occurs a short time after Enable returns HIGH. It can always capture new programming data even during power-down. After software power down is terminated, it is not necessary to reprogram the device. Previous programming data is preserved during power-down as long as the supply voltage is present.

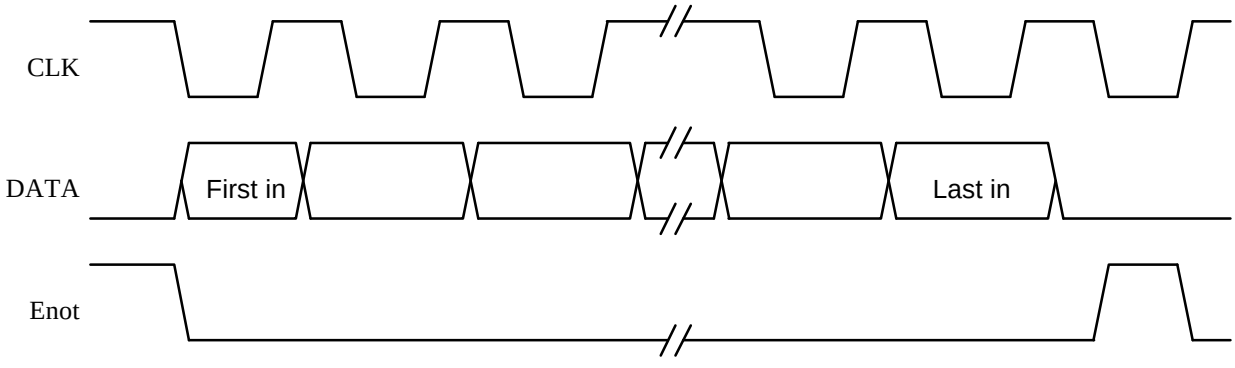


Fig. 1 - Serial Interface Timing Diagram.

The leading bits (dt15 to dt0) make up the data field, while the trailing three bits (ad2 to ad0) are used for the address. For the divider ratios, the first bits entered (P0, R0 and A0) are the Least Significant Bits (LSB). **This is different from previous Philips synthesisers**. The bits are decoded on the rising edge of Enot. A worked example of programming is shown overleaf.

2.1 Power-down mode

When turned on, the dividers and phase detector are synchronised to avoid random phase errors. When turned off, the phase detector is synchronised to avoid interrupting charge-pump pulses. For synchronisation functions to work correctly on power-up or power-down, the presence of TCXO and VCO signals is required to drive the appropriate divider inputs.

2.2 UMA1022M typical programming example

Crystal reference input frequency: 13 MHz
RF input frequency: 902 MHz (main divider ratio = RFM = 4510)
IF input frequency: 178 MHz (main divider ratio = IFM = 178)
RF comparison frequency: 200 kHz ; IF comparison frequency: 1000 kHz
(common reference divider ratio = 13 ; separate reference divider ratio = 5)
(F_{CPIF} > F_{CPRF} so P/A bit set to 1)
Charge pump currents: I_{CPRF} = 2.4 mA/cycle ; I_{CPIF} = 800 µA/cycle (CPI = 1 ; S/D = 1)

first in **Register bit allocation in** **last**	
dt15 Data field dt0	Address
Control reg = 0000 1100 0001 0010b	3 h
RF main divider coefficient = 4510d	0 h
Reference divider coefficient = 13d	1 h
IF main divider coefficient = 178d	2 h

Table 1- UMA1022M Register Data Allocations Expressed in Decimal.

first in (msb) **Data field in** **(lsb) last**																**Address**		
0	0	0	0	1	1	0	0	0	0	0	1	0	0	1	0	0	1	1
0	1	1	1	1	0	0	1	1	0	0	0	1	0	0	0	0	0	0
0	0	0	0	0	0	1	0	1	1	0	0	0	0	0	0	0	0	1
0	0	0	1	0	0	1	1	0	1	0	0	0	0	0	0	0	1	0

Table 2 - UMA1022M Register Data Allocations Expressed in Binary.

2.3 UMA1022M preset values

After the supply voltage is switched on, the different registers are loaded with following preset values. They correspond to a typical DCS application. When using a 13 MHz VTCXO, the RF PLL is directly locked at 2082 MHz (if it is within the VCO range) with a 200 kHz comparison frequency and the IF PLL at 178 MHz with a 1000 kHz comparison frequency.

first in **Register bit allocation in** **last**	
dt15 Data field dt0	Address
Control reg = 0000 1110 0001 0010b	3 h
RF main divider coefficient = 10410d	0 h
Reference divider coefficient = 13d	1 h
IF main divider coefficient = 178d	2 h

Table 3 - UMA1022M Preset Values Expressed in Decimal.

first in (msb)								Data field in							(lsb) last	Address		
0	0	0	0	1	1	1	0	0	0	0	1	0	0	1	0	0	1	1
0	1	0	1	0	1	0	1	0	0	0	1	0	1	0	0	0	0	0
0	0	0	0	0	0	1	0	1	1	0	0	0	0	0	0	0	0	1
0	0	0	1	0	0	1	1	0	1	0	0	0	0	0	0	0	1	0

Table 4 - UMA1022M Preset Values Expressed in Binary.

Since the preset state is not tested, Philips Semiconductors does not guarantee these values. Programming of all registers is recommended after switching ON the synthesiser supply voltage.

3 Loop Filter Design

3.1 Basic Loop Filter Design Procedure

This section gives the procedure to ensure a quick and simple loop filter design. The method is based on first order approximations, and provides a working solution without the need for computer simulation. Reading appendixes 6.1 and 6.2 can be useful to clarify some PLL terms and equations in this section.
The purpose of a Phase Locked Loop (PLL) frequency synthesiser as shown in Fig. 2 is to transfer the spectral purity and stability of a fixed reference frequency oscillator (TCXO or VTCXO) to that of the Voltage Controlled Oscillator (VCO) for a number of output frequencies.

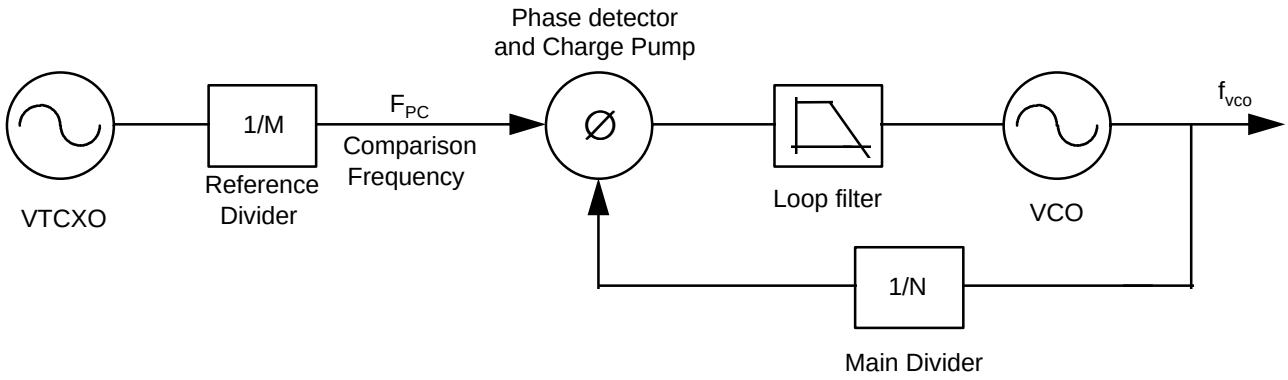
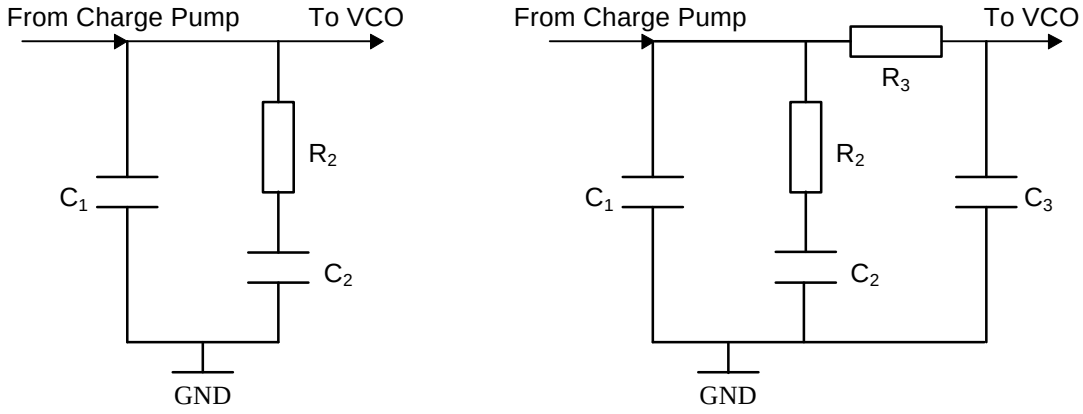


Fig. 2 - Basic Phase Lock Loop Block Diagram.

The correct design of the loop filter is of considerable importance to have the optimum performance from the synthesiser. The filter should be designed so as to achieve the required compromise between noise performance, switching time, comparison frequency spur rejection and modulation requirements.
Loop filters are usually passive when used with current charge pumps, but can be active if desired. Passive loops have the advantage of reduced noise, fewer parts count and low cost. With UMA1022M synthesiser, only passive loop filters are necessary. Two common configurations are shown overleaf. The filters in Fig. 3 are classified in terms of the order of the control loop formed. With UMA1022M, the use of the loop filter (a) is often sufficient. For applications requiring further comparison frequency breakthrough rejection, a low pass filter stage ($R_{3,}$, C_3) can be added. This reduces comparison frequency breakthrough spurs without affecting too much the transient response of the loop, with appropriate design.



(a) Third Order PLL (b) Fourth Order PLL

Fig. 3 - Different Types of Passive Loop Filter.

Loop parameters are first chosen:

- f_{VCO}: VCO frequency (in Hz)
- f_{PC}: Phase comparator frequency (in Hz)
- t_s: Switching time (in seconds)
- K_{vco}: VCO gain (in Hz/V)
- I_{CP}: Phase comparator gain (in Amps/cycle)

As a starting point, the equations below are used.

- $$w_n = 2 \times \Pi \times f_n = \sqrt{\frac{K_{VCO} \times I_{CP}}{C_2 \times N}} \quad (1)$$
- $$R_2 = 2 \times \rho \times \sqrt{\frac{N}{K_{VCO} \times I_{CP} \times C_2}} \quad (2)$$

Where f_n is the natural frequency (in Hz) and ρ is the damping coefficient.

☞ Use rule of thumb to determine the natural frequency f_n based on desired switching time t_s.

$$f_n = \frac{2.5}{t_s} \quad (3)$$

It has been found by experience that a good PLL loop filter design takes a switching time (t_s) of less than $2.5/f_n$ to settle to a new frequency. This rule of thumb allows a good compromise between switching time, stability and noise performance when using the UMA1022M synthesiser. Of course the switching time will also depend on the size of the frequency jump and the definition of when the PLL is settled (i.e. acceptable frequency or phase error with respect to target).

☞ Determine main divider ratio from:

$$N = \frac{f_{VCO}}{f_{PC}} \quad (4)$$

☞ Determine angular velocity w_n (in rad/seconds) from:

$$w_n = 2 \times \Pi \times f_n \quad (5)$$

☞ Determine C_2 from (1)

$$C_2 = \frac{K_{VCO} \times I_{CP}}{w_n^2 \times N} \quad (6)$$

☞ Select damping ratio of approximately 0.9 for a good compromise between switching time and stability.

☞ Determine R_2 from (2)

- $R_2 = 2 \times \rho \sqrt{\frac{N}{K_{VCO} \times I_{CP} \times C_2}}$
- Choose C_1 between 1/10 and 1/15 the value of C_2
- Determine R_3 from:

  $R_3 \geq 2 \times R_2$ (8)
- Determine C_3 from:

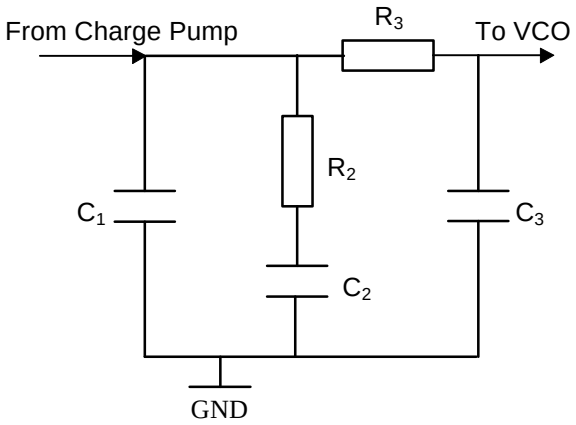
  $C_3 \leq \frac{R_2 \times C_2}{20 \times R_3}$ (9)

A program using this cook book method has been written for use on IBM PC (and compatibles). It is included with the three wire serial bus control software diskette. Values given by the program are approximate and the final values should be optimised. For further optimisation both computer simulation programs as well as practical experiments are required.

Capacitors with high leakage currents and other undesirable effects such as capacitance value dependant on voltage across dielectric are not preferred because of higher comparison frequency breakthrough and increased switching times. A polyester film capacitor is recommended for C_2. However in many cases high quality NP0 surface mount capacitors are adequate for values up to 100 nF.

3.2 Analysis and Simulation

For detailed analysis, optimisation and worst case design with more complex filters, use of a PLL simulation program may be needed.
Normally a stable loop with an acceptable phase noise performance and a given switching time is required. Unfortunately, these two requirements are in conflict and a compromise must be found. Generally, the optimum compromise between stability and fastest switching time is reached when the phase margin is at its maximum at the open loop gain crossover frequency.



$T_1 = (R_2 \times C_2 \times C_1) / (C_1 + C_2)$; $T_2 = R_2 \times C_2$; $T_3 = R_3 \times C_3$ if $C_2 >> C_1 >> C_3$

Fig. 4 - Third Order Loop Filter.

The phase margin is easily determined from Bode plot. A Bode plot displays the open loop transfer function magnitude and phase. Fig. 5 shows Bode plot of a fourth order loop with third order filter (see Fig. 4) and a pole in the origin due to the VCO.
The phase margin is defined as the different between 180° and the phase of the open loop transfer function at the frequency where the gain is 1 (Gain cross over). The critical point for stability is a phase margin of 0°. The factor by which the system gain would have to be increased for the phase margin to reach the critical value of 0° is called the gain margin.
The time constants in the loop filter are key to controlling the overall loop performance and phase margin. The effect of different time constants can be evaluated from the Bode diagram. The reciprocal of the time constants of the loop filter in Fig. 4 are the breakpoints in the magnitude plot of Fig. 5.
When increasing the time constant $T_3 = C_3 \times R_3$, the breakpoint $(T_3)^{-1}$ will move left and the magnitude curve will start to roll off at a lower frequency. Therefore, the greater the time constant T_3, the better the comparison frequency breakthrough is suppressed. But increasing T_3 will force the point of inflection of the phase margin curve to move to the left as well, this decreasing the phase margin and eventually reducing system stability.
By iteration and inspection of the Bode plot, adjusting the loop filter values and measuring the performance, a compromise between switching time, stability and noise can be reached. Simulation programs may give reasonable approximations of PLL behaviour, but their accuracy is limited due to the fact that many practical imperfections, non linearities and saturation effects are often not taken into account.
Phase margin between 30° and 70° is required for most applications. The larger the phase margin, the more stable the loop, but slower the transient response and hence the switching time. A loop with a low phase margin may still be stable but could exhibit oscillatory problems, associated with undamped loops which also give longer switching times and increased noise. A phase margin of 45° is a good compromise between desired stability and the other generally undesired effects.

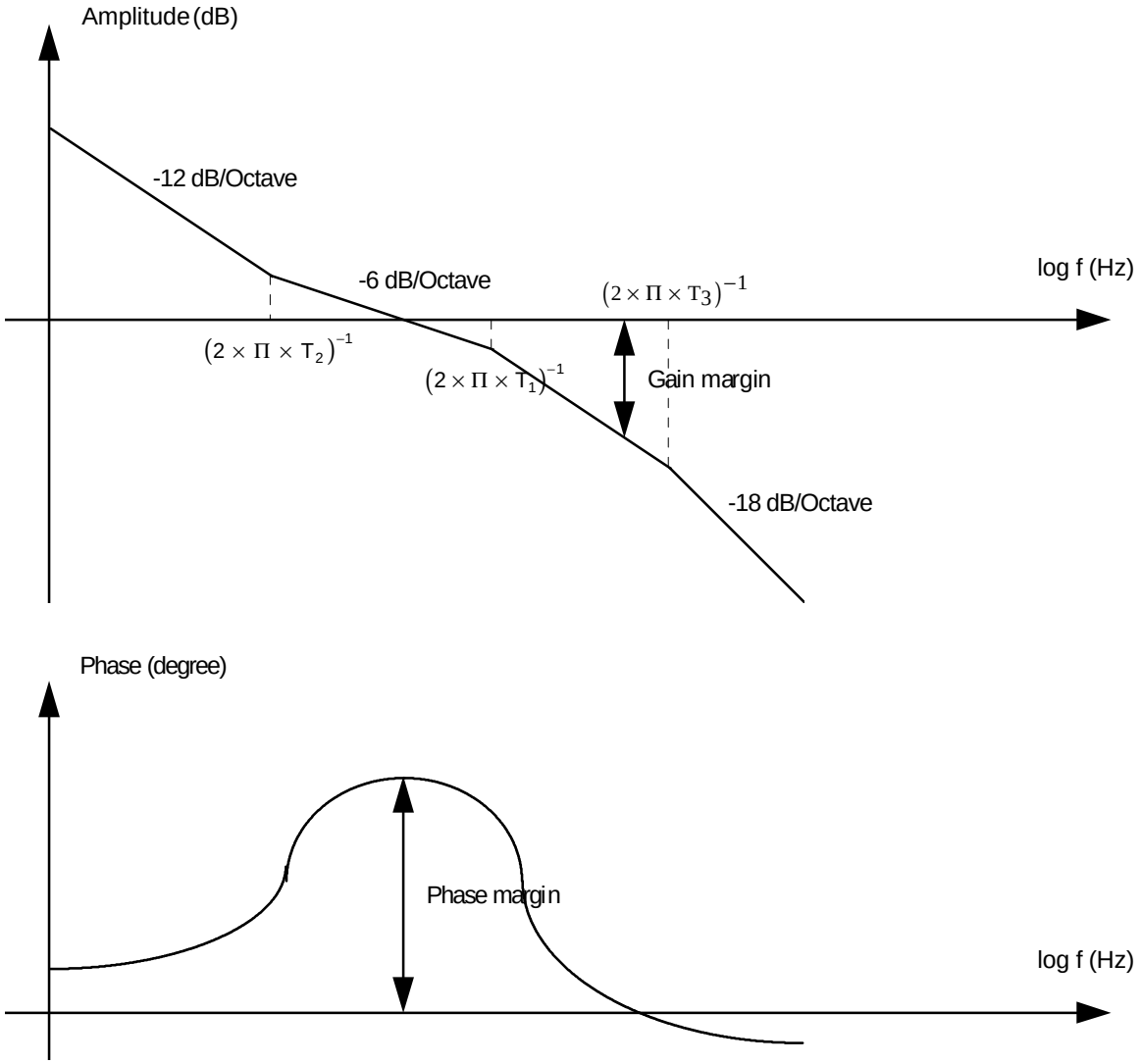


Fig. 5 - Bode Plot 4th Order Open PLL Transfer Function Magnitude and Phase.

3.3 Worked Example

In this section, a design example based on the third order PLL for GSM is shown.

Loop parameters relevant to meet the GSM application:
- VCO frequency f_{VCO} = 902 MHz
- Phase comparator frequency f_{PC} = 200 kHz
- Switching time t_s = 600 µs
- VCO gain K_{VCO} = 26 MHz/V
- Phase comparator gain I_{CP} = 2.4 mA/cycle (CPI = 1 ; S/D = 1). As close in noise is improved by increasing the charge pump gain, a highest gain is used.

Following the basic design procedure from paragraph 3.1 yields:
Natural frequency $f_n = 2.5 / t_s = 2.5 / 600\ \mu S = 4170$ Hz
Main divider ratio N: $f_{VCO} / f_{PC} = 902\ MHz / 200\ kHz = 4510$

The main components in the loop filter are:

☞ Main capacitor $C_2 = \frac{K_{VCO} \times I_{CP}}{w_n^2 \times N} = \frac{26e6 \times 2.4e-3}{(2 \times \Pi \times 4170)^2 \times 4510}$

C_2 = 22 nF

☞ Damping resistor $R_2 = 2 \times \rho \times \sqrt{\frac{N}{K_{VCO} \times I_{CP} \times C_2}} = 2 \times 0.9 \times \sqrt{\frac{4510}{26e6 \times 2.4e-3 \times 22e-9}}$

R_2 = 3.3 kΩ

☞ Filter capacitor $\frac{C_2}{15} \le C_1 \le \frac{C_2}{10}$

C_1 = 1.5 nF

An extra order (R_3 and C_3) is not needed as UMA1022M charge pump leakage current and comparison frequency breakthrough are very low.

4 Measurements and typical results

This section gives the performance of UMA1022M in different applications.

The relevant performance criteria for a synthesiser are usually:

- Close in phase noise / Integrated phase jitter
- Comparison frequency breakthrough
- Switching time

Close in noise was measured using a direct reading from the spectrum analyser and referred to 1 Hz bandwidth. This was done at a specified offset from the carrier whilst still inside the loop bandwidth. It is expressed in dBc/Hz.
Integrated phase jitter was measured on a Rohde and Schwarz Modulation Analyser in a 10 Hz to 200 kHz audio bandwidth.
Switching time was measured using a HP 53310A Modulation Domain Analyser (MDA) with option 031. Under the TRIGGER Menu of the MDA, “Triggered”, “Ext Edge” and “Arm Only” were selected. The instrument was setup to accept an external trigger, which was the Enot (Enable) signal used for programming the synthesiser. This signal was connected to the Ext Arm input while the RF signal was fed into the Channel C. The MDA would display the frequency versus time variation of the VCO signal upon the arrival of the Enot rising edge signal.

Table 5 to Table 7 summarise the measurement results. Fig. 6 to Fig. 12 show some of the actual measurements.

Parameters			
Conditions: V_{CC} = 5 volts ; V_{DD} = 3V ; Temperature = 25°C			
Loop components (Refer to Fig. 4)		C_1 = 1.5 nF C_2 = 22 nF C_3 = NNP*	 R_2 = 3.3 kΩ R_3 = NNP*
VCO EX814A ALPS (5V)	VCO gain K_{VCORF} VCO frequency f_{VCORF} Frequency range	26 MHz/V 902 MHz 864 - 915 MHz	
Comparison frequency f_{PC}		200 kHz	
Charge pump	Current gain I_{CPRF}	2.4 mA/cycle	
	Bits CPI, S/D	CPI = 1 ; S/D = 1	
Reference frequency: VTCXO TOYOCOM TCO982 (3V)		13 MHz	
Results			
Closed loop bandwidth		7.5 kHz	
Close in noise (at 1 kHz distance from carrier) (see Fig. 6)		-86.5 dBc/Hz	
Integrated phase jitter	890 MHz 902 MHz 915 MHz	10.9 mrad rms 11.1 mrad rms 11.3 mrad rms	
Comparison frequency breakthrough at 200 kHz (see Fig. 7)		87 dBc	
Switching time to within 1 kHz	890 to 915 Mhz (see Fig. 8) 915 to 890 Mhz (see Fig. 9)	544 µs 556 µs	

Table 5 - Demoboard Measurement Results on UMA1022M RF Synthesiser. GSM Application.

Parameters			
Conditions: V_{CC} = 5 volts ; V_{DD} = 3 volts ; Temperature = 25°C			
Loop components (Refer to Fig. 4)		C_1 = 1 nF C_2 = 15 nF C_3 = NNP*	 R_2 = 3.9 kΩ R_3 = NNP*
VCO MQE721-178 MURATA (4.2V)	VCO gain K_{VCOIF} VCO frequency f_{VCOIF} Frequency range	2.5 MHz/V 178 MHz 174.5 - 181.5 MHz	
Comparison frequency f_{PCIF}		1000 kHz	
Charge pump	Current gain I_{CPIF}	0.8 mA/cycle	
	Bits CPI, S/D	CPI = 1 ; S/D = 1	
Reference frequency: VTCXO TOYOCOM TCO982 (5V)		13 MHz	
Results			
Closed loop bandwidth		12 kHz	
Close in noise (at 1 kHz distance from carrier) (see Fig. 10)		-104 dBc/Hz	
Integrated phase jitter	175 MHz 178 MHz 181 MHz	1.8 mrad rms 1.7 mrad rms 1.6 mrad rms	
Comparison frequency breakthrough at 1000 kHz		better than 90 dBc	

Table 6 - Demoboard Measurement Results on UMA1022M IF Synthesiser. GSM Application.

(*) NNP Normally Not Populated

Parameters			
Conditions: V_{CC} = 5 volts ; V_{DD} = 3V ; Temperature = 25°C			
Loop components (Refer to Fig. 4)		C_1 = 1 nF C_2 = 15 nF C_3 = NNP*	 R_2 = 4.7 kΩ R_3 = NNP*
VCO URAE8X812A ALPS (5V)	VCO gain K_{VCORF} VCO frequency f_{VCORF} Frequency range	41 MHz/V 2082 MHz 2070 - 2095 MHz	
Comparison frequency f_{PC}		200 kHz	
Charge pump	Current gain I_{CPRF}	2.4 mA/cycle	
	Bits CPI, S/D	CPI = 1 ; S/D = 1	
Reference frequency: VTCXO TOYOCOM TCO982 (3V)		13 MHz	
Results			
Closed loop bandwidth		7.5 kHz	
Close in noise (at 1 kHz distance from carrier) (see Fig. 11)		-78.8 dBc/Hz	
Integrated phase jitter	2070 MHz 2082 MHz 2095 MHz	15.8 mrad rms 16 mrad rms 15.9 mrad rms	
Comparison frequency breakthrough at 200 kHz (see Fig. 12)		82 dBc	
Switching time to within 1 kHz	2070 to 2095 MHz 2095 to 2070 MHz	550 µs 550 µs	

Table 7 - Demoboard Measurement Results on UMA1022M RF Synthesiser. DCS Application.

(*) NNP Normally Not Populated

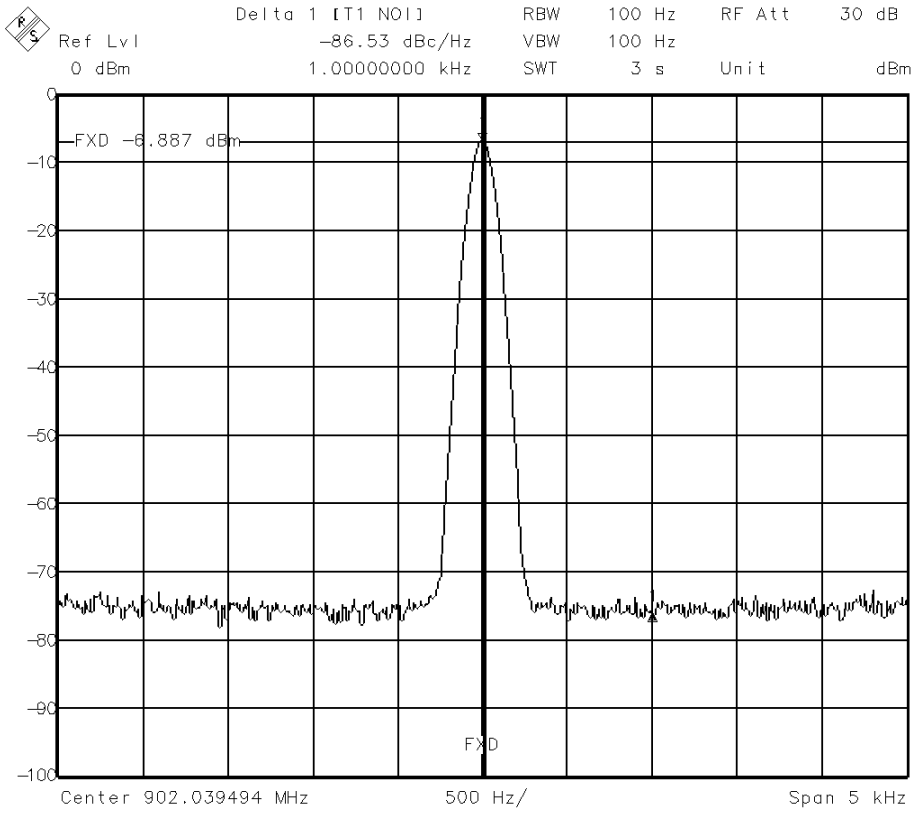


Fig. 6 - UMA1022M RF Synthesiser Output Spectrum - Close in Noise at 902 MHz.

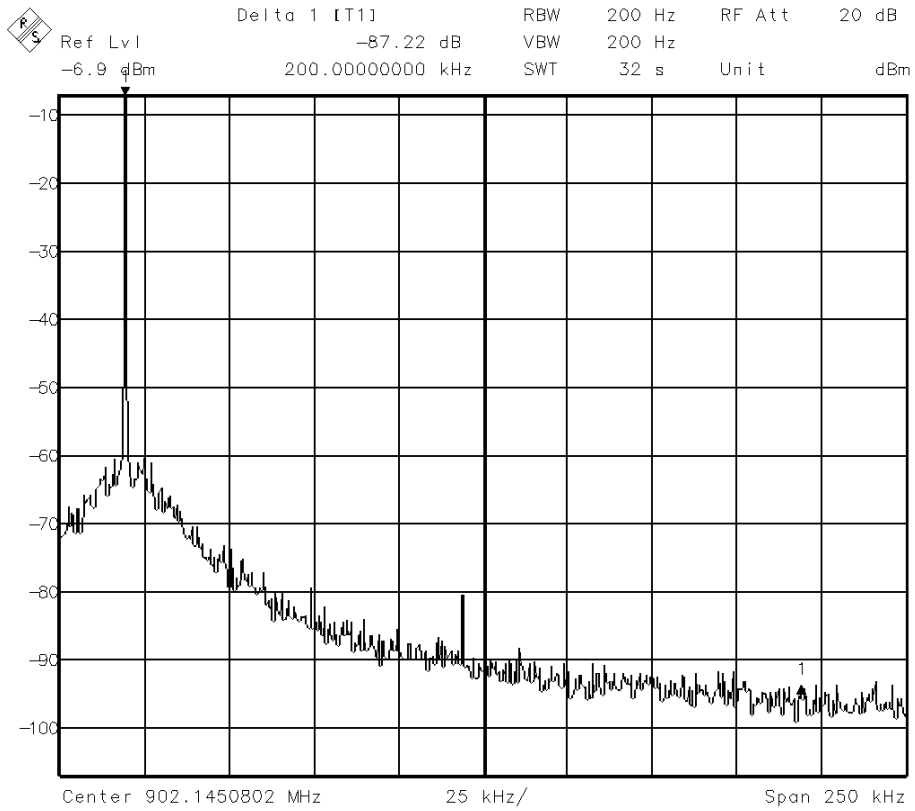
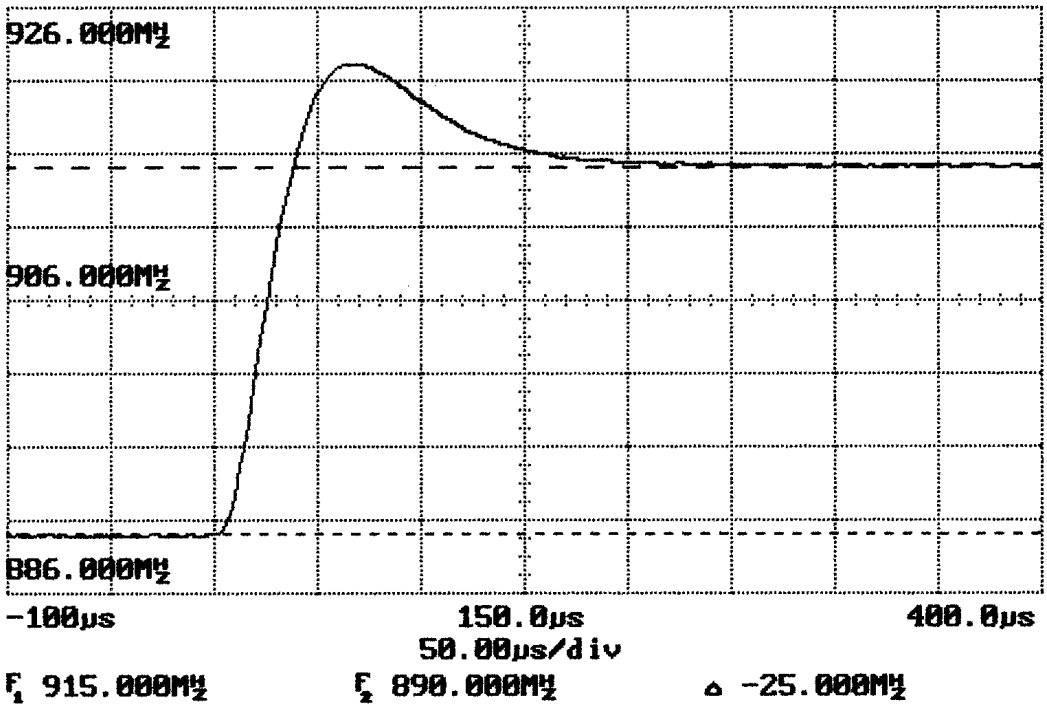


Fig. 7 - UMA1022M RF Synthesiser - Comparison Frequency Breakthrough.



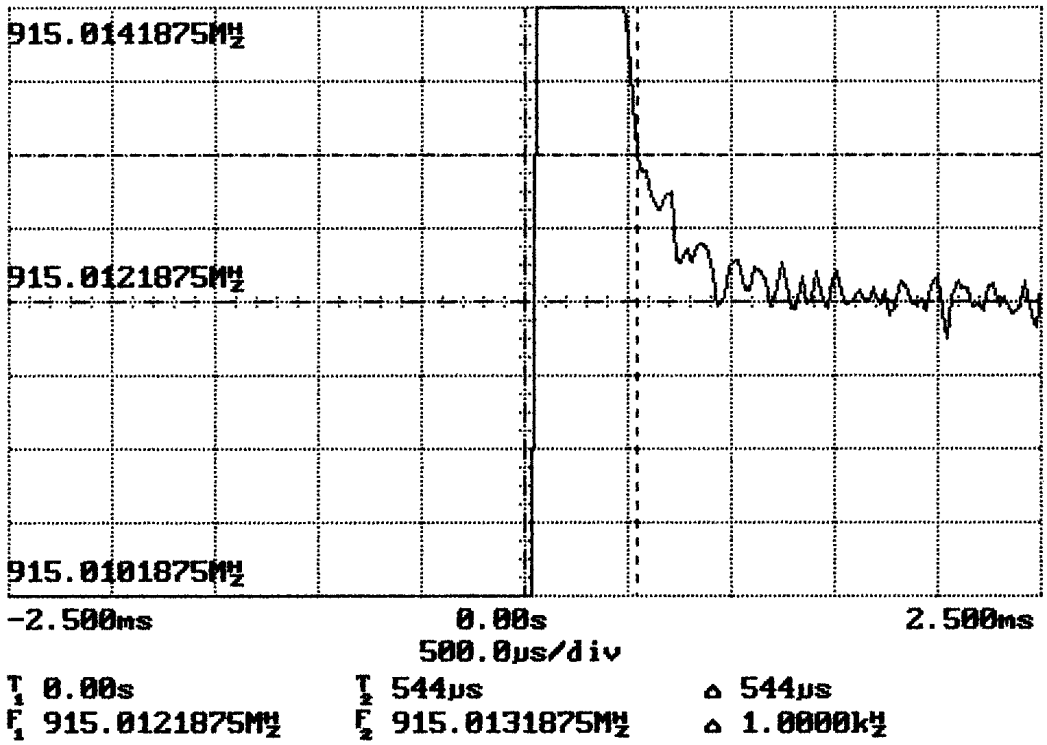


Fig. 8 - UMA1022M RF Synthesiser - Settling Time (890 to 915 MHz Step to Within 1kHz).

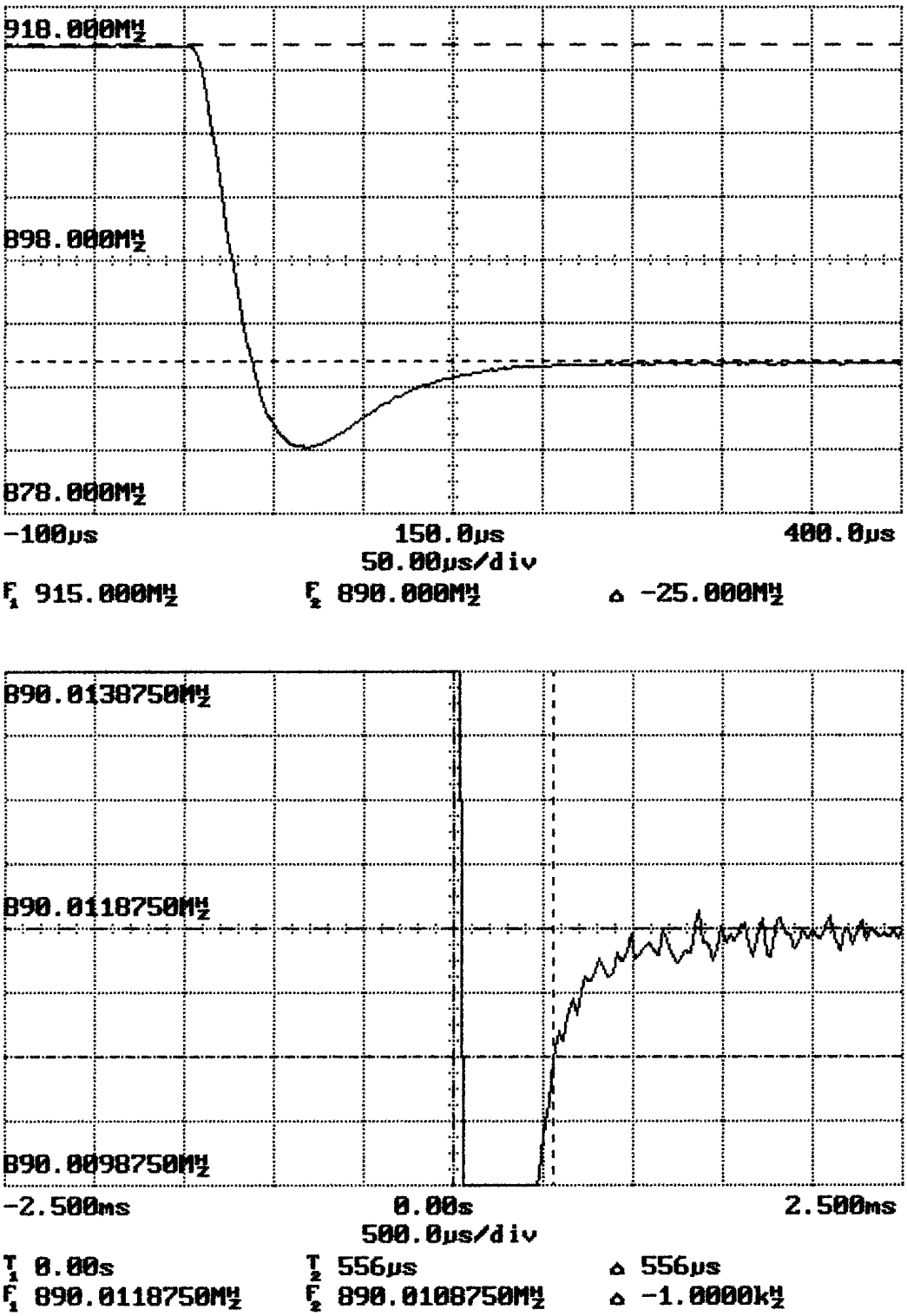


Fig. 9 - UMA1022M RF Synthesiser - Settling Time (915 to 890 MHz Step to Within 1 kHz).

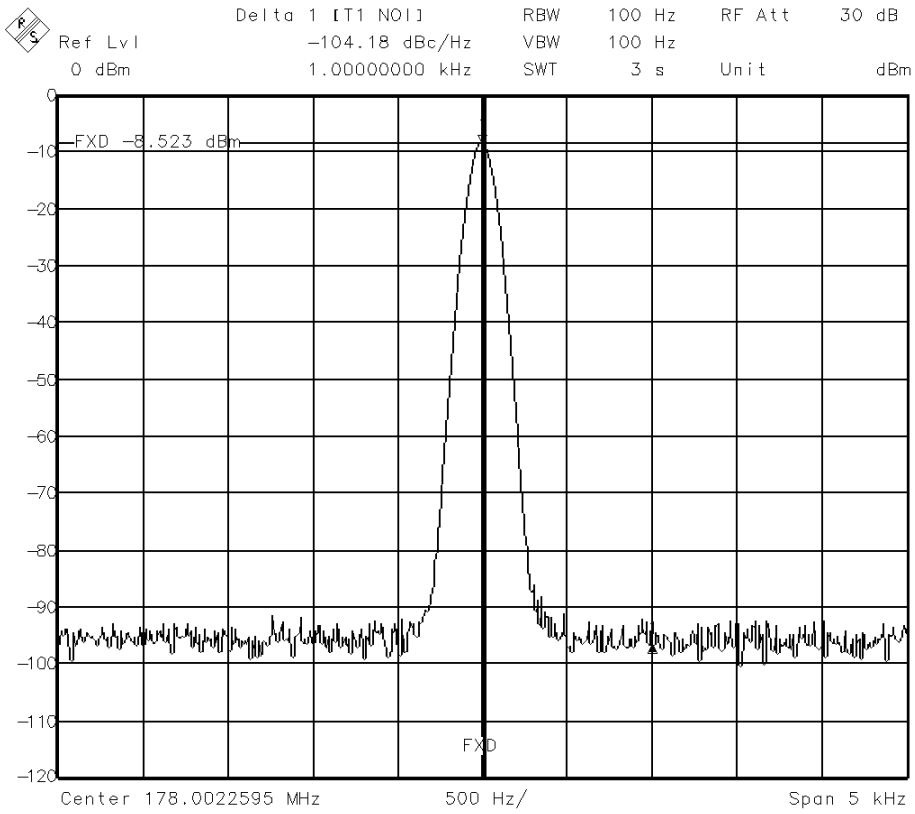


Fig. 10 - UMA1022M IF Synthesiser Output Spectrum - Close in Noise at 178 MHz.

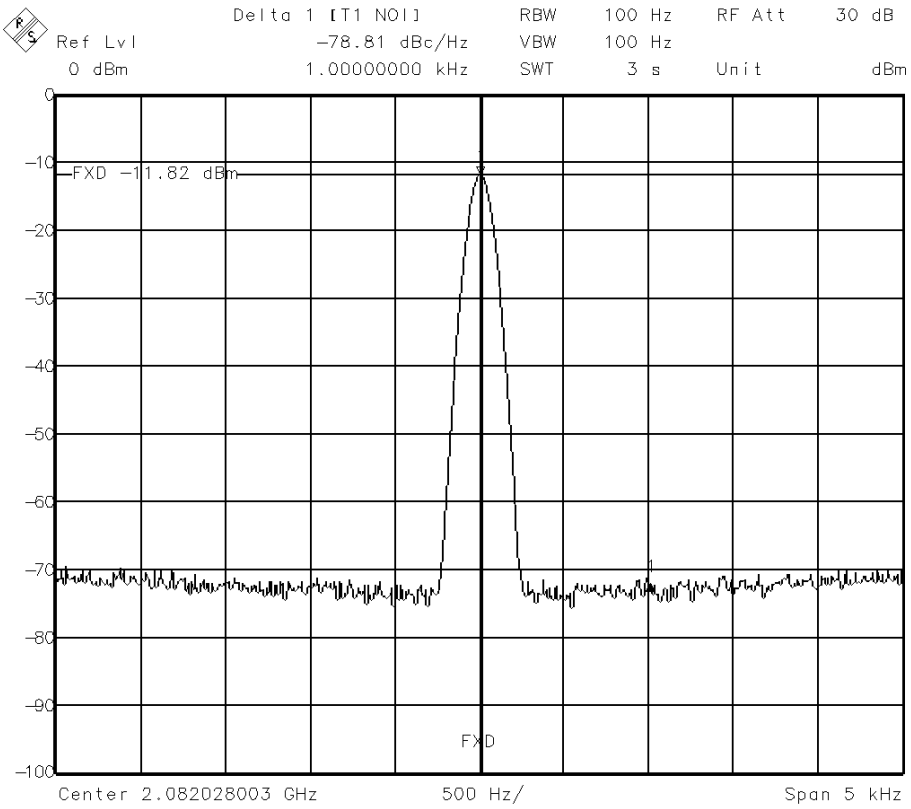


Fig. 11 - UMA1022M RF Synthesiser Output Spectrum - Close in Noise at 2082 MHz.

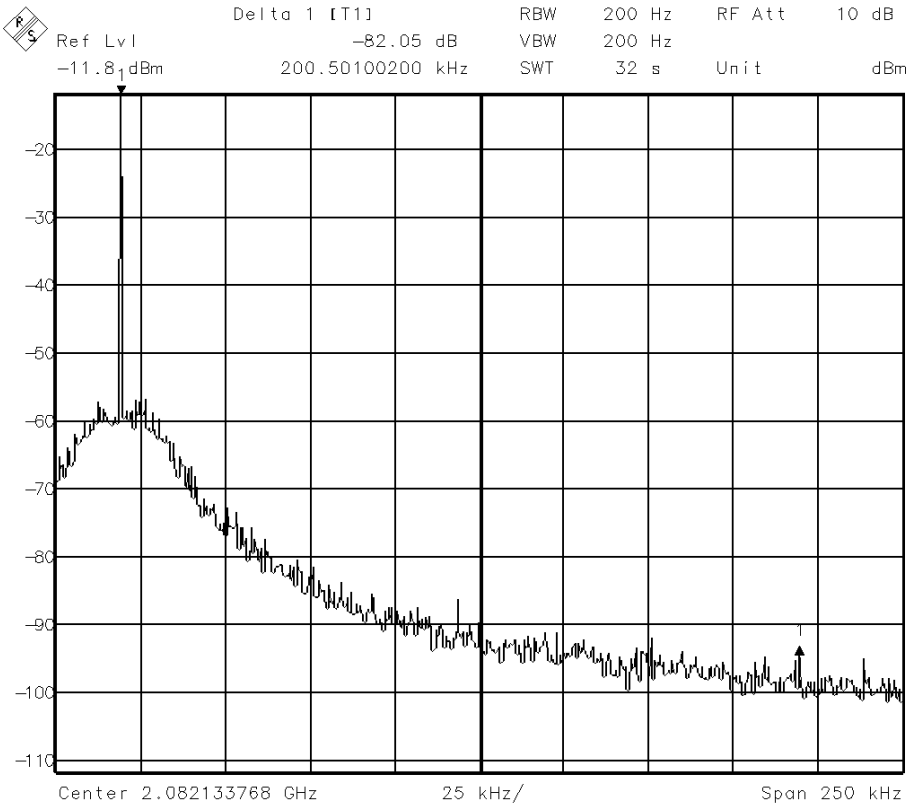


Fig. 12 - UMA1022M RF Synthesiser - Comparison Frequency Breakthrough.

5 Frequently Asked Questions

Question 1: How can the synthesiser noise be improved?
Answer: Five things can be done to improve the synthesiser noise.
1/ Use a higher crystal frequency. Doubling the reference frequency can improve the close in noise by 3 dBc/Hz.
2/ With a VTCXO as the reference frequency, use the pin XIN as input and decouple to ground the pin not_XIN (see explanations next question).
3/ Use the biggest charge pump current.
4/ Use a narrower loop filter. But this increases the switching time.
5/ Ensure that the supply is well decoupled.
Number 4 does not improve the close in noise, just the total phase noise. Other points can improve the close in noise and also the total phase noise of the PLL.

Question 2: Do you recommend the use of a particular reference input (XIN or not_XIN)?
Answer: The pin XIN (and so the reference divider) is driven by the falling edge of the reference signal, whilst the pin not_XIN is driven by the rising edge.
Since this signal is the reference in term of frequency but also purity, the reference input must be chosen according to the phase jitter of the edge. The better the phase jitter of the reference edge, the better will be the total close in noise (in the loop bandwidth).
Normally with a VTCXO the falling edge has a better jitter than the rising edge. So we recommend to use the pin XIN with such a VTCXO. The pin not_XIN needs to be decoupled to the ground.

Question 3: What is the phase detector gain? Is it charge pump output current divided by 2π or just the charge pump output current, itself?
Answer: The phase detector gain is equal to the charge pump output current I_{CP} divided by 2π since the phase detector covers 2π range. However, when using the design formulas, the phase detector gain be replaced directly by I_{CP} (or $I_{CP} + I_{CPF}$ if both charge pumps are enabled) because the 2π factor will be cancelled out by the 2π also in the VCO gain, when given in Hz/volt.

Question 4: What kind of main capacitor should be used in the loop filter?
Answer: Higher leakage current raises comparison frequency breakthrough and the memory effect of some dielectric (COG, X7R series) or, worse, electrolytic types can degrade the settling time. A polyester film capacitor is recommended for the main capacitor of the loop filter.

Question 5: Can I anticipate the close in noise with any application?
Answer: Different experiments show that when using the UMA1022M, the main divider follows a 20log(N) (6 dB/octave) slope (i.e. when doubling the RF, you degrade the close in noise by 6 dB), whilst with the reference divider the noise floor is seen to follow a 10log(N) (3 dB/octave) slope.

The expected RF synthesiser close in noise of any application can be extrapolated from the results of the GSM application (RF = 902 MHz, F_{CP} = 200 kHz, close in noise = -86.5 dBc/Hz) with the following rule:

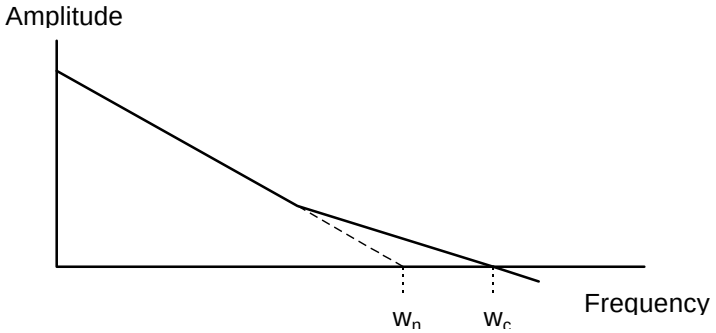
$$\text{Close in Noise (expected)} = -86.5\text{dBc/Hz} + 20\log\left(\frac{RF}{902\text{MHz}}\right) - 10\log\left(\frac{F_{CP}}{200\text{kHz}}\right)$$

6 Appendixes

6.1 PLL terms

The following is a brief glossary of frequently encountered terms in the PLL literature.

- **Natural frequency w_n**: the natural frequency of the loop. This is the frequency at which the loop would theoretically oscillate if the damping factor was zero.
- **Open loop cross-over frequency w_c**: this is the frequency at which the open loop gain is unity. It is useful in determining the phase margin and hence the stability.



- **Damping coefficient**: r can be used as a measure of the stability in second order systems. It is seldom used as a direct measure of stability in higher order designs.
- **Order of the loop**: the order of the loop is the highest power of s (s=jw) in the denominator of the open loop transfer function. The example, below, shows a second order loop.

$$G(s) \times H(s) = (K_{VCO} \times I_{CP}) \times \frac{(s \times \tau_2 + 1)}{(N \times C \times s^2)}$$

- **Type of the loop**: the type of control system formed is defined by the number of perfect integrators in the loop. In the example, above, the loop is a type two system.
- **Phase margin Fm**: the phase margin, in degrees, is expressed as Fm = $F(w_c)$+180 where $F(w_c)$ is the open loop phase shift at the frequency w_c.
- **SSB phase noise or close in noise**: it is the noise level within the loop bandwidth relative to carrier at a given frequency offset. It is referred to a 1 Hz bandwidth. It is expressed in dBc/Hz.
- **Integrated phase jitter or residual FM**: this is another measure of the noise performance of a signal source. This measure of integrated noise is usually specified over a particular audio bandwidth, e.g. 10 Hz to 200 kHz. It is expressed in degrees rms. An ideal synthesiser would have zero integrated phase jitter.
- **Spurious**: this defines the spectral purity of the oscillator. Common sources of spurious are the comparison frequency and harmonics. Comparison frequency breakthrough is generated by leakage in the loop filter components, VCO variable capacitor, printed circuit or the charge pump.
- **Settling time or switching time**: this indicates the time for a given frequency jump to be within a specified distance (frequency or phase) from target value.

6.2 Basic PLL transfer function

Fig. 13 shows the block diagram of a basic control loop.

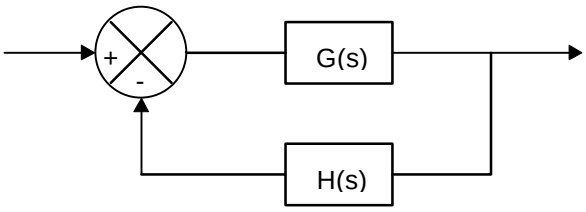


Fig. 13 - Block Diagram of a Loop.

In open loop, the transfer function is $H(s) \times G(s)$ (a)

In closed loop, the transfer function is $\frac{G(s)}{1+(G(s)+H(s))}$ (b)

If we apply these transfer functions to the phase loop in Fig. 14, with equations expressed in Laplace notation.

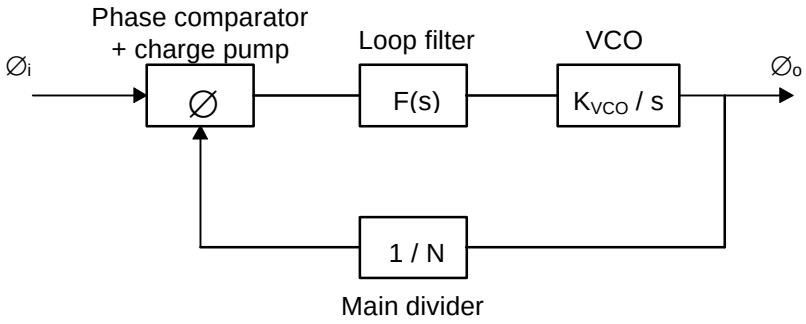


Fig. 14 - Block Diagram of a Phase Locked Loop.

$$G(s) = \frac{I_{CP} \times K_{VCO} \times F(s)}{s} \quad (c)$$

$$H(s) = \frac{1}{N} \quad (d)$$

The PLL open loop transfer function is $\frac{I_{CP} \times K_{VCO} \times F(s)}{s \times N}$ (e)

The PLL closed loop transfer function is

$$\frac{\phi_o(s)}{\phi_i(s)} = \frac{K_{VCO} \times I_{CP} \times F(s)/s}{1+\frac{K_{VCO} \times I_{CP} \times F(s)}{s \times N}} = \frac{N \times K_{VCO} \times I_{CP} \times F(s)}{(s \times N)+(K_{VCO} \times I_{CP} \times F(s))} \quad (f)$$

Basic performance of PLL is determined by R_2 and C_2 (see Fig. 4) in the loop filter.
Note: When introducing more components in the loop filter, the expression for the transfer function becomes a lot more complicated. Anyway, this design can serve as a starting point for even more complicated loop filters.
The transfer function of this simple second order loop filter is

$$F(s) = R_2 + (\frac{1}{s \times C_2}) = \left[\frac{(s \times R_2 \times C_2)+1}{s \times C_2}\right] \quad (g)$$

Then the closed transfer function is

$$\frac{\phi_o(s)}{\phi_i(s)} = \frac{N \times K_{VCO} \times I_{CP} \times F(s)}{(s \times N) + (K_{VCO} \times I_{CP} \times F(s))} = \frac{N \times K_{VCO} \times I_{CP} \times \frac{(s \times R_2 \times C_2) + 1}{s \times C_2}}{(s \times N) + (K_{VCO} \times I_{CP} \times \frac{(s \times R_2 \times C_2) + 1}{s \times C_2})}$$

$$= \frac{N \times ((s \times R_2 \times C_2) + 1))}{\frac{s^2 \times C_2 \times N}{K_{VCO} \times I_{CP}} + (s \times R_2 \times C_2) + 1} \qquad \text{(h)}$$

If we compare the denominator of (h) with $\frac{s^2}{w_n^2} + \frac{2 \times \rho \times s}{w_n} + 1$

We find the equations shown below:

$$w_n = \sqrt{\left(\frac{K_{VCO} \times I_{CP}}{C_2 \times N}\right)} \qquad \text{(i)} \Rightarrow \text{(1)}$$

$$\rho = \frac{w_n \times R_2 \times C_2}{2} \qquad \text{(j)}$$

$$R_2 = 2 \times \rho \times \sqrt{\frac{N}{K_{VCO} \times I_{CP} \times C_2}} \qquad \text{(k)} \Rightarrow \text{(2)}$$

6.3 Guidance to Assembly and Operation

6.3.1 Introduction

The enclosed demonstration board is an universal tool to demonstrate and evaluate the UMA1022M under several conditions.
Together, with the Philips 3-Wire bus and the UMA1022M demonstration software, a quick and easy starting is provided. The enclosed application information is preliminary and corresponds to the GSM standards. However, the demoboard may easily be configured for other digital cellular or cordless systems like DCS1800, PHS, etc...

We hope that you will find no problems in realising this evaluation set-up and will come quickly to an application that fits perfectly to your needs.

6.3.2 Assembly

Assembly is done according to the documentation which comes with the demonstration board. Please note that the board may be assembled with VCO's of different style. The existing version of the board can hold surface mount VCO's (e.g. ALPS URAX8, Murata MQE001 type). Since the VCO and the VTCXO use a common on-board supply rail, it is recommended to select both components with the same supply voltage specification.

The supplied circuit diagram corresponds to a typical GSM system. For the RF PLL, a VCO sensitivity of about 26 MHz/V and a typical comparison frequency of 200 kHz have been assumed. The charge pump current has been selected to 2.4 mA/cycle (CPI bit set to 1, S/D bit set to 1). With the IF PLL, a VCO sensitivity of about 2.5 MHz/V and a comparison frequency of 1000 kHz have been chosen. The charge pump current has been selected to 800 µA/cycle.

6.3.3 Board configuration

Two regulators allow to supply independently the analog supply (V_{CC}) and the digital voltage (V_{DD}). The VCOs and the VTCXO are supplied by the analog voltage.
A VTCXO, a crystal or an external generator can be used as the reference. On the demonstration board, the VTCXO drives the reference divider.

6.3.4 Getting started

1. Connect the Philips 3-wire interface board with the serial printer port (LPT1) of your PC. Copy the two files (BUS3WIRE.WB and BUS3WIRE.EXE) onto your hard disk or run the software from the disk. Type BUS3WIRE to start. Select UMA1022M option in the 'DEVICE TYPE' menu. Verify that the displayed window is well configured as you wish.

2. Connect the interface card with the UMA1022M demonstration board.

3. Connect the board to a 7.5V well regulated and low noise power supply.

4. The UMA1022M demonstration board is operational now and the two PLLs should be locked.

5. Start your synthesiser evaluation...

If you need assistance or do have any questions or comments don't hesitate to call your local Philips Semiconductors representative.

Ref	Value/Type	Size	Ref	Value/Type	Size
R1		0603 SMD	C1	1n	0603 SMD
R2		0603 SMD	C2	1n	0603 SMD
R3	3.9k	0603 SMD	C3	15n	0603 SMD
R4	0	0603 SMD	C4	NNP	0603 SMD
R5		0603 SMD	C5		0603 SMD
R6	120	0603 SMD	C6	100n	0603 SMD
R7	18	0603 SMD	C7	4.7µ/10V	Tant. chip cap.
R8	18	0603 SMD	C8	56p	0603 SMD
R9	18	0603 SMD	C9	56p	0603 SMD
R10	56	0603 SMD	C10	100p	0603 SMD
R11	12	0603 SMD	C11	100n	0603 SMD
R12	100k	0603 SMD	C12	33p	0603 SMD
R13	12	0603 SMD	C13	33p	0603 SMD
R14	12	0603 SMD	C14	33p	0603 SMD
R15	12	0603 SMD	C15	100p	0603 SMD
R16	12	0603 SMD	C16	100n	0603 SMD
R17	100k	0603 SMD	C17	56p	0603 SMD
R18	56	0603 SMD	C18	56p	0603 SMD
R19	18	0603 SMD	C19	100n	0603 SMD
R20	18	0603 SMD	C20	4.7µ/10V	Tant. chip cap.
R21	18	0603 SMD	C21		0603 SMD
R22	12	0603 SMD	C22	330p	0603 SMD
R23		0603 SMD	C23	22n	0603 SMD
R24	8.2k	0603 SMD	C24	1.5n	0603 SMD
R25	3.3k	0603 SMD	C25	100p	0603 SMD
R26	12	0603 SMD	C26	100n	0603 SMD
R27		0603 SMD	C27	NNP	0603 SMD
R28	12	0603 SMD	C28		0603 SMD
R29	10k	0603 SMD	C29	1n	0603 SMD
R30	10k	0603 SMD	C30	100n	0603 SMD
R31	12	0603 SMD	C31	4.7µ/10V	Tant. chip cap.
R32	100k	0603 SMD	C32	22p	0603 SMD
R33	100k	0603 SMD	C33	100p	0603 SMD
IC1	UMA1022M	SSOP20	C34	100n	0603 SMD
IC2	TK11250M (TOKO)	SOT-23L	C35	100n	0603 SMD
IC3	TK11230M (TOKO)	SOT-23L	C36	1µ/6.3V	Tant. chip cap.
VTCXO	13 MHz (TOYOCOM)	TCO-982P	C37	4.7µ/10V	Tant. chip cap.
CRYSTAL	NNP (TOYOCOM)	TSX-1A	C38	100n	0603 SMD
VCO1	EX814A (ALPS)		C39	1µ/6.3V	Tant. chip cap.
VCO2	MQE721-178 (MURATA)		C40	4.7µ/10V	Tant. chip cap.
J1	2 pins		CV1	NNP	
J2	2 pins		T1		SOT23
X1	PN-Minicoax-SMB		X2	1 pin	
X3	PN-Minicoax-SMA		X4	5 pins	
X5	PN-Minicoax-SMA		X6	PN-Minicoax-SMB	
X7	PN-Minicoax-SMB		X8	2 pins	

Table 8 - Part List for UMA1022M Demonstration Board (GSM Application).

(*) NNP: Not Normally Populated.

X1: crystal oscillator buffer output.
X2: IF VCO modulation input.
X3: IF output 50Ω.
X4: 3-WireBus control.
X5: RF output 50Ω.
X6: RF VCO modulation input.
X7: external reference input.
X8: supply.

J1: controls power down for the IF synthesiser.
J2: controls power down for the RF synthesiser.

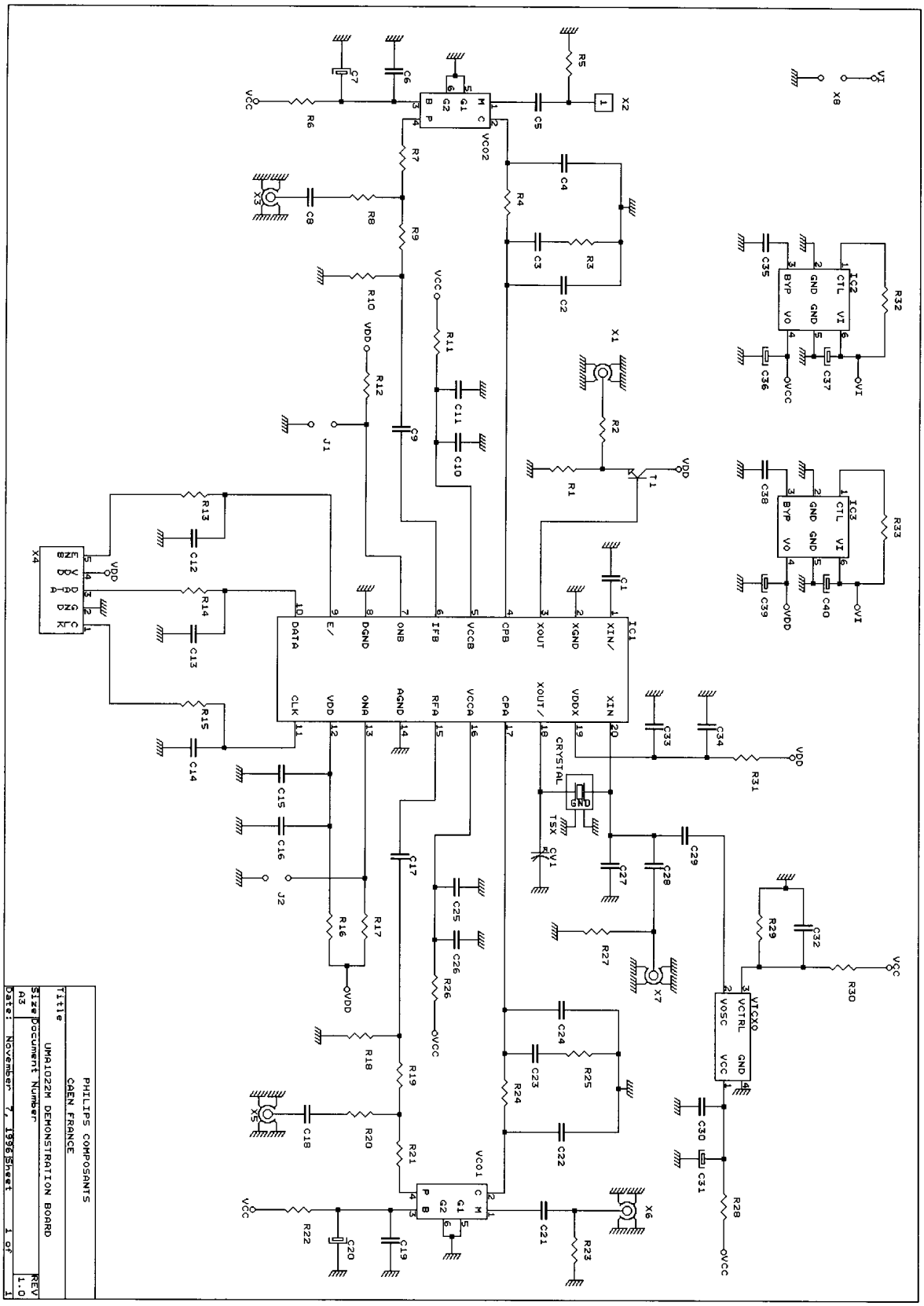


Fig. 15 - UMA1022M Demonstration Board Circuit Diagram.

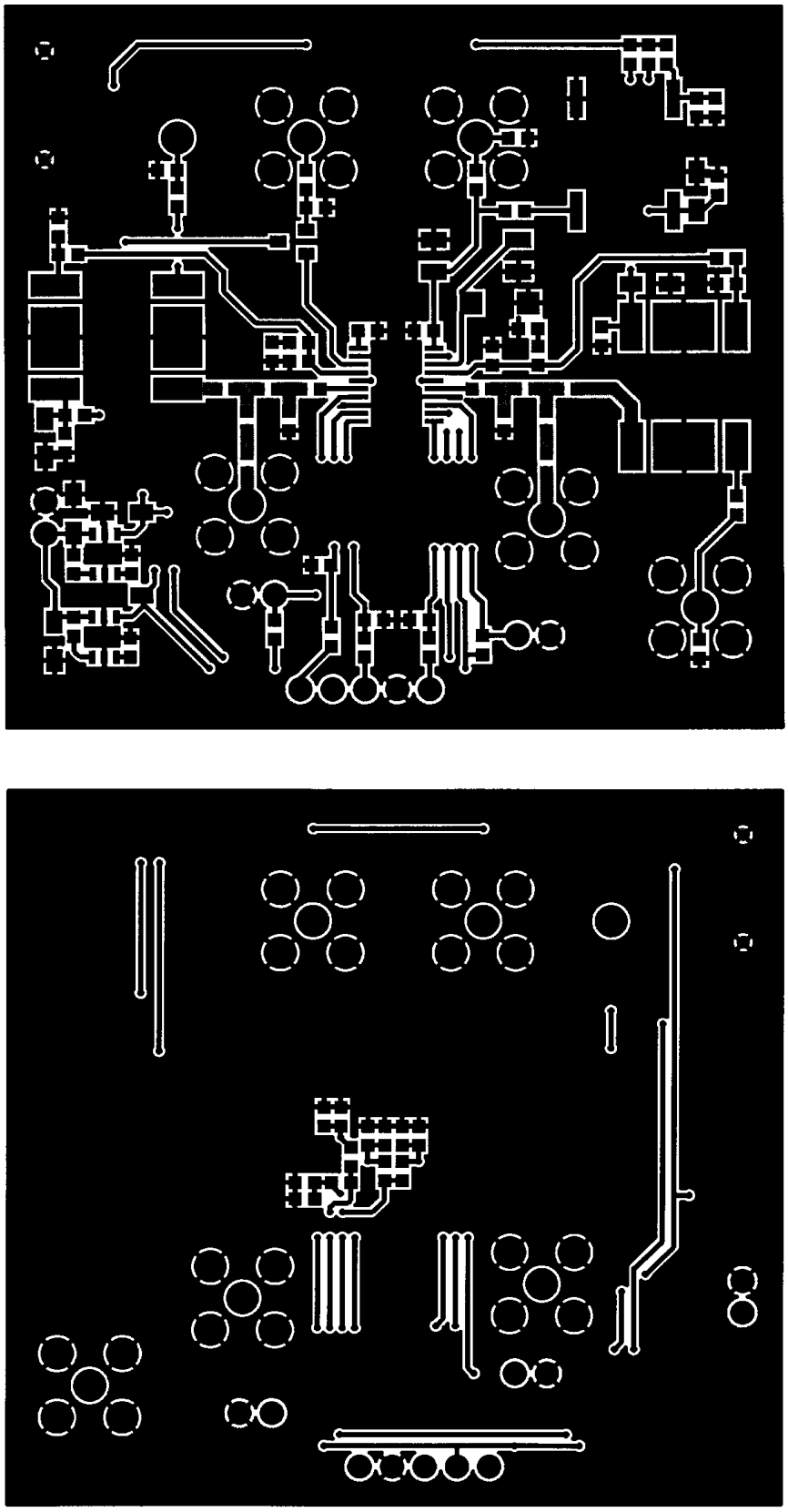


Fig. 16 - UMA1022M Demonstration Board pcb Layout.

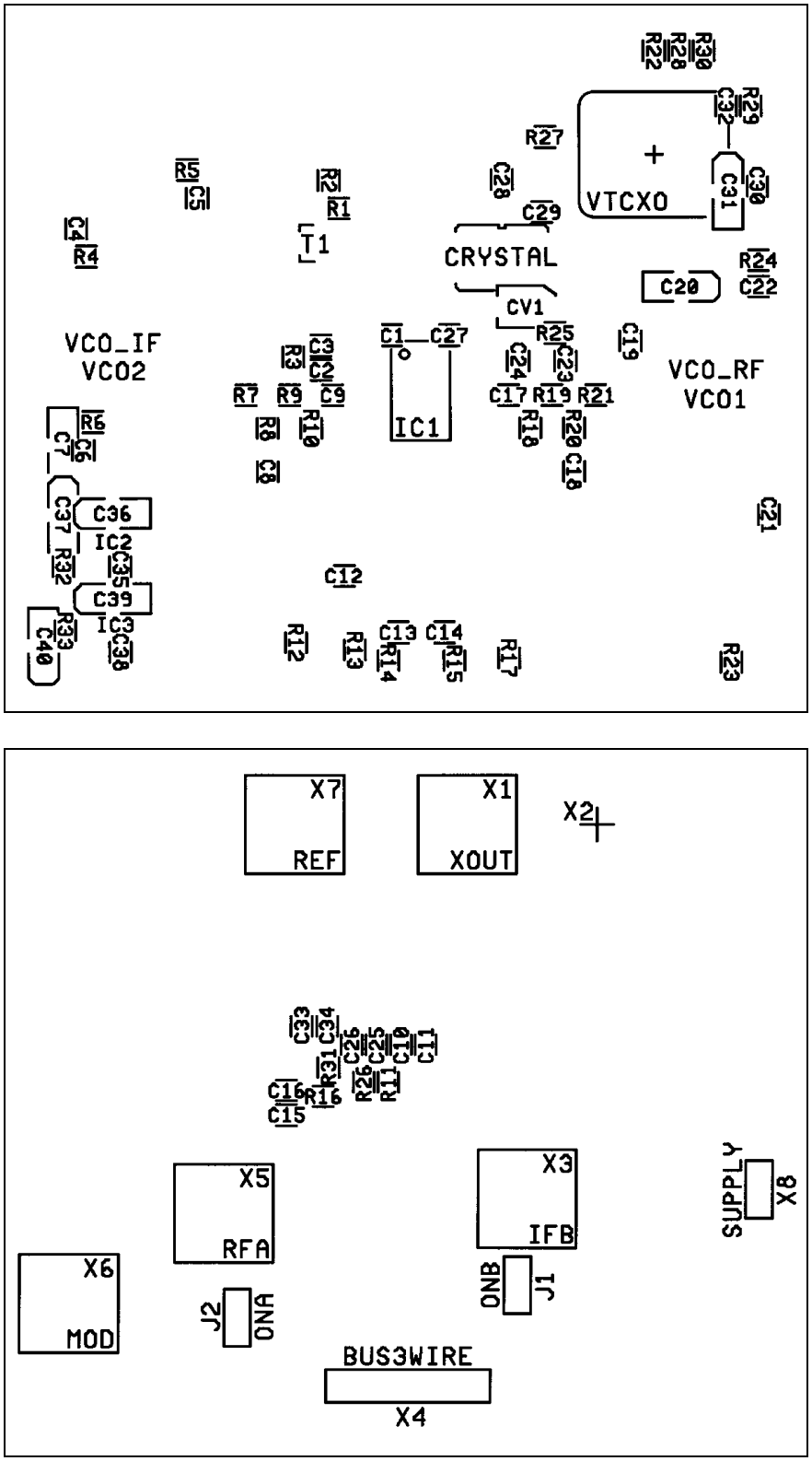


Fig. 17 - UMA1022M Demonstration Board Placement of Components.

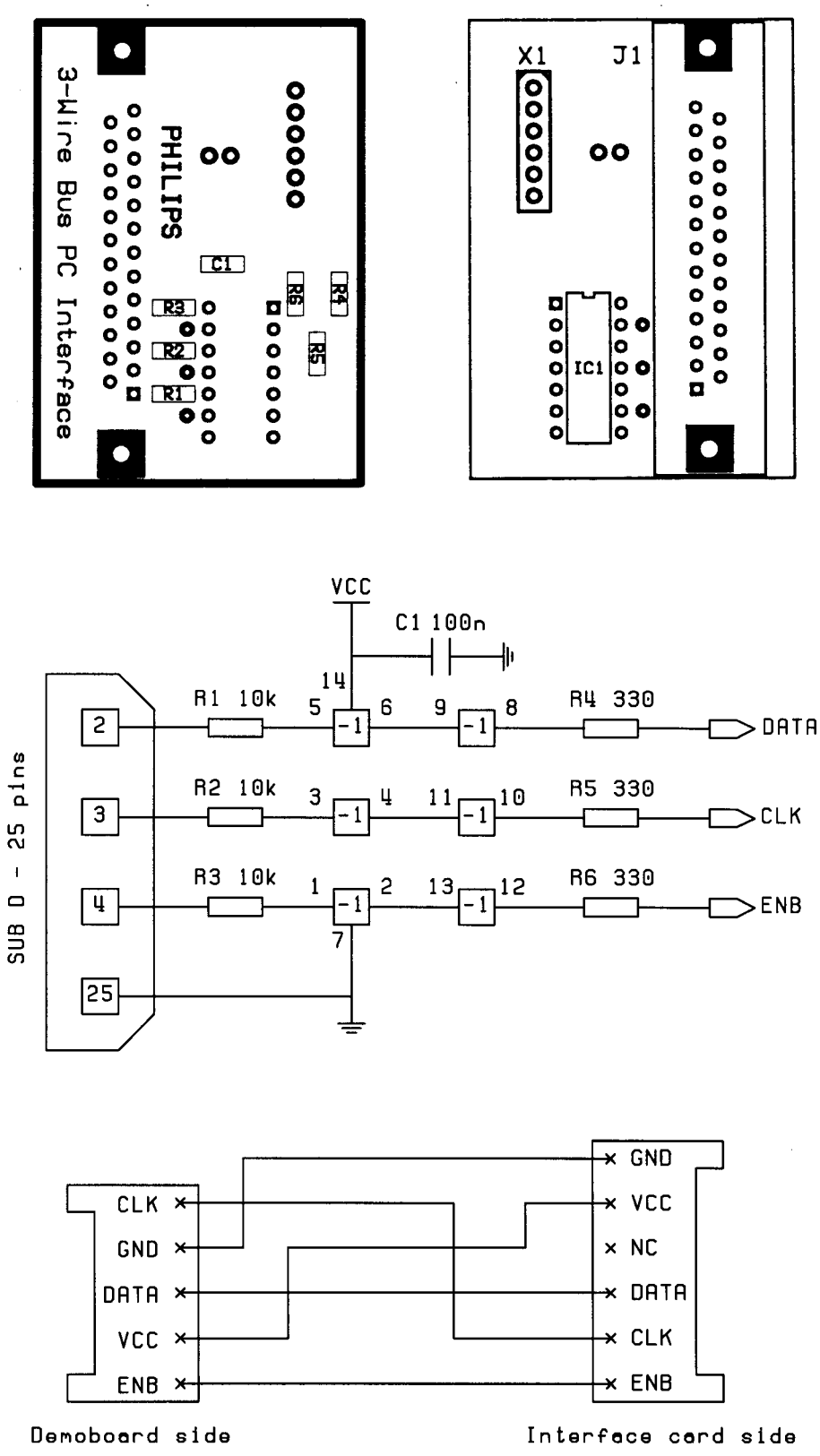


Fig. 18 - Interface Card pcb Layout and Cable Connection.

7 References

[1] UMA1022M Product specification, Philips Semiconductors, 1998 Sept. 29.
[2] UMA1021M Application Note, Philips Semiconductors, AN96083, August 12nd 1996.
[3] Gardner, Floyd M. Phase lock Techniques, 2nd ed, Wiley, New York. 1980.
[4] Rohde, Ulrich, L. Digital PLL Frequency Synthesisers, Theory and Design, Prentice-Hall, Englewood Cliffs, New Jersey 1983.