APPLICATION NOTE

TZA3001A minimized PCB layout

AN98098

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Abstract

A minimized layout for a optical transmitter, consisting out of the TZA3001A laserdriver and a coax laser is presented. The the size of the PCB is 15.7x10.6 mm.

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Keywords

TZA3001A
SDH
SONET
FC
GE

Number of pages: 15

Date: 98-10-19

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Summary

A minimized layout for a optical transmitter, consisting out of the TZA3001A laserdriver and a coax laser is presented. The the size of the PCB is 15.7x10.6 mm^2.

CONTENTS

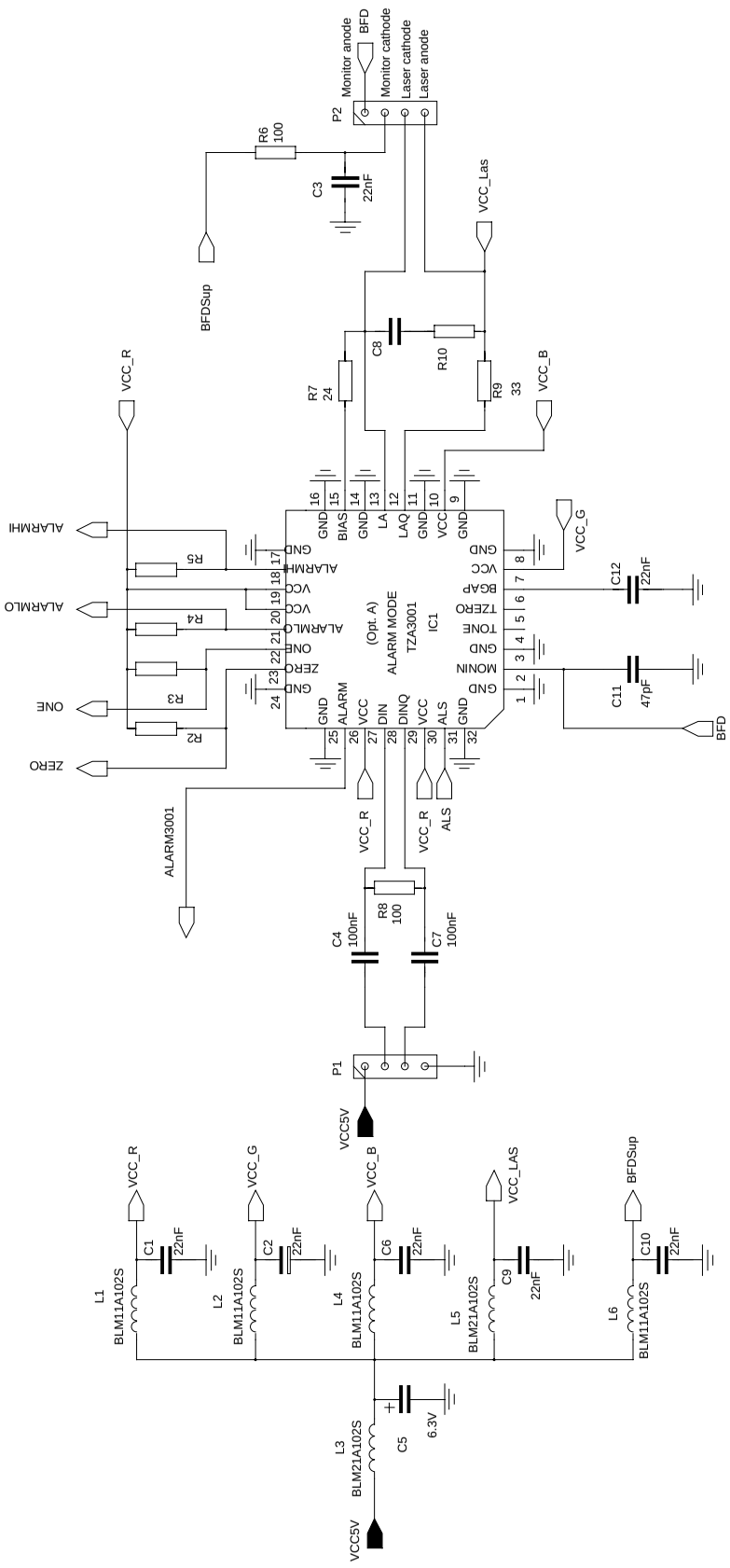
1. INTRODUCTION

For the use of the TZA3001A laserdriver, customers can use the OM5802 demoboard for design suggestions. However, for minimized application, the suggested layout had to be reworked.

In order to give a suggestion in minimized applications, this apnote has been written.

The apnote starts with a schematic, followed by the layout of each layer.

2. SCHEMATIC



Schematics of transmitter. The supply domains are decoupled via a central lowpass filter (L3/C5) and individual filters for each domain (L1/C1, L2/C2, L4/C6, L5/C9, L6/C10). The data is AC coupled via C4 and C7, and terminated by R8. The set resistors for the optical “0” (R2), optical “1” (R3), alarm low level (R4) and alarm high level (R5) are connected to the VCC_R domain. The LA output is connected to the cathode of the laser (P2-2). The LAQ output is terminated with a dummy load (R9) to the supply of the laser (VCC_LAS to P2-3, Laser anode). The bias current flows via a 1206 shape resistor (R6, 1206 shape) for impedance increment of the bias source and removal of unnecessary power dissipation out of the IC. An equalization or pulse shape filter is foreseen as C8/R10. The bandgap voltage is decoupled with C12. The input of the monitor current (MONIN) must ‘see’ 30 to 50 pF. Therefore an additional capacitor is placed at its input. All components are 0603 shape, except R6 (power dissipation) and C5 (value).

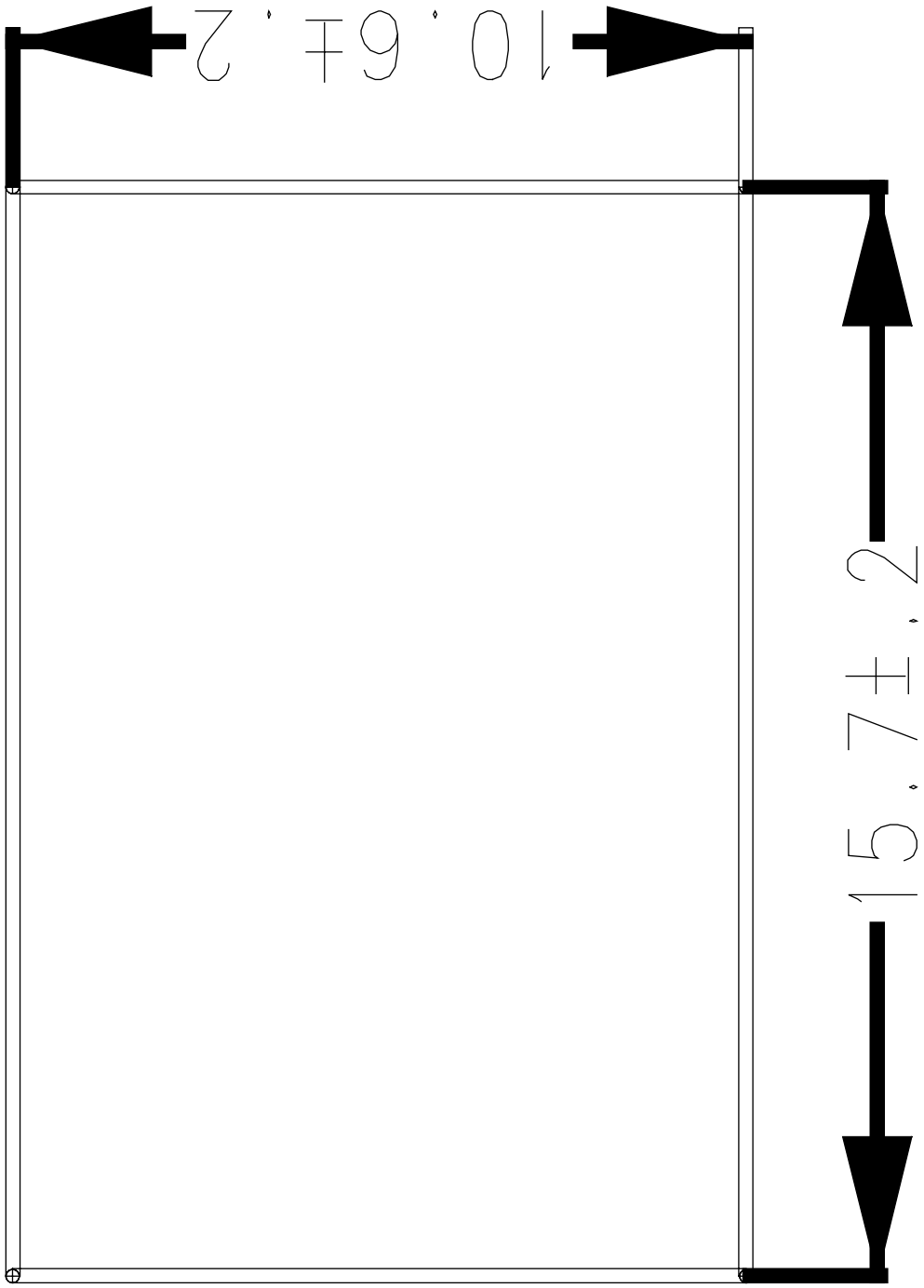
3. LAYOUT INFORMATION

The layout is viewed as seen from the top layer. A two layer PCB is foreseen. No attempts are made for matching of the line, since the lengths are minimized.

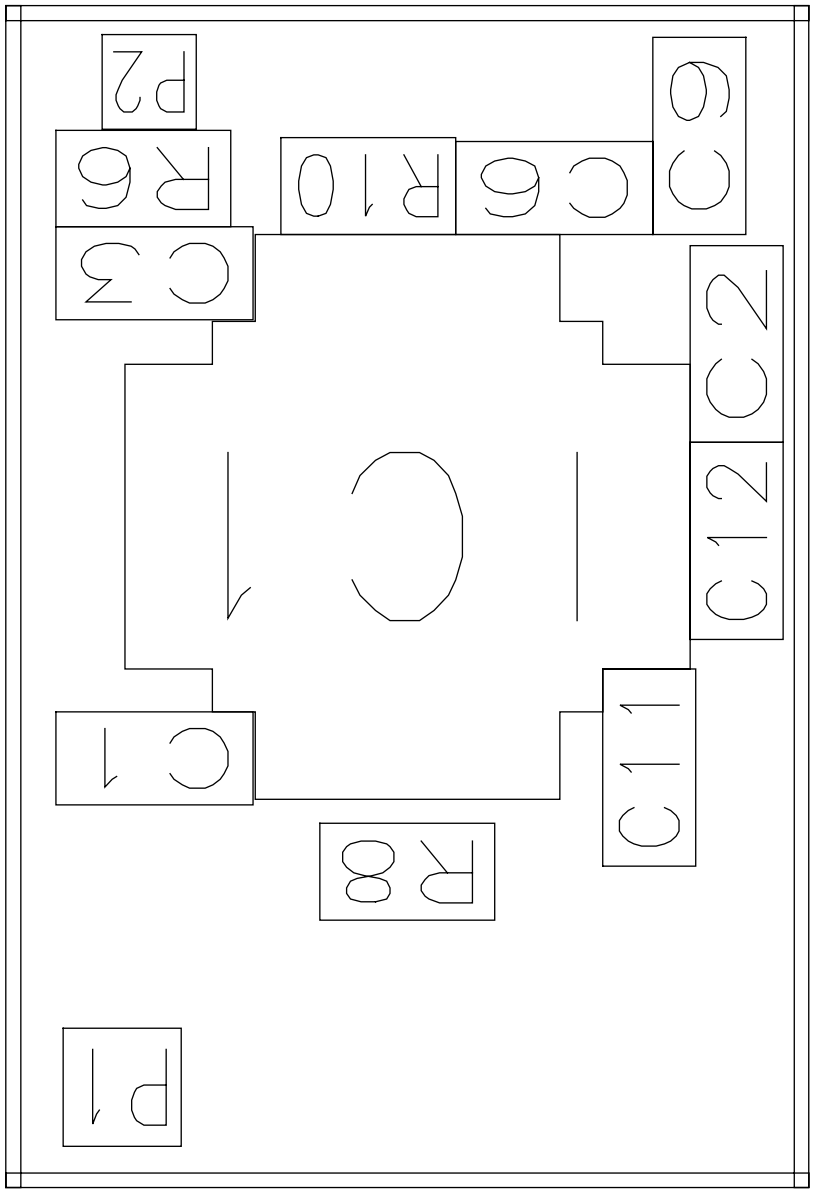
In order to maximize the heat flow from the IC it is strongly recommended to connect as much as possible metal area to the GND plane.

4. DIMENSIONS

Units: mm

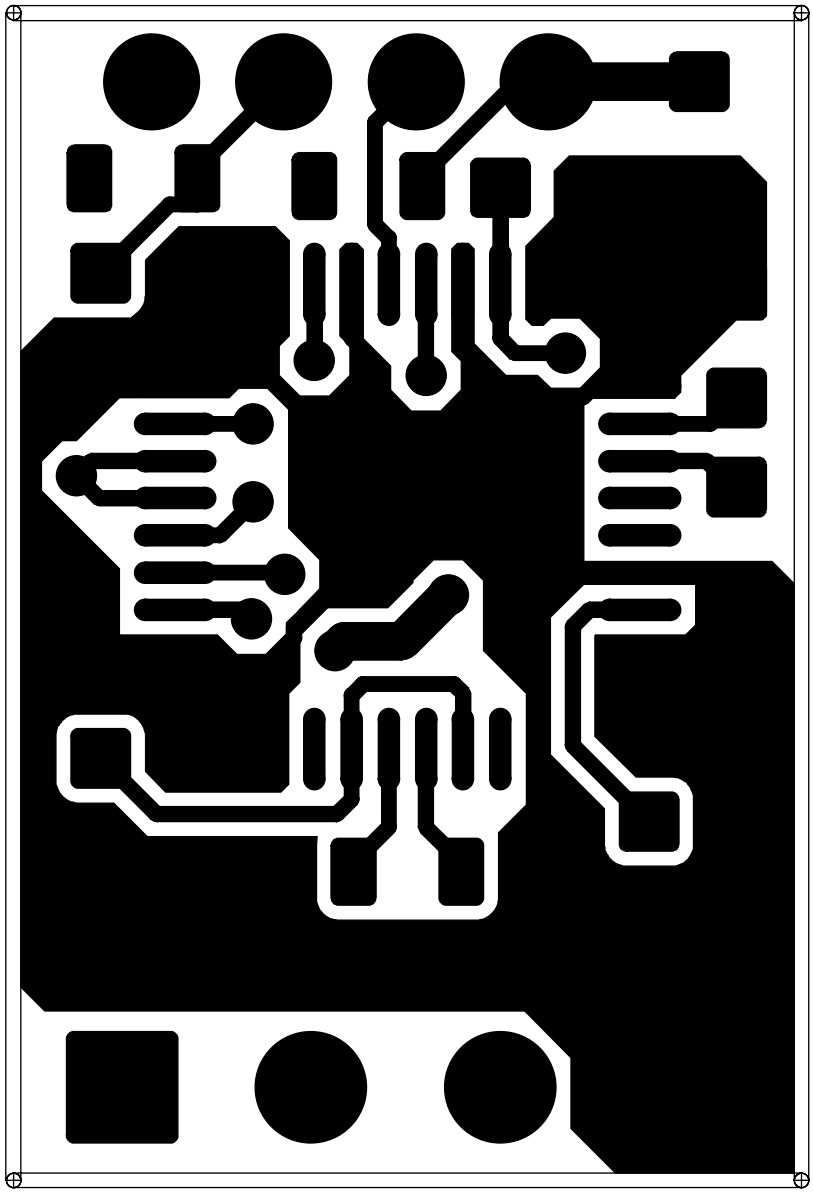


5. COMPONENT PLACEMENT TOP



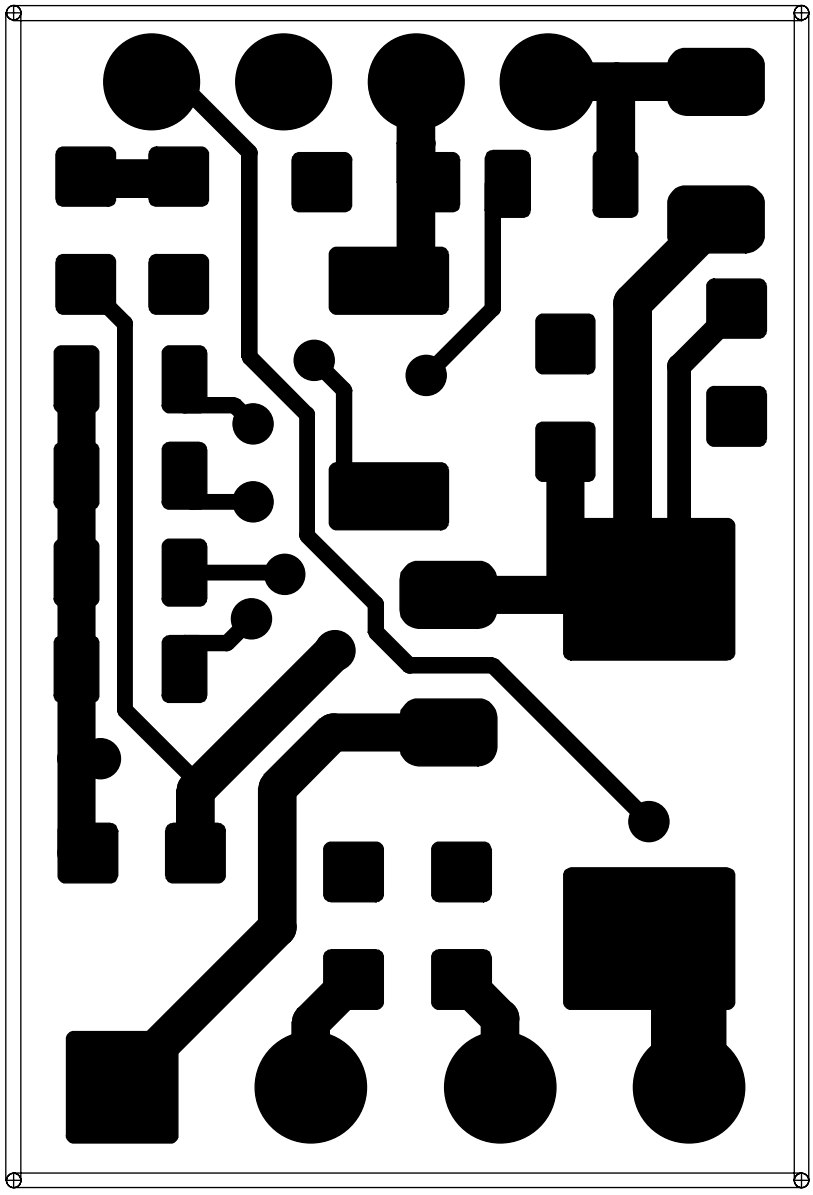
Component placement top

6. SIGNAL LAYER TOP



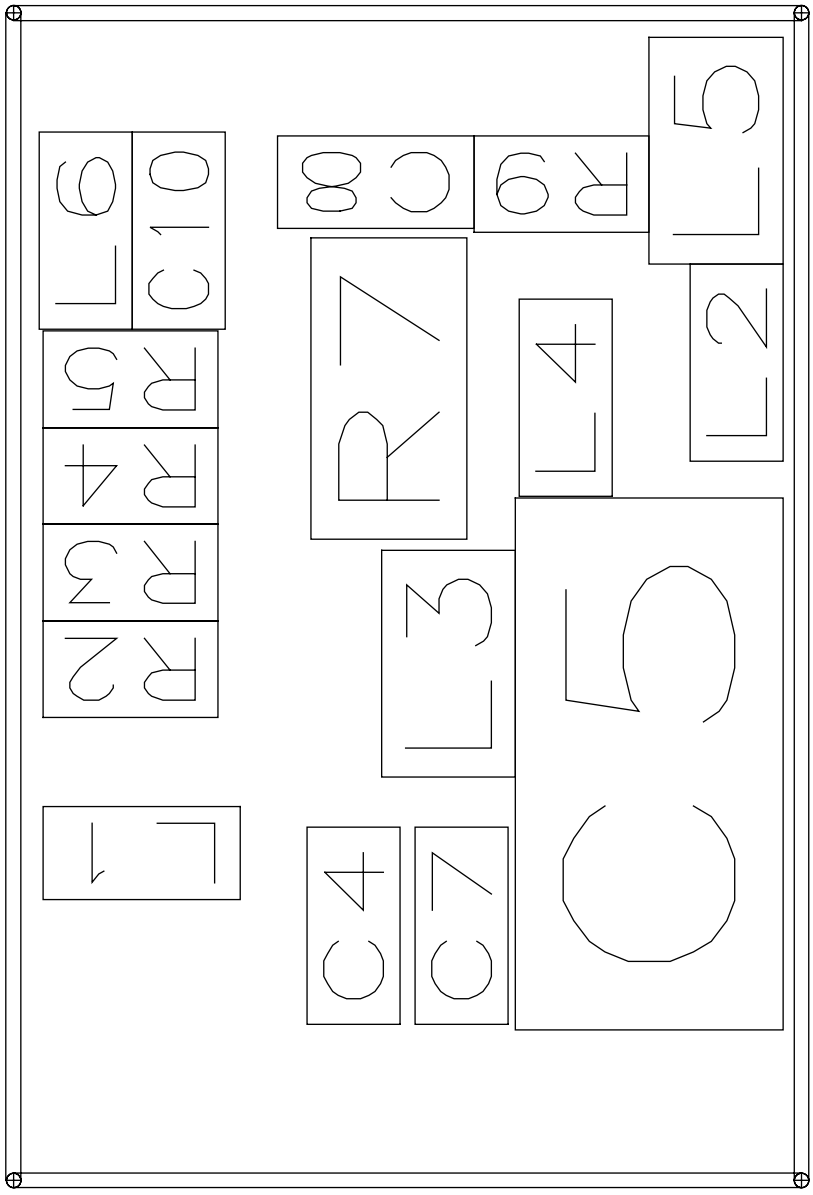
Signal layer top

7. SIGNAL LAYER BOTTOM

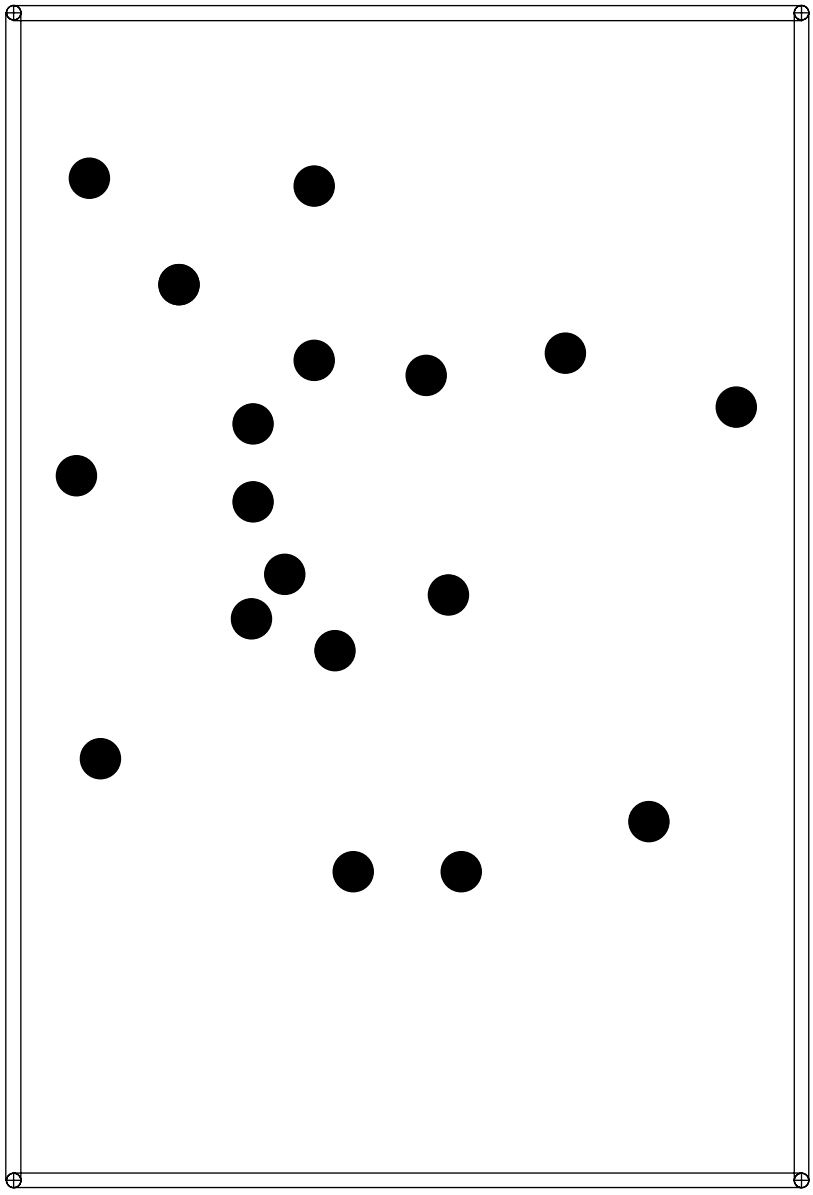


Signal layer bottom

8. COMPONENT PLACEMENT BOTTOM



Component placement bottom



Via

9. VIAS