APPLICATION NOTE

UMA1021M
Low Voltage
Frequency Synthesizer

AN96083

Philips
Semiconductors

PHILIPS

Abstract

The UMA1021M is a low noise, low power 2.2 GHz single synthesizer. It is intended for radiocommunication systems like GSM, DCS1800, PCS1900, DECT, PHS, DAMPS, ... where good noise performance and fast switching time are required.

A close in noise value of -90 dBc/Hz has been measured in the loop bandwidth of a typical GSM application.

APPLICATION NOTE

UMA1021M
Low Voltage Frequency Synthesizer

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Keywords

Radio communications
PLL
UMA1021M
Frequency synthesizer
Low power
Low voltage
Low noise

Date: August 12th, 1996

Summary

This application note describes the UMA1021M IC from Philips Semiconductors. It permits low noise, low power single chip solution for designing a PLL frequency synthesizer. It is primarily intended for use in digital cellular and cordless communication equipment. Typical applications include GSM, DCS1800, PCS1900, DECT, PHS, CT2, DAMPS... It can also be used for any other radio applications up to 2 GHz, which need a single synthesizer, like PMR, marine, spread spectrum, security, ...

Section 1 contains a general presentation of the UMA1021M and section 2 details each part of the IC. Since the overall performance of any PLL frequency synthesizer system is critically determined by the lowpass filter used, a worked example of a PLL design is described in section 3. The following section shows measurement results from different applications (GSM, DCS1800, PHS, DECT and DAMPS). Guidance for the assembly and operation of the demonstration board is included in the annexe. Some rules of thumb and tricks are indicated in the last section in “Frequently Asked Questions”.

All data presented in this report have been obtained from the characterisation of a few typical samples. Whilst most samples have similar performance, only values indicated on the UMA1021M specification are guaranteed by Philips. These results must be considered as an aid to design the PLL in your application.

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1. Introduction to the UMA1021M single synthesizer

1.1 General description

The UMA1021M [1] is a low phase noise, low power, low voltage, one chip solution to a single frequency synthesizer for use in radiocommunications. Designed in a BICMOS process, it operates from 2.7 (3 NiCd cells) to 5.5 V. The UMA1021M contains all the necessary elements with the exception of the VTCXO, VCO and loop filter to build a PLL frequency synthesizer.

The synthesizer operates at RF input frequencies up to 2.2 GHz, with fully programmable main and reference dividers. The reference input operates from 3 to 35 MHz. Fast programming is possible via the three wire serial bus with clock speeds up to 10 MHz.

The phase detector drives low and high current charge pump simultaneously. Maximum current is 0.4 mA with the low current charge pump (pin CP) and 3.2 mA with the fast charge pump (pin CPF). The latter can be disabled by the pin FAST. The programmable charge pump currents are fixed by an external resistance R_{SET} (at pin I_{SET}). Only passive loop filters are necessary.

Separate power supply and ground pins are provided to the analog (charge pumps) and digital parts of the IC.

The synthesizer can be powered down to save current via software programming or by hardware pin PON.

1.2 Features

- Low power / power-down
- Very low noise BICMOS design (-90 dBc/Hz typically measured in the loop bandwidth in a GSM application)
- Small SSOP-20 package
- Fast 3-line serial bus interface
- RF input from 300 to 2200 MHz
- Fully programmable main and reference dividers
- Programmable charge pump currents
- Dual phase comparator outputs to allow fast frequency switching
- Out-of-lock indicator

1.3 Typical application

The UMA1021M single synthesizer is typically used in digital radiotelephone systems which require very low phase noise and spurious like GSM and DCS1800. It can also be used with applications which need fast switching like DECT. Fig. 2 shows a typical application which allows the use of the UMA1021M.

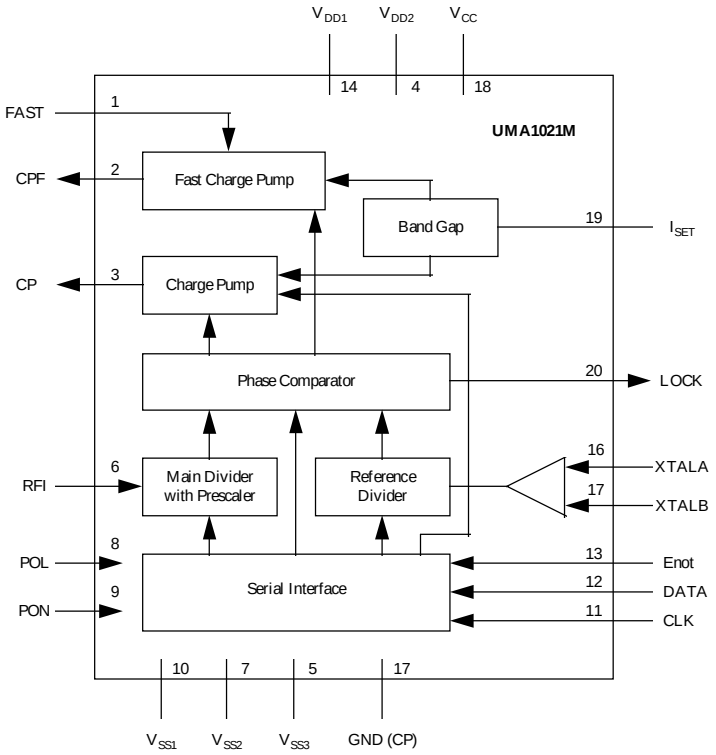


Fig. 1 - UMA1021M Block Diagram.

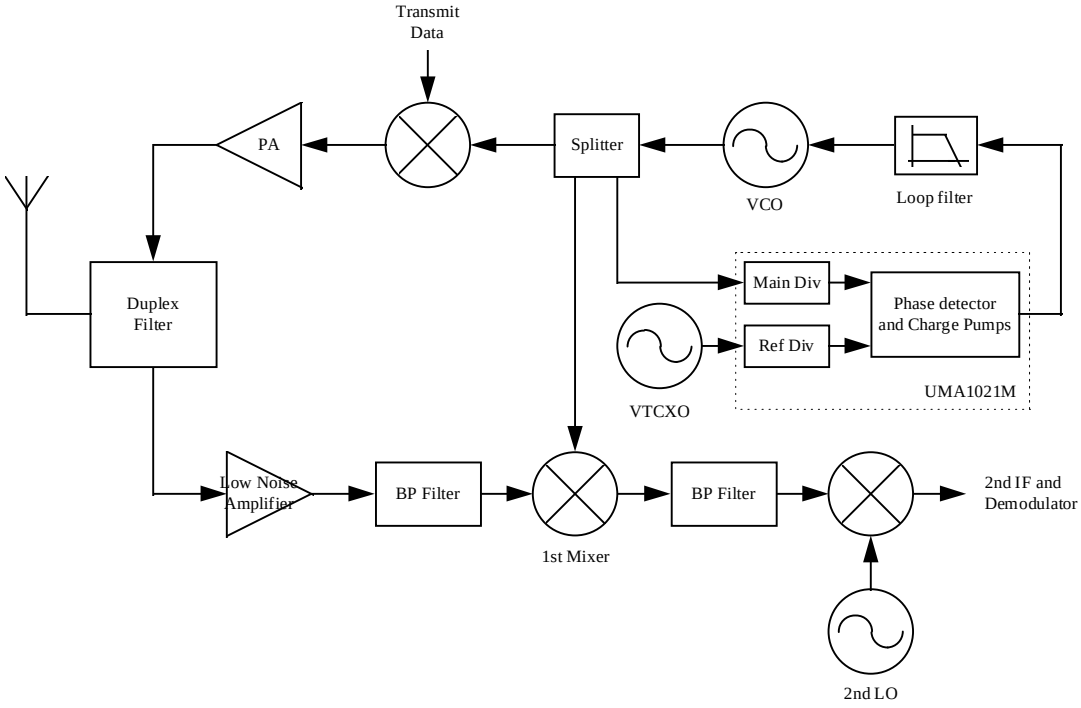


Fig. 2 - Typical Application Block Diagram.

2. Functional description of the UMA1021M synthesizer

Refer to the UMA1021M PLL block illustrated in the application diagram (Fig. 2).

A crystal (VTCXO) provides a high purity, stable reference frequency to the PLL. VCO and crystal frequencies are divided down to a common comparison frequency to feed the phase detector. The phase detector drives a charge pump to send correction current pulses to a low pass filter. The current pulses are proportional to the difference in phase between the two phase detector input signals. The filter integrates the pulses giving a voltage which controls the Voltage Controlled Oscillator. The PLL is locked when the phase difference between input signals to the phase detector is maintained zero.

2.1 Phase detector and charge pump

2.1.1 Description

The phase detector is sensitive to both phase and frequency. It reacts to very small phase differences between the main divider and reference divider inputs. The design responds to the full $\pm 2\pi$ radians range of phase inputs.

The operating principle of the phase detector is depicted in Fig. 3. The comparison frequency f_{PC} at the input of the phase detector is typically the same as the radio system channel spacing.

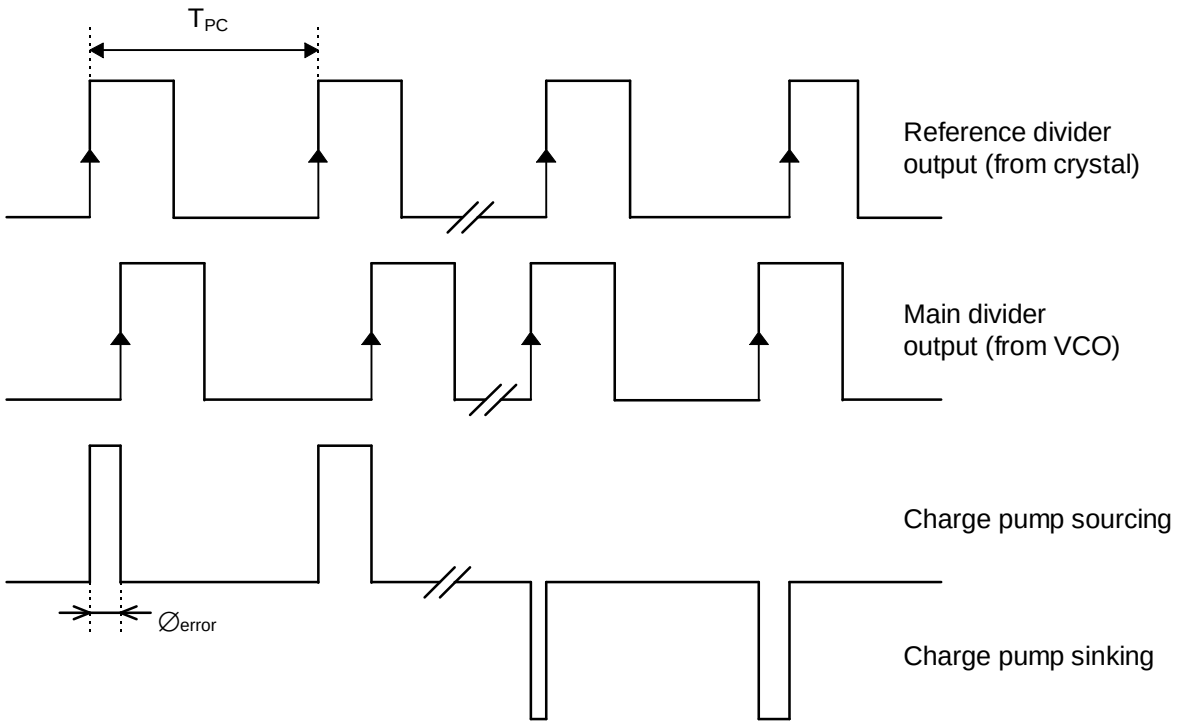


Fig. 3 - Principle of UMA1021M Phase Detector.

The charge pump outputs of the synthesizer are either sourcing, sinking or in high impedance. When the loop is locked, i.e. when the phase error at the input of the phase detector is zero, the charge pump output is in the high impedance state. When the loop is not locked, a phase error between the input signals is seen by the

phase detector and the charge pump sends correction pulses to the loop filter. If the output of the reference divider is leading, then the charge pump sources current pulses to increase the VCO control voltage and frequency. If the output of the reference divider is lagging, the charge pump sinks current pulses to decrease the VCO control voltage and frequency. The pulse duration is proportional to the phase error. The sinking and sourcing pulses charge or discharge the capacitors in the loop filter, to a voltage required to bring the PLL back into lock.

The phase detector drives two charge pumps (pins CP and CPF). The charge pump currents (the « height » of the positive or negative pulses in Fig. 3) are switch-selectable by software. The I_{CP}/I_{CPF} current ratio between the two charges pumps varies from 4 to 16. The reference current I_{SET} is set by an external resistance R_{SET} at pin I_{SET}, where a temperature independent voltage of 1.2 volts is generated. R_{SET} should be between 5.6 kΩ and 12 kΩ to give an I_{SET} between 200 µA and 100 µA approximately. The charge pump output currents can be programmed as shown below.

CR1	CR0	I_{CP}	I_{CPF}	$I_{CPF} : I_{CP}$
0	0	2 x I_{SET}	8 x I_{SET}	4:1
0	1	2 x I_{SET}	16 x I_{SET}	8:1
1	0	1 x I_{SET}	12 x I_{SET}	12:1
1	1	1 x I_{SET}	16 x I_{SET}	16:1

Table 1 - Charge Pumps Current Ratio Relationships.

There are two ways to connect the charge pump outputs to the principal loop filter:

- Generally, the two charge pump outputs (CP and CPF) are connected together to the loop filter. The loop filter design is given in section 3.1.
- The second way is to have a dual time constant loop. The loop uses both charge pumps during frequency switching. The phase detector drives just the slow charge pump after the required frequency is obtained. The fast charge pump is disabled by the pin FAST. A narrower loop filter allows the modulation of the VCO, with lower modulation frequencies than those possible with a wider loop filter.

The curves on the following pages show dc measurements of sink and source currents of the two charge pumps.

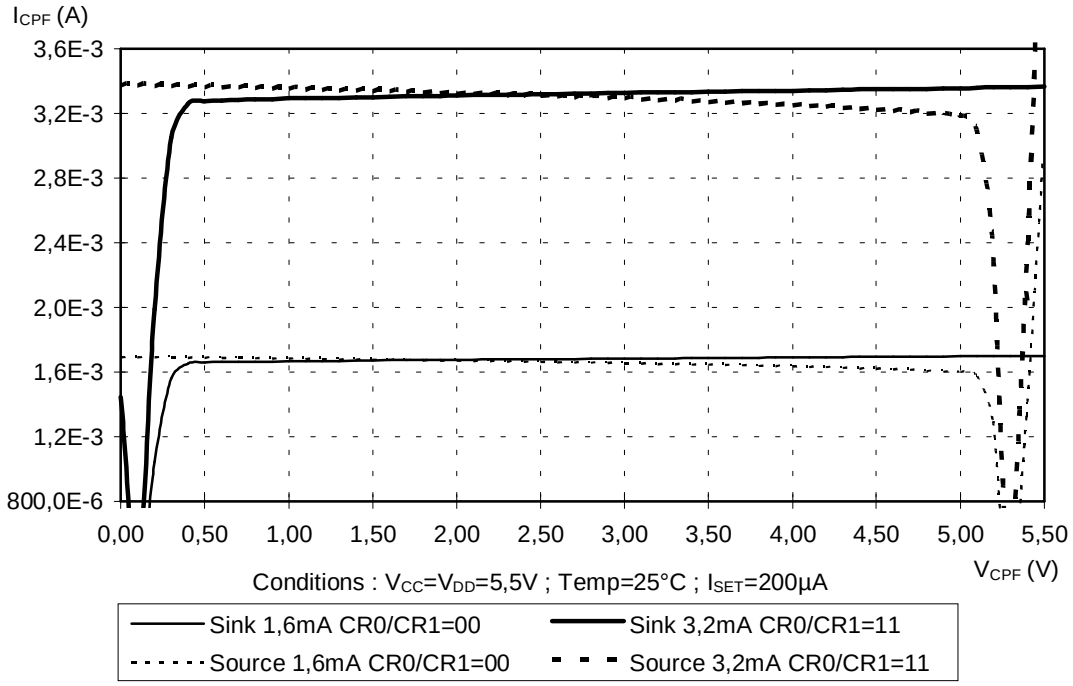


Fig. 4 - Fast Charge Pump (CPF) Output Current vs Voltage.

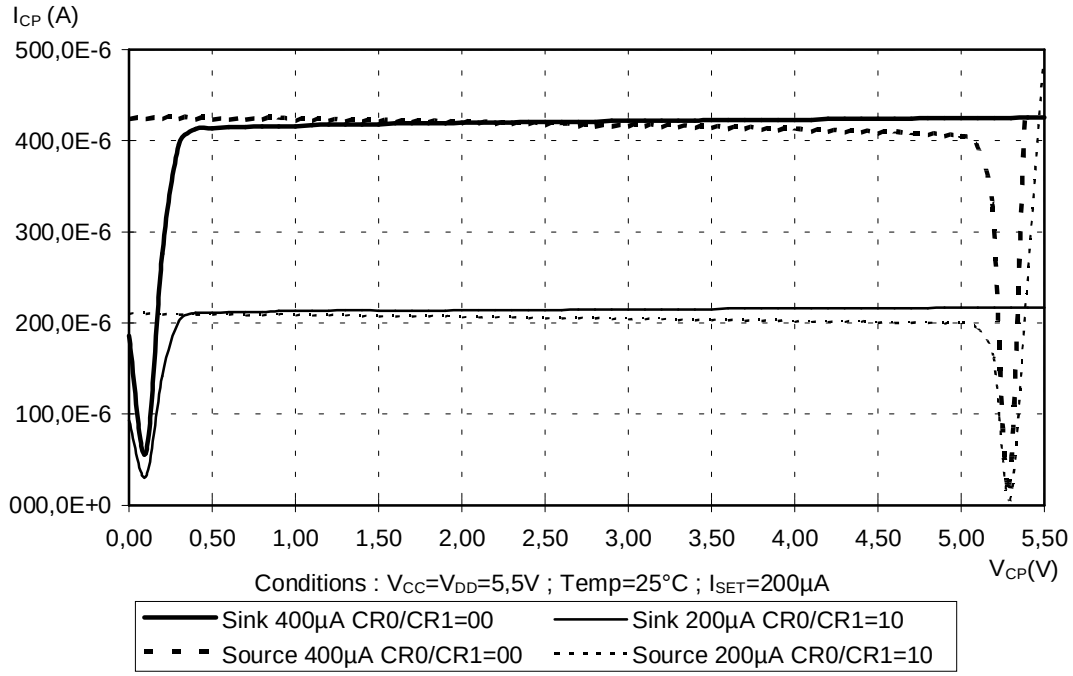


Fig. 5 - Slow Charge Pump (CP) Output Current vs Voltage.

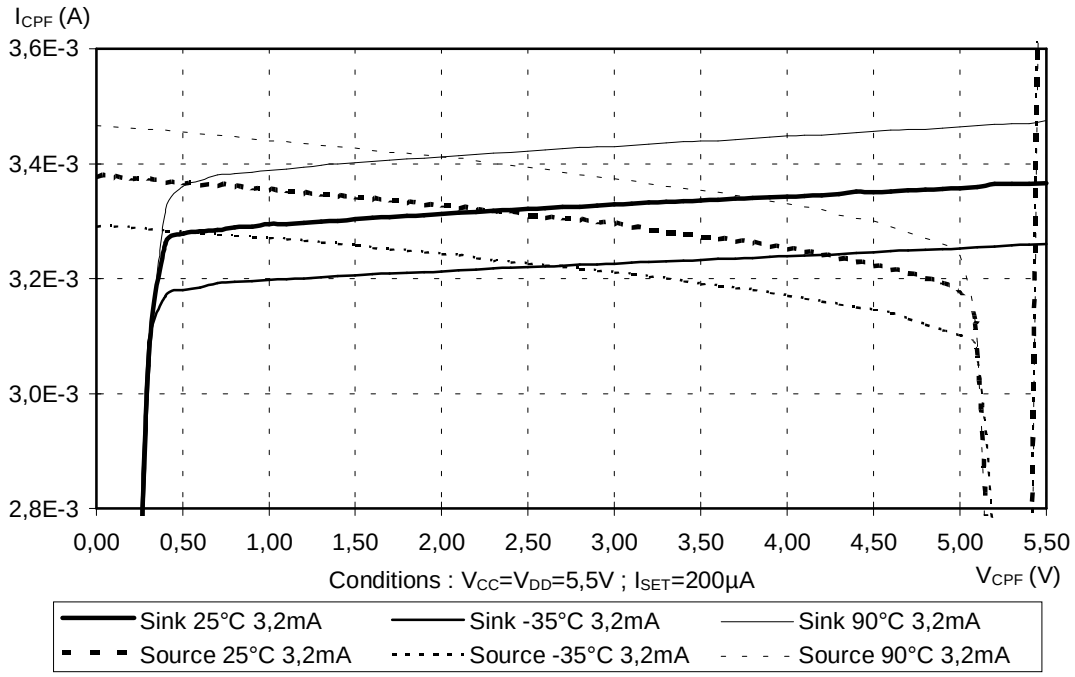


Fig. 6 - Fast Charge Pump (CPF) Output Current vs Voltage and Temperature.

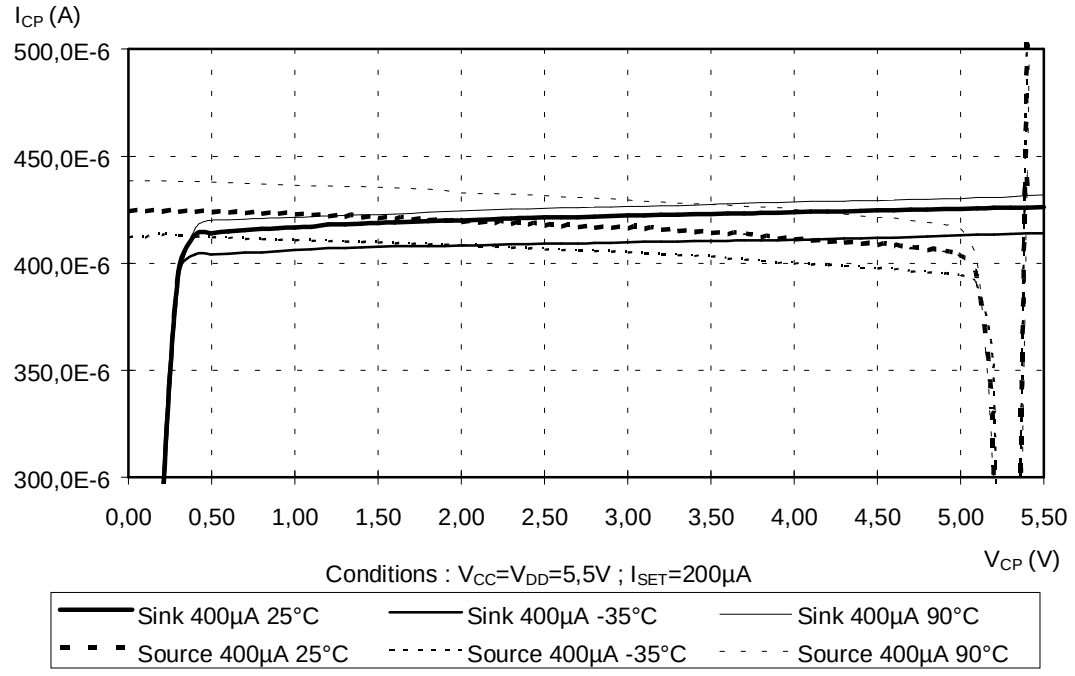


Fig. 7 - Slow Charge Pump (CP) Output Current vs Voltage and Temperature.

2.1.2 Dynamic characteristics

The method used to measure the charge pump dynamic characteristics is described on the next few pages. A multimeter with a resolution less than 1 nA and a frequency generator with a phase variation option are needed.

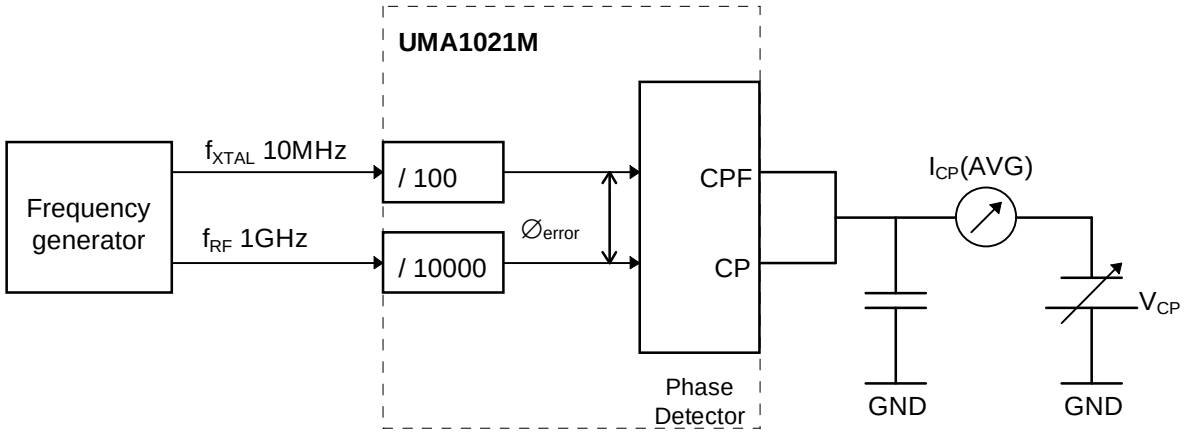
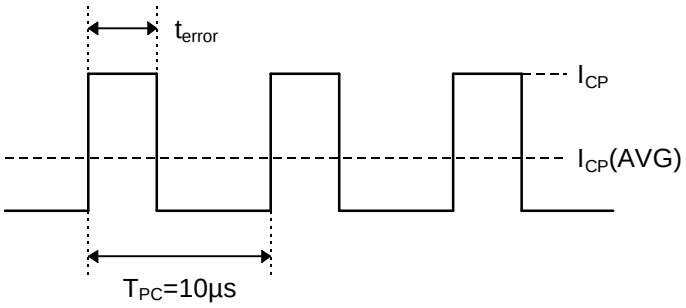
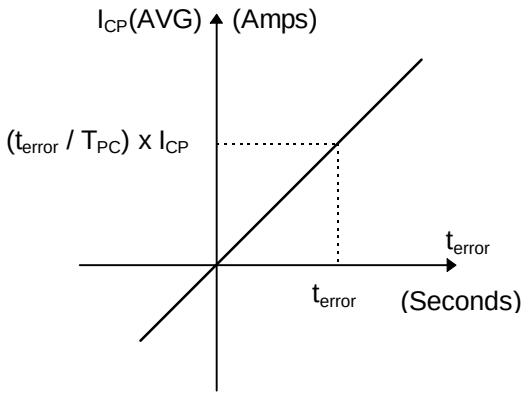


Fig. 8 - UMA1021M Principal Synthesizer Phase Detector Linearity Measurement.

A frequency generator supplies the reference divider (frequency f_{XTAL}) and the main divider (frequency f_{RF}). These frequencies are divided down to obtain a comparison frequency of 100 kHz. The generator allows the phase of the 1 GHz signal to be controlled with respect to the 10 MHz reference signal. The I_{CP}(AVG) phase detector current is measured as a function of the phase error.



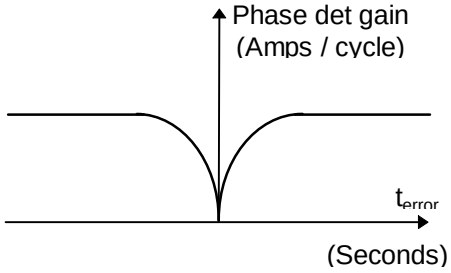
$$I_{CP}(AVG) = \left(\frac{t_{error}}{T_{PC}}\right) \times I_{CP}$$



In order to find the real phase detector and charge pump gain for very small phase errors, we transform this curve by the equation: Phase Detector Gain (Amps/cycle) = I_{CP}(AVG) x (T_{PC} / t_{error}). So the charge pump dynamic characteristics are obtained (see Fig. 10, Fig. 12, Fig. 14 and Fig. 16). Curves show measurements for source and sink gains.

Phase error values are taken in the region of ± 16 ns. This is where the phase detector and the charge pump are less linear and where the loop spends most of its time, i.e. when it is locked or nearly locked.

The charge pump must remain linear for small phase errors, to ensure a low and stable value of close in noise and to optimise settling time. Traditionally this has caused problems to PLL designers, the worst being the so-called “dead zone” in which the dynamic gain falls to zero (as shown below) due to the charge pump not reacting to small phase errors.



Philips Semiconductors has focused effort on the design of a very linear charge pump for the UMA1021M. Different curves show that the real charge pump gain for very small phase errors is mostly maintained within 15% of ideal value. The jagged nature of the curves can partly be explained by very small values of I_{CP}(AVG), and phase error granularity problems.

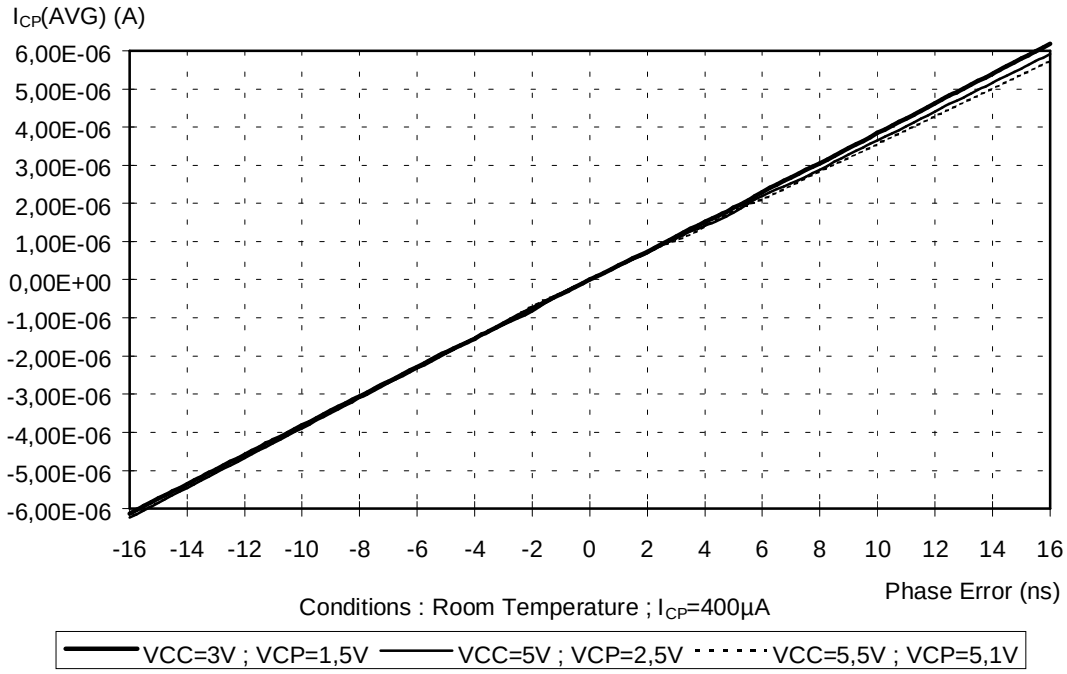


Fig. 9 - Phase Detector and Slow Charge Pump Characteristic vs V_{CC}.

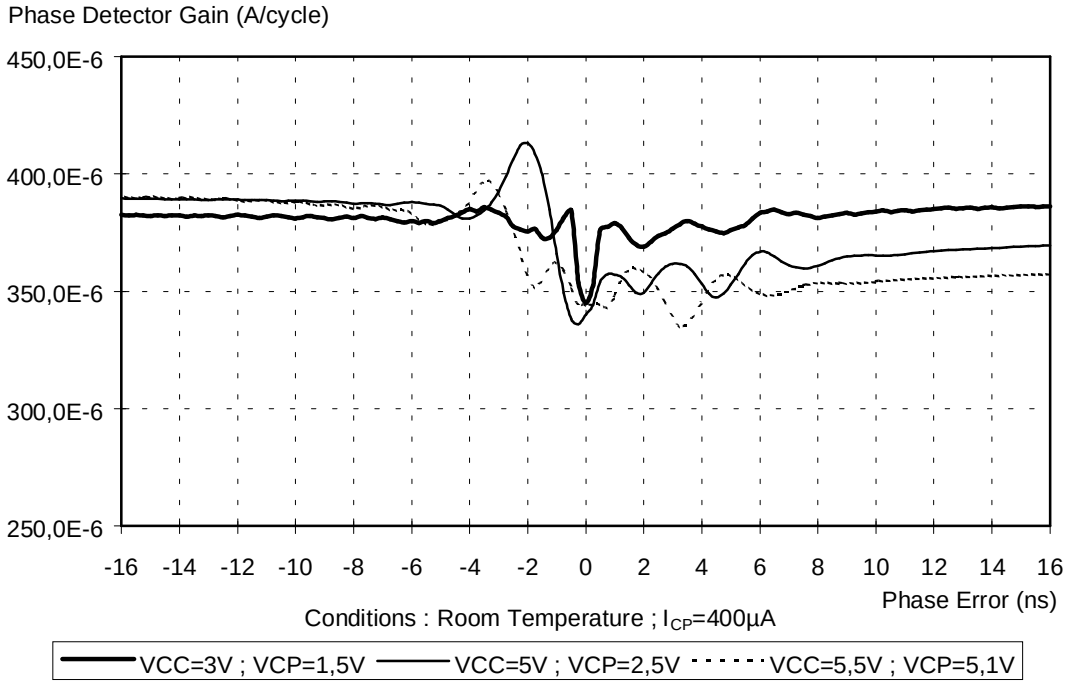


Fig. 10 - Phase Detector and Slow Charge Pump Gain vs V_{CC}.

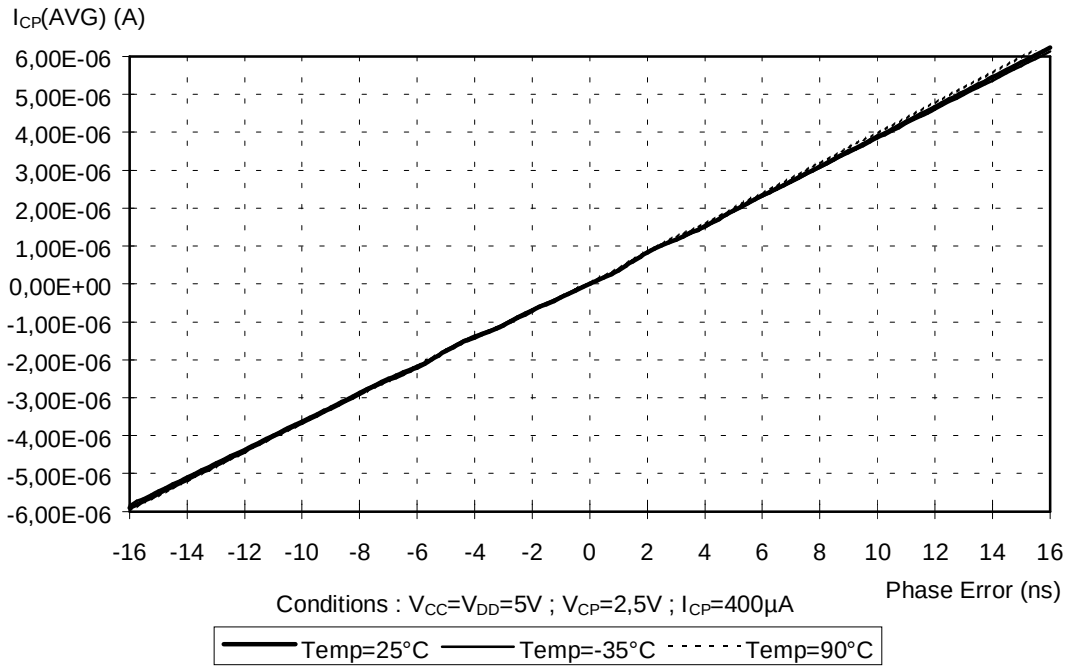


Fig. 11 - Phase Detector and Slow Charge Pump Characteristic vs Temperature.

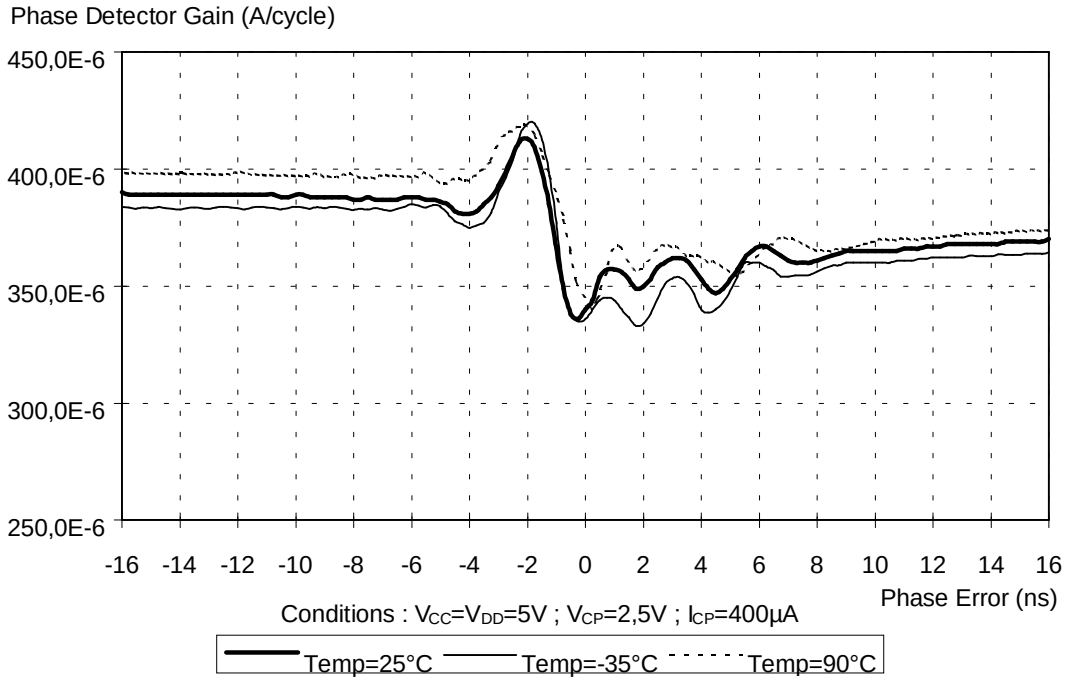


Fig. 12 - Phase Detector and Slow Charge Pump Gain vs Temperature.

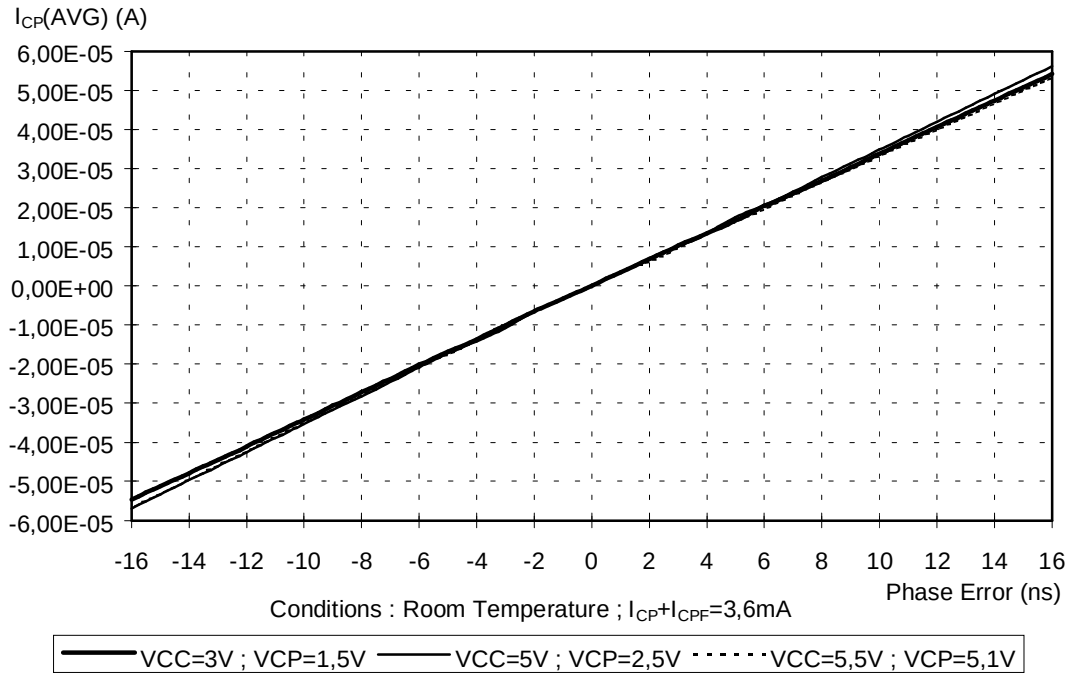


Fig. 13 - Phase Detector and Charge Pumps Characteristic vs V_{CC}.

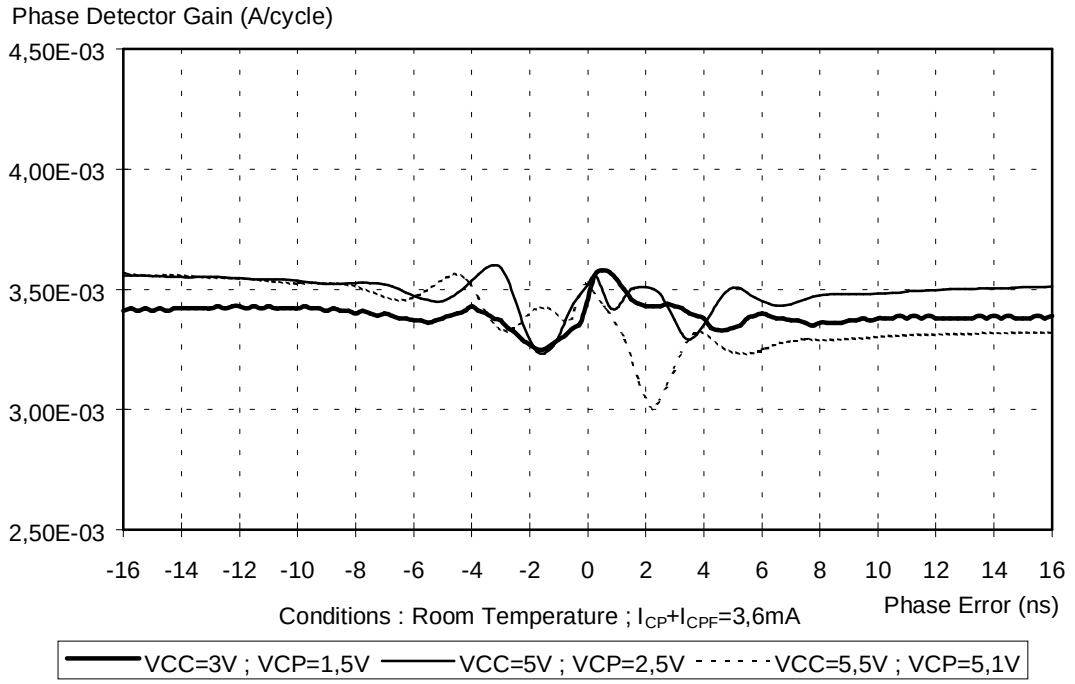


Fig. 14 - Phase Detector and Charge Pumps Gain vs V_{CC}.

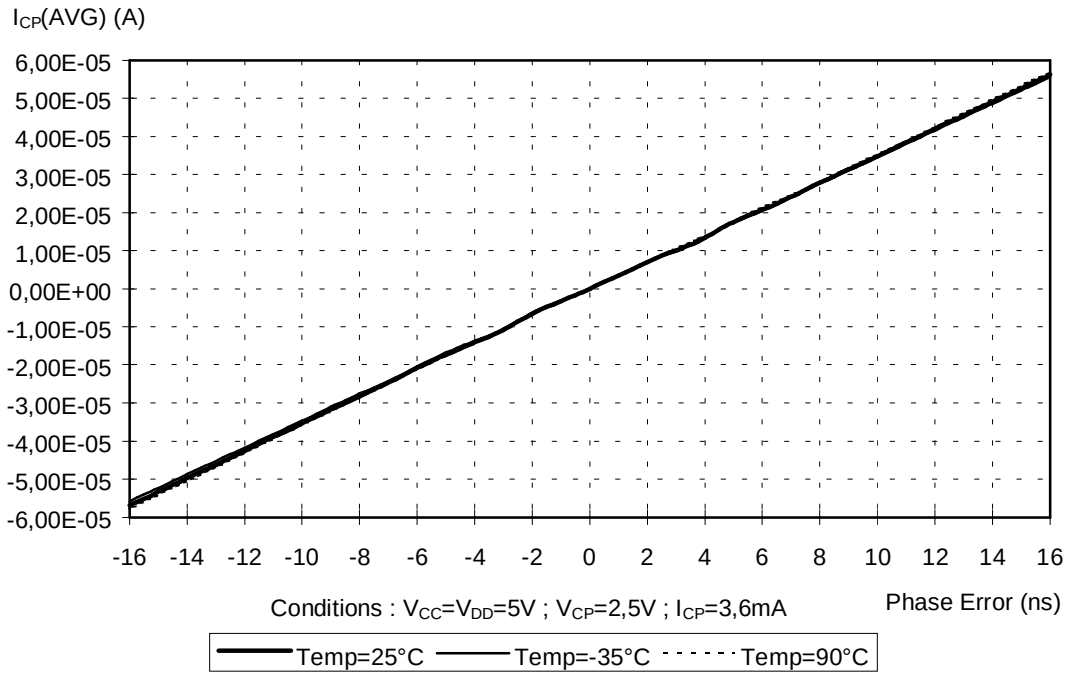


Fig. 15 - Phase Detector and Charge Pumps Characteristic vs Temperature.

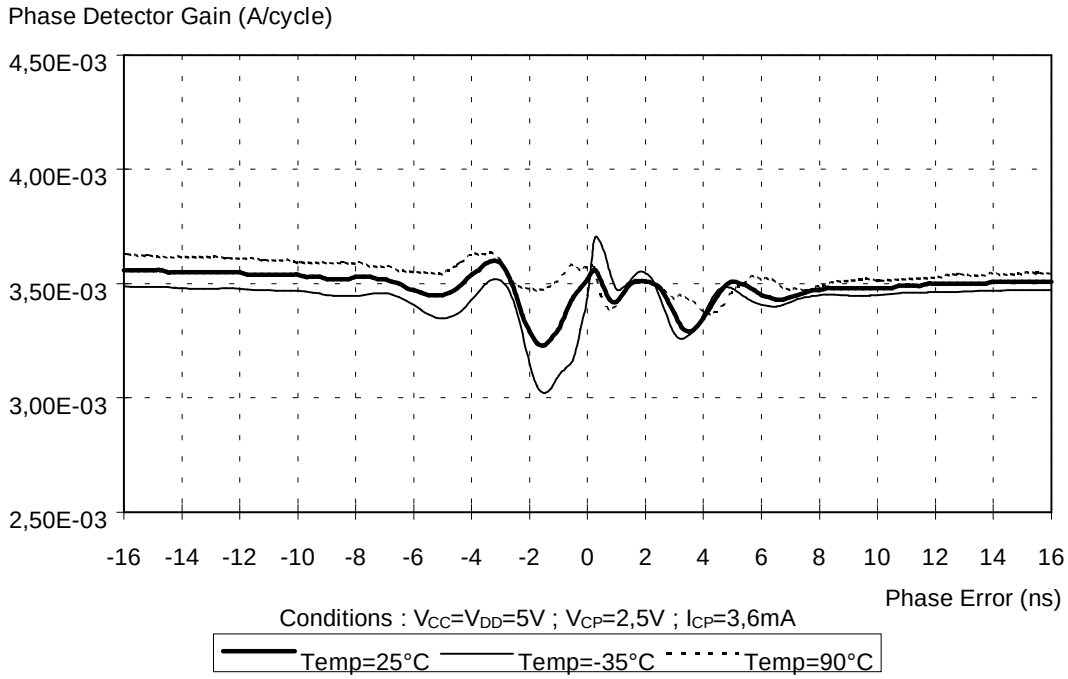


Fig. 16 - Phase Detector and Charge Pumps Gain vs Temperature.

2.2 Programming

A simple three wire unidirectional serial bus is used to program the synthesizer. The three lines are DATA, CLK (Clock) and Enot (Enable). The data sent to the device is loaded in bursts framed by Enot. Programming clock edges are ignored until Enot goes active low. The programmed information is loaded into the addressed latch when Enot returns inactive high. Only the last 21 bits serially clocked into the device are retained within the programming register. Additional leading bits are ignored, and no check is made on the number of clock pulses. The fully static CMOS design uses virtually no current when the bus is inactive. It can always capture new programming data even during power-down. After software or hardware power down is terminated, it is not necessary to reprogram the device. Previous programming data is preserved during power-down.

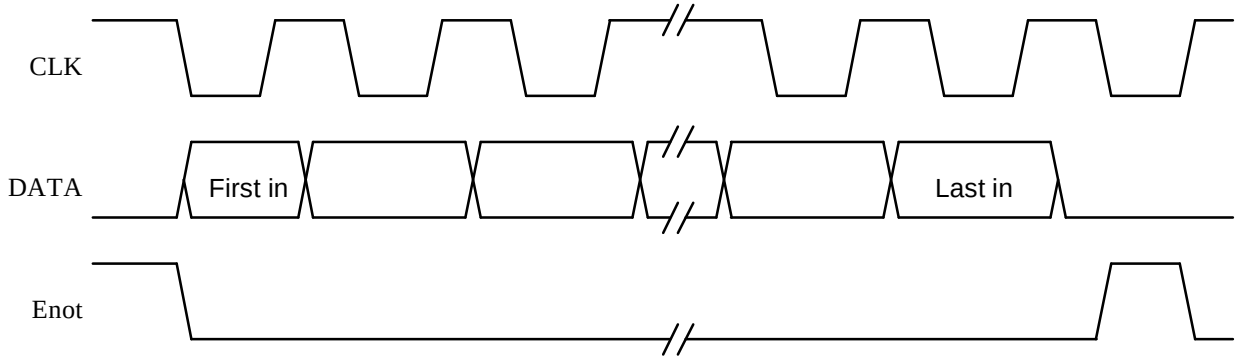


Fig. 17 - Serial Interface Timing Diagram.

Data is entered with the most significant bit first. The leading bits make up the data field, while the trailing four bits are used for the address. The bits are decoded on the rising edge of Enot. A worked example of programming is shown in section 2.2.2 below.

2.2.1 Power-down mode

The synthesizer is on when both the input signals PON and the programmed bit sPON are active. The ‘active’ level for these two signals is chosen at pin POL. When turned on, the dividers and phase detector are synchronized to avoid random phase errors. When turned off, the phase detector is synchronized to avoid interrupting charge-pump pulses. For synchronization functions to work correctly on power-up or power-down (using either hardware or software programming), the presence of TCXO and VCO signals is required to drive the appropriate divider inputs. The UMA1021M has a very low current consumption in the power-down mode.

2.2.2 UMA1021M typical programming example

Crystal reference input frequency: 13 MHz

RF input frequency: 902 MHz (Main divider ratio = PM = 4510)

Comparison frequency: 200 kHz (Reference divider ratio = PR = 65)

Synthesizer ON (PON=1) ; POL pin is pulled up

Out of lock indication (OOL=1)

Charge pump currents: I_{CPF} = 16 x I_{SET} ; I_{CP} = 2 x I_{SET} (CR1 = 0 ; CR0 = 1)

first in **Register bit allocation in** **last**	
dt16 Data field dt0	Address
Control reg = 0 0001 0010 0100 0000b	1 h
Main divider coefficient = 4510d = 0119Eh	4 h
Reference divider coefficient = 65d = 00041h	5h

Table 2 - UMA1021M Register Data Allocations Expressed in Decimal and Hexadecimal.

first in (msb) **Data field in** **(lsb) last**																	**Adress**			
0	0	0	0	1	0	0	1	0	0	1	0	0	0	0	0	0	0	0	0	1
0	0	0	0	1	0	0	0	1	1	0	0	1	1	1	1	0	0	1	0	0
0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	1	0	1	0	1

Table 3 - UMA1021M Register Data Allocations Expressed in Binary.

2.2.3 UMA1021M preset values

After the supply voltage is switched on, the different registers are loaded with following preset values. They correspond to a typical GSM application. When using a 13 MHz VTCXO, the PLL is directly locked at 910 MHz (if it is within the VCO range) with a 200 kHz comparison frequency.

Main divider ratio	4550
Reference divide ratio	65
Control register	OOL=0 ; CR1=1 ; CR0=1 ; sPON=1
Test register	all 0

Table 4 - UMA1021M Preset Values.

Since the preset state is not tested, Philips Semiconductors does not guarantee these values. Programming of all registers is recommended after switching ON the synthesizer supply voltage.

2.3 Reference divider

The input f_{XTAL} drives a pre-amplifier to provide the clock input for the reference divider. Fig. 18 shows the typical measured input sensitivity of the reference divider at room temperature.

Fig. 19 shows the sensitivity with different temperature measurements which were carried out for the worst case supply (i.e. V_{DD} = 2.7 V). Reference divider has been observed to work correctly for high input levels up to 10 dBm. For reference and main dividers sensitivity measurements, the input pins have been externally terminated by a capacitivly decoupled 50 Ω load.

Fig. 20 and Table 5 show the Fxtal input admittance. These parallel elements (conductance and susceptance) are given for typical samples. A high input resistance has been measured, 10 kΩ typically. There is no significant impedance change when powering down the synthesizer (as shown in Table 5).

Since the Fxtal input DC voltage is internally fixed, a DC decoupling capacitor must be inserted between these pins (XTALA and XTALB) and the reference source or ground.

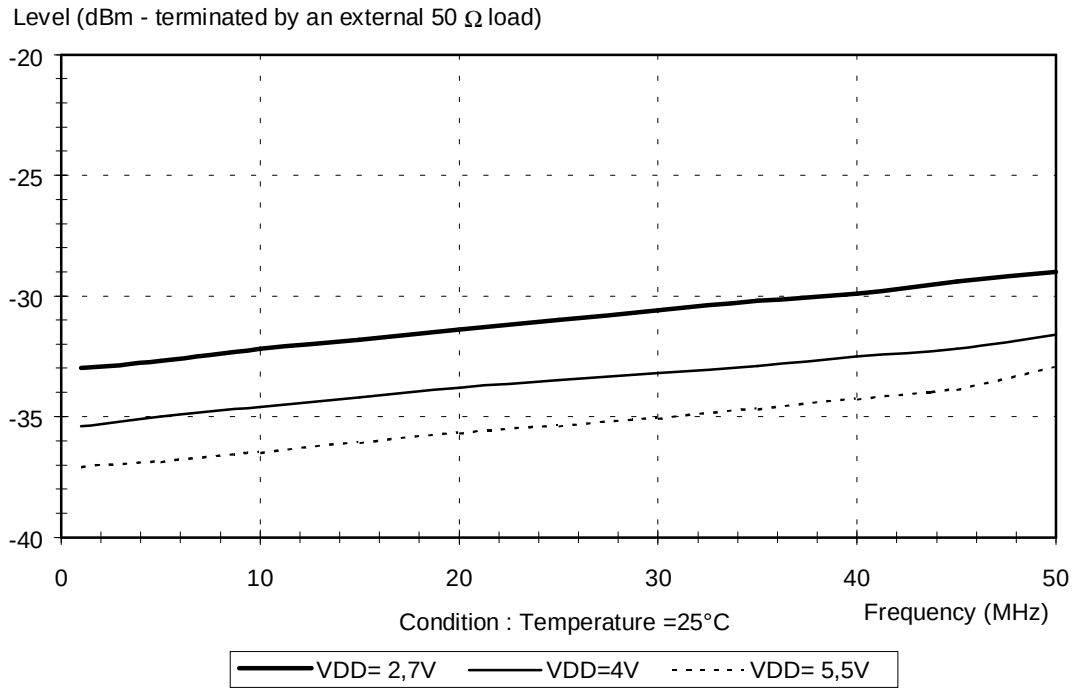


Fig. 18 - Reference Divider Input Sensitivity vs Frequency and Supply.

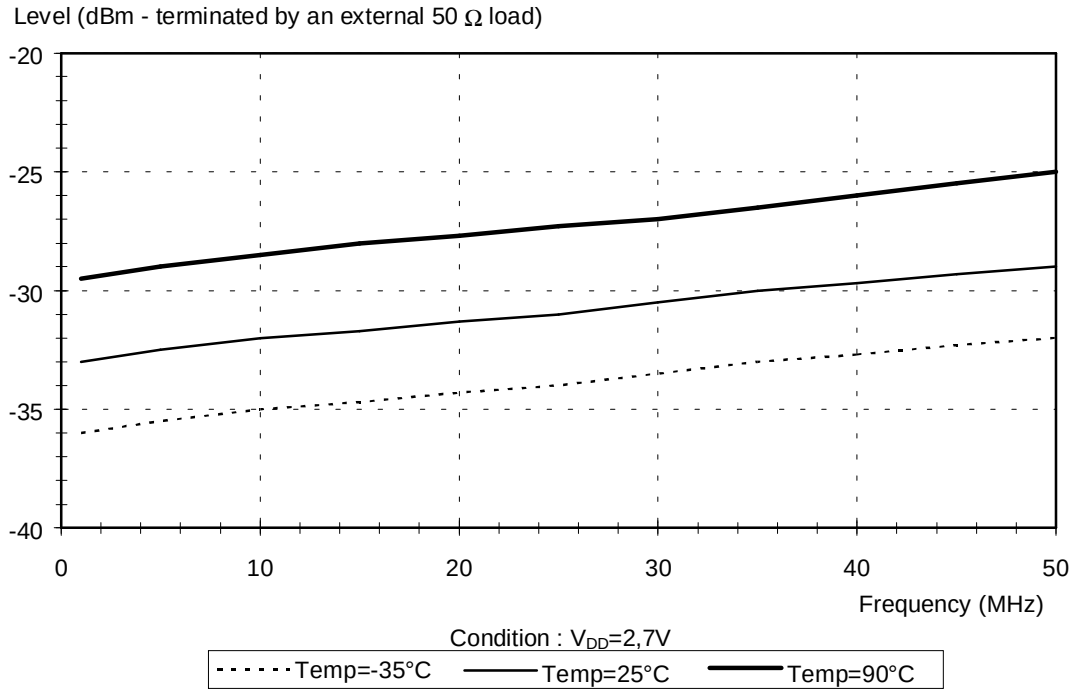


Fig. 19 - Reference Divider Input Sensitivity vs Frequency and Temperature.

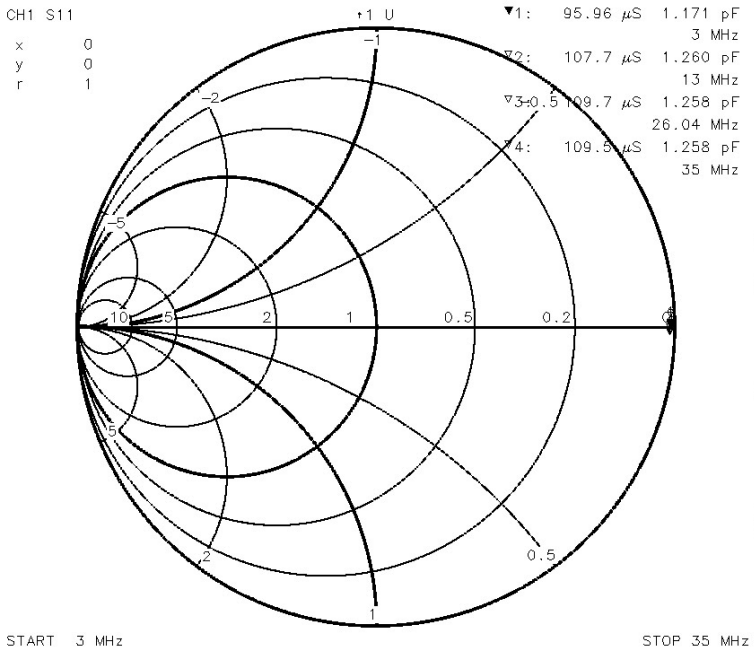


Fig. 20 - Typical F_{xtal} Input Admittance (IC powered up).

Input Frequency (MHz)	Power Up		Power Down	
	Real Part	Imaginary Part	Real Part	Imaginary Part
3	96 µS (10.4 kΩ)	22 µS (1.15 pF)	70 µS (14.3 kΩ)	29 µS (1.19 pF)
13	108 µS (9.3 kΩ)	102 µS (1.26 pF)	79 µS (12.7 kΩ)	100 µS (1.23 pF)
26	109 µS (9.2 kΩ)	205 µS (1.26 pF)	81 µS (12.3 kΩ)	200 µS (1.23 pF)
35	108 µS (9.3 kΩ)	276 µS (1.26 pF)	80 µS (12.5 kΩ)	270 µS (1.23 pF)

Table 5 - Typical F_{xtal} Input Admittance.

2.4 Main Divider

The RF input drives a pre-amplifier to provide the clock for the main divider. The pre-amplifier has a high input impedance, dominated by pin and pad capacitance. The high frequency sections of the main dividers are implemented using bipolar logic, while the slower sections use lower current CMOS logic. Fig. 21 shows the typical measured input sensitivity of the main divider at room temperature. For frequency sensitivity versus temperature measurement (Fig. 22), the IC is supplied with the worst case for V_{DD} (i.e. V_{DD} = 2.7 V).

Fig. 23 and Table 6 show RF input admittances. These parallel elements (conductance and susceptance) are given for typical samples. There is no significant impedance variation observed between power up and power down states.

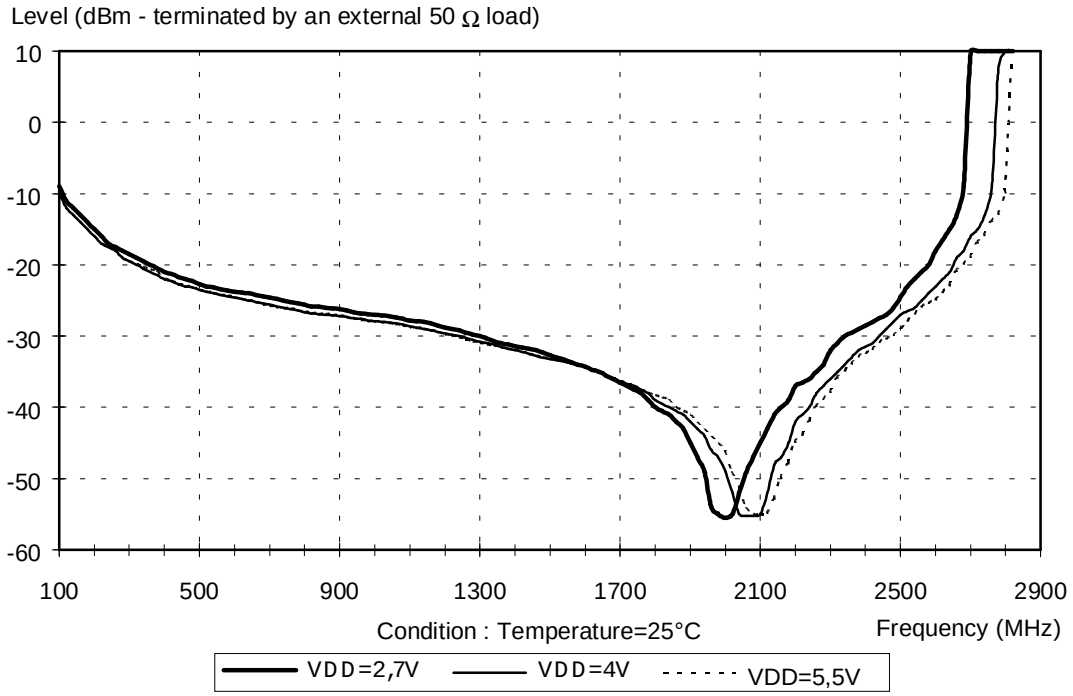


Fig. 21 - Main Divider Input Sensitivity vs Frequency and Supply.

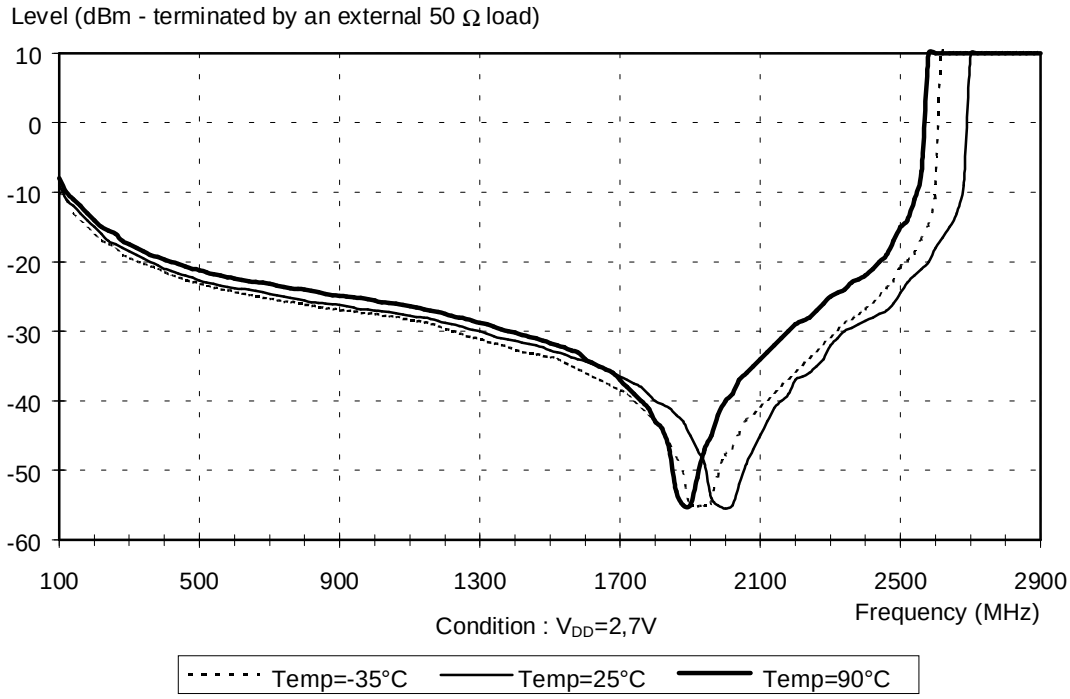


Fig. 22 - Main Divider Input Sensitivity vs Frequency and Temperature.

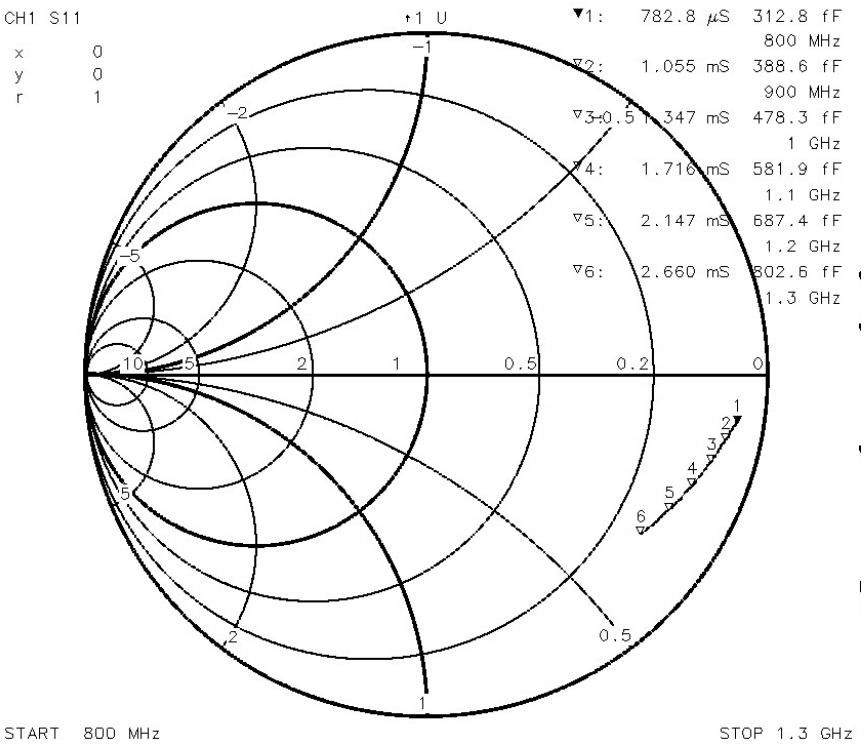


Fig. 23 - Typical RF Input Admittance (IC powered up).

Input Frequency	Power Up		Power Down	
(MHz)	Real Part	Imaginary Part	Real Part	Imaginary Part
300	279 µS (3.6 kΩ)	174 µS (90 fF)	262 µS (3.8 kΩ)	114 µS (60 fF)
400	348 µS (2.9 kΩ)	266 µS (110 fF)	322 µS (3.1 kΩ)	184 µS (70 fF)
500	454 µS (2.2 kΩ)	425 µS (136 fF)	420 µS (2.4 kΩ)	318 µS (100 fF)
600	558 µS (1.8 kΩ)	690 µS (180 fF)	513 µS (1.9 kΩ)	555 µS (150 fF)
700	688 µS (1.5 kΩ)	1.038 mS (240 fF)	632 µS (1.6 kΩ)	878 µS (200 fF)
800	784 µS (1.3 kΩ)	1.575 mS (310 fF)	722 µS (1.4 kΩ)	1.39 mS (280 fF)
900	1.06 mS (940 Ω)	2.2 mS (390 fF)	1 mS (1 kΩ)	1.98 mS (350 fF)
1000	1.35 mS (740 Ω)	3 mS (480 fF)	1.3 mS (770 Ω)	2.74 mS (435 fF)
1100	1.72 mS (580 Ω)	4.02 mS (580 fF)	1.66 mS (600 Ω)	3.65 mS (530 fF)
1200	2.15 mS (470 Ω)	5.18 mS (690 fF)	2.07 mS (480 Ω)	4.73 mS (630 fF)
1300	2.66 mS (380 Ω)	6.54 mS (800 fF)	2.55 mS (390 Ω)	6.01 mS (735 fF)
1400	3.29 mS (300 Ω)	8.11 mS (920 fF)	3.13 mS (320 Ω)	7.45 mS (850 fF)
1500	3.99 mS (250 Ω)	9.88 mS (1.05 pF)	3.76 mS (270 Ω)	9.07 mS (960 fF)
1600	4.8 mS (210 Ω)	11.75 mS (1.17 pF)	4.47 mS (220 Ω)	10.08 mS (1.07 pF)
1700	5.46 mS (180 Ω)	13.56 mS (1.27 pF)	5.11 mS (200 Ω)	12.57 mS (1.17 pF)
1800	6.08 mS (160 Ω)	15.3 mS (1.35 pF)	5.69 mS (180 Ω)	14.3 mS (1.26 pF)
1900	6.88 mS (150 Ω)	17.2 mS (1.44 pF)	6.37 mS (160 Ω)	16.1 mS (1.35 pF)
2000	7.6 mS (130 Ω)	18.9 mS (1.5 pF)	6.99 mS (140 Ω)	17.7 mS (1.4 pF)
2100	8.27 mS (120 Ω)	20.3 mS (1.54 pF)	7.56 mS (130 Ω)	19.2 mS (1.45 pF)
2200	8.87 mS (110 Ω)	21.5 mS (1.56 pF)	8.1 mS (120 Ω)	20.4 mS (1.47 pF)

Table 6 - Typical RF Input Admittance.

2.5 Voltage and Ground Pins

Separate power and ground pin are provided to the analog and digital sections. To reduce crosstalk between CMOS and bipolar parts, two independent pins supply the digital parts of the integrated circuit (V_{DD1} and V_{DD2}). V_{DD2} supplies the main divider bipolar section and V_{DD1} the other remaining digital sections. V_{DD1} and V_{DD2} could be shorted at the pins, however separate decoupling is better. The voltage difference between these pins should be no greater than 300 mV.

The ground leads should be externally shorted together otherwise large currents may flow across the die, and damage it.

2.6 In lock detector

The out-of-lock functions works in the following way:

- When the phase error ϕ_e is greater than T_{OOL} with $T_{OOL} \cong 20$ ns (approximately), the OOL signal goes low.
- When coming back into lock, ϕ_e has to be smaller than T_{OOL}. Then, the OOL signal goes high again.

This procedure is illustrated in the diagram below.

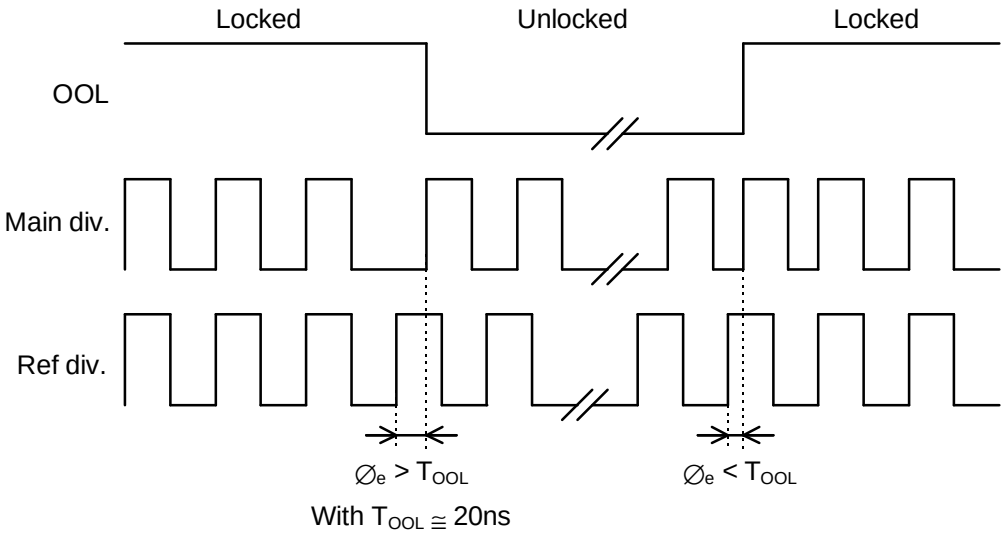
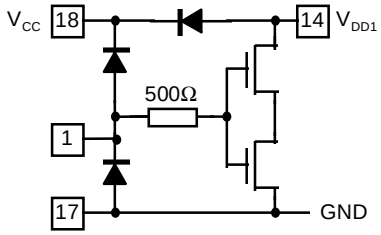
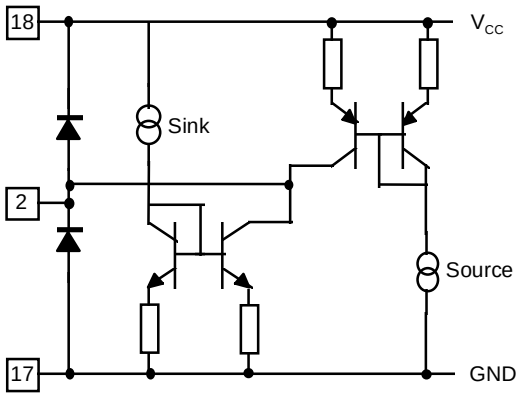
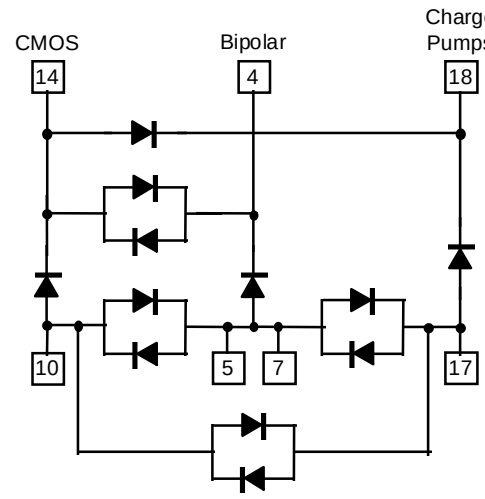
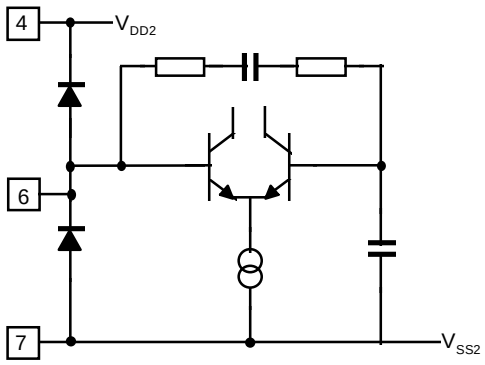
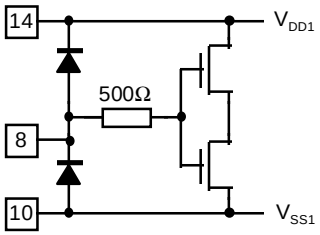
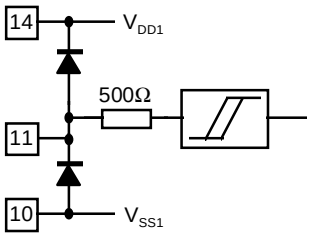
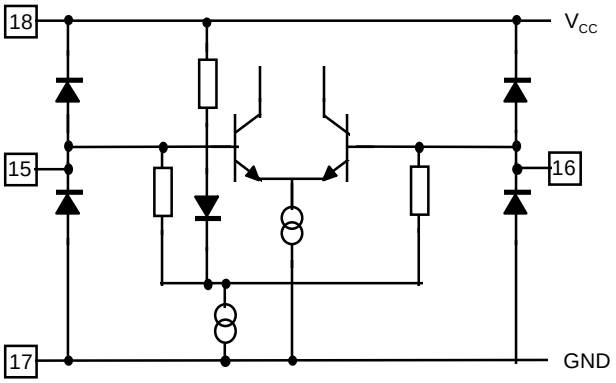


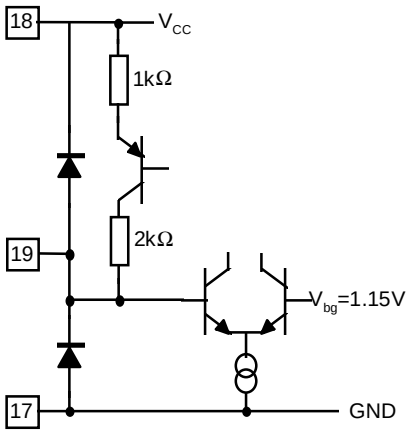
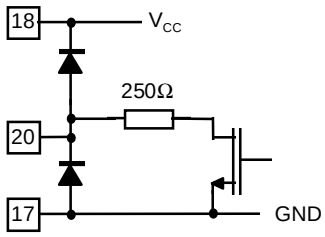
Fig. 24 - Operating Principle of the Out-Of-Lock Detector.

2.7 Functional pin description

DC voltage measurements were made on a demonstration board powered by 5 V analog and digital voltage supplies.

Pin No.	Pin Mnemonic	DC V	Equivalent Circuit
1	FAST	+5	
2 3	CPF CP	- -	
4 14 18 5 7 10 17	V_{DD2} V_{DD1} V_{CC} V_{SS3} V_{SS2} V_{SS1} GND	+5 +5 +5 0 0 0 0	

6	RFI	+4	
8 9	POL PON	+5 +5	
11 12 13	CLK DATA Enot	+5 0 +5	
15 16	XTALA XTALB	+3.5 +3.5	

19	I_{SET}	+1.2	
20	LOCK	+5	

3. Loop Filter Design

3.1 Basic Loop Filter Design Procedure

This section gives the procedure to ensure a quick and simple loop filter design. The method is based on first order approximations, and provides a working solution without the need for computer simulation. Reading appendixes 6.1 and 6.2 can be useful to clarify some PLL terms and equations in this section.

The purpose of a Phase Locked Loop (PLL) frequency synthesizer as shown in Fig. 25 is to transfer the spectral purity and stability of a fixed reference frequency oscillator (TCXO or VTCXO) to that of the Voltage Controlled Oscillator (VCO) for a number of output frequencies.

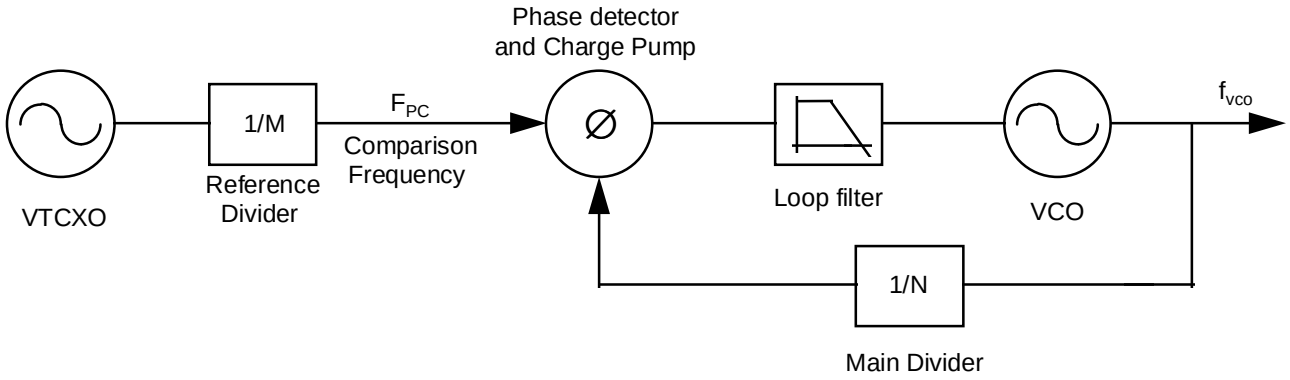
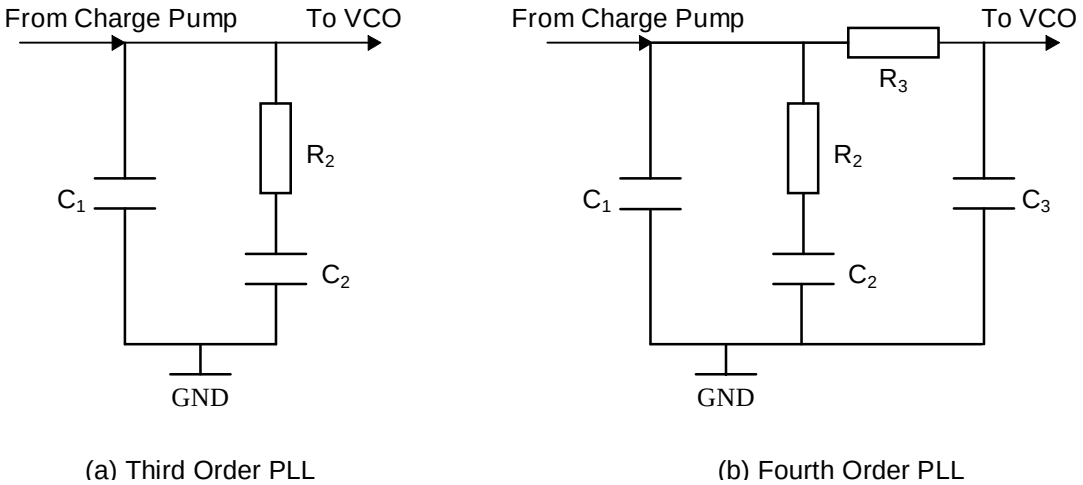


Fig. 25 - Basic Phase Lock Loop Block Diagram.

The correct design of the loop filter is of considerable importance to have the optimum performance from the synthesizer. The filter should be designed so as to achieve the required compromise between noise performance, switching time, comparison frequency spur rejection and modulation requirements.

Loop filters are usually passive when used with current charge pumps, but can be active if desired. Passive loops have the advantage of reduced noise, fewer parts count and low cost. With UMA1021M synthesizer, only passive loop filters are necessary. Two common configurations are shown overleaf. The filters in Fig. 26 are classified in terms of the order of the control loop formed.

With UMA1021M, the use of the loop filter (a) is often sufficient. For applications requiring further comparison frequency breakthrough rejection, a low pass filter stage (R_3, C_3) can be added. This reduces comparison frequency breakthrough spurs without affecting too much the transient response of the loop, with appropriate design.



(a) Third Order PLL (b) Fourth Order PLL

Fig. 26 - Different Types of Passive Loop Filter.

Loop parameters are first chosen:

- f_{VCO}: VCO frequency (in Hz)
- f_{PC}: Phase comparator frequency (in Hz)
- t_s: Switching time (in seconds)
- K_{vco}: VCO gain (in Hz/V)
- I_{CP}: Phase comparator gain (in Amps/cycle)

As a starting point, the equations below are used.

- $$w_n = 2 \times \Pi \times f_n = \sqrt{\frac{K_{VCO} \times I_{CP}}{C_2 \times N}} \quad (1)$$

- $$R_2 = 2 \times \rho \times \sqrt{\frac{N}{K_{VCO} \times I_{CP} \times C_2}} \quad (2)$$

Where f_n is the natural frequency (in Hz) and ρ is the damping coefficient.

☞ Calculate the resistor R_{SET} for setting the charge pump output current from:

$$R_{SET} = \frac{12}{I_{SET}} \quad (3)$$

Charge pump current is related to I_{SET} according to the relationship given in the Table 1 and whether the two charge pumps CP and CPF are connected together or not.

☞ Use rule of thumb to determine the natural frequency f_n based on desired switching time t_s.

$$f_n = \frac{2.5}{t_s} \quad (4)$$

It has been found by experience that a good PLL loop filter design takes a switching time (t_s) of less than $2.5/f_n$ to settle to a new frequency. This rule of thumb allows a good compromise between switching time, stability and noise performance when using the UMA1021M synthesizer. Of course the switching time will also depend on the size of the frequency jump and the definition of when the PLL is settled (i.e. acceptable frequency or phase error with respect to target).

- Determine main divider ratio from:

$$N = \frac{f_{VCO}}{f_{PC}} \quad (5)$$

- Determine angular velocity w_n (in rad/seconds) from:

$$w_n = 2 \times \Pi \times f_n \quad (6)$$

- Determine C_2 from (1)

$$C_2 = \frac{K_{VCO} \times I_{CP}}{w_n^2 \times N} \quad (7)$$

- Select damping ratio of approximately 0.9 for a good compromise between switching time and stability.
- Determine R_2 from (2)
- $$R_2 = 2 \times \rho \sqrt{\frac{N}{K_{VCO} \times I_{CP} \times C_2}} \quad (8)$$
- Choose C_1 between 1/10 and 1/15 the value of C_2
- Determine R_3 from:

$$R_3 \geq 2 \times R_2 \quad (9)$$

- Determine C_3 from:

$$C_3 \leq \frac{R_2 \times C_2}{20 \times R_3} \quad (10)$$

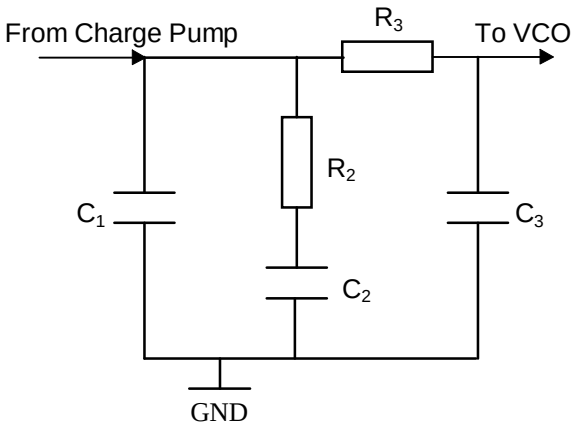
A program using this cook book method has been written for use on IBM PC (and compatibles). It is included with the three wire serial bus control software diskette. Values given by the program are approximate and the final values should be optimised. For further optimisation both computer simulation programs as well as practical experiments are required.

Capacitors with high leakage currents and other undesirable effects such as capacitance value dependant on voltage across dielectric are not preferred because of higher comparison frequency breakthrough and increased switching times. A polyester film capacitor is recommended for C_2. However in many cases high quality NP0 surface mount capacitors are adequate for values up to 100 nF.

3.2 Analysis and Simulation

For detailed analysis, optimisation and worst case design with more complex filters, use of a PLL simulation program may be needed.

Normally a stable loop with an acceptable phase noise performance and a given switching time is required. Unfortunately, these two requirements are in conflict and a compromise must be found. Generally, the optimum compromise between stability and fastest switching time is reached when the phase margin is at its maximum at the open loop gain crossover frequency.



$T_1 = (R_2 \times C_2 \times C_1) / (C_1 + C_2)$; $T_2 = R_2 \times C_2$; $T_3 = R_3 \times C_3$ if $C_2 >> C_1 >> C_3$

Fig. 27 - Third Order Loop Filter.

The phase margin is easily determined from Bode plot. A Bode plot displays the open loop transfer function magnitude and phase. Fig. 28 shows Bode plot of a fourth order loop with third order filter (see Fig. 27) and a pole in the origin due to the VCO.

The phase margin is defined as the different between 180° and the phase of the open loop transfer function at the frequency where the gain is 1 (Gain cross over). The critical point for stability is a phase margin of 0°. The factor by which the system gain would have to be increased for the phase margin to reach the critical value of 0° is called the gain margin.

The time constants in the loop filter are key to controlling the overall loop performance and phase margin. The effect of different time constants can be evaluated from the Bode diagram. The reciprocal of the time constants of the loop filter in Fig. 27 are the breakpoints in the magnitude plot of Fig. 28.

When increasing the time constant $T_3 = C_3 \times R_3$, the breakpoint $(T_3)^{-1}$ will move left and the magnitude curve will start to roll off at a lower frequency. Therefore, the greater the time constant T_3, the better the comparison frequency breakthrough is suppressed. But increasing T_3 will force the point of inflection of the phase margin curve to move to the left as well, this decreasing the phase margin and eventually reducing system stability.

By iteration and inspection of the Bode plot, adjusting the loop filter values and measuring the performance, a compromise between switching time, stability and noise can be reached. Simulation programs may give reasonable approximations of PLL behaviour, but their accuracy is limited due to the fact that many practical imperfections, non linearities and saturation effects are often not taken into account.

Phase margin between 30° and 70° is required for most applications. The larger the phase margin, the more stable the loop, but slower the transient response and hence the switching time. A loop with a low phase margin may still be stable but could exhibit oscillatory problems, associated with undamped loops which also give longer switching times and increased noise. A phase margin of 45° is a good compromise between desired stability and the other generally undesired effects.

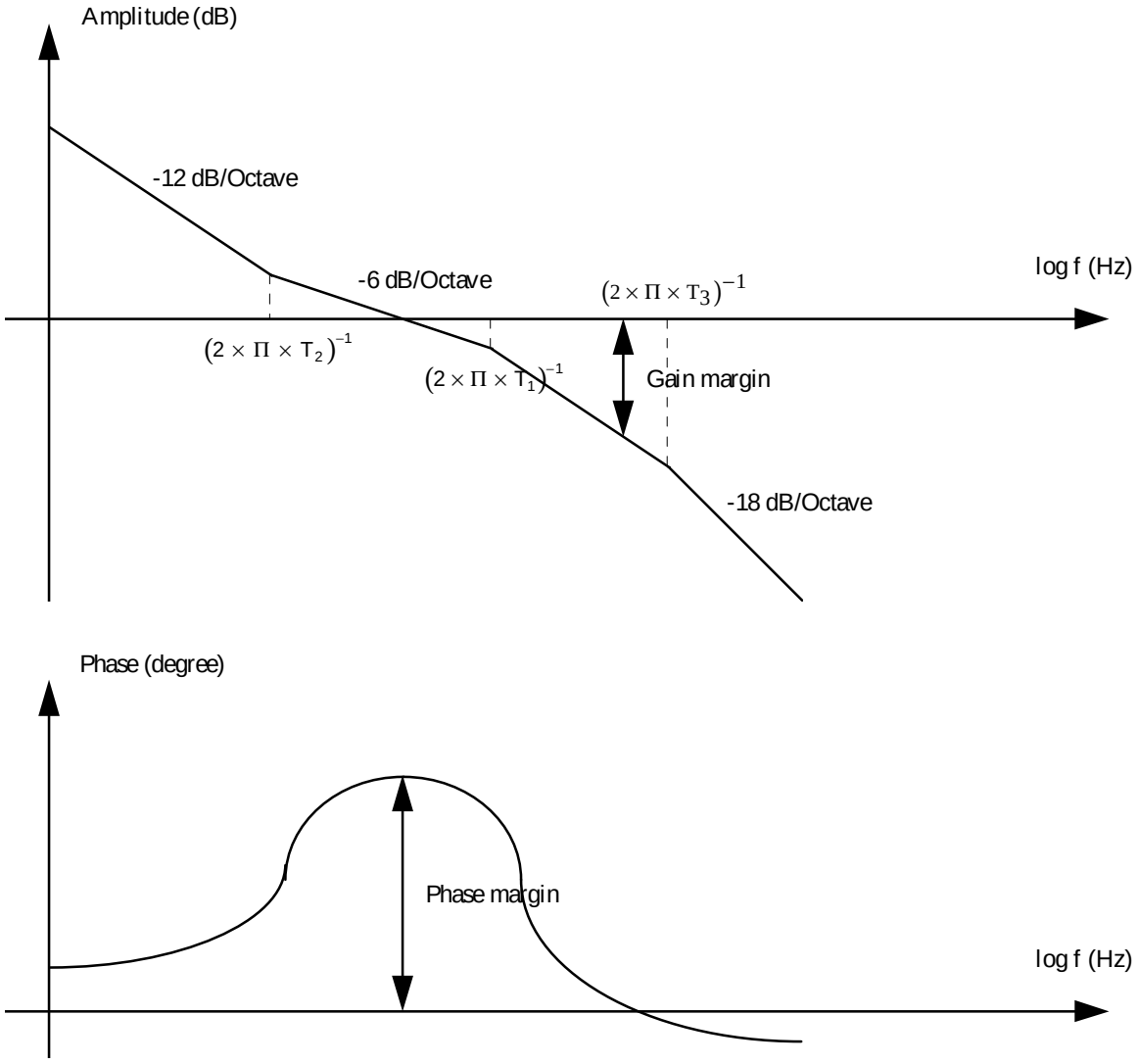


Fig. 28 - Bode Plot 4th Order Open PLL Transfer Function Magnitude and Phase.

3.3 Worked Example

In this section, a design example based on the third order PLL for GSM is shown.

As close in noise is improved by using higher charge pump gains, both charge pumps outputs (pin 2 and 3) are connected together before the loop filter.

Loop parameters relevant to meet the GSM application:

- VCO frequency f_{VCO} = 902 MHz
- Phase comparator frequency f_{PC} = 200 kHz
- Switching time t_s = 600 µs
- VCO gain K_{VCO} = 26 MHz/V
- Phase comparator gain I_{CP} = 3.6 mA/cycle

  R_{SET} = 5.6 kΩ ; With CR1 bit set to 0 and CR0 bit set to 1.

Following the basic design procedure from paragraph 3.1 yields:

I_{CP} = 3.6 mA/cycle = 18 x I_{SET} --> I_{SET} = 200 µA

R_{SET} = 1.2 / I_{SET} = 1.2 / 200 µA ≅ 5.6 kΩ

Natural frequency f_n = 2.5 / t_s = 2.5 / 600 µS = 4170 Hz

Main divider ratio N: f_{VCO} / f_{PC} = 902 MHz / 200 kHz = 4510

The main components in the loop filter are:

☞ Main capacitor $$C_2 = \frac{K_{VCO} \times I_{CP}}{w_n^2 \times N} = \frac{26e6 \times 3.6e-3}{(2 \times \Pi \times 4170)^2 \times 4510}$$

C_2 = 33 nF

☞ Damping resistor $$R_2 = 2 \times \rho \times \sqrt{\frac{N}{K_{VCO} \times I_{CP} \times C_2}} = 2 \times 0.9 \times \sqrt{\frac{4510}{26e6 \times 3.6e-3 \times 33e-9}}$$

R_2 = 2.2 kΩ

☞ Filter capacitor $$\frac{C_2}{15} \le C_1 \le \frac{C_2}{10}$$

C_1 = 220 pF

An extra order (R_3 and C_3) is not needed as UMA1021M charge pump leakage current and comparison frequency breakthrough are very low.

A software simulation program has been used to verify the stability of this loop filter. The phase margin is nearly maximum and equal to 61° at the gain cross over point, the requirement for basic loop stability is fulfilled as shown below.

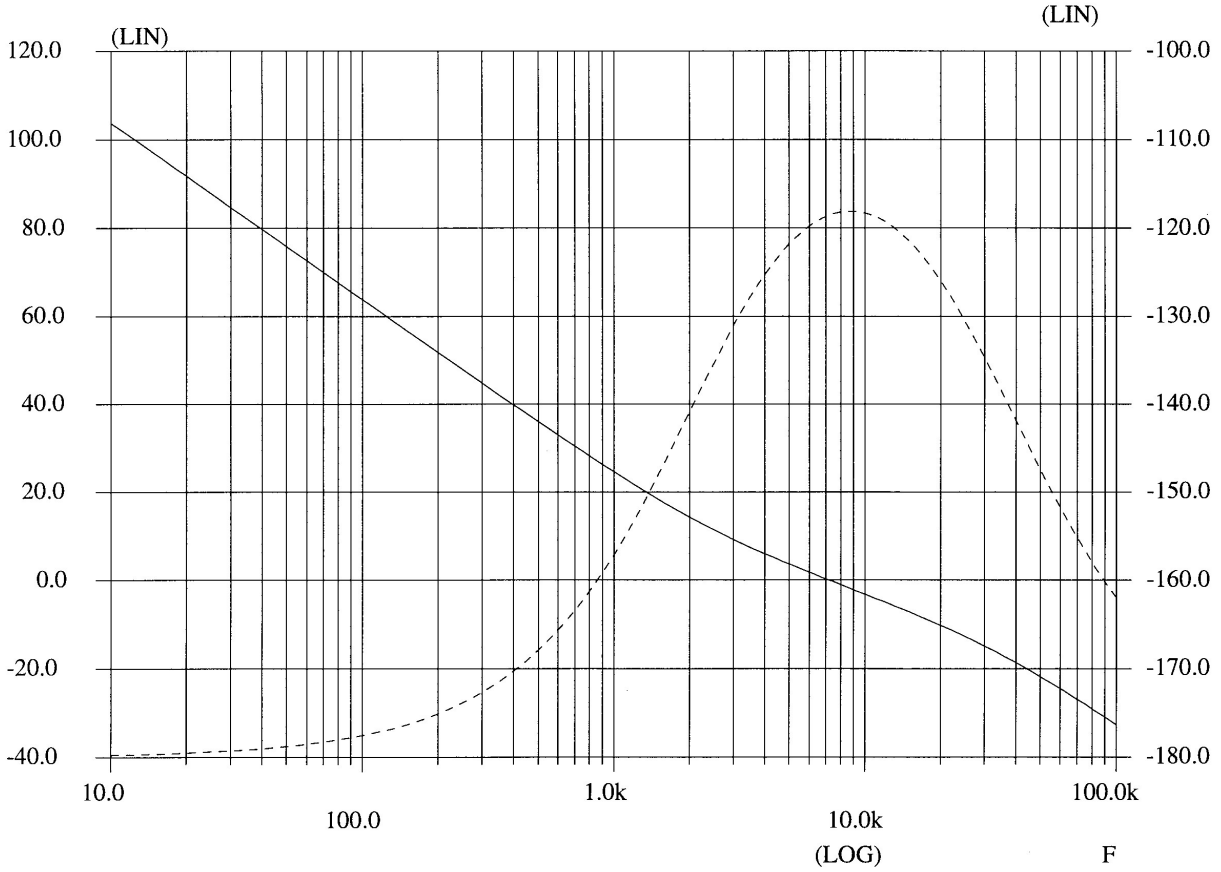


Fig. 29 - Simulated Bode Plot of Open Loop Transfer Function, Magnitude and Phase vs Frequency.

4. Measurements and typical results

Measurements

This section gives the performance of UMA1021M in different applications.

The relevant performance criteria for a synthesizer are usually:

- Close in phase noise / Integrated phase jitter
- Comparison frequency breakthrough
- Switching time

Close in noise was measured using a direct reading from the spectrum analyser and referred to 1 Hz bandwidth. This was done at a specified offset from the carrier whilst still inside the loop bandwidth. It is expressed in dBc/Hz.

Integrated phase jitter was measured on a Rohde and Schwarz Modulation Analyser in a 10 Hz to 200 kHz audio bandwidth. Residual FM (for DAMPS application) was measured using a CCITT filter.

Switching time was measured using a HP 53310A Modulation Domain Analyser (MDA) with option 031. Under the TRIGGER Menu of the MDA, “Triggered”, “Ext Edge” and “Arm Only” were selected. The instrument was setup to accept an external trigger, which was the Enot (Enable) signal used for programming the synthesizer. This signal was connected to the Ext Arm input while the RF signal was fed into the Channel C. The MDA would display the frequency versus time variation of the VCO signal upon the arrival of the Enot rising edge signal.

Table 7 to Table 11 summarise the measurement results. Fig. 30 to Fig. 41 show some of the actual measurements.

Parameters			
Conditions: V_{CC} = V_{DD} = 5 volts ; Temperature = 25°C			
Loop components (Refer to Fig. 27)		C_1 = 2.2 nF C_2 = 33 nF C_3 = NNP*	 R_2 = 2.2 kΩ R_3 = NNP
VCO EX814A ALPS (5V)	VCO gain K_{VCO} VCO frequency f_{VCO} Frequency range	26 MHz/V 902 MHz 864 - 915 MHz	
Comparison frequency f_{PC}		200 kHz	
Charge pump	Current gain I_{CP}	3.6 mA/cycle	
	R_{EXT}	5.6 kΩ	
	Bits CR0, CR1	CR0 = 1 ; CR1 = 0	
Reference frequency: VTCXO TOYOCOM TCO982 (3V)		13 MHz	
Results			
Closed loop bandwidth		7.5 kHz	
Close in noise (at 1 kHz distance from carrier) (see Fig. 30)		-90 dBc/Hz	
Integrated phase jitter	890 MHz 902 MHz 915 MHz	5.8 mrad rms 5.9 mrad rms 5.9 mrad rms	
Comparison frequency breakthrough at 200 kHz (see Fig. 31)		88 dBc	
Switching time to within 1 kHz	890 to 915 MHz (see Fig. 32) 915 to 890 MHz (see Fig. 33)	578 µs 567 µs	

Table 7 - Demoboard Measurement Results on UMA1021M Synthesizer. GSM Application.

(*) NNP Normally Not Populated

Parameters			
Conditions: V_{CC} = V_{DD} = 5 volts ; Temperature = 25°C			
Loop components (Refer to Fig. 27)		C_1 = 1.2 nF C_2 = 18 nF C_3 = 270 pF	 R_2 = 3.3 kΩ R_3 = 8.2 kΩ
VCO URAE8X812A ALPS (5V)	VCO gain K_{VCO} VCO frequency f_{VCO} Frequency range	41 MHz/V 2082 MHz 2070 - 2095 MHz	
Comparison frequency f_{PC}		200 kHz	
Charge pump	Current gain I_{CP}	3.6 mA/cycle	
	R_{EXT}	5.6 kΩ	
	Bits CR0, CR1	CR0 = 1 ; CR1 = 0	
Reference frequency: VTCXO TOYOCOM TCO982 (3V)		13 MHz	
Results			
Closed loop bandwidth		7.5 kHz	
Close in noise (at 1 kHz distance from carrier) (see Fig. 34)		-82.5 dBc/Hz	
Integrated phase jitter	2070 MHz 2082 MHz 2095 MHz	15.8 mrad rms 16 mrad rms 15.9 mrad rms	
Comparison frequency breakthrough at 200 kHz (see Fig. 35)		75 dBc	
Switching time to within 1 kHz	2070 to 2095 MHz 2095 to 2070 MHz	550 µs 550 µs	

Table 8 - Demoboard Measurement Results on UMA1021M Synthesizer. DCS1800 Application.

Parameters			
Conditions: V_{CC} = V_{DD} = 3 volts ; Temperature = 25°C			
Loop components (Refer to Fig. 27)		C_1 = 1.2 nF C_2 = 18 nF C_3 = NNP	 R_2 = 2.7 kΩ R_3 = NNP
VCO URAP8x431A ALPS (2.8V)	VCO gain K_{VCO} VCO frequency f_{VCO} Frequency range	40 MHz/V 1668 MHz 1662 - 1674 MHz	
Comparison frequency f_{PC}		300 kHz	
Charge pump	Current gain I_{CP}	3.6 mA/cycle	
	R_{EXT}	5.6 kΩ	
	Bits CR0, CR1	CR0 = 1 ; CR1 = 0	
Reference frequency: VTCXO TOYOCOM TCO982		19.2 MHz	
Results			
Closed loop bandwidth		13 kHz	
Close in noise (at 1 kHz distance from carrier) (see Fig. 36)		-86 dBc/Hz	
Integrated phase jitter	1662 MHz 1668 MHz 1674 MHz	11.6 mrad rms 11.6 mrad rms 11.5 mrad rms	
Comparison frequency breakthrough at 300 kHz (see Fig. 37)		79 dBc	
Switching time to within 1 kHz	1662 to 1674 MHz 1674 to 1662 MHz	320 µs 315 µs	

Table 9 - Demoboard Measurement Results on UMA1021M Synthesizer. PHS Application.

Parameters			
Conditions: V_{CC} = V_{DD} = 3 volts ; Temperature = 25°C			
Loop components (Refer to Fig. 27)		C_1 = 680 pF C_2 = 10 nF C_3 = NNP	 R_2 = 2.2 kΩ R_3 = NNP
VCO URAEX845 ALPS (3V)	VCO gain K_{VCO} VCO frequency f_{VCO} Frequency range	20 MHz/V 1890 MHz 1880 - 1890 MHz	
Comparison frequency f_{PC}		1728 kHz	
Charge pump	Current gain I_{CP}	3.6 mA/cycle	
	R_{EXT}	5.6 kΩ	
	Bits CR0, CR1	CR0 = 1 ; CR1 = 0	
Reference frequency: Frequency Generator SMHU (R&S)		13.824 MHz	
Results			
Closed loop bandwidth		26 kHz	
Close in noise (at 2 kHz distance from carrier) (see Fig. 38)		-92 dBc/Hz	
Integrated phase jitter	1881.792 MHz 1890.432 MHz 1897.344 MHz	5.8 mrad rms 6.1 mrad rms 5.9 mrad rms	
Comparison frequency breakthrough at 1728 kHz (see Fig. 39)		79 dBc	
Switching time to within 1 kHz	1881.792 to 1897.344 MHz 1897.344 to 1881.792 MHz	170 µs 170 µs	

Table 10 - Demoboard Measurement Results on UMA1021M Synthesizer. DECT Application.

Parameters			
Conditions: V_{CC} = V_{DD} = 5 volts ; Temperature = 25°C			
Loop components (Refer to Fig. 27)		C_1 = 1.5 nF C_2 = 22 nF C_3 = NNP	 R_2 = 10 kΩ R_3 = NNP
VCO MQE001 MURATA (4.2V)	VCO gain K_{VCO} VCO frequency f_{VCO} Frequency range	11 MHz/V 836 MHz 824 - 849 MHz	
Comparison frequency f_{PC}		30 kHz	
Charge pump	Current gain I_{CP}	3.6 mA/cycle	
	R_{EXT}	5.6 kΩ	
	Bits CR0, CR1	CR0 = 1 ; CR1 = 0	
Reference frequency: VTCXO TOYOCOM 982P (3V)		15.36 MHz	
Results			
Closed loop bandwidth		4 kHz	
Close in noise (at 1 kHz distance from carrier) (see Fig. 40)		-81.4 dBc/Hz	
Integrated phase jitter FM demodulation ; CCITT filter	824 MHz 836 MHz 849 MHz	8.5 Hz rms 8.6 Hz rms 8.6 Hz rms	
Comparison frequency breakthrough at 30 kHz (see Fig. 41)		75 dBc	
Switching time to within 2.5 kHz	824 to 849 MHz 849 to 824 MHz	2.05 ms 1.98 ms	

Table 11 - Demoboard Measurement Results on UMA1021M Synthesizer. DAMPS Application.

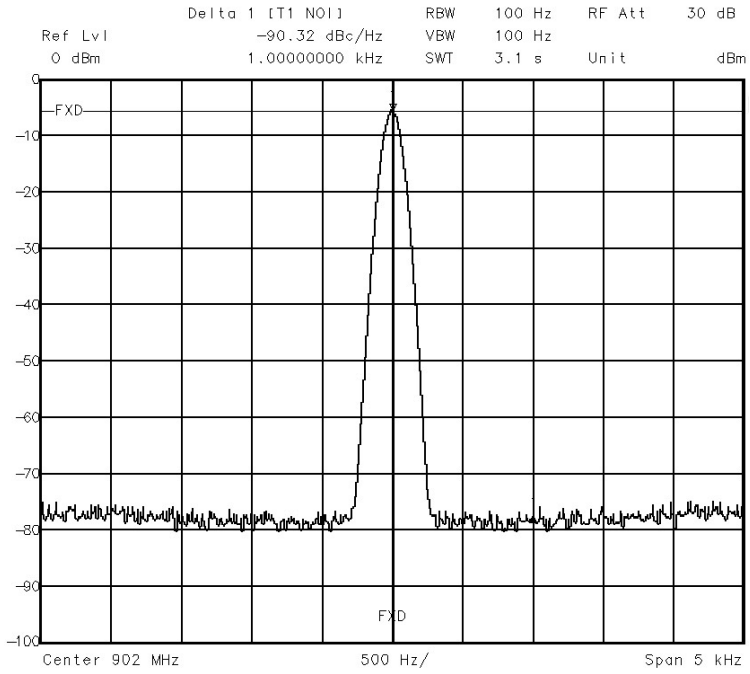


Fig. 30 - UMA1021M Synthesizer Output Spectrum - Close in Noise (GSM Application).

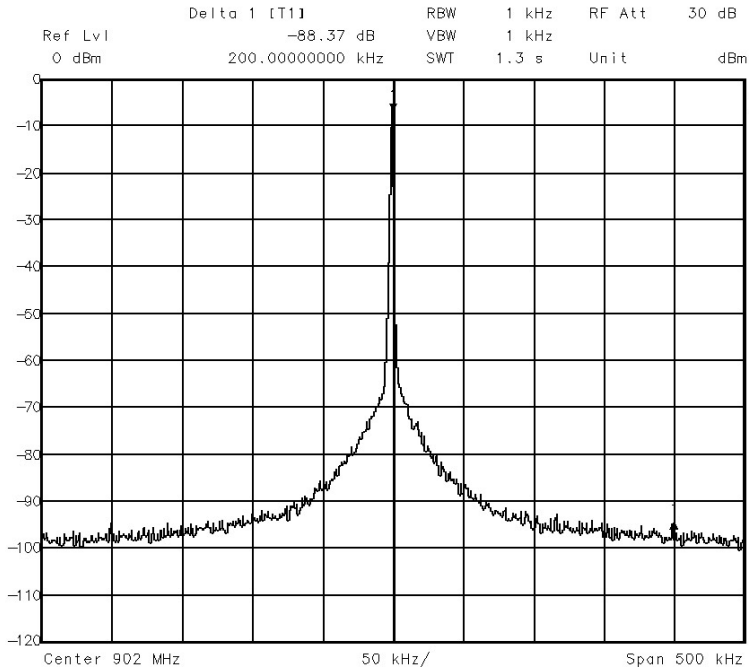


Fig. 31 - UMA1021M Synthesizer - Comparison Frequency Breakthrough (GSM Application).

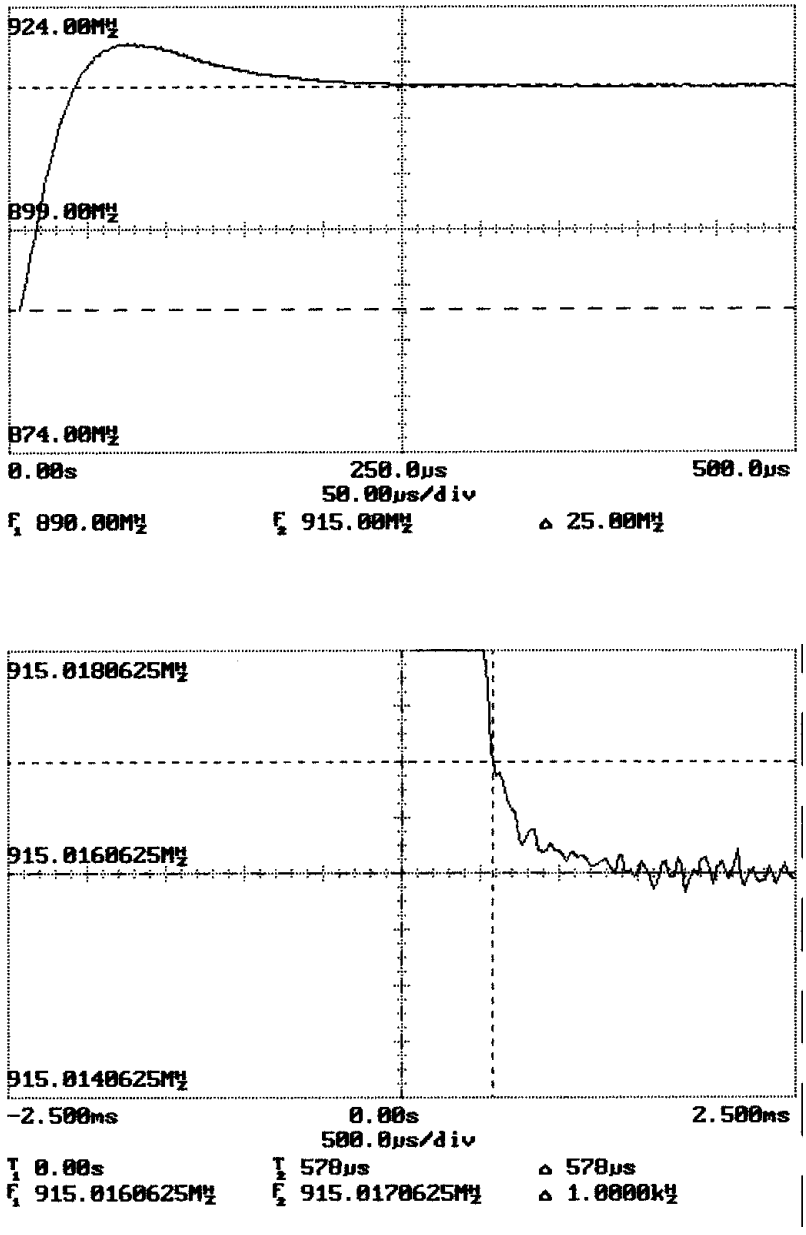
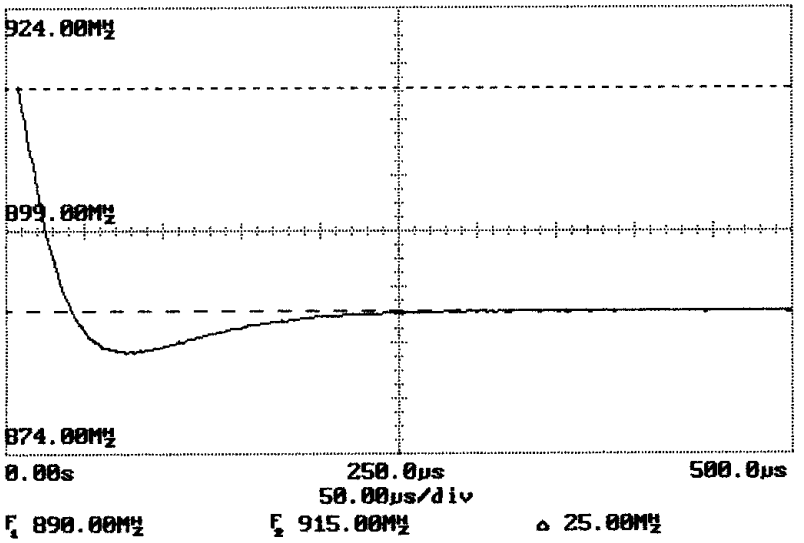


Fig. 32- Settling Time (890 to 915 MHz Step to Within 1 kHz).



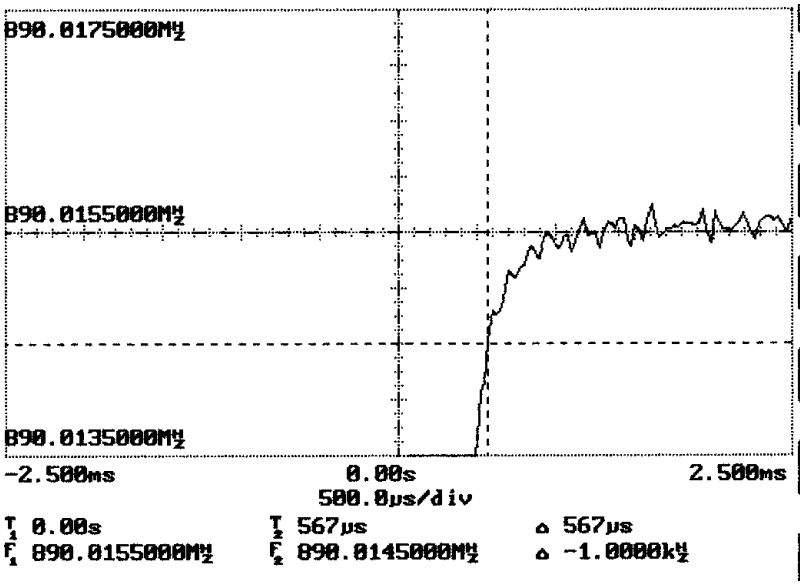


Fig. 33- Settling time (915 to 890 MHz Step to Within 1 kHz).

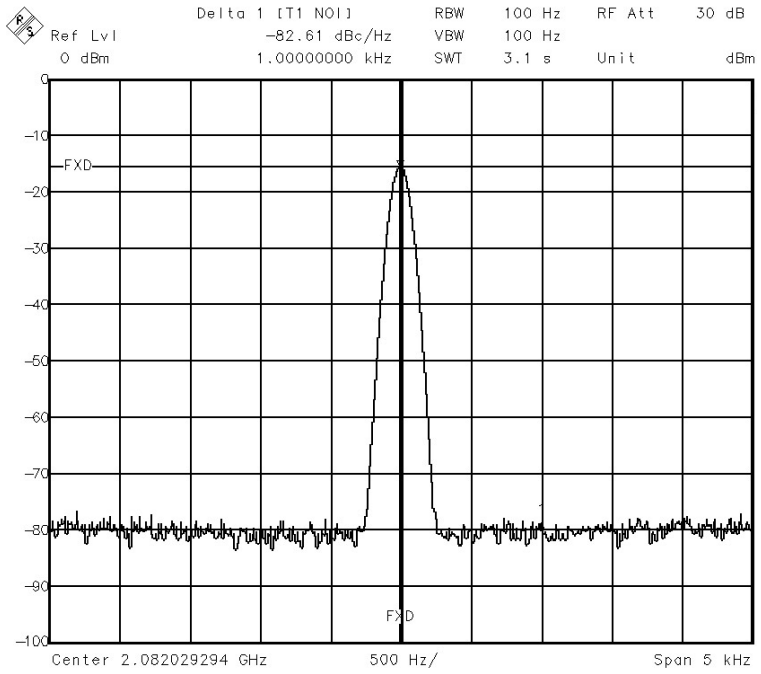


Fig. 34 - UMA1021M Synthesizer Output - Close in Noise (DCS Application).

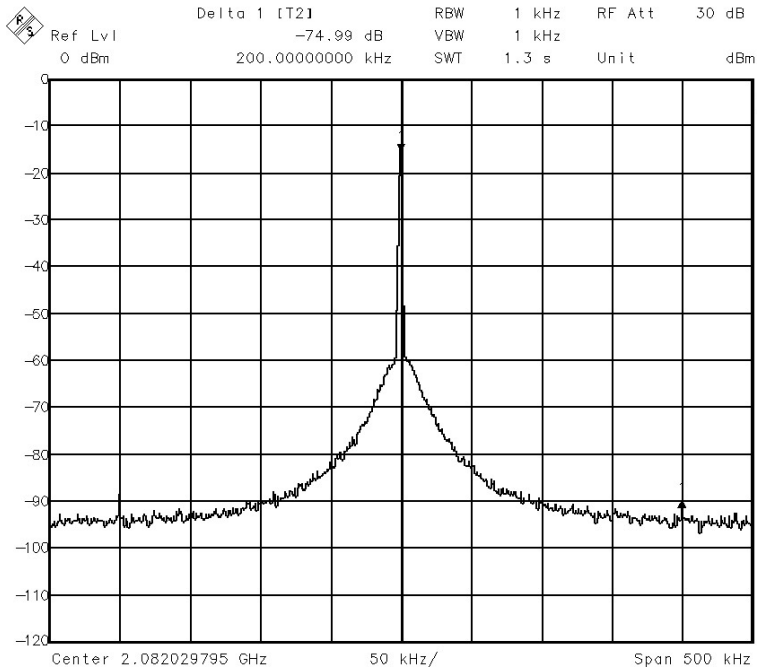


Fig. 35 - UMA1021M Synthesizer - Comparison Frequency Breakthrough (DCS Application).

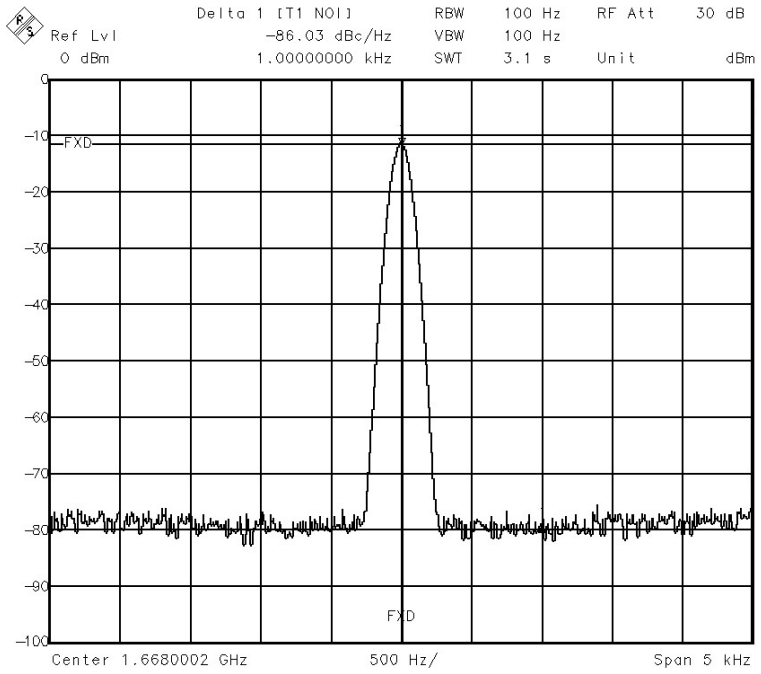


Fig. 36 - UMA1021M Synthesizer Output - Close in Noise (PHS Application).

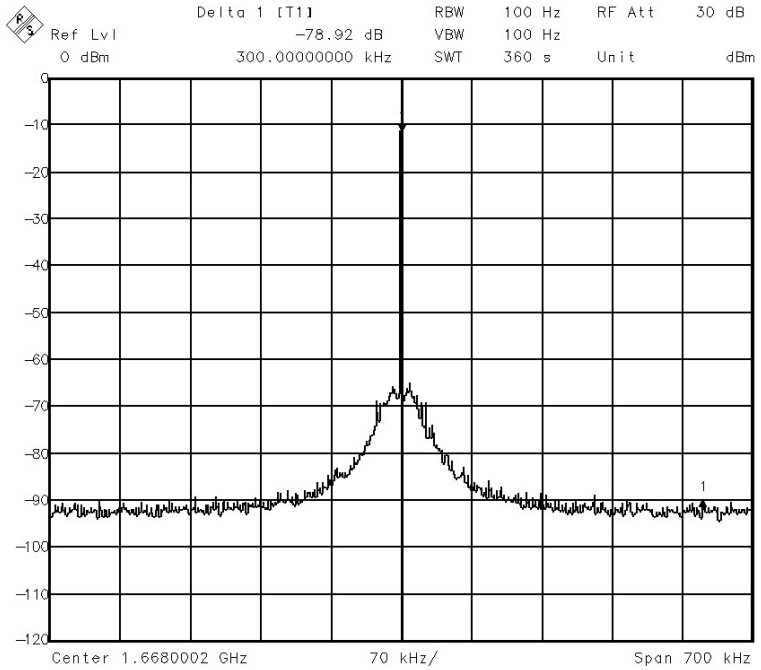


Fig. 37 - UMA1021M Synthesizer - Comparison Frequency Breakthrough (PHS Application).

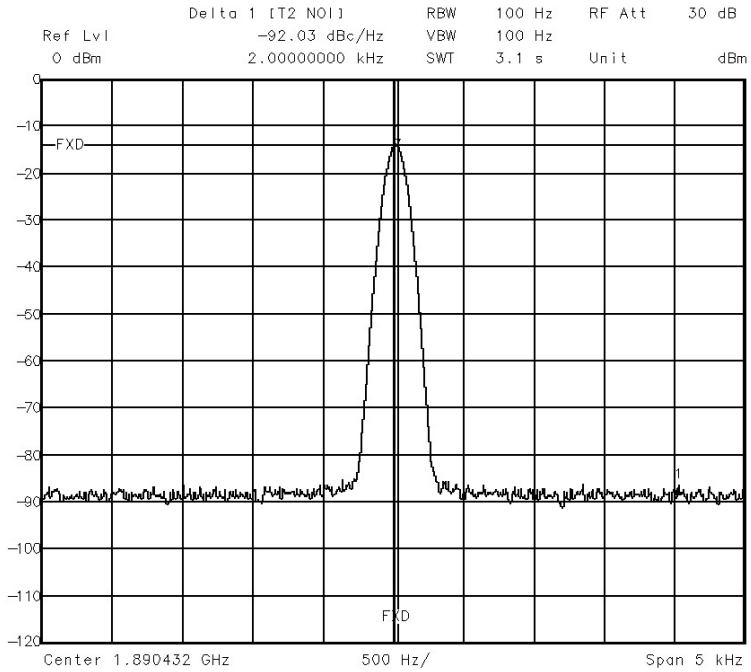


Fig. 38 - UMA1021M Synthesizer Output - Close in Noise (DECT Application).

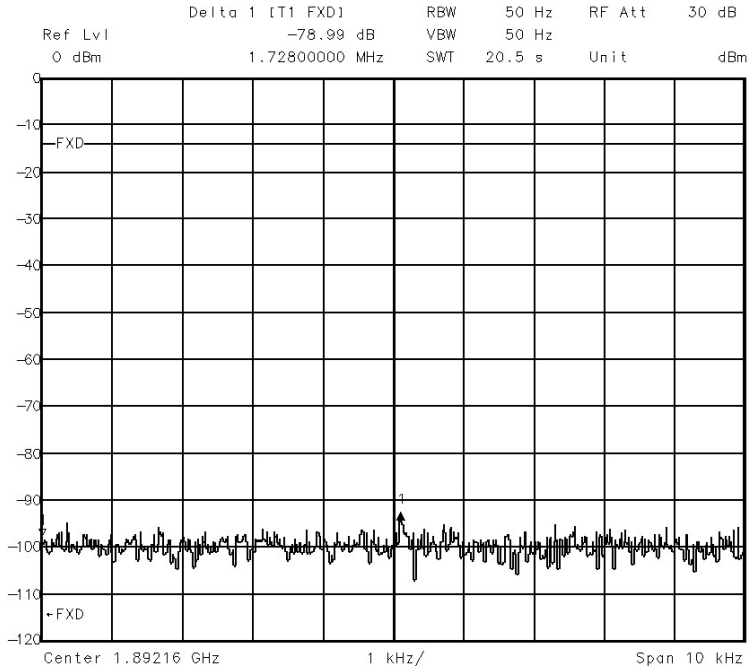


Fig. 39 - UMA1021M Synthesizer - Comparison Frequency Breakthrough (DECT Application).

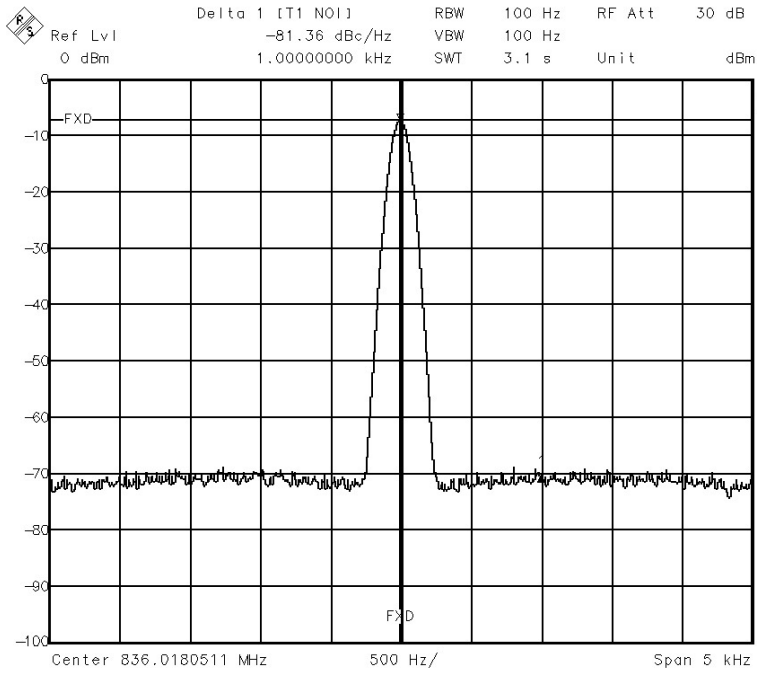


Fig. 40 - UMA1021M Synthesizer Output - Close in Noise (DAMPS Application).

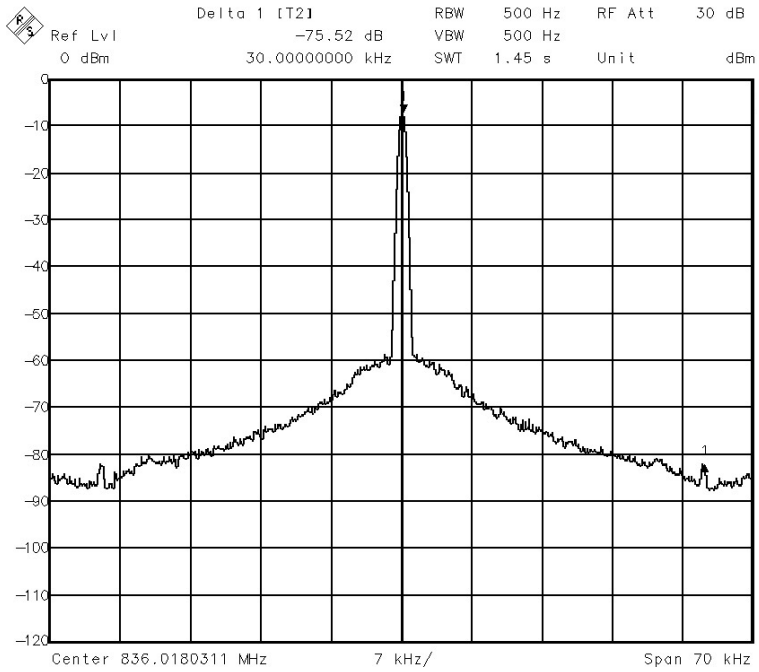


Fig. 41 - UMA1021M Synthesizer - Comparison Frequency Breakthrough (DAMPS Application).

5. Frequently Asked Questions

Question 1: How can the synthesizer noise be improved?

Answer: Five things can be done to improve the synthesizer noise.

1/ Use a higher crystal frequency. Doubling the reference frequency can improve the close in noise by 3 dBc/Hz.

2/ With a VTCXO as the reference frequency, use the pin XTALA as input and decouple to ground the pin XTALB (see explanations next question).

3/ Use the bigger charge pump current. In a typical GSM application, a difference of 7 dB has been measured between the lowest charge pump current (0.2 mA) and the biggest (3.6 mA). It is also recommended to use the lowest external resistor (5.6 kΩ), in order that the charge pump works with the highest current density.

4/ Use a narrower loop filter. But this increases the switching time.

5/ Ensure that the supply is well decoupled.

Number 4 does not improve the close in noise, just the total phase noise. Other points can improve the close in noise and also the total phase noise of the PLL.

Question 2: Do you recommend the use of a particular reference input (XTALA or XTALB)?

Answer: The pin XTALA (and so the reference divider) is driven by the rising edge of the reference signal, whilst the pin XTALB is driven by the falling edge.

Since this signal is the reference in term of frequency but also purity, the reference input must be chosen according to the phase jitter of the edge. The better the phase jitter of the reference edge, the better will be the total close in noise (in the loop bandwidth).

Normally with a VTCXO the rising edge has a better jitter than the falling edge. So we recommend to use the pin XTALA with such a VTCXO.

Question 3: What is the phase detector gain? Is it charge pump output current divided by 2π or just the charge pump output current, itself?

Answer: The phase detector gain is equal to the charge pump output current I_{CP} divided by 2π since the phase detector covers 2π range. However, when using the design formulas, the phase detector gain be replaced directly by I_{CP} (or $I_{CP} + I_{CPF}$ if both charge pumps are enabled) because the 2π factor will be cancelled out by the 2π also in the VCO gain, when given in Hz/volt.

Question 4: What kind of main capacitor should be used in the loop filter?

Answer: Higher leakage current raises comparison frequency breakthrough and the memory effect of some dielectric (COG, X7R series) or, worse, electrolytic types can degrade the settling time. A polyester film capacitor is recommended for the main capacitor of the loop filter.

Question 5: How to use the synthesizer with V_{DD} < 4.5 V whereas DATA, CLK and Enot signals are at 5 V logic?

Answer: Because of protection against electrostatic discharge (see section 2.7), the input voltage for these logic pins can not be greater than V_{DD} + 0.3 V. An interface between the microcontroller and the synthesizer is then needed to reduce voltage at serial bus pins. A voltage divider using two resistors is a simple and cheap solution to implement.

The design of this interface involves performance compromise between the current consumption and the programming speed, which depend on the resistor values in the voltage divider and the parasitic capacitance from the demonstration board.

Question 6: Can UMA1021M be used in open loop modulation?

Answer: Two methods of open loop modulation are briefly described.

☞ Method 1: Only the fast charge pump is used, and it is enabled/disabled using the pin FAST. The slow charge pump (pin CP) is grounded. An internal circuit synchronises the FAST signal with the fast charge pump correction current pulses. This avoids opening the loop when the fast charge pump is still active, which could cause a frequency drift. After the loop is opened, the UMA1021M synthesizer can then be powered down to reduce consumption.

Some precautions must be taken when the fast charge pump is switched off. A parasitic capacitance, due to the integrated circuit and the printed circuit, exists between the FAST and CPF pin. When the signal is sent to the FAST pin, a coupling through the parasitic capacitance results in a VCO frequency shift. This problem can be solved by decreasing the slope of the FAST signal with an RC filter.

The loop parameters indicated in Table 10 have been used for following open loop measurements. Fig. 42 shows a frequency drift of less than 800 Hz when the fast charge pump is switched off in a typical DECT application.

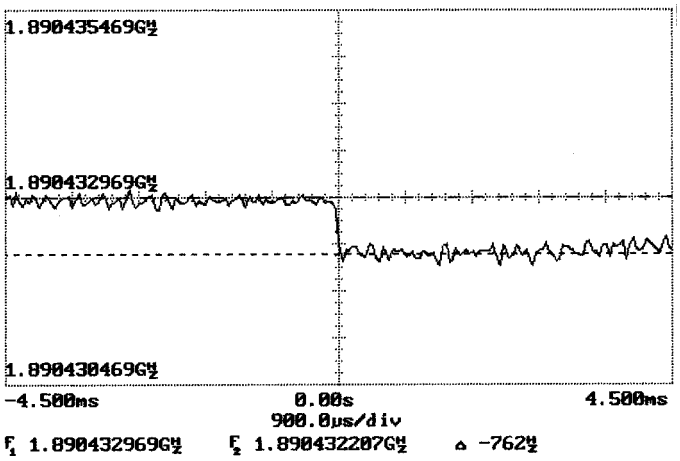


Fig. 42 - Open Loop Modulation: the Fast Charge Pump is Switched Off.

☞ Method 2: The loop is opened by powering down (PON pin) the principal synthesizer directly. The signal sent to the PON is also internally synchronised with the charge pumps to avoid powering down the synthesizer whilst they are still active. This method has additional advantage of reducing the synthesizer current consumption to nearly zero.

Two problems can occur when a synthesizer is powered down.

- The first is known as “Load Pulling”. When the synthesizer is switched off, its RF input impedance may change and then an unintended jump in frequency is possible, if the VCO is susceptible to load changes. This problem is negligible with the UMA1021M synthesizer (see Fig. 43).
- The second problem is called “Pushing”. The frequency of the VCO moves with changes in its supply voltage. When the principal synthesizer is powered down, it may temporally affect the supply voltage. Proper supply decoupling will attenuate it.

Fig. 43 shows a frequency jump of less than 500 Hz and a frequency drift of less than 600 Hz when the synthesizer is powered down in a DECT application.

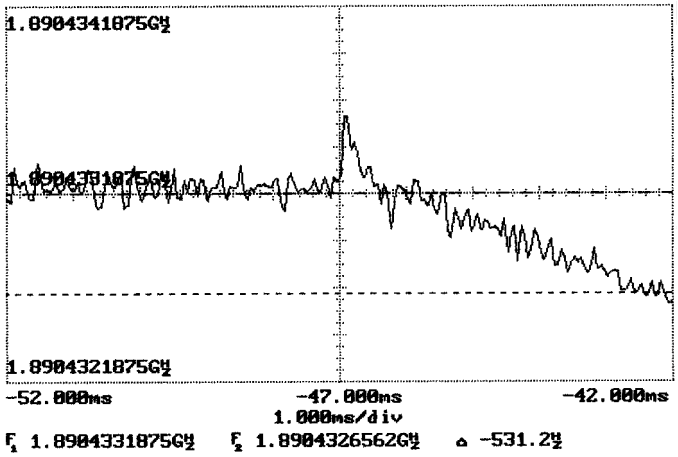


Fig. 43 - Open Loop Modulation: the Synthesizer is Powered Down.

Question 7: Can I anticipate the close in noise with any application?

Answer: Different experiments show that when using the UMA1021M, the main divider follows a 20log(N) (6 dB/octave) slope (i.e. when doubling the RF, you degrade the close in noise by 6 dB), whilst with the reference divider the noise floor is seen to follow a 10log(N) (3 dB/octave) slope.

The expected close in noise of any application can be extrapolated from the results of the GSM application (RF = 902 MHz, F_{CP} = 200 kHz, close in noise = -90 dBc/Hz) with the following rule:

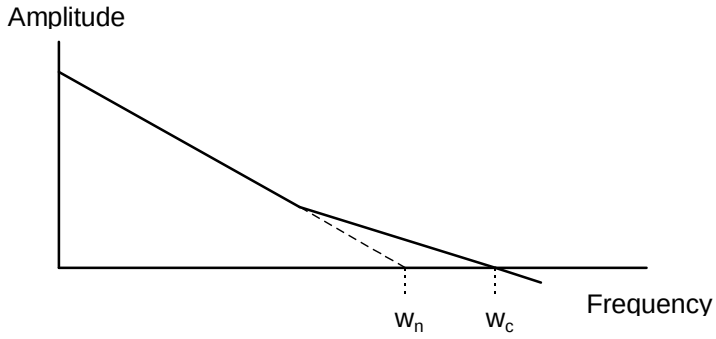
$$\text{Close in Noise (expected)} = -90\text{dBc/Hz} + 20\log\left(\frac{\text{RF}}{902\text{MHz}}\right) - 10\log\left(\frac{F_{CP}}{200\text{kHz}}\right)$$

6. Appendixes

6.1 PLL terms

The following is a brief glossary of frequently encountered terms in the PLL literature.

- **Natural frequency w_n**: the natural frequency of the loop. This is the frequency at which the loop would theoretically oscillate if the damping factor was zero.
- **Open loop cross-over frequency w_c**: this is the frequency at which the open loop gain is unity. It is useful in determining the phase margin and hence the stability.



- **Damping coefficient**: ρ can be used as a measure of the stability in second order systems. It is seldom used as a direct measure of stability in higher order designs.
- **Order of the loop**: the order of the loop is the highest power of s (s=jw) in the denominator of the open loop transfer function. The example, below, shows a second order loop.

$$G(s) \times H(s) = (K_{VCO} \times I_{CP}) \times \frac{(s \times \tau_2 + 1)}{(N \times C \times s^2)}$$

- **Type of the loop**: the type of control system formed is defined by the number of perfect integrators in the loop. In the example, above, the loop is a type two system.
- **Phase margin Φm**: the phase margin, in degrees, is expressed as $\Phi m = \Phi(w_c)+180$ where $\Phi(w_c)$ is the open loop phase shift at the frequency w_c.
- **SSB phase noise or close in noise**: it is the noise level within the loop bandwidth relative to carrier at a given frequency offset. It is referred to a 1 Hz bandwidth. It is expressed in dBc/Hz.
- **Integrated phase jitter or residual FM**: this is another measure of the noise performance of a signal source. This measure of integrated noise is usually specified over a particular audio bandwidth, e.g. 10 Hz to 200 kHz. It is expressed in degrees rms. An ideal synthesizer would have zero integrated phase jitter.
- **Spurious**: this defines the spectral purity of the oscillator. Common sources of spurious are the comparison frequency and harmonics. Comparison frequency breakthrough is generated by leakage in the loop filter components, VCO variable capacitor, printed circuit or the charge pump.
- **Settling time or switching time**: this indicates the time for a given frequency jump to be within a specified distance (frequency or phase) from target value.

6.2 Basic PLL transfer function

Fig. 44 shows the block diagram of a basic control loop.

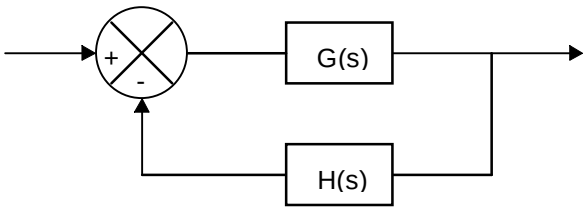


Fig. 44 - Block Diagram of a Loop.

In open loop, the transfer function is $H(s) \times G(s)$ (a)

In closed loop, the transfer function is $\frac{G(s)}{1+(G(s)+H(s))}$ (b)

If we apply these transfer functions to the phase loop in Fig. 45, with equations expressed in Laplace notation.

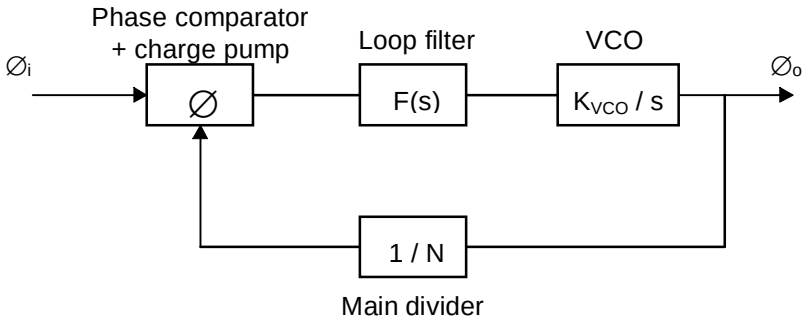


Fig. 45 - Block Diagram of a Phase Locked Loop.

$$G(s) = \frac{I_{CP} \times K_{VCO} \times F(s)}{s} \quad \text{(c)}$$

$$H(s) = \frac{1}{N} \quad \text{(d)}$$

The PLL open loop transfer function is $\frac{I_{CP} \times K_{VCO} \times F(s)}{s \times N}$ (e)

The PLL closed loop transfer function is

$$\frac{\phi_o(s)}{\phi_i(s)} = \frac{K_{VCO} \times I_{CP} \times F(s)/s}{1+\frac{K_{VCO} \times I_{CP} \times F(s)}{s \times N}} = \frac{N \times K_{VCO} \times I_{CP} \times F(s)}{(s \times N)+(K_{VCO} \times I_{CP} \times F(s))} \quad \text{(f)}$$

Basic performance of PLL is determined by R_2 and C_2 (see Fig. 27) in the loop filter.

Note: When introducing more components in the loop filter, the expression for the transfer function becomes a lot more complicated. Anyway, this design can serve as a starting point for even more complicated loop filters.

The transfer function of this simple second order loop filter is

$$F(s) = R_2 + (\frac{1}{s \times C_2}) = \left[\frac{(s \times R_2 \times C_2) + 1}{s \times C_2}\right] \quad \text{(g)}$$

Then the closed transfer function is

$$\frac{\phi_o(s)}{\phi_i(s)} = \frac{N \times K_{VCO} \times I_{CP} \times F(s)}{(s \times N) + (K_{VCO} \times I_{CP} \times F(s))} = \frac{N \times K_{VCO} \times I_{CP} \times \frac{(s \times R_2 \times C_2) + 1}{s \times C_2}}{(s \times N) + (K_{VCO} \times I_{CP} \times \frac{(s \times R_2 \times C_2) + 1}{s \times C_2})}$$

$$= \frac{N \times ((s \times R_2 \times C_2) + 1))}{\frac{s^2 \times C_2 \times N}{K_{VCO} \times I_{CP}} + (s \times R_2 \times C_2) + 1} \quad \text{(h)}$$

If we compare the denominator of (h) with $\frac{s^2}{w_n^2} + \frac{2 \times \rho \times s}{w_n} + 1$

We find the equations shown below:

$$w_n = \sqrt{\left(\frac{K_{VCO} \times I_{CP}}{C_2 \times N}\right)} \quad \text{(i)} \Rightarrow \text{(1)}$$

$$\rho = \frac{w_n \times R_2 \times C_2}{2} \quad \text{(j)}$$

$$R_2 = 2 \times \rho \times \sqrt{\frac{N}{K_{VCO} \times I_{CP} \times C_2}} \quad \text{(k)} \Rightarrow \text{(2)}$$

6.3 Demonstration board documentation: Guidance for assembly and operation

The demonstration board is an universal tool to demonstrate and evaluate the UMA1021M under various conditions.

Together, with the Philips 3-Wire bus and the UMA1021M demonstration software, a quick and easy start to evaluation is provided. The enclosed part list corresponds to a GSM application. However, the demoboard may easily be configured for other digital cellular or cordless systems like DCS1800, PHS, etc...

We hope that you will find no problems in realising the evaluation set-up and will come quickly to an application that fits perfectly to your needs.

Assembly

Assembly is done according to the documentation which comes with the demonstration board. Please note that the board may be assembled with VCO's of different style. The existing version of the board can hold surface mount VCO's (e.g. ALPS URAX8, Murata MQE001 type). Since the VCO and the VTCXO use a common on-board supply rail, it is recommended to select both components with the same supply voltage specification.

The loop filter design depends on the system requirements and the VCO's used. A loop filter calculation program has been written for use on IBM PC. It is included with the three wire bus control software diskette (« Tool|Calculate filter » menu option). It uses the same cook book method as described on the paragraph 3.1.

The supplied circuit diagram corresponds to a typical GSM system. A VCO sensitivity of about 26 MHz/V and a typical comparison frequency of 200 kHz have been assumed. The charge pump current has been selected to 3.6 mA (CR1 bit set to 0, CR0 bit set to 1). The loop filter is the one calculated in the worked example. The parameters and measurement results are summarised in section 4 (Table 7 and Fig. 30 to Fig. 33).

Board configuration

Two regulators allow the analog supply (V_{CC}) and the digital voltage (V_{DD}) to be supplied independently. The VCO and the VTCXO are supplied by the analog voltage.

The digital input POL allows to select the polarity of power on inputs, POL is grounded for power on to be active low and POL is supplied to V_{DD} for power on to be active high. The demonstration board is configured with the latter.

A VTCXO or an external generator can be used as the reference. On the demonstration board, The VTCXO drives the reference divider via the pin 16. If an external generator is used, the resistor R18 must be removed and the resistor R19 grounded with a 10 kΩ value.

Getting started

1. Connect the Philips 3-wire interface board to the serial printer port (LPT1) of your PC. Copy the two files (BUS3WIRE.WB and BUS3WIRE.EXE) onto your hard disk or run the software from the disk. Type BUS3WIRE to start. Select UMA1021M option in the DEVICE TYPE menu. Verify that the displayed window is well configured as you wish.
2. Connect the interface card with the UMA1021M demonstration board.
3. Connect the board to a 7.5V well regulated and low noise power supply.
4. The UMA1021M demonstration board is operational now and the PLL should be locked.
5. Start your synthesizer evaluation...

If you need assistance or do have any questions or comments don't hesitate to call your local Philips Semiconductors representative.

Ref.	Value/Type	Size	Ref.	Value/Type	Size
R1	100 kΩ	0805 SMD	C1	2.2 nF	0805 SMD
R2	0 Ω	0805 SMD	C2	NNP	0805 SMD
R3	2.2 kΩ	0805 SMD	C3	33 nF	0805 SMD
R4	0 Ω	0805 SMD	C4	NNP	0805 SMD
R5	12 Ω	0805 SMD	C5	4.7µ/10V	Tant. chip cap.
R6	12 Ω	0805 SMD	C6	100 nF	0805 SMD
R7	18 Ω	0805 SMD	C7	100 pF	0805 SMD
R8	18 Ω	0805 SMD	C8	100 nF	0805 SMD
R9	18 Ω	0805 SMD	C9	56 pF	0805 SMD
R10	56 Ω	0805 SMD	C10	56 pF	0805 SMD
R11	100 k Ω	0805 SMD	C11	33 pF	0805 SMD
R12	NNP (*)	0805 SMD	C12	33 pF	0805 SMD
R13	100 k Ω	0805 SMD	C13	33 pF	0805 SMD
R14	12 Ω	0805 SMD	C14	100 pF	0805 SMD
R15	12 Ω	0805 SMD	C15	100 nF	0805 SMD
R16	12 Ω	0805 SMD	C16	1 nF	0805 SMD
R17	12 Ω	0805 SMD	C17	1 nF	0805 SMD
R18	10 k Ω	0805 SMD	C18	4.7 µF / 10 V	Tant. chip cap.
R19	NNP	0805 SMD	C19	100 nF	0805 SMD
R20	1.5 k Ω	0805 SMD	C20	22 pF	0805 SMD
R21	10 k Ω	0805 SMD	C21	100 pF	0805 SMD
R22	10 k Ω	0805 SMD	C22	100 nF	0805 SMD
R23	5.6 k Ω	0805 SMD	C23	100 nF	0805 SMD
R24	100 k Ω	0805 SMD	C24	4.7 µF / 10 V	Tant. chip cap.
R25	4.7 k Ω	0805 SMD	C25	4.7 µF / 10 V	Tant. chip cap
R26	1.5 k Ω	0805 SMD	C26	100 nF	0805 SMD
R27	4.7 k Ω	0805 SMD	C27	4.7 µF / 10 V	Tant. chip cap
R28	1.5 k Ω	0805 SMD	IC1	UMA1021M	SSOP20
R29	12 Ω	0805 SMD	IC2	LM317LZ	TO92
XTAL	13 MHz	TOYOCOM	IC3	LM317LZ	TO92
VCO	URAE8X814A	ALPS			

Table 12 - Part List for UMA1021M Demonstration Board (GSM Application).

(*) NNP: Not Normally Populated

X1: Out of lock detector

X2: RF output 50Ω

X3: 3-Wire Bus Control

X4: External reference input

X5: Supply

J1: activates fast charge pump

J2: controls power down for the synthesizer

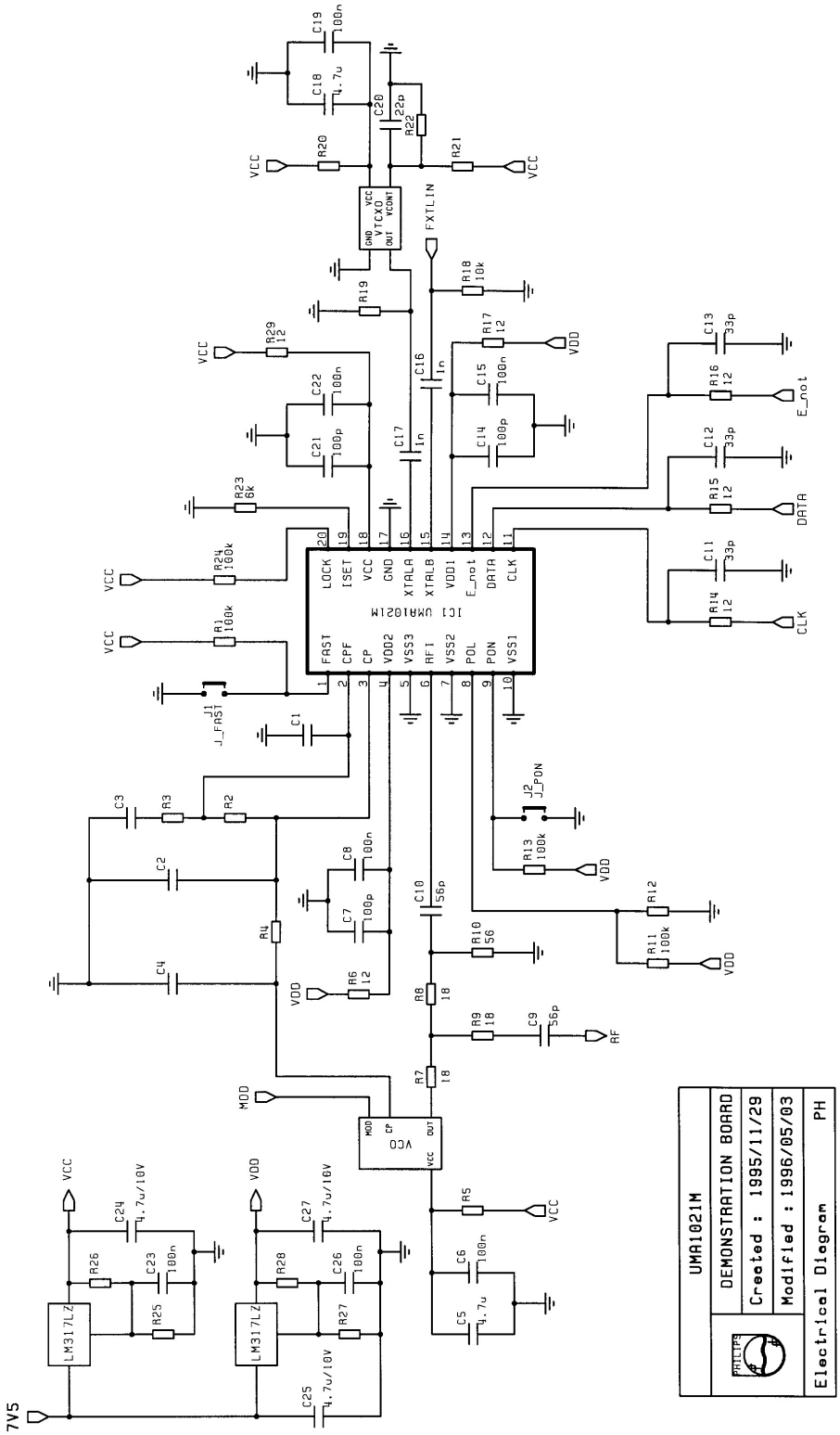


Fig. 46 - Demonstration Board Circuit Diagram.

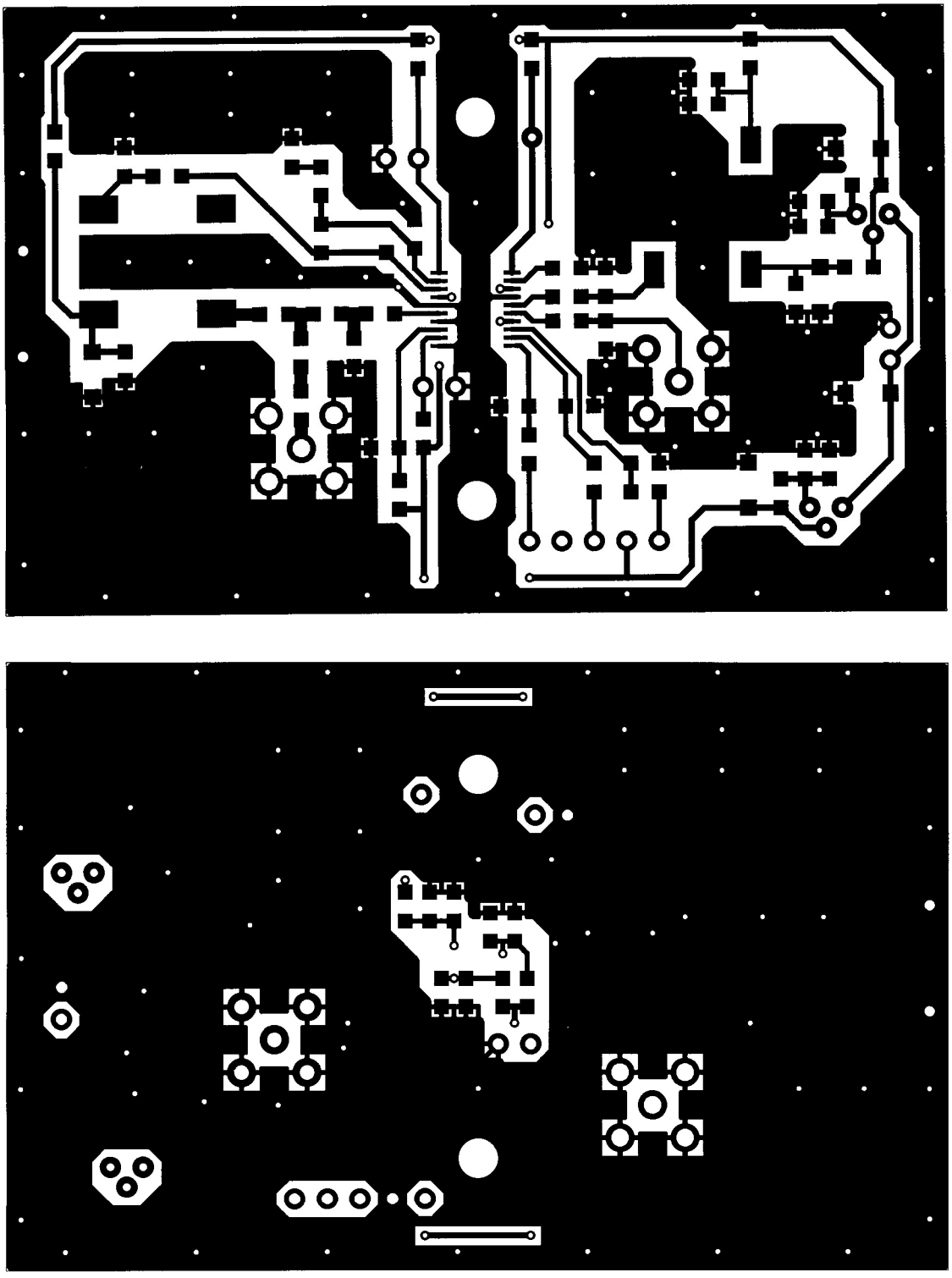


Fig. 47 - Demonstration Board pcb Layout.

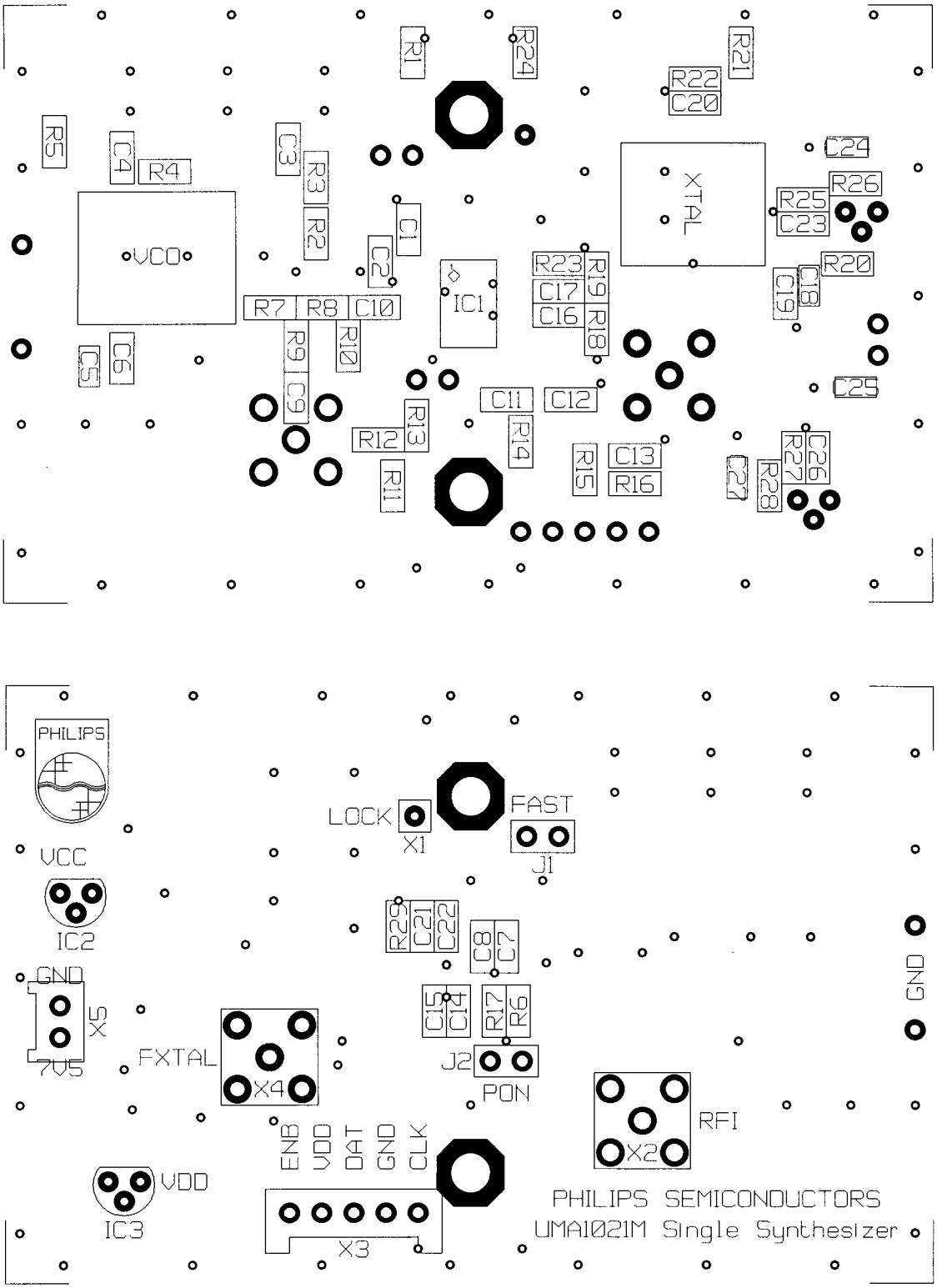


Fig. 48 - Demonstration Board Placement of Components.

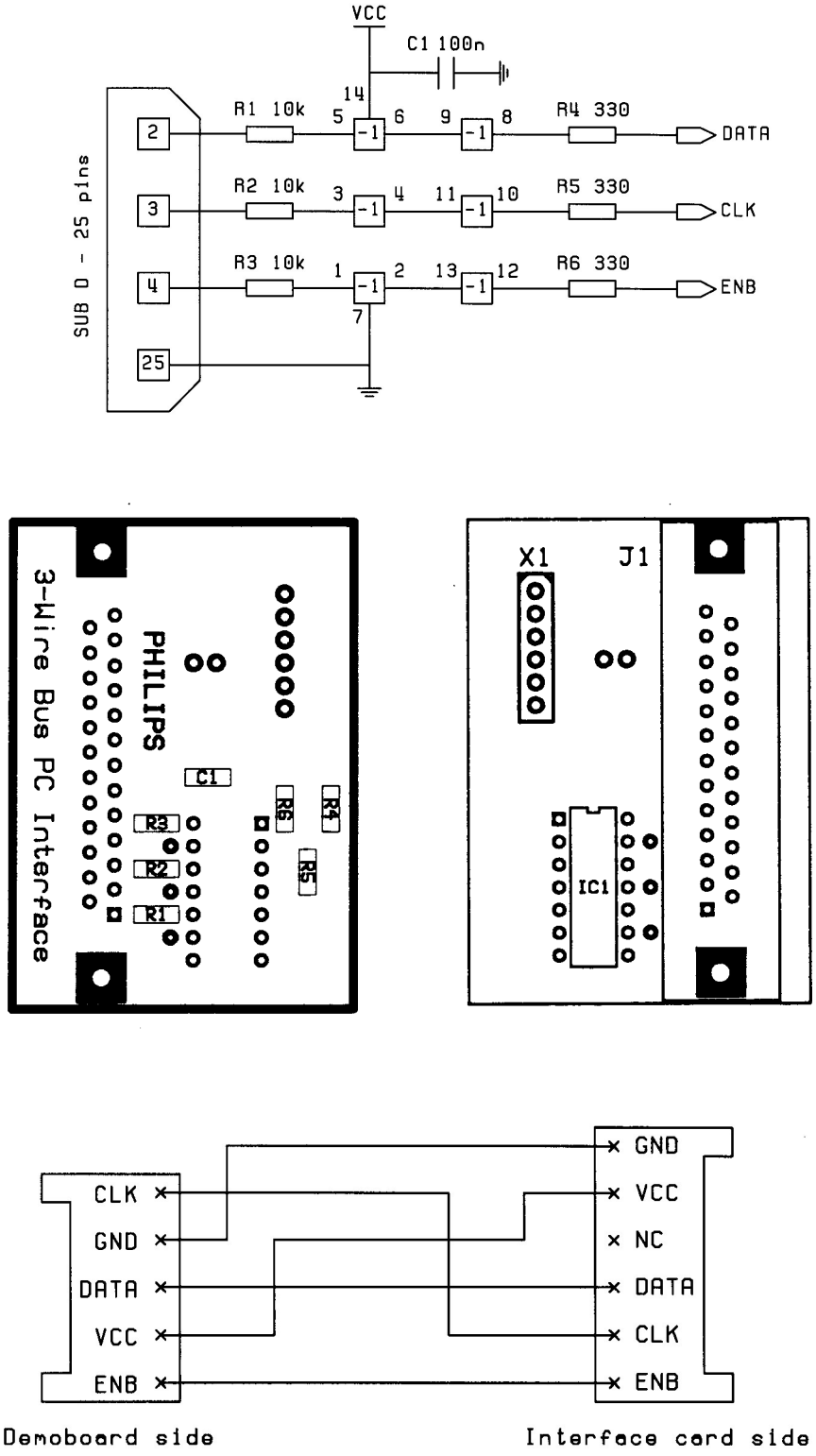


Fig. 49 - Interface Card pcb Layout and Cable Connection.

7. References

[1] Product specification UMA1021M, Philips Semiconductors, 28 August 1996.

[2] Gardner, Floyd M. Phase lock Techniques, 2nd ed, Wiley, New York. 1980.

[3] Rohde, Ulrich, L. Digital PLL Frequency Synthesizers, Theory and Design, Prentice-Hall, Englewood Cliffs, New Jersey 1983.