APPLICATION NOTE

Broadband impedance matching for S-Band Transistors

AN98029

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1 INTRODUCTION

Due to fact that no accurate model or S-parameters exist which describe RF power transistors, the design of RF power amplifiers is often done in an empirical way. Not only is this method very time consuming, but it also means that it is at least doubtful whether the optimum performance of the transistor is obtained, especially when broadband matching is required. In this paper a method of designing an input and output matching circuit for a broadband power transistor operating in the low S-band (2.7 – 3.1 GHz) is described. The design and evaluation of the transistor is left out in this paper.

2 DESIGN METHOD

The whole design can be separated into the design and evaluation of the input and output circuit. This is done in the same way for both circuits. The following steps can be distinguished:

- Impedance measurement
- Fit impedance data to an appropriate model
- Design of lumped element input and output circuit
- Translation of lumped element to stripline
- Evaluation of stripline circuit with CAD-tools.

In the following each step will be discussed separately.

3 IMPEDANCE MEASUREMENT

The first step is to measure the impedance at nominal output power. This is done by tuning the device with slugtuners at the input and output to maximum output power and minimum reflection at the input with gradually increased input power. In Fig.1 the impedance measurement test set up is depicted.

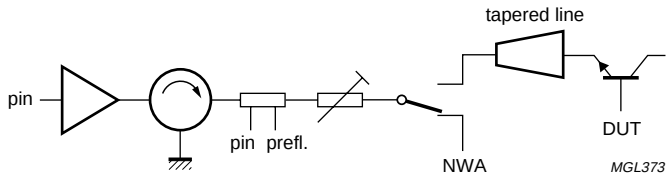

Fig.1 Impedance measurement set up.

In Fig.1 it can be seen that not the actual input impedance is measured, but the source-impedance. The input impedance is the complex conjugated of this source-impedance. This may be done under the assumption that minimum input reflection is achieved when source and load are complex conjugated. For the output the load impedance is directly measured. Also in Fig.1 it can be seen that between tuner and device a tapered line is connected. With this tapered line the relatively low impedance of the devices is transformed to a higher value thus ensuring that with the tuners all required impedance's can be obtained. This is especially required with high power devices where the slugtuners cannot handle a

high VSWR. In the network analyzer the S-parameters of the tapered line are stored and the measured data is recalculated for the transformation of the tapered line. During deembedding of the tapered circuit the following errors can be introduced:

- Reference plane is not accurately defined
- Launcher is very thin compared to the lead of the transistor. This introduces a discontinuity (step in width) which can cause a large error.

The errors introduced may be as large as j6 Ω at 3 GHz. The Philips Data Handbook contains values for the input and load impedance of the transistor which are corrected for these errors.

4 FITTING DATA TO MODEL

Although no accurate two-port models exist to describe the transistor completely, simple equivalent one-port models which describe the input and output impedance of the transistor can be used to enable the use of CAD-Tools in the design of the matching circuit. In Fig.2 the model for the input of the transistor based on the internal matching topology is depicted in Fig.3 measured and fitted data are given in the Smith Chart. From the relation $B = \frac{f_0}{Q}$ it can be seen that for a large bandwidth a low Q-transformation at all stages is required. To evaluate this the one-port model proves to be a useful tool. The bandwidth limitations of the intrinsic transistor are dominated by the input rather than by the output. This also can be found in the transistor model. In the model the active die is represented by R_{DIE}. The first (internal) matching stage is formed by the first emitter bondwire (L_{E1}) and the prematch capacitor (C_{PRE}). L_{E2} represents the bondwire connecting die and prematch to the lead. L_P, C_P and L_{PAR} are parasitic elements caused by the header.

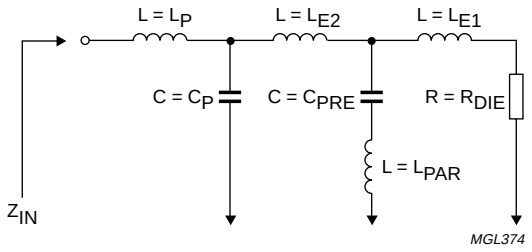

Fig.2 Input equivalent model.

Apart from bandwidth considerations, the location of the resonance frequency of the first matching stage at the input and of the resonance frequency of the internal shunt inductance (inshin) at the output also have a large influence on gain and efficiency. More on this subject can be found in Pitzalis[1]

(1) *"broad-band Microwave Class-C Transistor Amplifiers"*, Pitzalis and Gilson; IEEE Transactions on Microwave Theory and Techniques, November 1973.

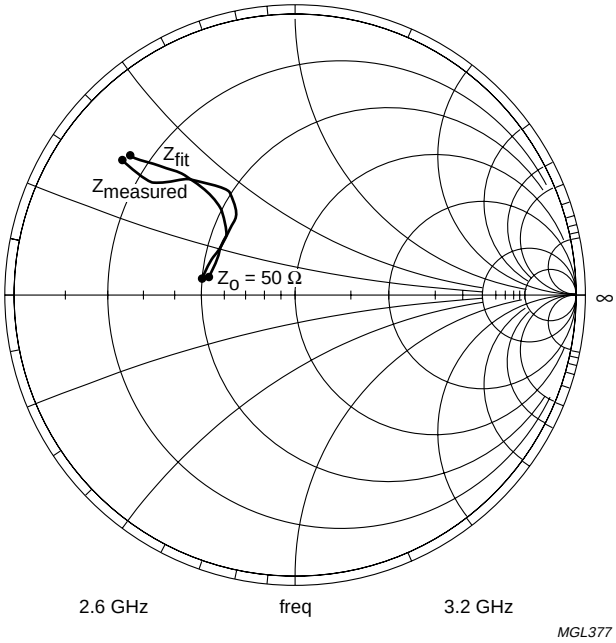

Fig.3 Measured and fitted data.

In Fig.4 the model of the output is given. Here the die is represented by a single resistor in combination with a capacitor which represents the output capacitance of the active die. The die is connected to the lead by means of L_{C1} and L_{C2}. The point of impact of the internal shunt inductance (L_{INS}) determines the ratio between L_{C1} and L_{C2}. C_{DC} is a DC-decoupling capacitor and C_{PAR} is modelling the parasitic capacitance caused by the header.

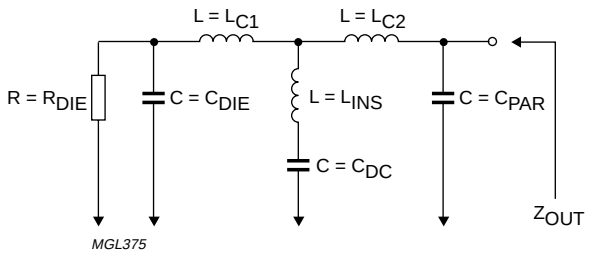

Fig.4 Output model.

A second method in designing the matching circuit is to use the measured data in a dataset. This has the disadvantage that inconsistency in data will have a larger influence than when a model is used.

A second advantage of the use of a model is that this gives the possibility to evaluate the influence of production spread of each parameter on the performance (e.g. Γ_{IN}).

5 LUMPED ELEMENT INPUT AND OUTPUT CIRCUIT

Before designing the input and output circuit with stripline techniques it is preferred to synthesize a low pass lumped element prototype first. The advantage of using a lumped element model first is:

- Optimum solution easier and faster found with CAD-Tools
- Better insight in feasibility of found solution. High inductance are very difficult to realize in stripline techniques. An inductance may also converge to zero (or negative values) indicating that the given low pass structure is not appropriate.

Similar to the requirements for the internal matching network, the external matching circuit (see Fig.5) must also be a low Q design to ensure broadband performance of the device.

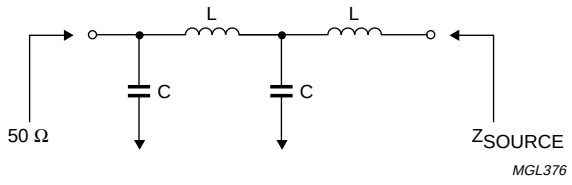

Fig.5 Lumped element model input circuit.

After having found the optimum values for the lumped elements, these can be translated to stripline elements.

This is done by using the basic formula's[1] to find the initial values for stripline circuit which then can be optimized with CAD-tools.

(1) A very good description of microstrip matching networks can be found in: *"Microwave Transistor Amplifiers"*, Guillermo Gonzalez.

6 EVALUATION OF STRIPLINE CIRCUIT

Although stripline models used in CAD-tools such as MDS are fairly accurate, they still have their limitations (such as steps, crosses and substrate thickness). To examine whether these limitations de not mask any significant errors in the design a field simulator can be used (e.g. Momentum). The output of such a simulator is a datafile containing the S-parameters of the stripline circuit. In order to prevent the introduction of additional errors in the simulator output, special attention should be paid to the following:

- Use the appropriate port definition and location of the reference plane. Be aware of any unexpected steps in width at the edge of the simulated circuit.
- Make sure that the MESH is sufficiently small, especially at discontinuities.
- Use a sufficient number of frequency points.

With the combination of simulator output and transistor model an accurate idea of the performance of the transistor in the matching circuit can be obtained without having to go through the time and money consuming process of ordering and assembling printed-circuit boards. When measuring the printed-circuit board with a network analyzer it should be noted that an error can be made due to the difference in width between printed-circuit board and launcher (see Chapter 3). In Fig.6 the input reflection can be seen of the BLS2731-10 in a 50 Ω matching circuit. Both measured and simulated data show a similar curve, only the minimum value is reached at a different frequency. this difference between measured and simulated curve can be explained by the following:

- Small air gaps between reference plane of transistor and edge of printed-circuit boards.
- Impedance data used in the design of the printed-circuit board is from an average device. The measured device may differ from average due to normal production spread.
- Placing components such as DC-blocking.
- Influence bias circuit.
- Connectors not incorporated in simulation.

Also in Fig.6 it can be seen that excellent matching is achieved over the entire frequency band from 2.7 – 3.1 GHz. For the output a similar performance is found.

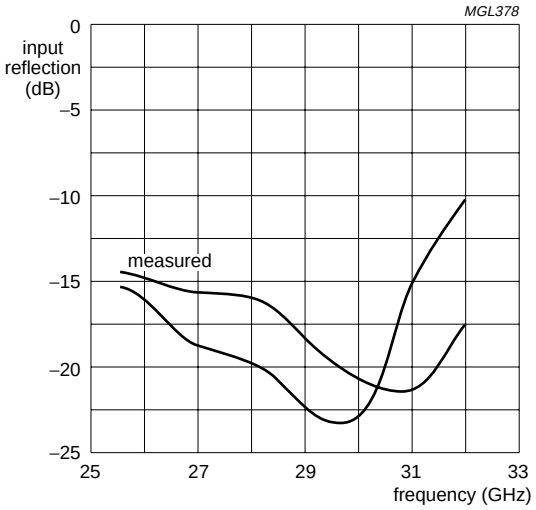

Fig.6 Measured and simulated input reflection of BLS2731-10.

7 CONCLUSIONS

Although the lack of an accurate model for S-band high power transistors would suggest that the use of CAD-tools in the design of matching circuits is impossible, it is shown that with the use of the impedance data from the data handbook and a simple model for the input and output impedance an excellent matching can be achieved. This enables RF-engineers not only to design and evaluate printed-circuit board much faster, but also over a much larger bandwidth.

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