APPLICATION NOTE

Mounting consideration for SOT409 (ceramic SO-8) devices

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Philips
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CONTENTS

1 INTRODUCTION

For both 820 – 960 MHz (GSM) and 1800 – 1990 MHz (PCN and PCS), Philips has introduced a series of RF power transistors for base station applications at 26 V power supply. The driver stage transistors are mounted in a SO-8 style surface mount package (SOT409B), suitable for pick and place assembly. SOT409B packages have an AIN substrate to electrically isolate the flange from the leads. Table 1 summarizes the RF performance and thermal resistances of the transistors.

Table 1 SOT409B driver stage transistors with typical values between brackets

TRANSISTOR TYPE	f (MHz)	PL-1 dB (W)	Gp (dB)	Eff (%)	$R_{thj\text{-}mb}$ (K/W)	P_{dmax} (W)
BLV904	960	5	>13 (15.5)	>50 (55)	10	17
BLV909	960	9	>9.5 (11.5)	>50 (55)	6	29
BLV2042	1990	4	>11 (13)	>40 (45)	10	17

In this paper the mounting of the SOT409B devices is considered. By focusing on the heatflow from junction (at die level) to the heatsink of the application, criteria for best thermal performance (lowest thermal resistance between mounting base and heatsink), can be derived. Simulation results are presented to show the behaviour of using different ways of mounting the device, resulting in a proposal for surface mounted assembly.

2 MOUNTING OF SOT409B DEVICES

Thermal investigations has shown that both the copper pad of the device’s backside (connected to the AIN substrate) as well as the leads of the SOT409B, contribute to the heat transfer from junction to heat-sink. For the most optimal results two options are available:

The most effective way to thermally connect the SOT409B devices, is to directly solder the device’s backside, together with the device’s emitter leads (4 are available, at the edges; see Fig.1) to the heatsink or to an insert mounted to the heatsink; see Fig.2. A more practical option is a footprint on the P.C.B. with a number of through metallized holes to transfer the heat. In that case the device’s copper pad is soldered to a footprint, of at least the same dimensions as the device (see Fig.3). Connection to the fully metallized backside of the P.C.B. is achieved by placing a sufficient number of plated through metallized holes just under the device:

- To achieve good grounding for best R.F. performance
- To optimize the heat transfer.

To optimize the thermal contact between the board and the heatsink a thin coating of thermal past should be applied locally to minimize voids. Further that P.C.B. should be fastened to the heatsink with extra screws as close as possible to the device. Another possibility is to solder the P.C.B. to the heatsink or use thermal conductive glue.

Pinning SOT409B

PIN	DESCRIPTION
1	emitter
2	base
3	base
4	emitter
5	emitter
6	collector
7	collector
8	emitter

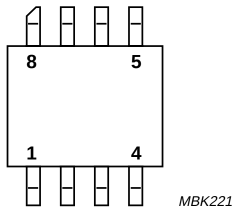

Fig.1 SOT409B outline.

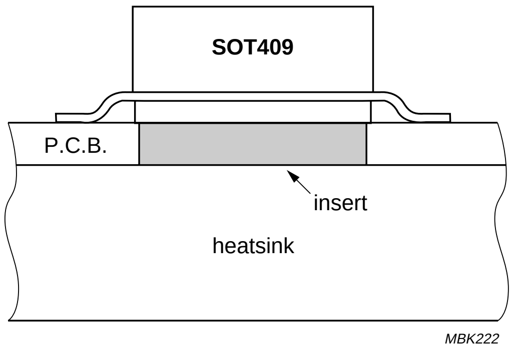

Fig.2 Cross section of the SOT409B mounted on an insert.

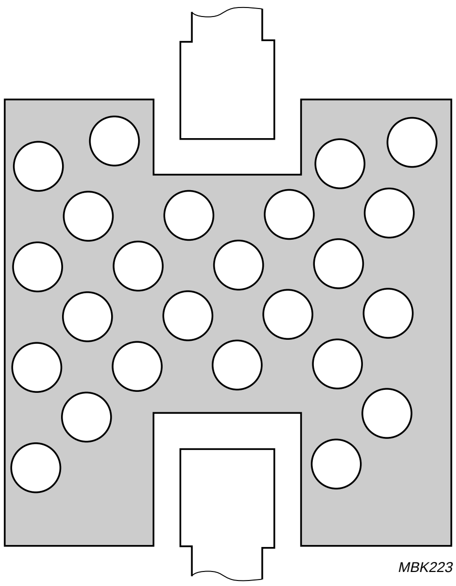

Fig.3 Example of a footprint for soldering.

3 HEATFLOW IN APPLICATION

In Fig.4 a cross section and a schematical representation is given of an application in which a mounted SOT409B device is used. The device has been mounted on top of a P.C.B. equipped with through metallized holes to transfer the heat from the device to the base to heatsink. This figure is used to determine the thermal resistance of the P.C.B.

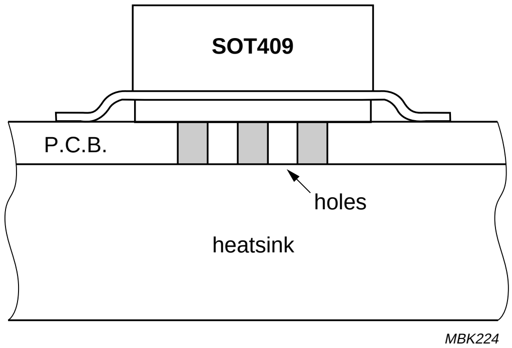

Fig.4 Cross section to the SOT404 mounted on the footprint.

4 IMPORTANT FACTORS FOR THERMAL RESISTANCE OF THE P.C.B.

- Thickness of P.C.B. material
- Thickness of metallization of P.C.B.
- Copper growth in holes (depending on process used)
- Fill factor (percentage of solder present in through plated holes)
- Number of plated through holes
- Diameter of plated through holes.

Other parameters were taken into consideration, but have marginal effects on thermal resistance:

- P.C.B. material used (Duroid, epoxy)
- Pb percentage in PbSn.

5 SIMULATION EXAMPLES

With the help of simulations, each of the critical factors have been investigated. For calculations, the following parameters have been used.

- Heat area dimensions: 4.13 × 3.18 mm
- PbSn thickness on top of P.C.B. metallization (24 μm)
- Pb % in PbSn (37%)
- Cu growth in via holes (32 μm)
- P.C.B. material (Duroid)
- P.C.B. copper thickness (1 Oz. or 35 μm).

The result on thermal resistance is given in Table 2 and 3, for 9 and 12 through metallized holes respectively:

Table 2 Footprint area equipped with 9 through metallized holes

CASE	FILL FACTOR (%)	HOLES DIAMETER (mm)	P.C.B. THICKNESS (mm)	Rth mb-hs (K/W)
1	10	0.65	0.79	5.4
2	100	0.65	0.79	3.4
3	100	0.65	1.59	5.7
4	100	1.00	1.59	2.9
5	100	1.00	0.79	1.7

Table 3 Footprint area equipped with 12 through metallized holes

CASE	FILL FACTOR (%)	HOLES DIAMETER (mm)	P.C.B. THICKNESS (mm)	Rth mb-hs (K/W)
1	10	0.65	0.79	–
2	100	0.65	0.79	2.5
3	100	0.65	1.59	4.3
4	100	1.00	1.59	–
5	100	1.00	0.79	1.3

6 CONCLUSION

Using the material and permanent values given in the example, thermal resistance of the footprint design can be as low as 1.5 K/W for the optimum case. Even the most powerful transistor available in the SOT409B range, BLV909 (nominal 9 W of RF power at 960 MHz) can be operated with a sufficiently low junction temperature (T_j). A T_j of 137 °C is possible while heatsink temperature (T_h) is assumed to be 70 °C and 50% collector efficiency is achieved at nominal loadpower.

7 REMARK

SOT409B is a SMD package which can withstand a normal reflow soldering process. Since the leads are plated with typically 3 μm of gold, either sufficient solder material (≈150 μm) should be applied or the leads should be pre-tinned in order to minimize brittle Au-Sn intermettalics which can introduce cracks during power cycling. A footprint for reflow soldering is available upon request.

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