APPLICATION NOTE

DPC7146-23
Version 1.1

AN98012

Philips
Semiconductors

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DPC7146-23 Version 1.1

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Abstract

The DPC7146-V23 turn key board is a multimedia board for use in a PCI bus based environment. For transfer of audio data, video data, and general data via the PCI bus, the SAA7146A controls the PCI bus as bus master and handles autonomously the transfer even for complex transfer schemes by embedded local control mechanisms.

The DPC7146 V2.3 turn key board is intended for chip demonstrations to customers and software development.

APPLICATION NOTE

DPC7146-23 Evaluation Board for SAA7146A

AN98012

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Keywords

SAA7146A Multimedia Scaler and PCI Bridge
SAA7111/11A Video Input Processor
SAA7185B Digital Video Encoder
TDA1309
PCI bus mastering
Video Capture and Playback via PCI
Audio Capture and Playback via PCI
VMI Video Modul Interface

Date: 11th Feb., 1998

Summary

The DPC7146-**23** board provides a turn-key solution board for the SAA7146A Multi Media Bridge Scaler and PCI Circuit. It features all the base elements for a PCI Bus Mastering device: video and audio recording and play-back, and also video inlay. Further advanced features like compression devices (MPEG2, videophone, and AC3) are supported by the additional data interface (DEBI port and GPIO-pins) and can be implemented on a sub-board. The connectivity is already foreseen.

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1. Introduction

The following sections provide a description of the DPC7146 turn key board. It features the SAA7146A *Multimedia bridge, high performance Scaler and PCI circuit* with its video, audio, and data I/O capability. The board provides interfaces and connectors to access the local signals of the SAA7146A for a daughter-board.

The DPC7146 supports video input, video output, audio input, audio output and data I/O via the PCI bus with full PCI bus mastering capability thus off loading the data transfer workload from the host CPU to the SAA7146A. The mechanism which enables the local data flow control is called RPS (=Register Programming Sequencer).

1.1 Scope

The DPC7146 V2.3 turn key board´s primary purpose is to serve as a versatile board for the SAA7146A and to provide a solid backbone for customized board developments. Therefore it offers various interfaces, connectors and configuration options. Secondary the board is a useful hardware platform for software development and debugging with respect to hardware drivers, Application Programmers Interfaces and application software.

1.2 Overview

The DPC7146 V2.3 turn key board is intended to provide all general functionality for recording and play-back of video and audio signals. On top of that it enables enhancements like MPEG2 encoding and decoding, videophone application and AC3 application with an appropriate daughter-board.

The DPC7146 V2.3 turn key board can be used for evaluation of the SAA7146A *Multimedia bridge, high performance Scaler and PCI circuit*. It features the following Philips ICs:

SAA7146A The SAA7146A *Multimedia bridge, high performance Scaler and PCI circuit* is a versatile PCI Bus interface chip allowing several video and audio data streams to be processed in parallel and transferred via PCI bus. The SAA7146A operates as bus master. It has 2 video input/output ports, 5 audio ports, 4 programmable I/O signals and one ISA bus-like interface (DEBI = Data Extension Bus Interface) for connection of MPEG decoders and other peripheral devices. The internal register programming sequencer allows autonomous execution of two tasks like individual scaling of even and odd fields. This local data stream processing off-loads the host CPU.

SAA7111(A) The SAA7111A *Video Input Processor* (VIP) is a digital multi standard decoder with analog input processing and clock generation. It supports 2 CVBS inputs and one S-VIDEO input. The implemented A version operates under 3.3 V power supply.

SAA7185B The SAA7185B *DEN*C is a low cost digital video encoder providing several outputs.

TDA1309 The TDA1309 combines low cost bit stream ADC and DAC for digital audio systems.

TDA1308 The TDA1308 is a low cost audio amplifier.

PCF8598E The EEPROM PCF8598E contains the identification data of the board and its vendor. It will be read out at the boot sequence of the PC.

1.3 Features of the turn-key board

- Enable video and audio data transfer via PCI bus mastering
- Analog (Scaled) Video to memory or to VGA via PCI bus (Video Capture)
- Analog audio to memory (Audio Capture)
- Video from memory to analog video (CVBS signal or S-Video signal) (Video Play-Back)
- Audio from memory to analog stereo (Audio Play-Back)
- AC3 decoded audio via daughter board
- MPEGx decoding and encoding via daughter board

2. Architecture

2.1 The PCI Bridge SAA7146A inside the PC

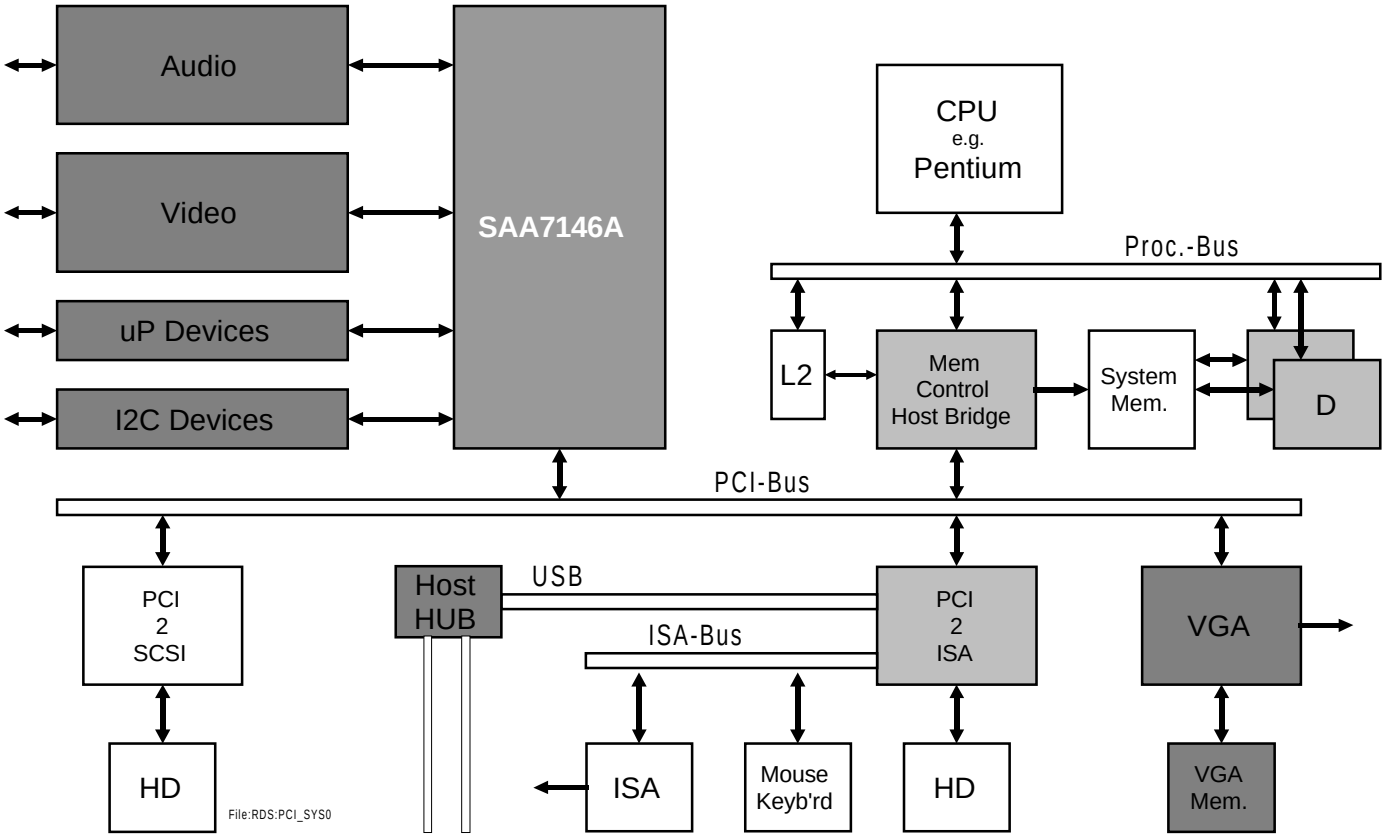


Fig.1 Architecture of a PC

A modern PC (= Personal Computer) consists of a CPU (CPU = Central Processing Unit), a PCI chip set, the memory, and a VGA. The HD (HD = Hard Disk), and the input devices of Keyboard and Mouse are completing a standard PC system. The PCI-chip set itself consists in general of the memory controller and PCI host bridge (Host Bridge), the system memory data buffers (D), and the PCI-to-ISA bridge.The system can be enhanced by units hooked to the PCI-bus or the slower ISA-Bus.

The PCI-bus is **the** high bandwidth bus inside the PC, with data rates of up to 132MByte/s (33MHz * 4 Byte). On this bus **all** information exchange is handled, except the traffic between the system memory (including the second level cache L2) and the CPU. The bus arbitration concept allows the access of every bus member in a certain order. This arbitration scheme is proprietary to the host bridge.

2.1.1 The CPU

The CPU, e.g. a Pentium processor, does its data exchange via the processor bus to the second level cache L2 and/or the system memory. The memory management unit provides the access control for different memory types and its memory cycles. It also interfaces the CPU and the system memory to the PCI-bus with its different devices. The access structure to the PCI bus is adapted to the needs of the CPU in first instance.

2.1.2 The host bridge and the PCI bus

The PCI-bus is operating in burst mode to achieve the maximum bandwidth performance. The maximum bandwidth of the PCI-bus depends on the clock speed of the CPU. The derived clock rates of the PCI-bus are 25MHz, 30MHz, and 33MHz. The theoretical maximum bandwidth results out of the product of PCI clock rate times bus data width(4 Byte for the commonly used 32bit bus) 132MByte/s (33MHz * 4 Byte). The actual achieved bus bandwidth is decreased due to the multiplexed address/data concept with limited data bursts, and the setup time for a new data transmission (Arbitration latency and target latency; each item in clocks). The achievable PCI bus efficiency is drawn in the following figure. ArbL stands for the arbitration latency and TarL stands for target latency. The clock rate of the PCI bus is set to 33MHz.

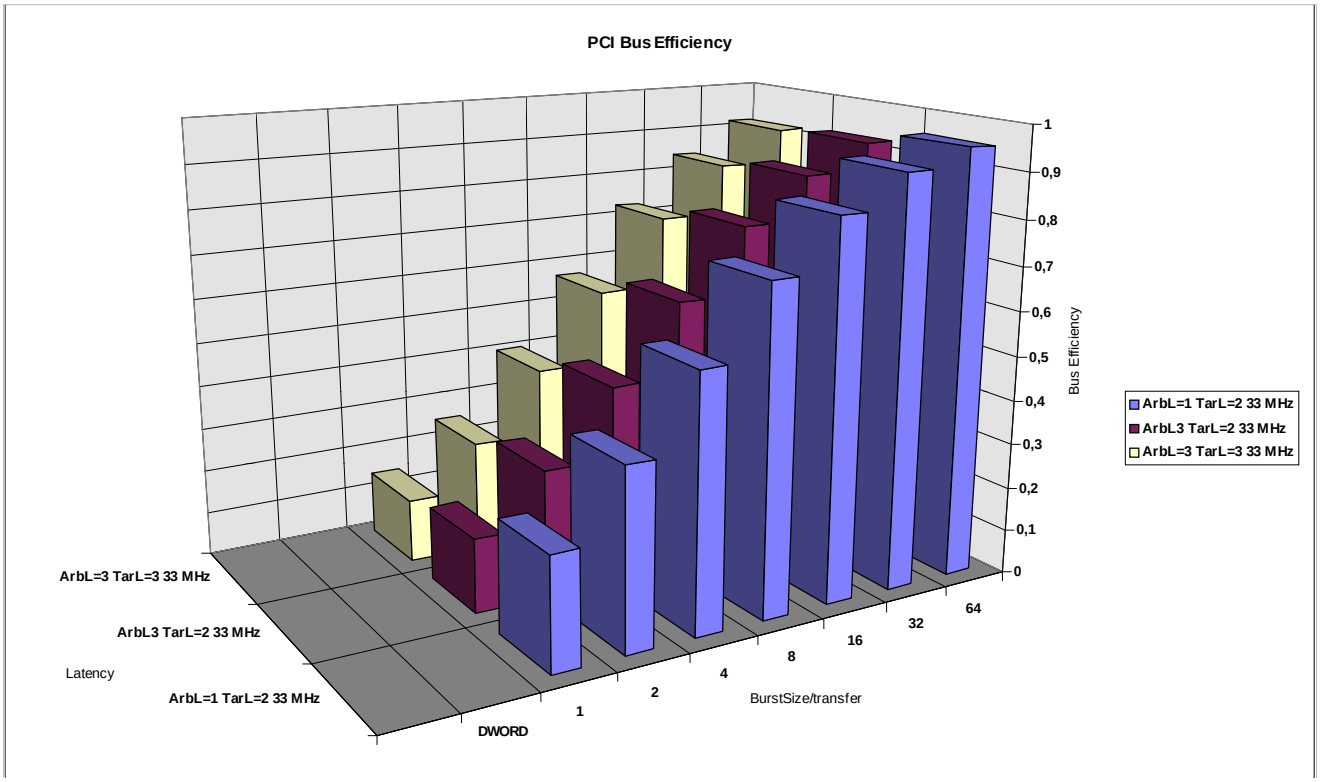


Fig.2 PCI Bus Performance versus Latency

The host bridge arbitrates the bus and allows the access of every member to the bus in a certain order. Depending on the used PCI chip set this order might be different.

2.1.3 The PCI to ISA bridge

The PCI to ISA bridge is part of the PCI chip set. It interfaces not only to the ISA bus but also features connectivity to hard disk and CD player by EISA bus and other components like mouse and keyboard. On newer PCI chip sets the PCI to ISA bridge contains also the interface for the USB hub. The ISA bus has been developed from the early 8085 microprocessor bus system. In the past this bus system had been the interconnect for nearly all boards. Due to the limited speed of the ISA bus all these devices will go now onto the PCI bus or will be integrated into an USB device.

2.1.4 The VGA

The VGA (VGA = Video Graphics Adapter) is in general only an output device for the PC and acts as a slave device on the PCI bus.The VGA provides the means to display graphical objects and textual characters. The architecture of a VGA is very appropriate to its vendor, aside to some ‘standardised‘ registers.

2.1.5 The SAA7146A

Beside the CPU as central processing unit, the PCI bus master device SAA7146A *Multimedia bridge, high performance Scaler and PCI circuit* can take over the control of the PCI bus. Due to its local control possibilities it can control the data flows of audio, video, and other data streams through its interface.Therefor it off-loads the CPU. It can interface the system memory and/or the memory of the VGA with the audio, video, and other local systems. The architecture and its functionality will be explained in the next sections.

2.2 The Architecture of the PCI Bridge SAA7146A

For multimedia over PCI, the SAA7146A *Multimedia bridge, high performance Scaler and PCI circuit* is the heart of the Philips' solution. It has many on-board interfaces, supporting video and audio inputs/outputs via the PCI interface, and has a high performance scaler core similar to that in the SAA7140. As a PCI bus master it can send data from its local sources of video, audio, and data interface (DEBI) to the main memory or it can request data from the memory. The data streams can be handled locally by powerful control engines. Operating autonomously, these engines (RPS and TSL) off-load the data control workload from the host CPU and enable real time control. The two RPS (RPS = register Programming Sequencer) engines can control in combination with the Local Event Management on almost all data streams, independent of the CPU. The TSL (TSL = Time Slot List) engines of the audio interface provide additional enhanced features to the SAA7146A like concurrent multi-channel input and output.

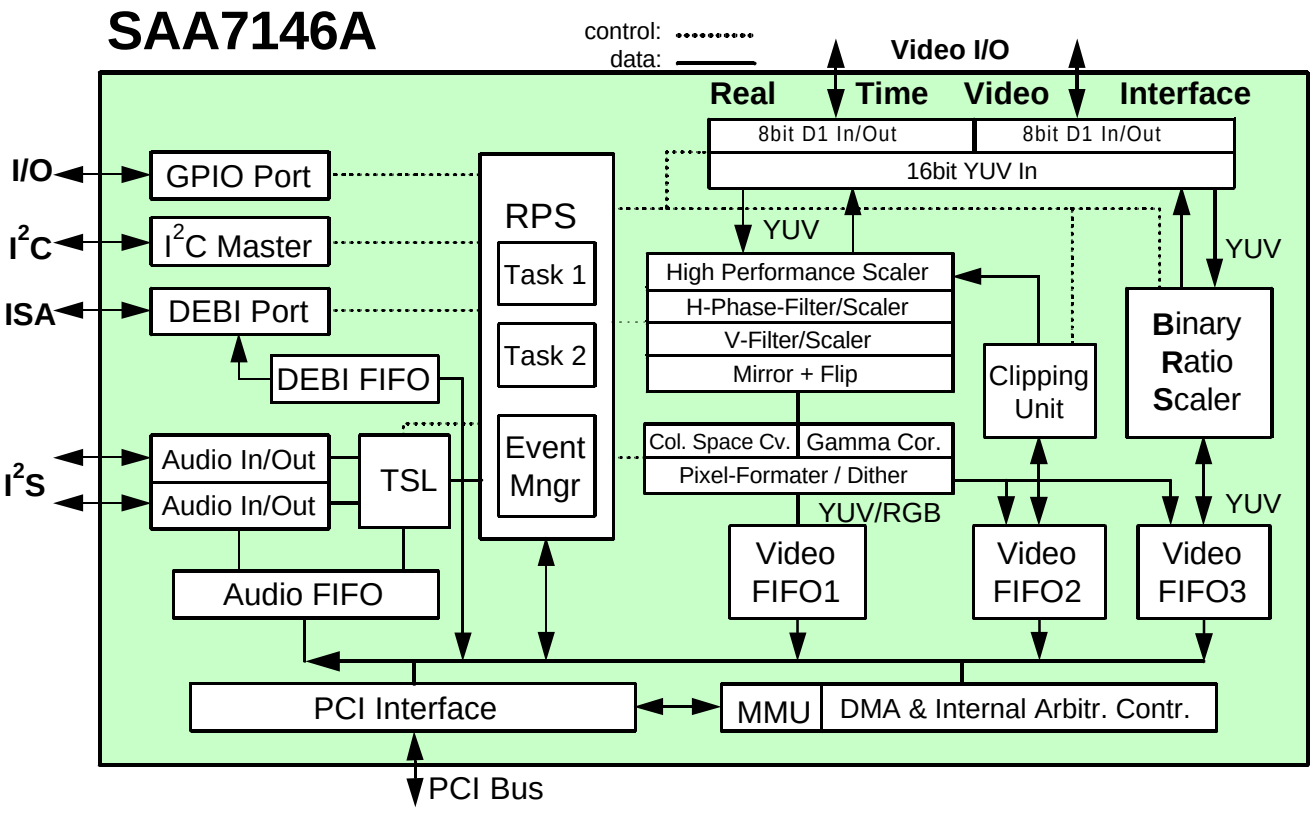


Fig.3 Architecture of the SAA7146A

2.3 PCI Interface

2.3.1 PCI Commands

The PCI specification provides a set of commands to indicate to the target the type of transaction the master is requesting. The bus commands are encoded on the C/BE(3..0)# lines during the address phase. The SAA7146A utilises only a subset of these commands for its own purposes. These utilised commands differ between slave mode and master mode.

TABLE 1 PCI Commands used by SAA7146A

C/BE(3..0)#	Command Type	Comments
0110	Memory Read	also used for Master Mode
0111	Memory Write	also used for Master Mode
1010	Configuration Read	
1011	Configuration Write	
1100	Memory Read Multiple	
1110	Memory Read	
1111	Memory Write and Invalidate	

2.3.2 ID‘s at PCI Configuration Space

The PCI spec describes 4 different ID'sat the PCI configuration space.

TABLE 2 ID‘s at PCI Configuration Space

Address	NAME	BIT	TYPE	Description
00	Device ID	31-16	RO 7146H	SAA7146A
00	Vendor ID	15-0	RO 1131H	Philips
2C	Subsystem ID	31-16	RO xxxxH	read from I2C EEPROM at PCI reset
2C	Subsys Vendor ID	15-0	RO xxxxH	read from I2C EEPROM at PCI reset

The vendor ID 1131 is registered for Philips Semiconductors only. For further questions on PCI issues pls. contact the official entry point of the PCI Special Interest Group (SIG):

PCI SIG
2575 NE Kathryn #17
Hillsboro, OR, 97124
USA
Ph +1.503.693.6232
fax +1.503.693.8344
email: pcisig@teleport.com or techsupp@pcisig.com

2.3.3 Organisation of EEPROM

The data of the subsystem ID and the subsystem vendor ID is organized in the EEPROM in the following order:

TABLE 3 Organisation of the EEPROM

Address in EEPROM	value	Place in Configuration Space
00	Subsystem ID (high byte)	byte: 2C, bits: 31 - 24
01	Subsystem ID (low byte)	byte: 2C, bits: 23 - 16
02	Subsys Vendor ID (high byte)	byte: 2C, bits: 15 - 8
03	Subsys Vendor ID (low byte)	byte: 2C, bits: 7 - 0
04	Max_Lat	byte: 3C, bits: 31 - 24
05	Min_Gnt	byte: 3C, bits: 23 - 16

2.4 Blockdiagram

The DPC7146-V23 board deploys video and audio ICs and a range of interfaces and connectors. It is primarily promoting the SAA7146A and provides with its connectivity a base for a wide range of functionality, where AC3-playback and MPEG-2 codecs are solutions beside the Video-conferencing application. But it also features the SAA711A, the TDA1309T, and the PCF8598E. The SAA7185B and the TDA1308 provide the output functionality of video and audio signals. The functions are placed on a 4-layered PCB of size 146 mm x 98mm (with out connectivity).

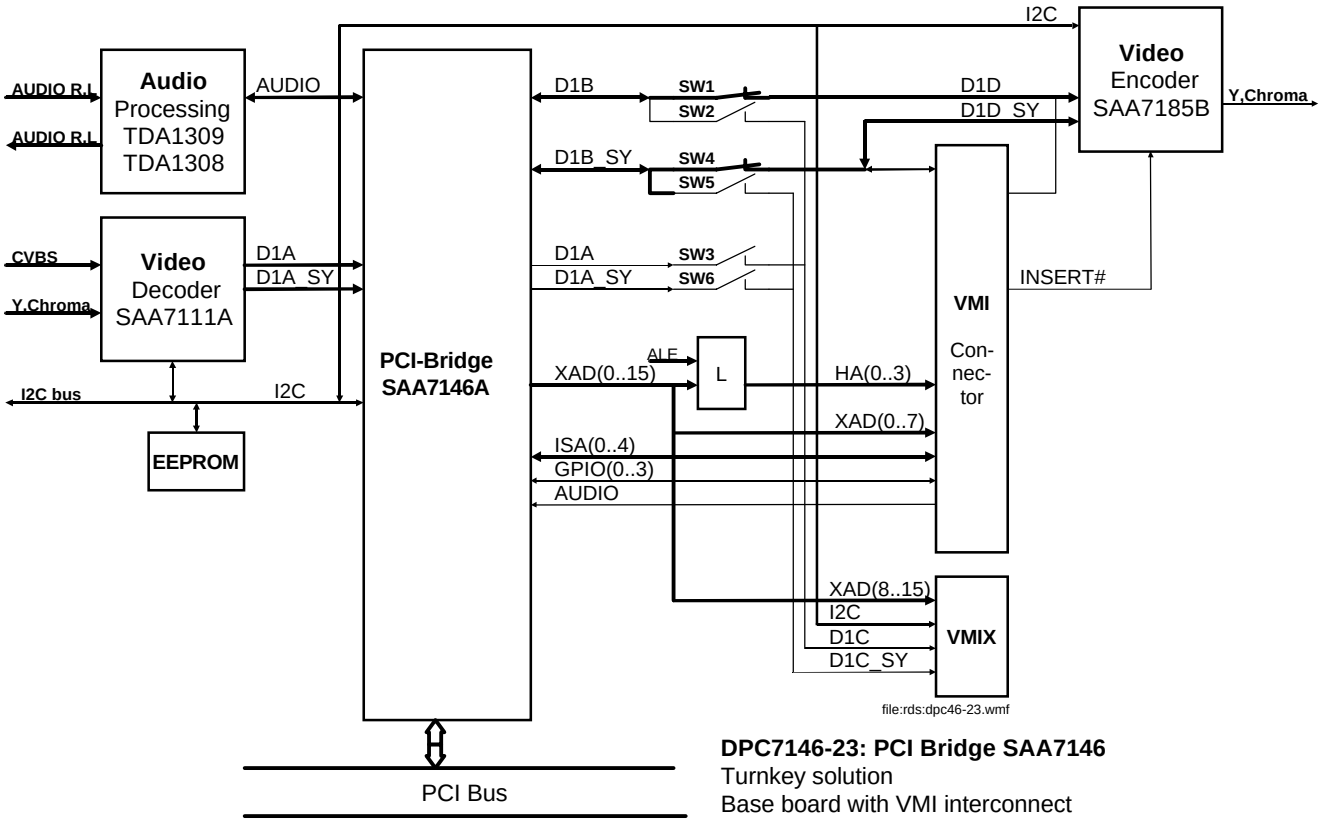


Fig.4 Blockdiagram of the DPC7146 V2.3 turn key board

The SAA7146A is the central component. It is controlled via the PCI bus. The data for identifying the board can be up-loaded from the EEPROM PCF8598E. This is a specific requirement from Windows95 specification (Windows95 is a trademark of Microsoft). With its two D1 ports it can provide simultaneous video-capture and video-play-back capability. The two independent audio I/O engines can be mapped on four of the 5 SD (SD = Serial Data) lines and on three of the 5 WS (WS = Word Select) lines arbitrarily. The DEBI port features either 8/16bit ISA bus style or the Motorola bus style. The GPIO interface and the multi-master I2C bus interface provide additional functionality.

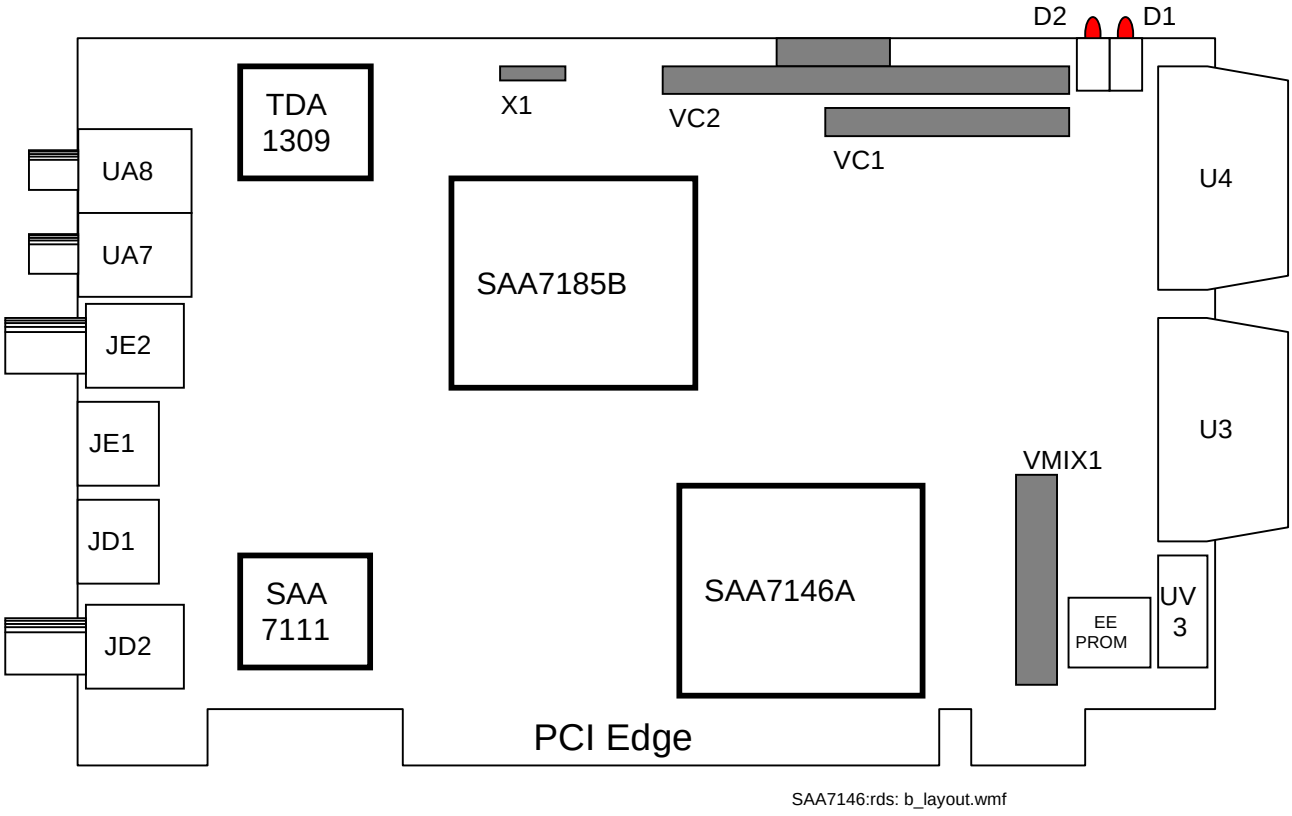
3. Hardware Configuration

This chapter describes the hardware configuration of the DPC7146 V2.3 board. Information will be given especially on:

- Board layout and placement of IC´s and connectors.
- Description of I/O signals.
- PCI bridge: The SAA7146A interfacing and hardware configuration.
- Video Front End: The video decoders SAA7111 and SAA7111A.
- Daughter board connectivity with e.g. VMI connectivity.
- Video Back End: The video encoder block.
- Audio input and output: Audio clock generation, A/D and D/A conversion.
- Power supply.

3.1 Board Layout

All connectors and most of the ICs and other components are assembled on the top of the **4-layered** PCB board, as shown by the following figure. The parts on the soldering side are still inside the tolerated height, specified by the PCI SIG. The approach of 4 layers had been chosen to meet an optimum between cost and signal performance.



SAA7146:rds: b_layout.wmf

SAA7146A: DPC7146 Board Layout

Fig.5 Board Layout of DPC7146-23

The following table lists all ICs used on the board:

TABLE 4 DPC7146: IC content

#	Device	Function
1	SAA7146A	PCI Bridge
2	SAA7111A	Video Decoder
3	SAA7185B	Video Encoder
4	PCF8598E	EEPROM
5	TDA1309H	Audio Codec
6	TDA1308	Head phone amplifier
7	74HC04	Inverter for audio clock generation
8	74HCT04	Inverter as LED driver
9	74F574	Latch for DEBI addresses
10	74F245	Driver for DENC signals to daughter boards

In the table below all connectivities are listed:

TABLE 5 DPC7146: Board Connector Overview

#	Connector	Function
1	PCI Edge	PCI Bus Edge Connector
2	JD1	S-Video Input + I2C Bus + 12V Power Supply
3	JD2	CVBS Video Input
4	JE1	S-Video Output
5	JE2	CVBS Video Output
6	UA7	Audio Input
7	UA8	Stereo Audio Output
8	U3	Digital Audio Connector
9	U4	Digital Audio Connector
10	UV3	I2C Bus Connector
11	VC1	Video Modul Interface Connector 1
12	VC2	Video Modul Interface Connector 2
13	VMIX1	Extended Video Modul Interface Connector
14	X1	Audio Clock Switch

The base line builds the PCI edge connector. Directly next it is the PCI bus master IC SAA7146A placed. Due to the short distance, the trace length of the PCI bus signals meet the PCI bus specification requirements. The limit is 1.5 inch for all PCI bus signals and 2.5 inch for the PCI CLK signal. The PCI CLK signal has a wounded track on the PCB to achieve this length. Only one clock load is allowed.
At the left side of the board, visible to the computer outlet, the analog video connectors are lined up. It starts with two video-in connectors (Cinch connector JD2 for CVBS and a S-Video connector JD1 with extra features). Two video-out follow (a S-Video connector JE1 and a Cinch connector JE2 for CVBS). The stereo audio-in connector UA7 and the audio-out connector UA8 complete the set.

Opposite the PCI edge connector feature the two double LED (D1 and D2), which indicate the status of the GPIO pin‘s. Very close to them, the VMI connectors VC1 and VC2 provide the interface to e.g. a daughter board. Left to connector VC2, the audio clock switch X1 is placed.
At the right side, opposite to the analog connectors, the two digital audio connectors U3 and U4, and the I2C bus connector UV3 are placed. The digital audio data can be fed to an other board, e.g. a daughter board.
The video decoder SAA7111A block is grouped on a dense area close to the video-in connector. Due to the small board area and the short analog paths, this will not have any impact on the video performance.
The video encoder is placed more to the middle of the board area. This give room for the analog video post filter stages. The video signalling paths are shielded by a separate ground. This prevents distortion from other parts.
The audio codec TDA1309 is placed at the edge of the board, close to the connectors. This enables a good audio performance. The output amplifier TDA1308 is on the soldering side, to provide a dense packaging of the audio codec module.
The EEPROM is placed closed to the I2C bus connector. It contains the ID‘s of vendor and board. The complete content of the EEPROM is listed further below.

3.2 I/O Signals

The set of I/O signals of the board consists of the PCI bus signals, video input and output and audio input and output signals as described in table 1-11

3.2.1 PCI Bus Connector

The PCI connector interfaces the SAA7146A device with the PC system. All signals are standardised by PCI SIG.

TABLE 6 Board: PCI Bus Connector

Signal	I/O	Function
AD0..AD31	I/O	Address, Data lines for interconnect with PCI bus
C/BE0..C/BE3	I/O	Bus Command / Byte Enable
PAR	I/O	Parity Signal
PERR-	O	Parity Error
STOP-	I/O	Stop Signal
DEVSEL-	I/O	Device Select Signal
TRDY-	I/O	Target Ready Signal
IRDY-	I/O	Initiator Ready Signal
FRAME-	I/O	Frame Signal
IDSEL	I	Initialisation Device Select
GNT-	I	Bus grant input signal
REQ-	O	Bus request output signal
PCLK	I	PCI clock input signal
RST-	I	Device reset input signal
INTA-	O	Interrupt A

3.2.2 Analog Video Inputs

The CVBS input connector and the S-Video input connector are feeding their video signals to the multi standards video decoder SAA7111/SAA7111A.

The S-Video input connector features additional to the video signals a power supply and an I2C bus connectivity to an external tuner or video camera device. Care should be taken, that the external device is capable of handling the **+12 V power supply**.
IMPORTANT: There is no fuse on the PCB for the supply voltage!.

TABLE 7 Board: Analog S-Video Input

Connector	Name	Pin	Signal
JD1	S-VIDEO1	1	GND
		2	GND
		3	Y (Luminance)
		4	C (Chrominance)
		5	SCL (I2C bus)
		6	**+12V**
		7	SDA (I2C bus)

TABLE 8 Board: Analog CVBS video Input

Connector	Name	Pin	Signal
JD2	CVBS	1	Composite Video
		2	GND

3.2.3 Analog Video Outputs

The CVBS output connector and the S-Video output connector are distributing their video signals from the multi standards video encoder SAA7185B. Holders of a macrovision licence, can use the SAA7184 alternatively.

TABLE 9 Board: Analog S-Video Output

Connector	Name	Pin	Signal
JE1		1	GND
		2	GND
	Y_OUT	3	Y (Luminance)
	C_OUT	4	C (Chrominance)

TABLE 10 Board: Analog CVBS video Output

Connector	Name	Pin	Signal
JE2	CVBS_OUT	1	Composite Video
		2	GND

3.2.4 Audio Input

The stereo audio input is on connector UA7. The signals directly connect to the codec without any amplification.

TABLE 11 Board: Audio Input

Connector	Name	Pin	Signal
UA7	Audio Input	1	Left
		2	GND (analog)
		3	Right

3.2.5 Audio Output

The stereo audio output is on connector UA8. The codec signals are amplified by the head-phone amplifier TDA1308, which is on the soldering side of the PCB.

TABLE 12 Board: Audio Output

Connector	Name	Pin	Signal
UA8	Audio Output	1	Right
		2	GND (analog)
		3	Left

3.2.6 Digital Audio Connectors

The digital audio connectors feature a bidirectional audio port to the SAA7146A. This feature has been used for an audio daughter board.

TABLE 13 Board: Digital Audio Connector

Connector	Name	Pin	Signal
U3	NC	1, 9	NC
	GND	2, 4, 6, 8, 10	GND
	A_BCLK0	3	Bit Clock
	A_WS3	5	Word Select
	A_SD3	7	Serial Data

TABLE 14 Board: Digital Audio Connector

Connector	Name	Pin	Signal
U4	NC	1, 9	NC
	GND	2, 4, 6, 8, 10	GND
	A_BCLK1	3	Bit Clock
	A_WS4	5	Word Select
	A_SD4	7	Serial Data

3.2.7 I2C Bus Connector

The I2C bus connector is placed on the board for auxiliary purpose. Other I2C bus devices inside the PC can be controlled, or the devices on the board can be controlled without the use of the SAA7146A. The connector is

mounted in the new fashion of pinning. On behalf there might be older pinning version used, the connector can be slightly shifted to fit to another pinning. Please check the pinning of your I2C bus connector.

TABLE 15 Board: I2C Bus Connector

Connector	Name	Pin	Signal
UV3	SCL	1	Serial Clock
	GND	2	GND
	SDA	3	Serial Data
	VCC	4	5 V supply

TABLE 16 Board: I2C Bus Connector: Old Pinning when modified

Connector	Name	Pin	Signal
UV3: Old Pinning	VCC	1	5 V supply
	SDA	2	Serial Data
	GND	3	GND
	SCL	4	Serial Clock

3.3 I2C Bus Port

The I2C bus is implemented as a bus master device.

At PC start up time a routine scans for a local EEPROM with subsystem, vendor ID support, maximum latency, and minimum grant. This is the expected case due to spec. The Philips part PCF8598E should be used.

3.3.1 Termination of I2C Bus

IMPORTANT: In case there is no local I2C bus device on the board, the I2C bus lines have to be pulled-up to VCC by resistors, to bring the port in a defined state! Otherwise the system might hang.

3.3.2 I2C Bus Connection between 5V and 3V Devices

The control of the video decoders is done by I2C bus signals. For connecting 3V devices with I2C bus devices operating on 5V rail, a circuitry of 3 components is proposed. Using a tuner with I2C bus interconnect, this can be handled by the S-Video connector JD1 which also supplies 12V power lines and the I2C bus signals to the external device.

Extra I2C bus connectivities are foreseen to control external devices. This I2C bus connectivity is normally not assembled. The connector can be placed in two ways to allow different connector arrangements.

The configuration settings for the SAA7111 and the SAA7111A which are explained below. The recommended decoder is the SAA7111A. This has been foreseen in the schematics.The I2C bus address can be selected by JV7.

The proposed I2C bus interface will transfer from 5 V of SAA7146A to 3 V environment.

3.4 Video Front End

The block consists of a multi standard video decoder of type SAA7111/11A with its passive components, a CVBS and a S-Video input connector and an I2C bus connector interface. The video decoder provides the colour decoded video data streams of one of the two video input sources.

The input is either an S-Video signal with separated luma and chroma components on connector JD1, or a CVBS signal on connector JD2. The unused analog inputs are grounded by a capacitor, to prevent distortion.

The decoded video is provided in 4:2:2 format as 8 bit wide data stream D1 format. The data are clocked by the LLC as V_SY3. The HREF or the HS can be assigned to the output signal V_SY1 by selector JP2. The V_SY0 contains the signal VS. The input signal FEIN is used, when video data buses are merged. The edges of LLC signal are damped by resistor RV20. It can be switched off by disassembling the resistor.

3.4.1 Video Clock

IMPORTANT: The video section with its DMA channels will not operate correctly, if no video clock is provided. The internal control is operating on this clock!

3.4.2 Decoder selection: SAA7111A versus SAA7111

Decoder SAA7111A:

The supply voltage is VCC_VIP = 3.3V.
The analog inputs ports of the SAA7111A expect a reduced video input swing. Therefore the termination resistors combination has to adapt the video input swing to the IC inputs. The values are as drawn:
RV1 = RV3 = RV5 = 27R,
RV2 = RV4 = RV6 = 47R

Decoder SAA7111 (not implemented on the board):

The supply voltage is VCC_VIP = 5V.
The I2C bus input configuration of RV11, RV12, and UV2 is obsolete.
The video inputs are directly terminated by 75 Ohms:
RV1 = RV3 = RV5 = 0R (Obsolete),
RV2 = RV4 = RV6 = 75R

3.4.3 Layout considerations

The block of the video decoder should be placed on a separate ground plane. This concept is not completely realized, due to the required small placement area and the limited number of layers. The power supplies for the analog part and the digital one are separated and decoupled individually.
The +3.3V supply is generated from the +12V board supply. The decoupling capacitance should be realized by electrolytic and ceramic capacitors each with low inductance values. Instead of having a series inductance (LV2 of 2u2H) in the power rail, it is more recommended to use a simple series resistor of 4R7. For enhanced decoupling each pin might be decoupled individually by a RC-combination of 47nF and 10 Ohm. Small SMD packages like 0805 are recommended.

The supply for the analog part of the decoder can be treated in a similar way. The series inductance LV1 is replaced by a resistor of 4R7. A good ground plane layout and a shielding of the analog video signals is very much recommended. Due to the very dense layout this is not completely realized.

A short between the analog ground and the digital ground close to the decoder has been foreseen, but it is not used.

3.4.4 Switching the SAA7111A OFF

In some cases it is necessary to switch off the internal video decoder. to let another video source operate to the port A of the SAA71146. For this case the actions are listed:

- Bring video data bus of SAA7111A into tri-state by pulling input pin FEIN from GND to VCC_VIP. This includes the removing of resistor RV8.
- Switch off the H and V sync signals and the CREF line by pulling input pin CE from VCC_VIP to GND. This includes the removing of resistor RV18.
- Remove resistor RV20 for disrupting the LLC clock line.
+ Introduce the new video signals, the new H and V sync signals, and the new clock signals of LLC and PXQ via VMI connector

For further details see section on “Non continuous video data streams to SAA7146A”.

3.5 Video Back End

The block consists of the digital video encoder SAA7185B with its peripheral components, the output filter stages, and an S-Video output connector.

The digital video encoder operates in master mode. The clock and sync signals are generated and provided to the data source. The encoded analog video signals are fed via an output filter stage to the SVHS connector JE1 and the CVBS connector JE2.

The sync signals are buffered by a 74F245, to decoupled the encoder when the signals are used on the sub-board. The active high VIDSEL signal, used at direct play-back mode (DM), keys the video data to a standard colour value provided by a SAA7185B register.

3.6 Video Switch Matrix

The Video switch matrix interconnects the SAA7146A with the video front end SAA7111A, the video back end SAA7185B, and the VMI 1.4 connector plus extended connectors for connecting a daughter-board to the SAA7146A. The switches itself are laid out as set of resistors.

For standard use the switches SW1 and SW4 are closed and assembled with zero ohm resistors.The switches SW2, SW3, SW5, and SW6 are open assembled with resistors in order to minimize the components.

3.7 Audio Input/Output

The audio data output stage comprises of two parts: the audio input and output stage with a TDA1309 and the head-phone amplifier TDA1308T, and the audio clock oscillator.

3.7.1 Audio Performance

The analog audio performance has been measured inside an operating PC in a direct looping. It results in a total harmonic distortion of only 75dBTHD inside the audio band.

3.7.2 Audio Clock

The audio clock is generated by a crystal oscillator (here 11.2896 MHz, resulting in a sampling frequency of 44.1KHz).The output signal is distributed via two inverters on the board. The inverters are used to prevent line reflection from the oscillator. For using an external oscillator this clock can be switched off at connector X1. For default operation **pin3 and pin 4 have to be bridged!**

IMPORTANT: The audio engines of the SAA7146A will not operate correctly, if there no audio clock provided at the input. The internal control is operating on this clock! This holds also for situations when the audio section is in slave mode.

3.8 DEBI Port

The DEBI port features a ISA bus like interface when using the Intel mode. It can also be switched into the Motorola mode. The read/write signals as well as the address latching and ready signal are connected to the VMI-connector. When latching the addresses, devices of the FAST series (e.g. 74F574, 74F04) have to be used, to comply to the DEBI bus timing.

3.9 GPIO Port

The GPIO port consists of 4 lines which can be uses for standard level I/O signals as well as interrupt inputs. On the board they are connected to the VMI-connector VC2, and to a LED driver. A logical-High of the I/O pin switches the LED ON.

3.10 Daughter Board Connectivity

The board is equipped with a VMI 1.4 (Video Modul Interface) connector. It features one video output port with the appropriate synchronization signals. It is important to remark that the synchronization signals can operate in both directions. This gives the opportunity for digital encoders to operate in master mode. The VMI 1.4 specification mentions only a output direction of the synchronization signals.

The extended VMI connector enables the possibility for video I/O, which is not foreseen in the VMI spec. These video lines can be connected either to the A-port or to the B-port of the D1 interface.

The addresses for the data interface are latched by a register. An additional connector houses the further signals like the upper 8 bit of DEBI port Address/Data bus. This allows full 16 bit-transfer for the daughter board devices.

Two additional digital audio connectors interface external audio devices.

In standard operation mode the video data from SAA7146A will be fed to the digital encoder SAA7185B. This mode is also called Direct mode. Beside this mode other modes, like Line-Memory-Mode, and Field-Memory-Mode, are supported by the SAA7146A. These modes might be useful for special situations. They can be implemented via the provided connectivity.

3.11 Power Supply

Power supply of the board is splitted in different sections. The 12V supply of the PCI edge connector is used to generate the decoupled 3.3V supply and the analog 5V supply for the digital decoder, the digital encoder and the analog audio supply. The 5V supply of the PCI edge connector is used for a general supply of all standard 5V devices and it is used to generate the 3.3V supply of the SAA7146A. The reason for this splitting of the power supply is to decouple all parts from the main PC supply as well as from each other. This supports the concept of local decoupling of function blocks. The noise content of the video from a visual inspection is very little. The decoupling for the analog signals seems to be optimal even with respect to the large amount of digital components.

3.12 JTAG Pins

The SAA7146A follows the “IEEE Std. 1149.1 - Standard Test Access Port and Boundary-Scan Architecture” set by the Joint Test Action Group (JTAG). Nevertheless a JTAG test procedure is not implemented on this board. Here some handling information:

- The TRSTN signal at pin 24 of SAA7146A should be connected to the PCI connector pin 1A, to comply to fully to the PCI specification.
- The pin TRSTN can, alternatively, be grounded to achieve the application mode.
- On the board the pin TRSTN is connected with the general PCI reset signal RSTN at pin 33 of SAA7146A. In this case the other test pins (TMS, TCLK, TDO, and TDI) should left open. The internal pull-up resistor prevent them from toggeling.

4. SW Structures

4.1 Architecture of 16 bit SW

The architecture of the 16 bit driver SW consists of the SAA7146.DLL and the SAA714x.VXD. The SAA7146.DLL has an object-oriented interface. The different high-level functional blocks like Video, DEBI, IIC, ArbCntrl, and EventCnt are operating in ring 3. Partly these blocks consist of several classes. They all access the HW of the SAA7146A via the IO class. The video classes are inherited from the scaler, and the clipper classes. The Event control resides in ring 3.

HW interrupts will be directly handled by the IO class.

The VXD SAA714x.386 is essentially responsible for the allocation of linear memory.

For details pls check the SAA7146A software description.

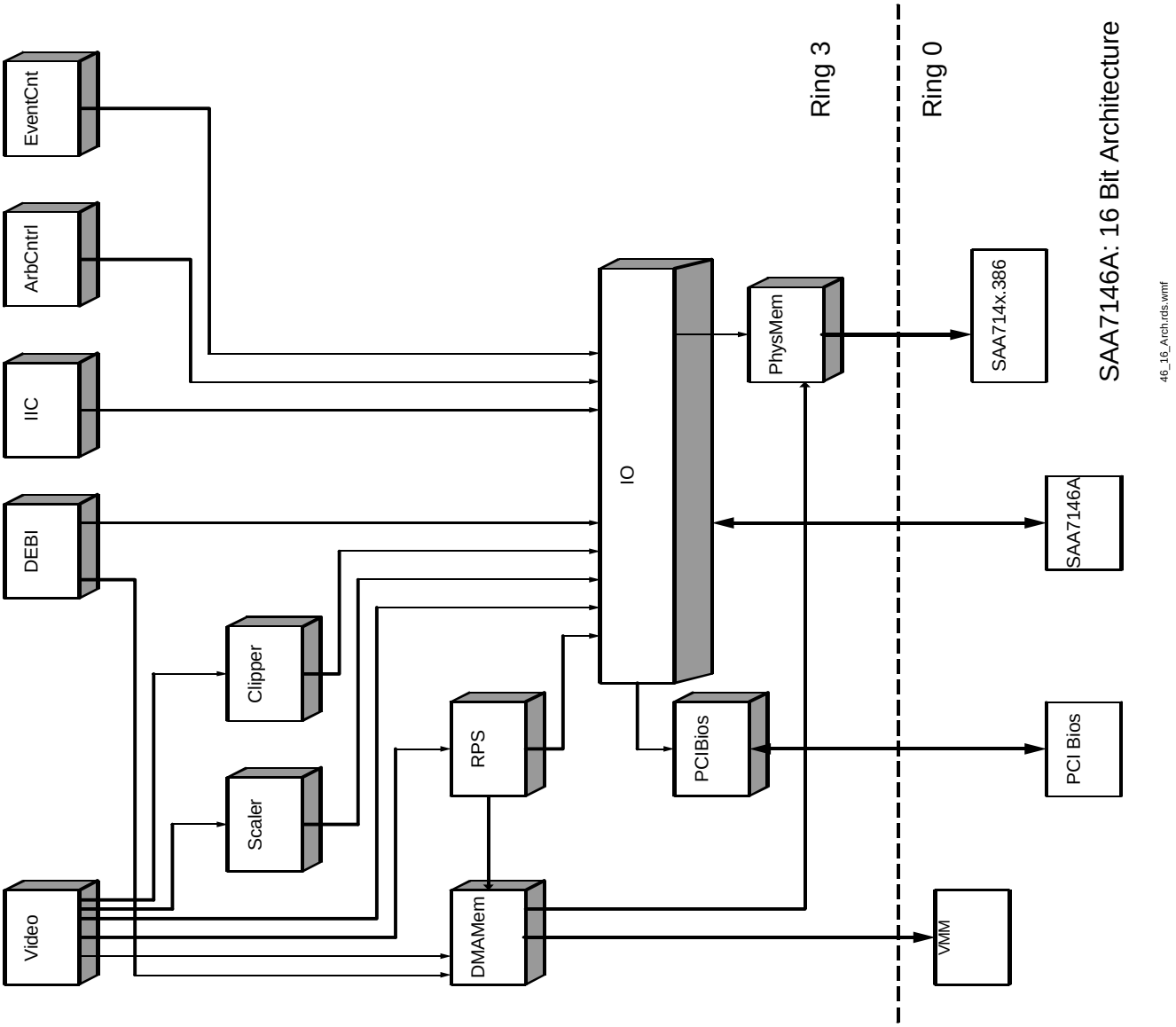


Fig.6 Architecture of 16 bit SW

4.2 Architecture of 32bit SW

The 32 bit architecture is different from the 16bit architecture in some parts. As in the previous version, one driver is operating in ring 3, while the other works from ring 0.

The access to the SAA7146A HW is done at ring 0 via the SAA7146.VXD. The HW interrupts are handled directly at the inner ring. An interface allows the access from other 3rd party VXDs.

The event control class is moved into the VXD with a remaining interface in ring 3. For faster access the DEBI class is also moved into ring 0, with similar constraints like the Event control class.

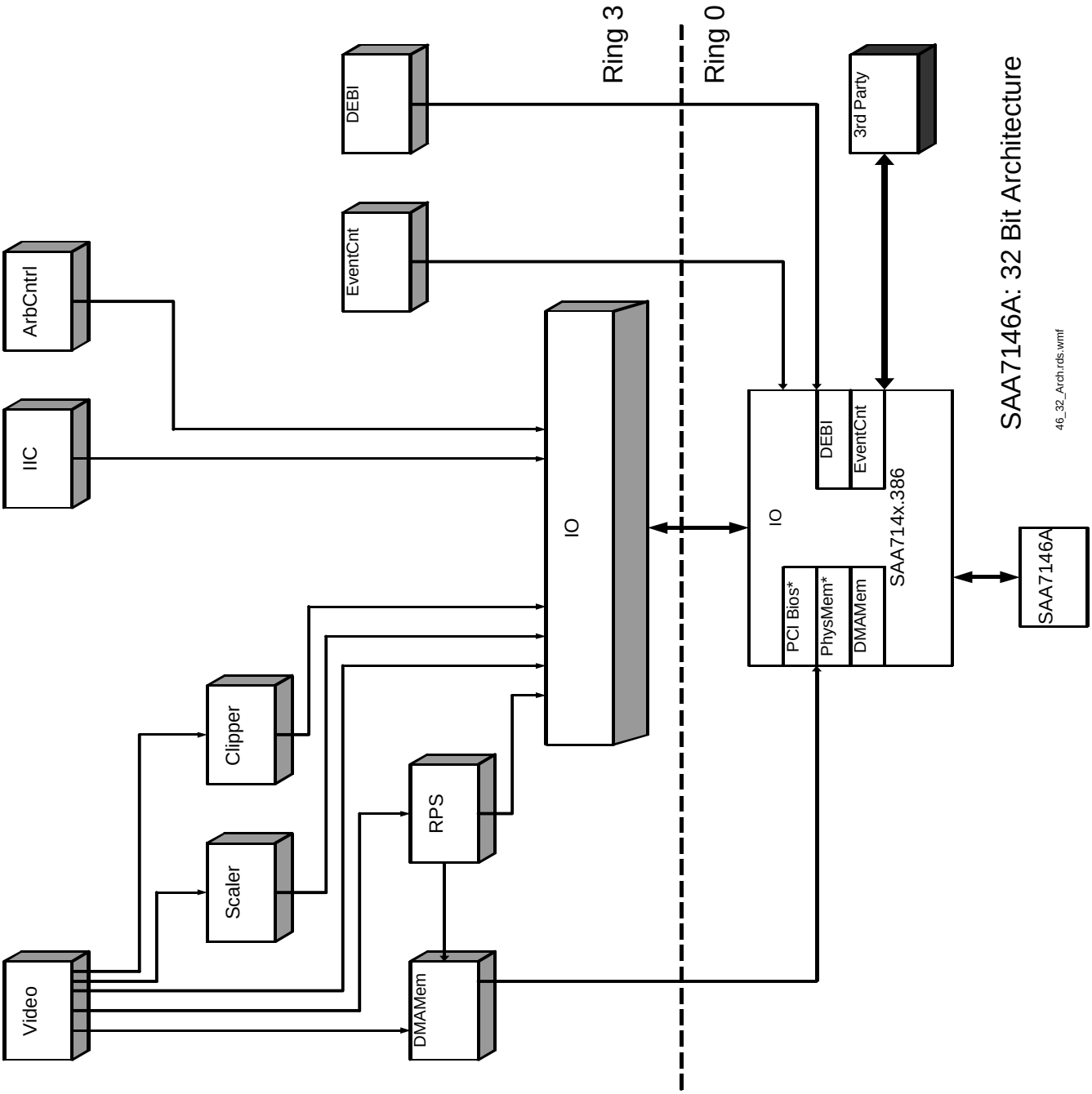


Fig.7 Architecture of 32bit SW

4.3 Architecture for Video-for-Windows with Intercast

The picture shows the general outline for a Video-for-Window architecture including Intercast.

Philips provides to this architecture the Video Capture driver with the Intercast extension. The driver controls the DecHAL (HAL = Hardware Abstraction Layer). and the SAA7146 HAL. The DecHAL is the existing DMSD46.DLL, while the SAA7146 HAL refers to the SAA7146.DLL. An extension accesses the VBI Decoder VXD provided from INTEL.

The control of the tv-tuner is split into two functions. One is the overall control and the second is the access to the tuner HW. The interface to the tuner control DLL in application specific.

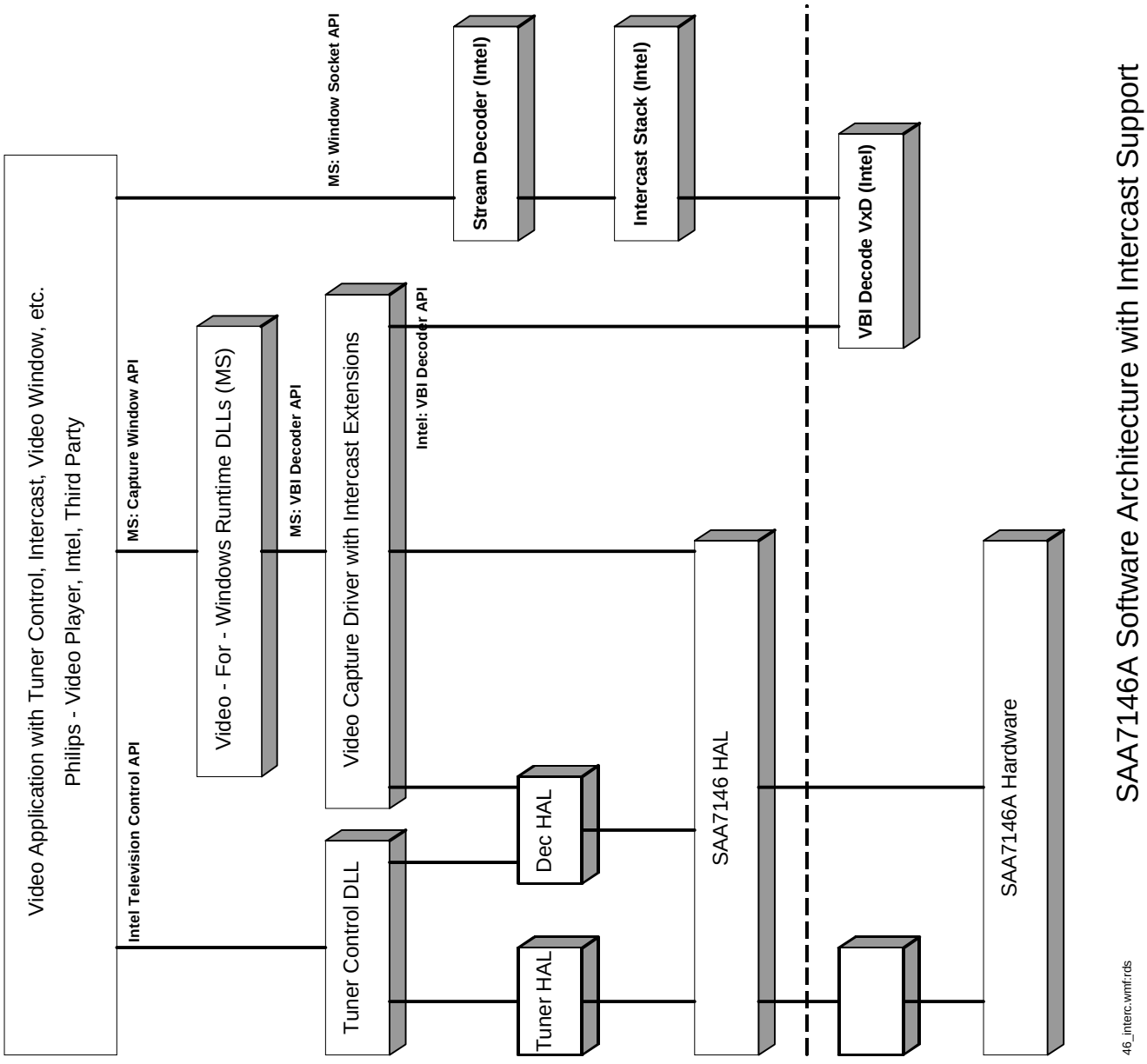


Fig.8 Architecture for Video-for-Windows with Intercas

5. Applications

5.1 Continuous Video Data from Video Decoder Saa7111A

The default for video capture is an 8 bit video data bus sourced from the SAA7111A to the SAA7146A. The clock LLC (27 MHz) is provided by the SAA7111A. The sync signals are fed on their lines to the SAA7146A. It is no CCIR656 data stream expected in terms of decoded synchronisation information.

The following figure explains the used internal structure of the SAA7146A video engine. It makes clear that beside the video capture also the video play-back is possible on the same structure. While the active data and signal pathes are drawn in bold lines, the inactive ones are drawn in small lines.

Video Capture: the video data is coming from the D1_A port and is fed via the input multiplexer to the HPS (HPS = High Performance Scaler) as 8 bit wide video data stream. The luma and chroma values are multiplexed, due to CCIR656 specification. After the appropriate scaling, modification of contrast, brightness, and saturation, clipping of unused parts, and colour space conversion, the data is transferred to FIFO1. FIFO1 collects the data from the HPS and bursts them to their drain destination (system memory or VGA memory) under control of the PCI bus arbitration.

FIFO2 contains the clipping data for the HPS.

The sync signals of H and V, and the clock are selected by the appropriate multiplexers. The pixel qualifier PXQ_A is not used for the default case. It has to be set to high state.

Video Play-Back: The video data is placed from the PCI-bus source into FIFO3 under bus master control of the SAA7146A. From FIFO3 the data is transferred to the BRS (BRS = Binary Ratio Scaler) to provide an up scaling of the 8 bit multiplexed video data. (A down scaling is only possible in inbound mode.) The local control of the video data (here in Direct mode) is done under the sync signals of H and V, and the clock LLC_B. A Philips digital video encoder DENC (here a e.g. SAA7185B) provides these signals with its necessary high performance time accuracy. The pixel qualifier PXQ_B accompanies the active video data. (In Direct mode the signal PXQ_B is the KEY signal.)

The drawn case, the video input (video capture) and the video output (Video Play-Back) operate independently. The video engines of the SAA7146A provide a strong capability to enable both features simultaneously, nevertheless the need a certain support from the rest of the system. Early PCI-chip sets and early PCI VGA boards might not follow completely to PCI requirements. This can have some impact on the combined video performance.

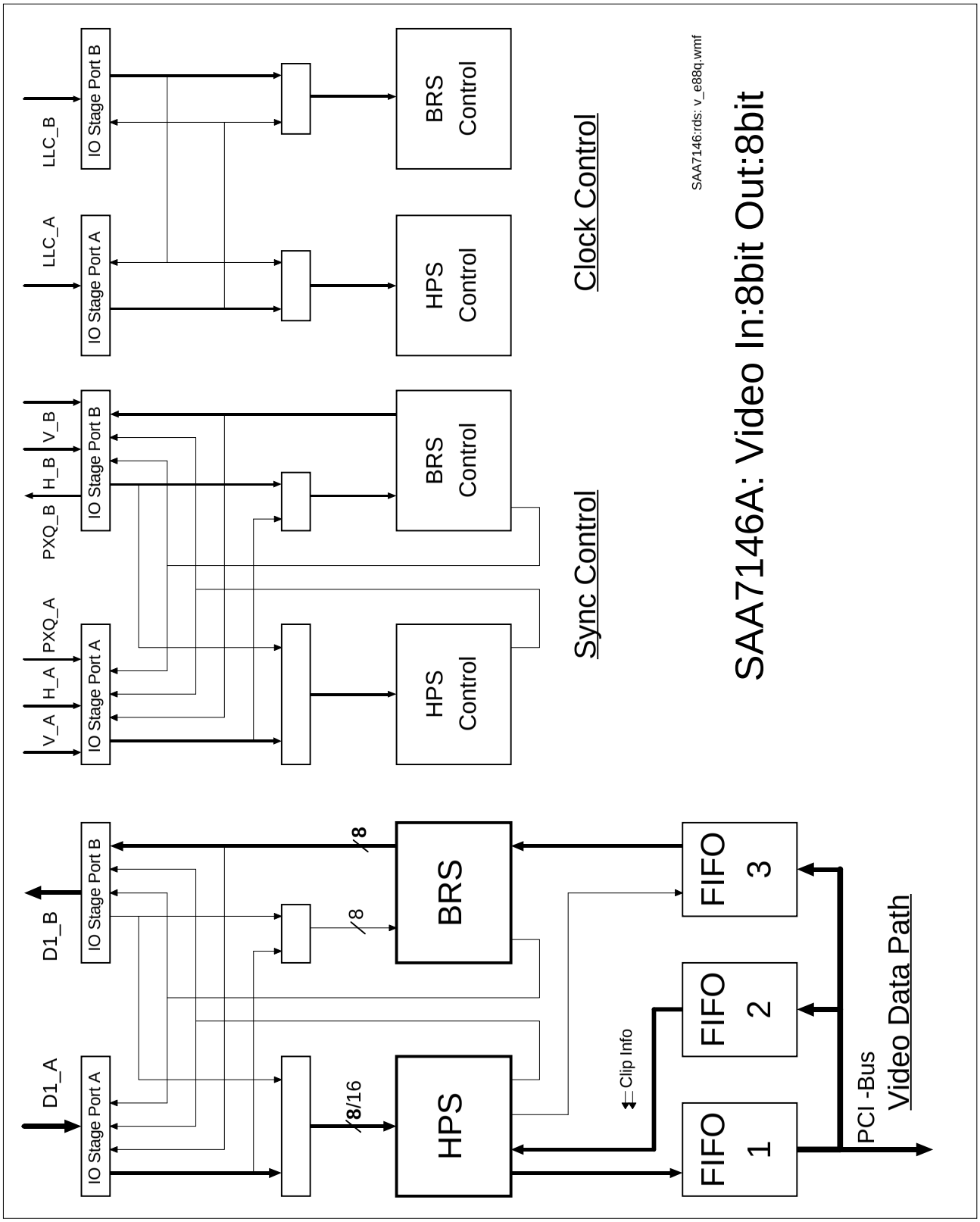


Fig.9 Video Engines: Concurrent Recording and Play-Back

5.2 Scaling Non-Continues Video Data from an Local Device to another Local Device

This case discusses the possibilities of using a non-continuous video data stream, scale the video data with the means of the HPS and send the scaled video out of the other port to another video device. The use of the SAA7146A video engine is drawn in the following figure. The change of the video data paths on a field-by-field base is possible, but will not be discussed.

The video data might come from a MPEGx decoder via the VMI connectors. The drain of the video data is e.g. a video port of e.g. a VGA. The video data enters at port D1_A the SAA7146A. The multi standards decoder SAA7111A has to be switched off for this, to disable any interference. Pls see also section 'Video Front End' for further details. The non-continuous video data are selected by the pixel qualifier PXQ_A before feeding them into the HPS. After the scaling process, only down scaling is available, inside the HPS, the data are provided to the D1_B port. They are validated by the pixel qualifier signal PXQ_B aside to the sync signals H_B and V_B. The clock line LLC_B is derived from the input clock LLC_A.
It has to mentioned, that the video output sequence of Y, CR, Y, and CB is always correct in terms of CCIR656 standard. But the length of active and inactive data bursts is arbitrarily, and may go down to only two or three byte! When using the PCI-bus transfer, the FIFO structure only buffers the active video data. This gives a continuous data stream again, for PCI-bus transmission.

Aside to the mentioned modification on the HW part also some small modification on the SW have to be done.

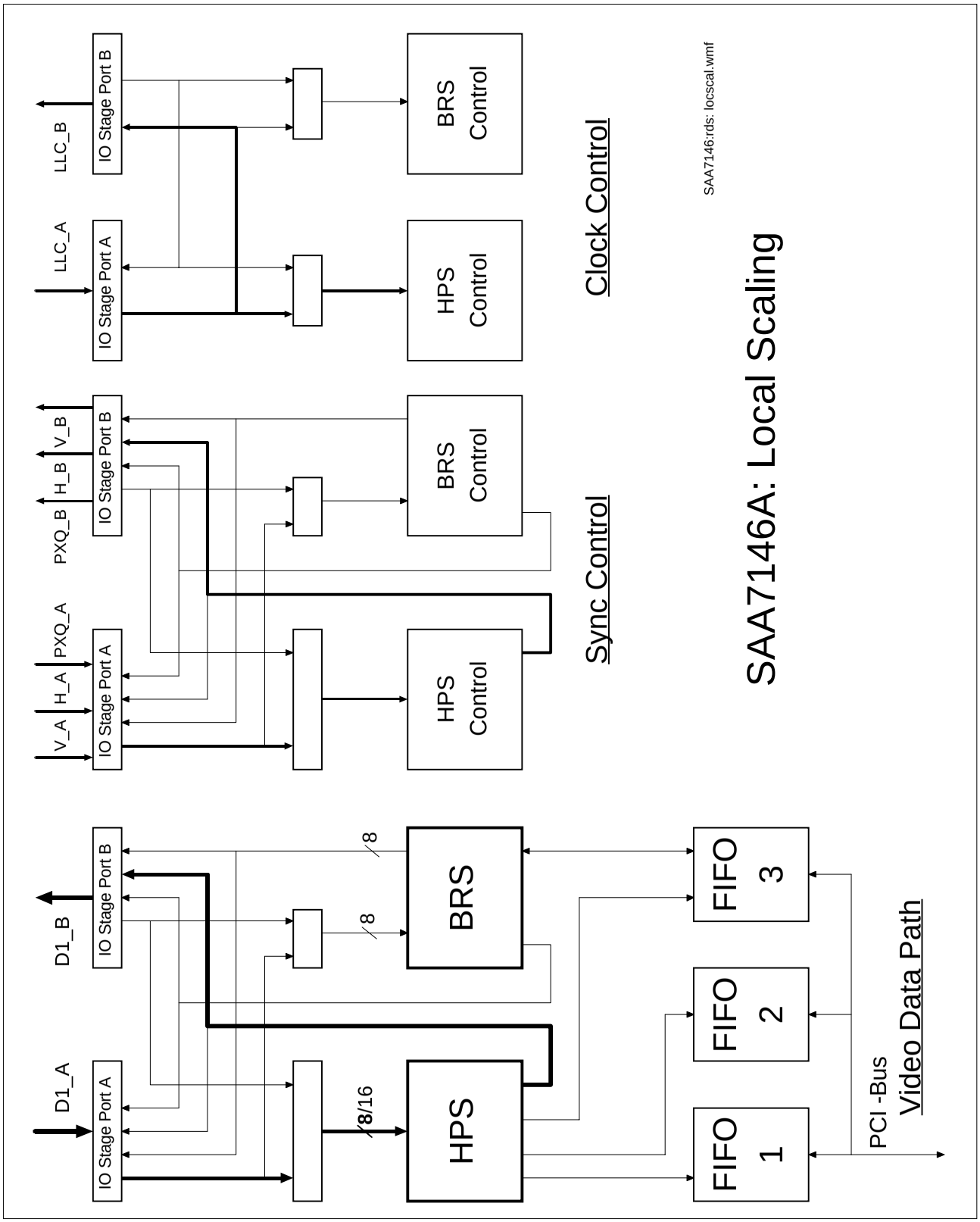


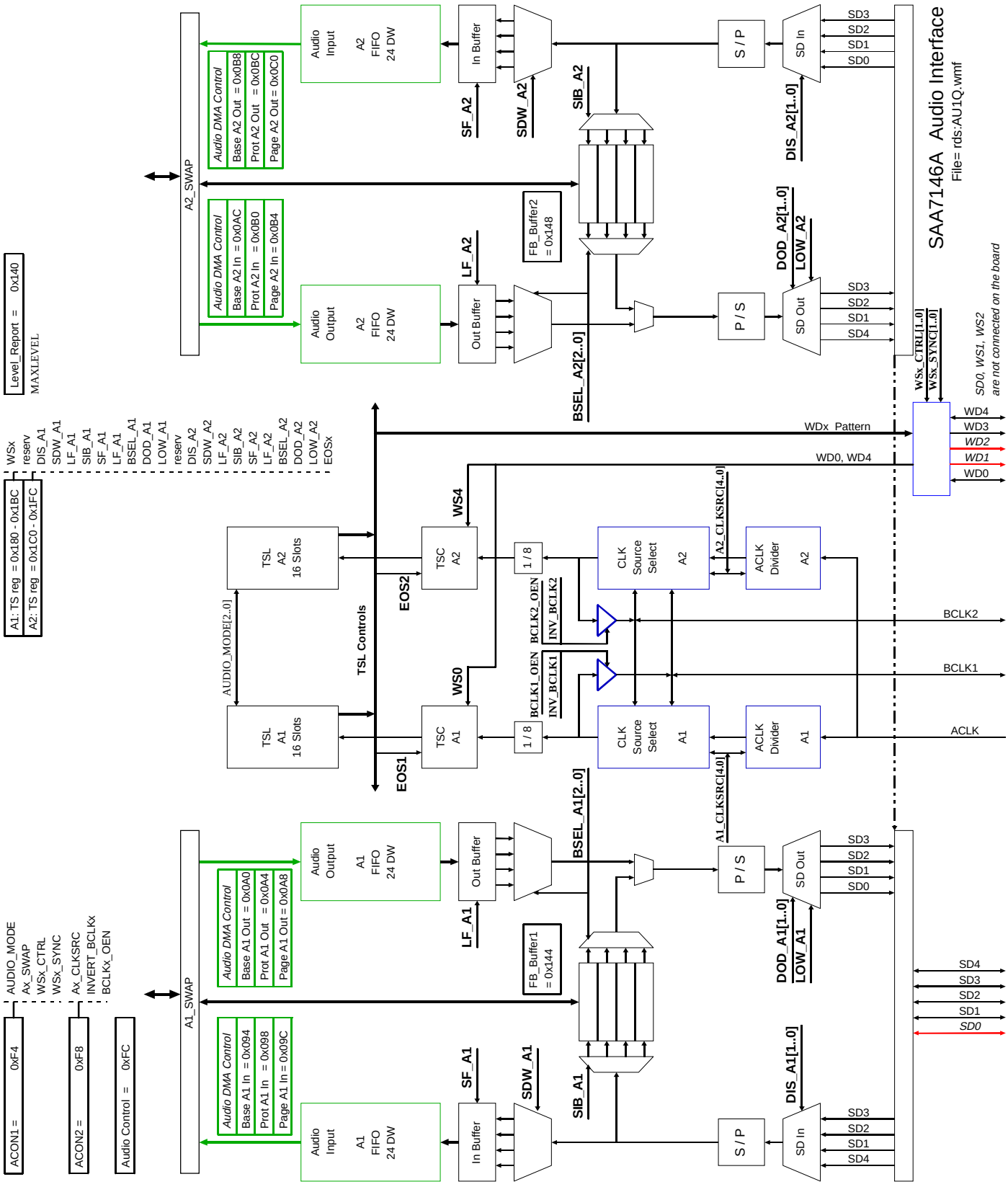
Fig.10 Video Engines: Local High Performance Scaling

5.3 Audio engines

The following figure explains the structure of the two audio engines. They can operate independently or combined.
The feed-back buffers between the input and output section of the audio engines can be read at every time. The write access is only possible when the audio engine is inactive.

The signal lines WD1, WD2, and SD0 are not fed to a special connector pin.

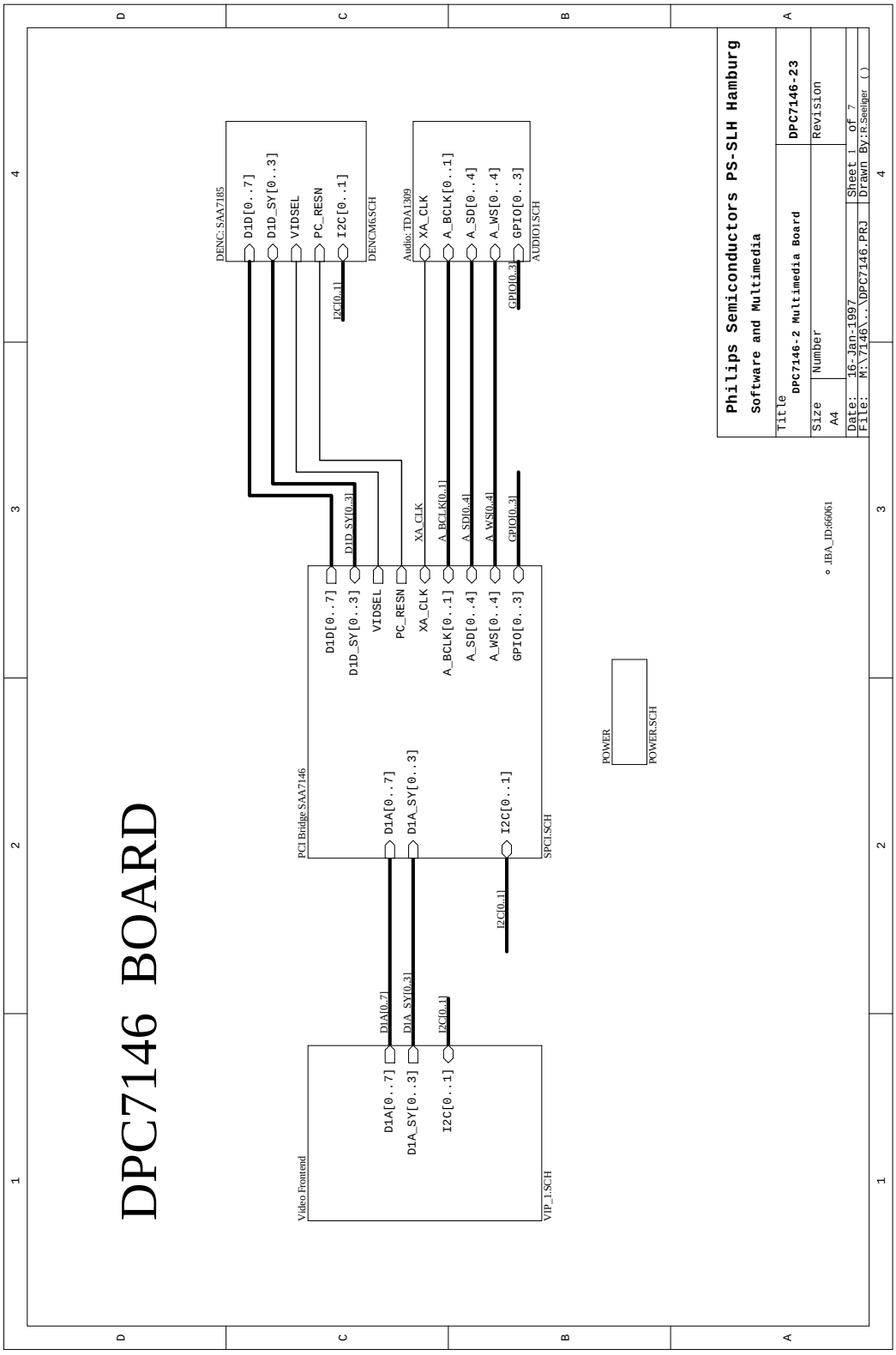
Fig.11 Audio Engines



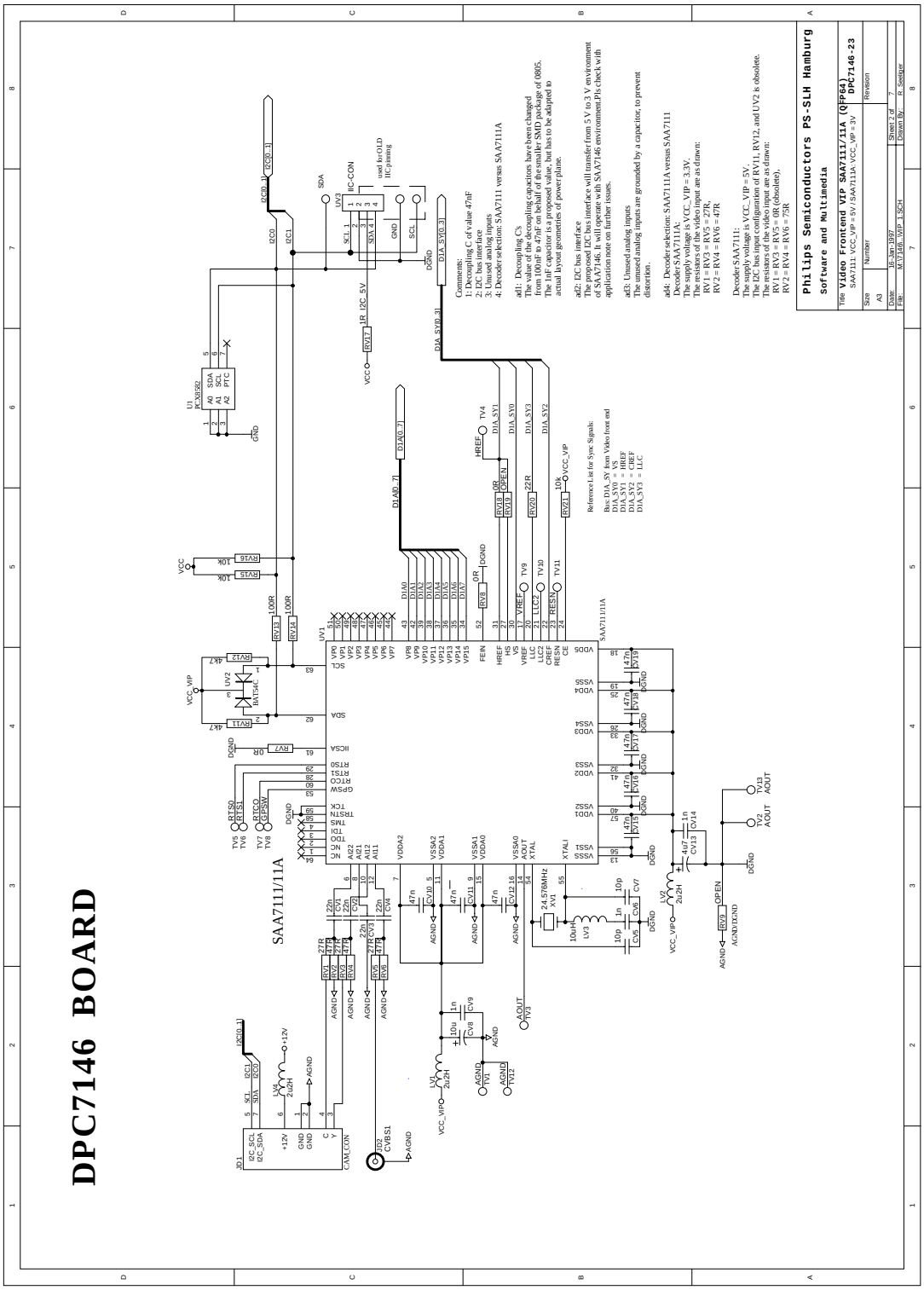
APPENDIX 1 Schematics

The following pages contain the complete set of board schematics.

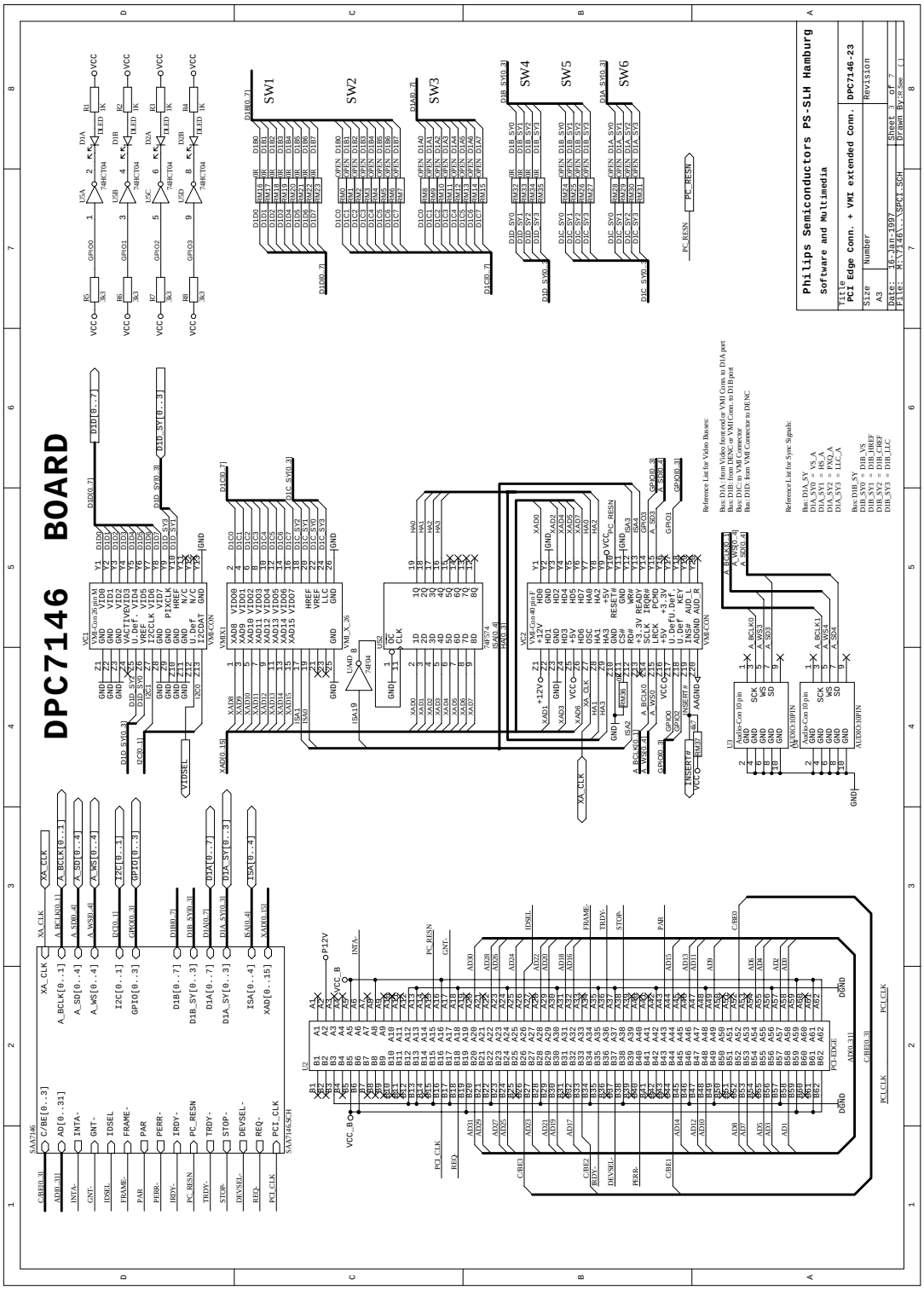
DPC71462.eps



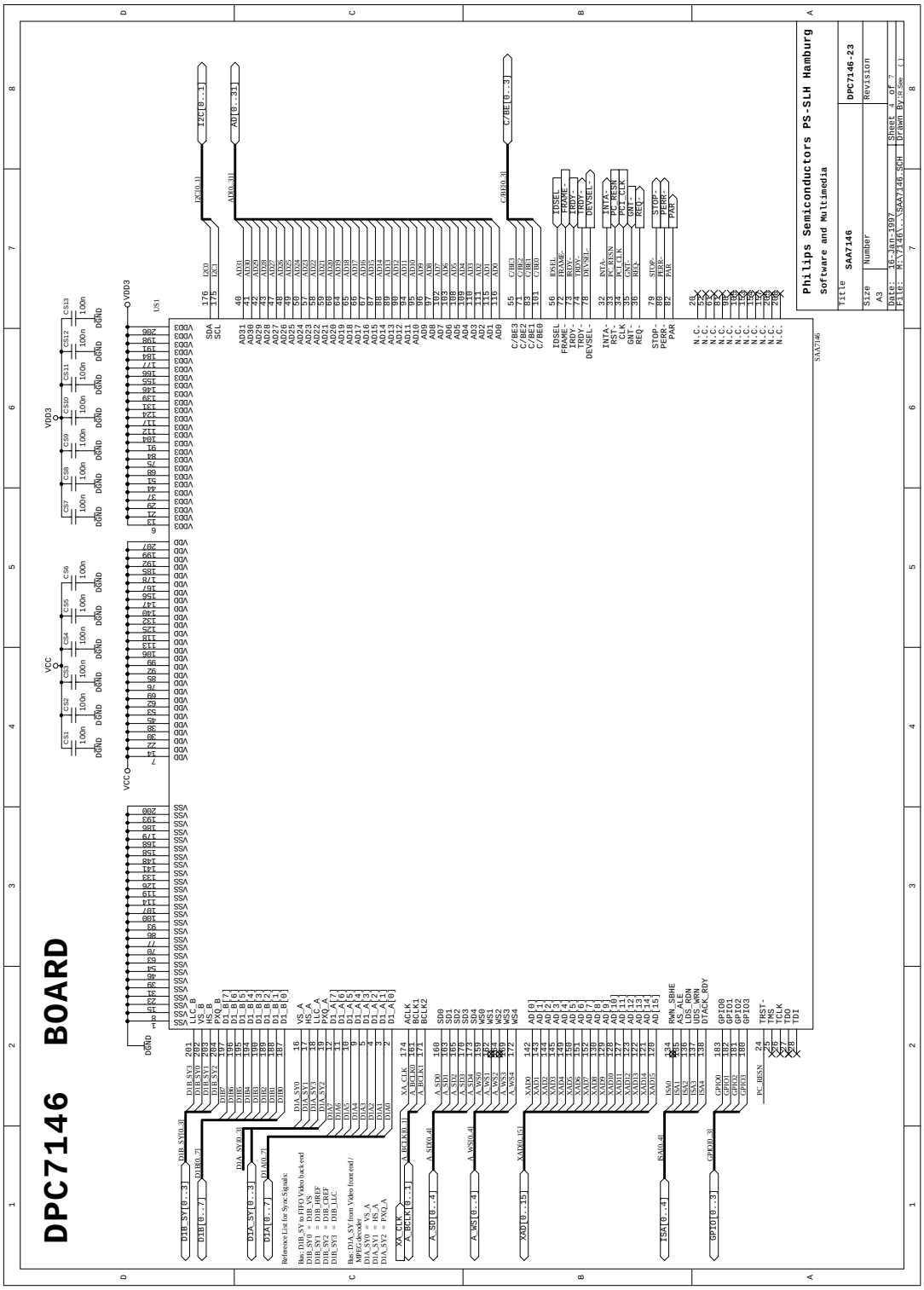
VIP.eps


DPC7146 BOARD
SAA7111/11A
Philips Semiconductors PS-SLH Hamburg
Software and Multimedia
Video Frontend VIP SAA7111/11A (QFP64)
DPC7146-23
SAA7111: VCC_VIP = 5V / SAA7111A: VCC_VIP = 3V
Size A3
Number
Revision
Date 6. Jan 1997
Sheet 1 of 7
File M:\7146_VIP_1.SCH
Drawn By: R. Seelige
Comments:
1: Decoupling C of value 47nF
2: I2C bus interface
3: Unused analog inputs
4: Decoder selection: SAA7111 versus SAA7111A
ad1: Decoupling Cs
The value of the decoupling capacitors have been changed from 100nF to 47nF on behalf of the smaller SMD package of 0805. The 1nF capacitor is a proposed value, but has to be adapted to actual layout geometries of power plane.
ad2: I2C bus interface
The proposed I2C bus interface will transfer from 5 V to 3 V environment of SAA7146. It will operate with SAA7146 environment.Pls.check with application note on further issues.
ad3: Unused analog inputs
The unused analog inputs are grounded by a capacitor, to prevent distortion.
ad4: Decoder selection: SAA7111A versus SAA7111
Decoder SAA7111A:
The supply voltage is VCC_VIP = 3.3V.
The resistors of the video input are as drawn:
RV1 = RV3 = RV5 = 27R,
RV2 = RV4 = RV6 = 47R
Decoder SAA7111:
The supply voltage is VCC_VIP = 5V.
The I2C bus input configuration of RV11, RV12, and UV2 is obsolete.
The resistors of the video input are as drawn:
RV1 = RV3 = RV5 = 0R (obsolete),
RV2 = RV4 = RV6 = 75R
Reference List for Sync Signals:
Bus DIA_SY from Video front end
DIA_SY0 = VS
DIA_SY1 = HREF
DIA_SY2 = CREF
DIA_SY3 = LLC
SAA7111/11A
XTALI
24.576MHz
VCC_VIP
I2C_5V
VCC
DGND
AGND
SDA
SCL
I2C0
I2C1
IIC-CON
used to OLD IIC-planing
CAM_CON
+12V
CVBS1
AOUT
OPEN

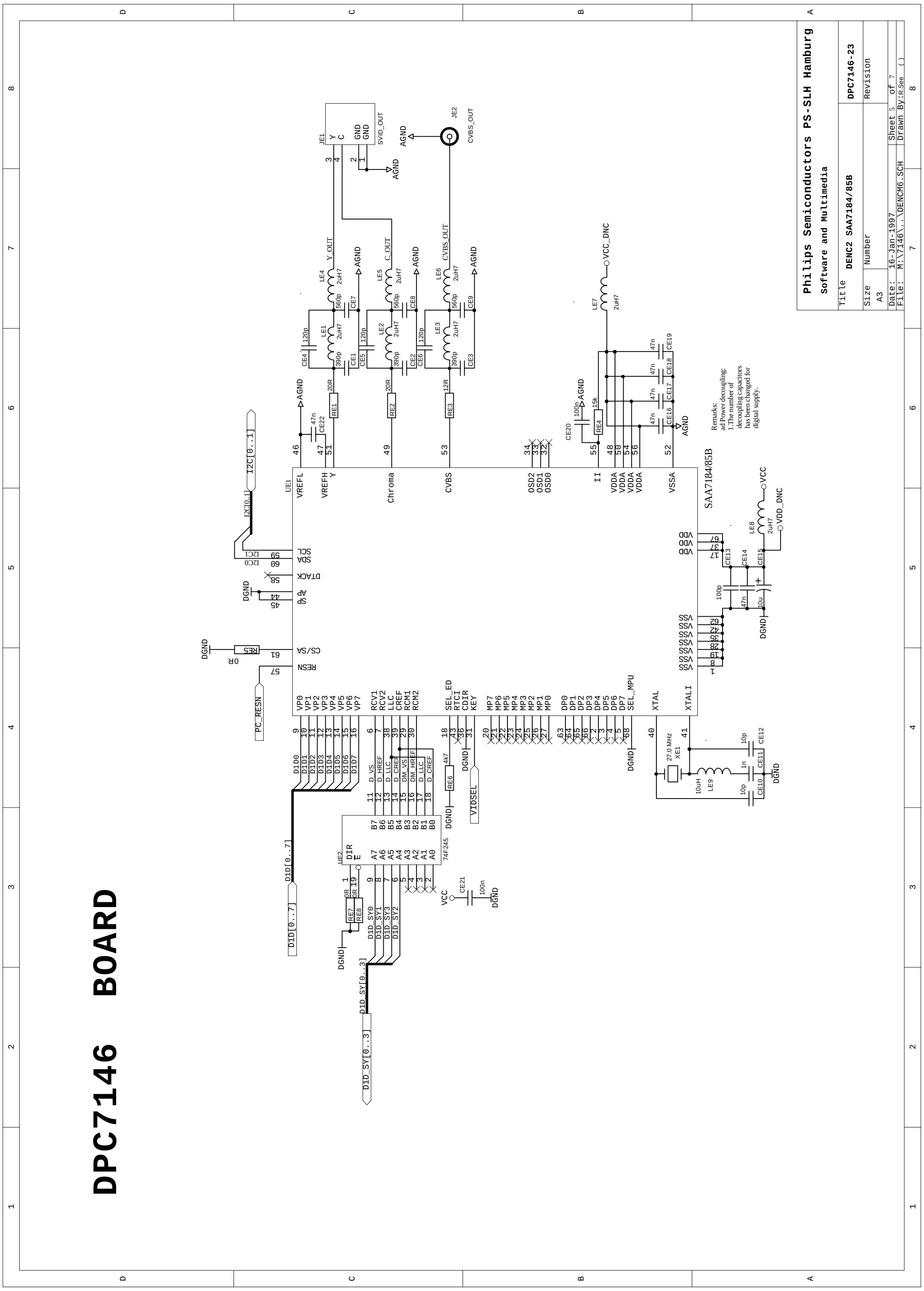
SPCI.eps


DPC7146 BOARD
SW1
SW2
SW3
SW4
SW5
SW6
Philips Semiconductors PS-SLH Hamburg
Software and Multimedia
PCI Edge Conn. + VMI extended Conn.
DPC7146-23
PC_RESN
XA_CLK
P12V
VCC_B
PCI_CLK
PCI-EDGE
AUDIO-10PIN

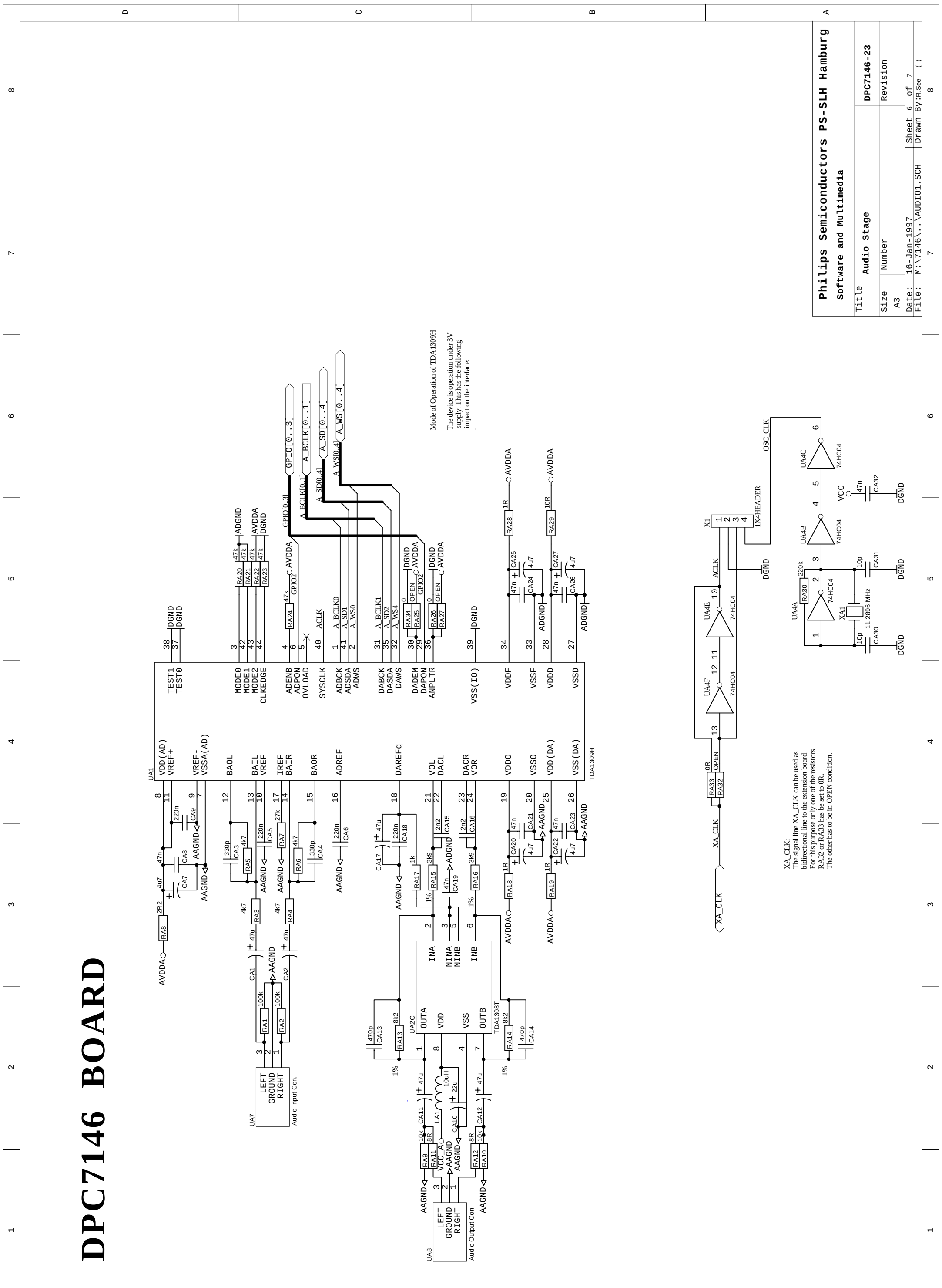
SAA7146.eps


DPC7146 BOARD
Philips Semiconductors PS-SLH Hamburg
Software and Multimedia
DPC7146-23
SAA7146
SAA7146

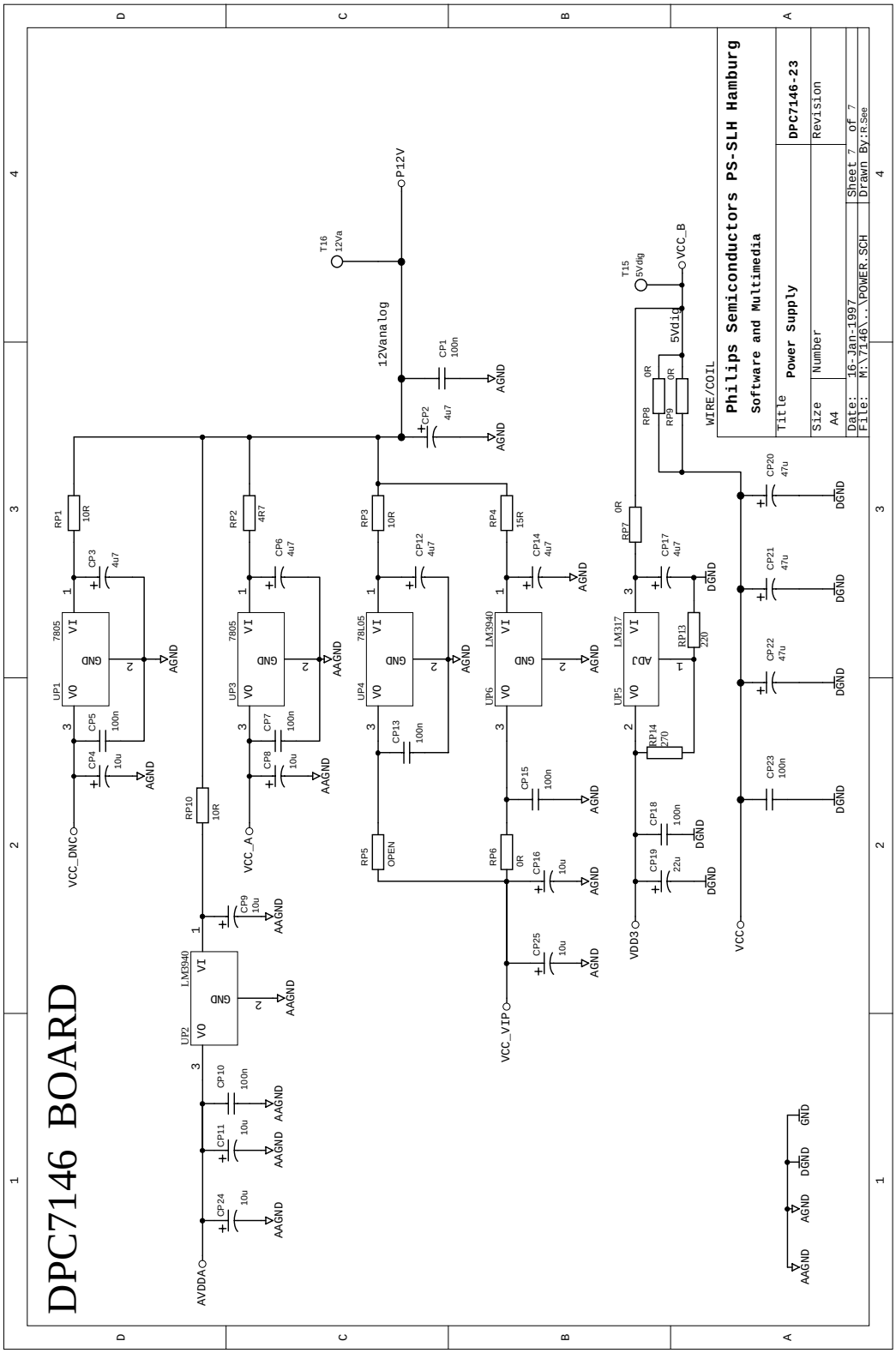
DENC.eps


Philips Semiconductors PS-SLH Hamburg
Software and Multimedia
Title DENC2 SAA7184/85B
DPC7146-23
SAA7184/85B
DPC7146 BOARD

AUDIO.eps


DPC7146 BOARD
Philips Semiconductors PS-SLH Hamburg
Software and Multimedia
Title Audio Stage
Size A3
Number DPC7146-23
Revision
Date: 16-Jan-1997
Sheet 6 of 7
File: M:\7146\..\AUDIO1.SCH

POWER.eps


DPC7146 BOARD
Philips Semiconductors PS-SLH Hamburg
Software and Multimedia
Title Power Supply
DPC7146-23
Size A4
Number
Revision
Date: 16-Jan-1997
File: M:\7146\...\POWER.SCH
Sheet 7 of 7
Drawn By:R.See
WIRE/COIL
P12V
12Vanalog
5Vdig
VCC_B
VCC_DNC
VCC_A
VCC_VIP
VDD3
VCC
AVDDA
AGND
AAGND
DGND
GND