APPLICATION NOTE

Digital Video Encoder Module System: 7120/21MOD2

AN 97086

Philips
Semiconductors

PHILIPS

Module System: 7120/21MOD2

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Abstract

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The Digital Video Decoder converts an analog video input signal into a digital output signal. This signal can be processed by a wide range of applications and fed to the Digital Video Encoder, which delivers analog video signals to TV receivers or video cassette recorders.

This note gives a detailed description of the schematics and some hints how to design the PCB (Printed Circuit Board) with mixed analog and digital signal processing.

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Digital Video Encoder Module System: 7120/21MOD2

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Summary

This application note is intended to provide application support for Philips´ Digital Video Decoders and Encoders. It contains a description of one evaluation board as well as I²C-bus programming of the respective device.

The Digital Video Decoder converts an analog video input signal into a digital output signal. This signal can be processed by a wide range of applications and fed to the Digital Video Encoder, which delivers analog video signals to TV receivers or video cassette recorders.

This note gives a detailed description of the schematics and some hints how to design the PCB (Printed Circuit Board) with mixed analog and digital signal processing.

CONTENTS

1. Introduction

The Digital Video Decoder/Encoder Modules provide the basis to evaluate various Philips Digital Video Decoders and Encoders and give the opportunity to simply insert the modules into customized applications and systems.

On the following pages the assembly and function of a Digital Video Encoder Module is shown. The module can operate in stand alone mode (colourbar generator) as well as extension to other systems like PCI-bridges, MPEG decoders or Video input/output systems.

The module has a socket for an I²C-bus EEPROM (e.g. PCF8582, PCF8594, PCF8598, X24164) in order to store data for initialization and for simple control functionality operated by a (future) microcontroller module.

Software for IBM compatible personal computers enables access to all features and settings of the devices. It handles the I²C-bus via a printer port adaptor. This adaptor and a fitting cable is part of the accessory.

This modular concept was designed to combine different video decoders with various video encoders. Some modules (e.g. the 7128MOD2) can be configured for several devices and packages without the necessity of having a new PCB. This could be achieved by using multiple footprints for one IC and some configurational parts. For interfacing a 96-pin module connector is used.

The modules need a 5V analog and a 5V digital supply voltage. A respective power connector is placed at each backend (encoder-) module whereas frontend modules are supplied via the 96-pin module connector.

If necessary, an internal voltage regulator generates the required 3.3V onboard. Alternative it’s also possible to bypass the regulators on some encoder modules and connect 3.3V supply directly to the respective pins. You can find a fitting power connector cable as a part of the accessory as well.

2. Digital Video Encoder Module 7120/21MOD2

The digital encoder module 7120/21MOD2 contains the encoder type SAA7120 (with Macrovision Pay-per-View copy protection) or SAA7121 (without copy protection) in the QFP44 package. Both are 3.3V devices.

The circuit accepts CCIR compatible YUV data with 720 active pixels per line in 4 : 2 : 2 multiplexed formats, for example MPEG decoded data.

The digital data is fed via the 96-pin input connector to the 8bit wide input port. For interfacing an ECL - TTL converter can be used (accessory).

After passing the analog postfilters (to disable with jumper) the output signal is available simultaneously in CVBS and Y/C format at the respective connectors.

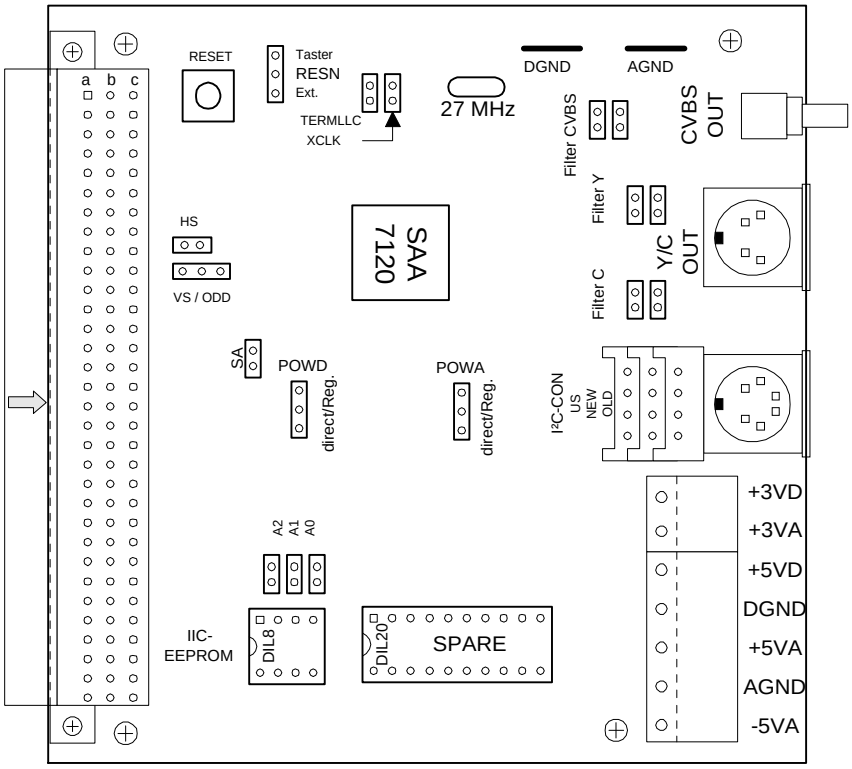


Fig.1 Location of ICs, jumpers and connectors on the 7120/21MOD2 PCB

Fig.1 shows the location of IC's, jumpers and connectors on the application module 7120/21MOD2. The function of the used connectors is described on page 10 and following. The function of jumpers is shown in a jumperlist on page 15.

2.1 Power supply

The +5V analog and digital power supply should be kept separate at the power connector. Analog and digital ground must be connected once near the power supply units.

The 3.3V supply pins at this connector are optional. When using the on board regulators (JP18, JP24 in the position 'Reg.'), these pins are not connected. Because of some pullup resistors, measurement of current consumption is not possible here.

A negative voltage (-5V) is one part of the MPC module system supply voltages but is not necessary for this application.

All supply voltages are available at the VG96 input connector according to the pinning on page page 10.

2.2 Reset

There are two different ways to reset the device:

Using this module in conjunction with a MPC decoder module, preferably the 'Reset Not' generated by the decoder should be used (JP13 = Extern). Therefore a dedicated pin exists at the VG96 input connector.

In case of a stand alone operation (e.g. colourbar generator) or in conjunction with other systems the Reset pushbutton can be used (JP13 = Taster).

During reset (RESN = LOW) and after reset is released, all digital I/O stages are set to input mode. A reset forces the I²C-bus interface to abort any running bus transfer and sets register 3A to 03H, register 61 to 06H,registers 6BH and 6EH to 00H and bit TTX60 to 0. All other control registers are not influenced by a reset.

2.3 Input- and Output- Connectors

2.3.1 VG96 Input Connector

TABLE 1 Pinning of the VG96 module input connector (bottom view)

IN	a	b	c
32	-5V ANALOG		
31	GND ANALOG		
30	+5V ANALOG		
29	GND DIGITAL		
28			
27	+5V DIGITAL		
26			
25	SDA	RESN	SCL
24			
23			
22			
21			
20			
19			
18			
17		LLC	
16		ODD	
15			
14			
13		RTCI	
12		VS	
11		HS	
10			
9			
8	MP7		TTXRQ
7	MP6		TTX
6	MP5		RCV2
5	MP4		RCV1
4	MP3		
3	MP2		
2	MP1		
1	MP0		

TABLE 2 Description of signals located at the VG96 module input connector

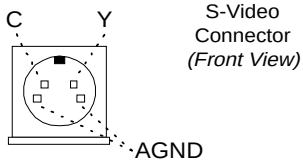
Signal	Specification
SDA	I^2C-bus serial data.
SCL	I^2C-bus serial clock.
RESN	Reset Not Input (active LOW). After Reset is applied, all digital I/O's are in input mode. The I^2C-bus receiver waits for the START condition.
MP (7..0)	MPEG port. Input for CCIR 656 style multiplexed Cb, Y, Cr data.
LLC	Line Locked Clock. This is the 27 MHz master clock for the encoder. The I/O direction is set by the CDIR pin.
HS	Horizontal Synchronous signal for synchronization via RCV2(JP11).
VS	Vertical Synchronous signal for synchronization via RCV1 (JP10).
ODD	ODD/EVEN Field Identification, for synchronization via RCV1 (JP10).
RCV1	Raster Control 1, the connected Encoder pin provides or receives a VS, FS or FSEQ signal.
RCV2	Raster Control 2, this pin provides an HS pulse of programmable length or receives an HS pulse.
RTCI	Real Time Control input. If the LLC clock is provided by a digital video decoder like SAA7111A, supporting this function. RTCI should be connected to the RTCO pin of the respective decoder to get information concerning actual subcarrier, PAL-ID, and more, depending on the video decoder.
TTXRQ	Teletext Request output, indicating when bit stream is valid.
TTX	Teletext bit stream input.

2.3.2 CVBS Output Connector (BNC, Subclick or Cinch)

This CVBS-output can be as a BNC, Subclick or Cinch- Connector because of a special footprint. Between device output and connector there is a MHz LOWPASS FILTER that can be switched off with jumpers (JP5,JP6).

2.3.3 Y/C Mini DIN Connector

The analog Y/C output signal is available at this connector. Like the outputs of the other D/A converters the signal is fed through analog postfilters to the connector.



S-Video
Connector
(Front View)

2.4 I²C-Bus

Two I²C-bus slave addresses are selected:

88H: LOW at pin SA (JP14 closed)

8CH: HIGH at pin SA (JP14 open)

On the Encoder Module 7120/21MOD2 a circuit was implemented to allow the connection of the internal 3.3V I²C-bus to an external 5V I²C-bus connected via the 4pin STOKO connector or 6pin Mini Din (the external I²C-bus has to provide its own pull-up resistors). The circuit also operates with 3.3V levels on the system connector, but if no level conversion is necessary, the circuit can be removed (R5, R6, Q1, Q2) and bypassed (Drain-Source).

Please note that there are no additional pullup resistors on this board. So supply of the I²C-bus must be done one time at the (single master-) I²C-bus interface.

The N-channel enhancement mode vertical D-MOS transistors Q1 and Q2 allow the bi-directional I²C-bus operation while shifting the levels. If the bus lines are pulled high (e.g. I²C-bus is inactive) the transistor is in high ohmic state (V_{GS} ~ 0V). If the Source is pulled to GND (3.3V side), V_{GS} exceeds $V_{GS(th)}$ and the transistor conducts so that the Drain is also forced to the level of the Source (low). If the Drain is pulled to GND, the parasitic diode conducts and the Source is also pulled down.

The lower the voltage on the I²C-bus, the more important is the threshold voltage $V_{GS(th)}$ of the transistor. For 3.3V environment, several types can be used (e.g. BSS123 in SOT123). For lower voltages it is recommended to use e.g. BSS138 (SOT123) or BS108 (TO92).

A new Single Master Interface with the IC 74HC9114D can be used, it replaces the former Single Master Interface with the IC 74LS05, which is only suited for 5V. The new interface operates on the I²C-bus from 1,8V to 5V.

On this backend module, two connectors can be used for I²C-bus control (alternative). The first one is a 6pin Mini DIN connector with the pinning shown on the right side of Fig.2. In order to consider different existing pinnings, the STOKO connector has a combifootprint for the standards 'Old', 'New' and 'US'. Please note that modules from the Philips Application Lab. Hamburg use the norm 'NEW' while the default configuration of the MPC module system is 'OLD'.

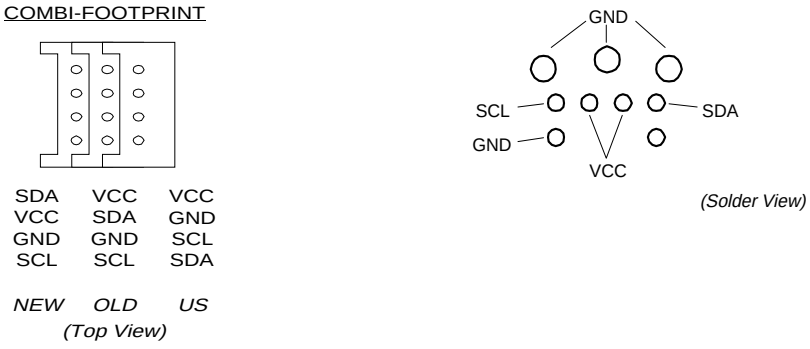


Fig.2 Pinning of I²C-STOKO and Mini-DIN connector

2.5 I²C EEPROM

A DIL 8 socket on each module is for adding an EEPROM with I²C interface in order to store data for initialization and simple control functionality operated by a (future) microcontroller module. Several EEPROM types can be assembled depending on their memory size (e.g. PCF8582, PCF8594, PCF8598, X24164). Additionally the I²C-bus device address can be adapted by using the jumper 1..3 (EEP-Adr).

2.6 Clock- and Synchronization signals

There are two operating modes for the SAA7120/21. In master mode, H- and V- signals are output of the RCV2 and RCV1 pins in order to synchronize an external source, e.g. a memory or Teletext.

In slave mode the synchronization signals H and V are generated out of the frame sync code embedded into the CCIR-656 data stream or fed to the encoder via RCV1 and RCV2 after passing JP10, 11. The configuration of RCV1 and RCV2 (direction, polarity etc.) is handled in Reg. 6BH (Some information about registerfunctions can be found on page 20). After a reset the RCV pins are programmed as inputs.

Regardless of master or slave mode operation, the system clock LLC can come from external or from the chip's own oscillator. With JP12, 'XCLK' closed, the clock can be generated by the internal oscillator and is fed to pin LLC and the respective pin at the VG96 connector. When an external clock is received (JP12,'XCLK' open) JP17 allows termination of LLC by adding a 240R resistor to ground. In addition to this, a series resistor (22R) terminates this clock line.

2.7 Jumperlist

TABLE 3 Jumperlist 7120/21MOD2

Jumper	Name	Description
JP1,2	'Filter C'	5MHz lowpass filter in Y/C path 'C' ON/OFF
JP3,4	'Filter Y'	5MHz lowpass filter in Y/C path 'Y' ON/OFF
JP5,6	'Filter CVBS'	5MHz lowpass filter in CVBS path ON/OFF
JP7	A0	EEPROM address A0
JP8	A1	EEPROM address A1
JP9	A2	EEPROM address A2
JP10	VS / ODD	Connects RCV1-pin with VS or ODD line
JP11	HS	Connects RCV2-pin with HS line
JP12	XCLK	Connects own oscillator output with LLC clock input and output at VG96 conn. (master-mode)
JP13	RESN	Selects source for Reset Not Signal, push button/inp. conn
JP14	SA	I²C slave address select, closed = 88H, open = 8CH
JP17	TERMLLC	Termination of LLC line with 240R
JP18	POWA	Analog power 3.3V from extern (power conn.) or regulator
JP24	POWD	Digital power 3.3V from extern (power conn.) or regulator

3. Tips for a PCB layout

3.1 Analog and digital signal processing

- use separate ground planes for analog and digital supply in one layer (no overlapping!)
- use separate supply planes for analog and digital with the same shape (or smaller) as ground
  (no overlap of analog supply with digital ground and vice versa!)
- if there are different (asynchronous) clock domains, use separate ground and supply planes
  (place the analog areas not in a direct neighbourhood; separate the clock domains)
- always use the inner layers for ground and supply planes (no signal layer in between!)
- try to keep digital signals away from analog areas
- place analog areas close to the border of a PCB
- avoid long tracks for analog signals
- place decoupling capacitors (22nF to 100nF) close to the power pins of the ICs
- prepare several provisions for connecting places for analog and digital ground on the PCB for further optimization on the final board.

3.2 IIC bus

always supply the I²C-bus with pull-up resistors, but avoid too high currents. The values of resistors Rp and Rs depend on the following parameters:

- supply voltage
- bus capacitance
- number of connected devices (input current + leakage current)

please see I²C-bus specification (e.g. chapter 10.1 in the Philips data handbook: 'Maximum and minimum values of resistors Rp and Rs').

3.3 Application information

Application environment of the Con-DENC (SAA7120/21)) is shown at the end of the datasheet of the respective device.

4. Software

The enclosed disk contains an install-version of the Universal Register Debugger Software (URD) and some files for easy debugging Philips encoders and decoders in conjunction with the I²C-bus Parallel Port adaptor.

For this module please open the file SAA7120_21.urd to get a default setup like described on the following page. The information will be transmitted by clicking the 'WD' (write default) push button.

To change this setting (e.g. for NTSC or SECAM encoding) there exist macros like shown on pages 17 and following. The program is caused to perform a macro operation by clicking the push button right in front of the macro name.

For editing single values use +/- on your keyboard and then click 'WN' (Write Now).

You can find further details concerning the software in the doc-file on the disk.

4.1 Programming tables for SAA7120/21

SAA7120/21: init data PAL Slave: 88H or 8CH	
Sub	**Data**
Reg 26H	00H
Reg 27H	00H
Reg 28H	**21H**
Reg 29H	**1DH**
Reg 3AH	13H
Reg 5AH	0CH
Reg 5BH	**7DH**
Reg 5CH	**AFH**
Reg 5DH	**23H**
Reg 5EH	**35H**
Reg 5FH	**35H**
Reg 60H	00H
Reg 61H	**06H**
Reg 62H	**2FH**
Reg 63H	**CBH**
Reg 64H	**8AH**
Reg 65H	**09H**
Reg 66H	**2AH**
Reg 67H	55H
Reg 68H	56H
Reg 69H	67H
Reg 6AH	58H

Sub	Data
Reg 6BH	20H
Reg 6CH	**05H**
Reg 6DH	**20H**
Reg 6EH	**A0H**
Reg 6FH	14H
Reg 70H	80H
Reg 71H	E8H
Reg 72H	10H
Reg 73H	42H
Reg 74H	03H
Reg 75H	03H
Reg 76H	05H
Reg 77H	16H
Reg 78H	04H
Reg 79H	16H
Reg 7AH	18H
Reg 7BH	38H
Reg 7CH	40H
Reg 7DH	00H
Reg 7EH	00H
Reg 7FH	00H

The table shows a default setup for the SAA7120/21 with following settings:

- working as clock slave
- detection of sync. signals (H, V) out of datastream
- output format = PAL
- WSS, TTX and Closed Caption disabled
- internal colour bar off

The colour bar with fixed colours is encoded if the MSB of register 3AH is set to ’1’.

Not listed registers must be programmed to 00H.

Bold signed registers must be edited for changing the output format (NTSC)

Macro functions in the software ’URD’ allow a quick and easy programming concerning the most important changes (see page 19).

TABLE 4 Changes for NTSC

SAA7120/21: changes for NTSC Slave: 88H or 8CH	
Sub	**Data**
Reg 28H	19H
Reg 29H	1DH
Reg 5BH	76H
Reg 5CH	A5H
Reg 5DH	2AH
Reg 5EH	2EH
Reg 5FH	2EH
Reg 61H	15H
Reg 62H	3FH
Reg 63H	1FH
Reg 64H	7CH
Reg 65H	F0H
Reg 66H	21H
Reg 6CH	F9H
Reg 6DH	00H
Reg 6EH	B0H

TABLE 5 Macros for Teletext

SAA7120/21: changes for TTX PAL Slave: 88H or 8CH	
Sub	**Data**
Reg 6FH	34H
Reg 73H	42H
Reg 74H	03H
Reg 76H	05H
Reg 77H	16H
Reg 78H	04H
Reg 79H	16H

SAA7120/21: changes for TTX NTSC Slave: 88H or 8CH	
Sub	**Data**
Reg 6FH	34H
Reg 73H	54H
Reg 74H	03H
Reg 76H	06H
Reg 77H	10H
Reg 78H	05H
Reg 79H	10H
Reg 7CH	10H

The tables shows the registers that are changed when performing a macro function.

4.2 Summary of Registerfunctions

In the following table the usage of registers is described in order to get a quick view of the most important functions and give help for programming the device. The table does not contain whole information about the function or determination of values. The subaddress is the location according to the described function but not exclusive in every case. For further details see chapter 'Slave Receiver' in the datasheet SAA7120/21.

TABLE 6 Registers of the SAA7120/21

Function	SubAdr	Description
Null	00H - 25H	Always program to 00H in order to avoid unexpected effects
Wide Screen Signal	26H - 27H	WSSON enables or disables completely the WSS encoding; for meaning of the individual bits refer to the table given in ETS-300 294
Real Time Control	28H, 5DH - 5EH	If RTCE is set to high, Real Time Control (RTC) of the generated subcarrier frequency is enabled. RTC should be used whenever the clock for the video encoder is generated by a digital line-locked video decoder to ensure stable encoding phase for clean colors. From a decoder supporting the new function DECCOL, a flag indicating that color was detected can be received if DECCOL=high. If DECFIS=high, the field frequency information detected by a decoder can be received. IF DECOE=high, the odd/even information can be received from a decoder supporting this function. If DECPH=high, a subcarrier oscillator phase reset initiated on the decoder side will reset the phase of the encoder oscillator.
Burst Start/End	28H - 29H	The begin and the end of the color burst can be adjusted in a certain range at an accuracy of LLC clock cycles; the suggested defaults should be used
Copy Guard	2AH - 2EH	Four bytes plus separate enable bits for each fields can be downloaded here identically to the Closed Captioning bytes. These bytes are encoded as Closed Caption information and output in the line preceeding the line defined by parameter SCCLN(4:0), address 6F
Null	2FH - 39H	Always program to 00H in order to avoid unexpected effects

Function	SubAdr	Description
Input Port Control	3AH	(0, 1): setting these bits high for straight binary data, inverts the MSB internally for correct processing; setting these bits low passes the data as it is. (2): setting this bit high allows for input of 8 bit luminance data at MP port and 8 bit multiplexed color difference data at DP port; setting this bit low allows for input of 8 bit luminance and color difference acc. to CCIR-656. (3): when this bit is set high, the color dematrix is by-passed, and video input is only up-sampled to 27 MHz data rate for output instead of RGB. (4): when this bit is set high, in slave mode the encoder is triggered by an embedded frame sync code within the CCIR-656 data input. If the embedded frame sync is not available, this bit must be set low and appropriate signals have to be provided at RCV1 and RCV2 inputs. (5): in a system using the clock qualifier CREF, the active polarity of CREF can be changed. Usually CREF=low. No relevance at all if FTM16=low. (6): when this bit is set high, overlay information, e.g. menu letters, do not appear on Y/C and CVBS output, which in many case are dedicated to be recorded on a VCR. (7): setting this bit high decouples the video input and inserts a test signal defined by eight color-programmable bars, e.g. a 100/75 color bar.
Chroma Phase	5AH	This register defines the absolute subcarrier phase w.r.t. the synchronization pulse scheme. Although in practice the absolute subcarrier phase is almost never relevant, values for the most common standards NTSC-M and European PAL are given. Please note that the value is different when the internal color bar function is active.
Gain_U, Gain_V	5BH, 5DH	These registers directly influence the amplitude of the internal color difference baseband signals and thus of the generated subcarrier for quadrature modulated standards (for SECAM, the frequency deviation is influenced!) Usually, the nominal settings given in the datasheet should be used; in case that an analog post filter contributes noticeable attenuation around the subcarrier frequency, both GAINU and GAINV should be enlarged accordingly. Note that the sign bit (0=positive, 1=negative) is located in 5DH for GAINU and in 5EH for GAINV.
Black Level	5DH	This parameter adds a certain offset to the luminance signal w.r.t. to the sync tip, but leaves the peak-peak amplitude unaffected.
Blanking Level	5EH - 5FH	This parameter adds a certain offset to the luminance blanking level w.r.t. the sync tip. Note that this parameter has to be set twice, i.e. outside (5EH) and inside (5FH) the vertical blanking interval. Usually, both blankings are identical.

Function	SubAdr	Description
CCR (Cross Colour Reduction)	5FH	? In order to reduce cross-color effects that can occur when a TV set is driven by a CVBS signal, a programmable notch filter can be activated. It provides significant attenuation of luminance components around frequencies occupied by subcarriers at 3.56 MHz or 4.43 MHz.
Standard Control	61H	(0): configures the internal pixel counter either to 858 pixels/line (high) or 868 pixels/line (low) (1): this bit set to high enables the PAL specific process of inverting the V color difference component line by line. (2): usually set to high for standard-compliant chrom bandwidth; in some cases (e.g. for best S-Video quality), it can be set to low. (4): this bit selects one of two possible gain factors for the luminance black-to-white amplitude; when set to high, luminance is adjusted for 92.5 IRE output amplitude, and when set to low for 100 IRE output amplitude. (5): only relevant when RTCE bit is high; usually set to low. (6): if set to high,internally a constant code corresponding to the lowest possible output voltage at the DACs for CVBS, Y/C is applied.
RTC enable	62H	If set to high, Real Time Control (RTC) of the generated subcarrier frequency is enabled. RTC should be used whenever the clock for the video encoder is generated by a digital line-locked video decoder to ensure stable encoding phase for clean colors.
Burst Amplitude	62H	These registers directly influence the amplitude of the color burst for quadrature modulated standards (for SECAM, the amplitude of the color burst cannot be modified!) Usually, the nominal settings given in the datasheet should be used; in case that an analog post filter contributes noticeable attenuation around the subcarrier frequency, this parameter should be enlarged accordingly.
Subcarrier Frequency	63H - 66H	The subcarrier frequency is synthesised by a 32 bit Discrete Time Oscillator; all four bytes are fully programmable
Line 21 Encoding	67H - 6AH	Closed Caption and Extended Data Service bytes to be downloaded including parity bit at the MSB position of each byte.
RCV-Port Control	6BH	Handles input- or output signal of RCV1 and RCV2 pins (see corresponding table in the datasheet). Although the usual definition for master mode stands for trigger I/O's to be switched to output, the device allows for a kind of mixed mode as to be slaved by a frame sync applied to pin RCV1 and simultaneously to output a horizontal pulse on pin RCV2.

Function	SubAdr	Description
H-Trigger Control	6CH - 6DH	Sets the Horizontal Trigger phase related to signal on RCV1 or RCV2. If a vertical sync is applied to RCV1, an additional horizontal sync at RCV2 is needed to adjust the postition of video horizontally.
V-Trigger Control	6CH - 6DH	Sets the Vertical Trigger phase related to the input signal on RCV1; value VTRIG - counting half lines - should be even, only.
V-Blanking Definition	6EH	setting this bit to low will define the Vertical Blanking Interval by the values loaded into registers FAL and LAL; if this bit is set to high, the Vertical Blanking Intervall is forced acc. to CCIR-624 (50Hz) or acc. to RS170A (60Hz)
V-Blanking Definition	6EH	setting this bit to low will define the Vertical Blanking Interval by the values loaded into registers FAL and LAL; if this bit is set to high, the Vertical Blanking Intervall is forced acc. to CCIR-624 (50Hz) or acc. to RS170A (60Hz)
Phase Reset Mode of the colour subcarrier generator	6EH	These two bits should exactly be set acc. to the table in the datasheet. For NTSC signals, both 'two-line reset' or 'four-field reset' are possible.
Field Length Control	6EH	Interlaced operation or two different non-interlaced modes are selectable for 525/60 signals or 625/50 signals.
Individual Line 21 Encoding	6FH	Two bits enabling field-dependent insertion of Closed Caption/ Eyxtended data.
Teletext Enable	6FH	For any line with Teletext insertion, this bit must be set to high, as it is a master switch. The actual selection for activated Text lines is made below.
Line Select for Closed Caption or extended data	6FH	This parameter selects one out of 32 possible position for Closed Caption encoding; usually it is line 21 for NTSC corresponding to 11h.
RCV2 Start / End	70H - 72H	These registers define start and end of a pulse repeating at line frequency: Note that if 'Start' is greater than 'End', the pulse will be inverted.
TTX request H start/ delay	73H - 74H	Every high-state of the signal at pin TTXRQ - depending on the chosen Text format - initiates the transfer of a new Teletext bit stream bit; as this bit stream must match to the internal pixel counter, the start of the first request pulse is programmable by TTXHD to accomodate to indiviual latencies of the bit stream source. TTXHS is an internally needed parameter and should be taken as given in the datasheet.
VSYNC shift	75H	In master mode (RCV1 and RCV2 as outputs), sometimes the phase of the horizontal pulse on RCV2 must be shifted against the phase of the vertical sync pulse on RCV1 in steps of 27 MHz clock cycles. This can be accomblished with this parameter in 3 steps.

Function	SubAdr	Description
TTX odd / even request VS/VE TTX60	76H - 79H, 7CH	For the odd and even field, the lines to carry Teletext information can be determined individually. Note that it is possible to nearly use the complete inactive and the complete active fields for Teletext insertion instead of video. Depending on the selected field frequency (Bit FISE), the Teletext standard is being selected through TTX60
Null	7DH	Always program to 00H in order to avoid unexpected effects
Disable TTX Line	7EH - 7FH	Starting with line line 8, ending with line 23 inclusive, each of these lines can be disabled for Teletext insertion (the respective bit set to high), although enabled by the global window definitions for Teletext. This can be useful in order to allow e.g. other information entering through the video input to be inserted between lines containing Teletext.

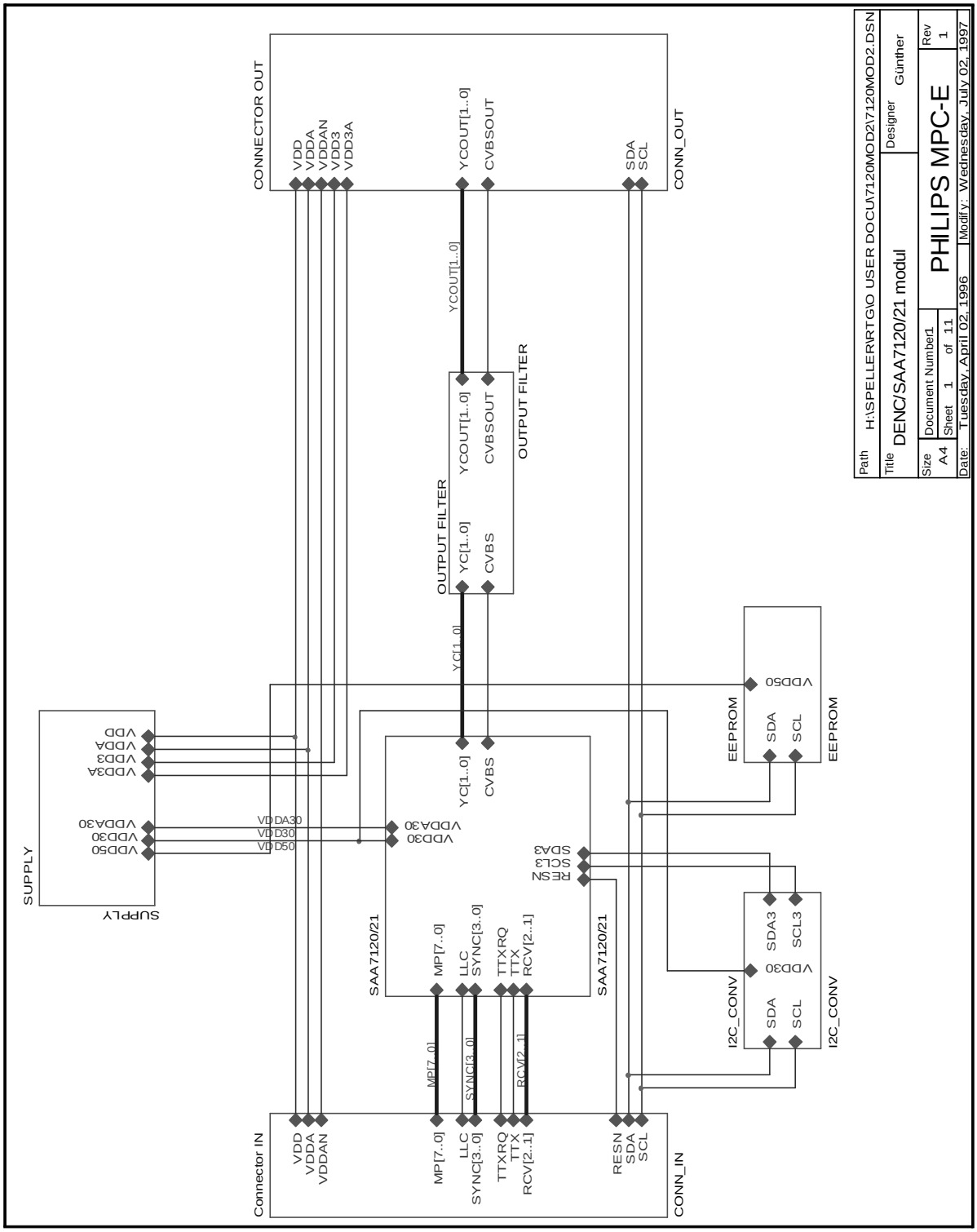
5. Appendix: Schematics and Layout

The schematics (made in ORCAD) can be delivered on request.

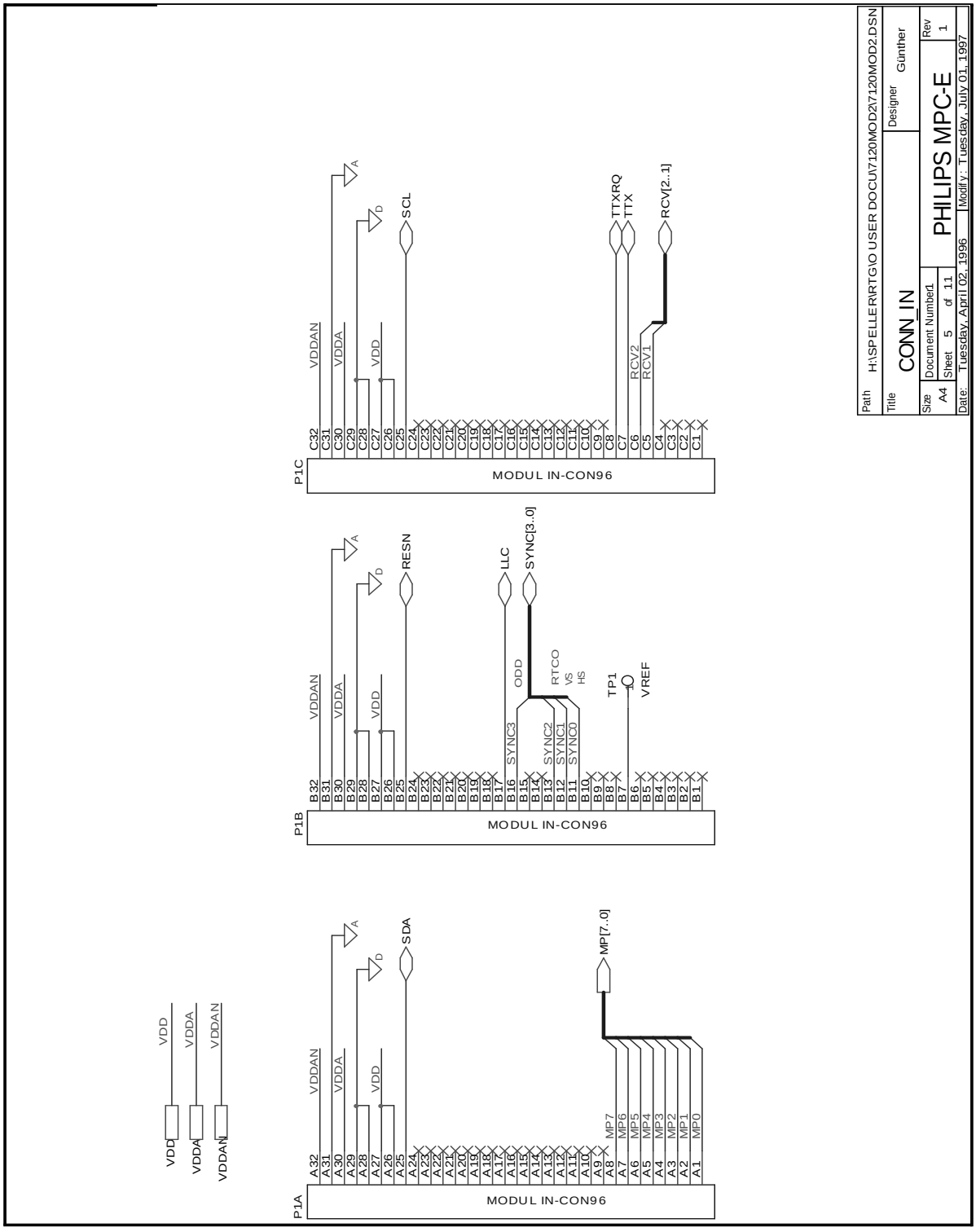
For a board layout GERBER files are available.

5.1 Schematic

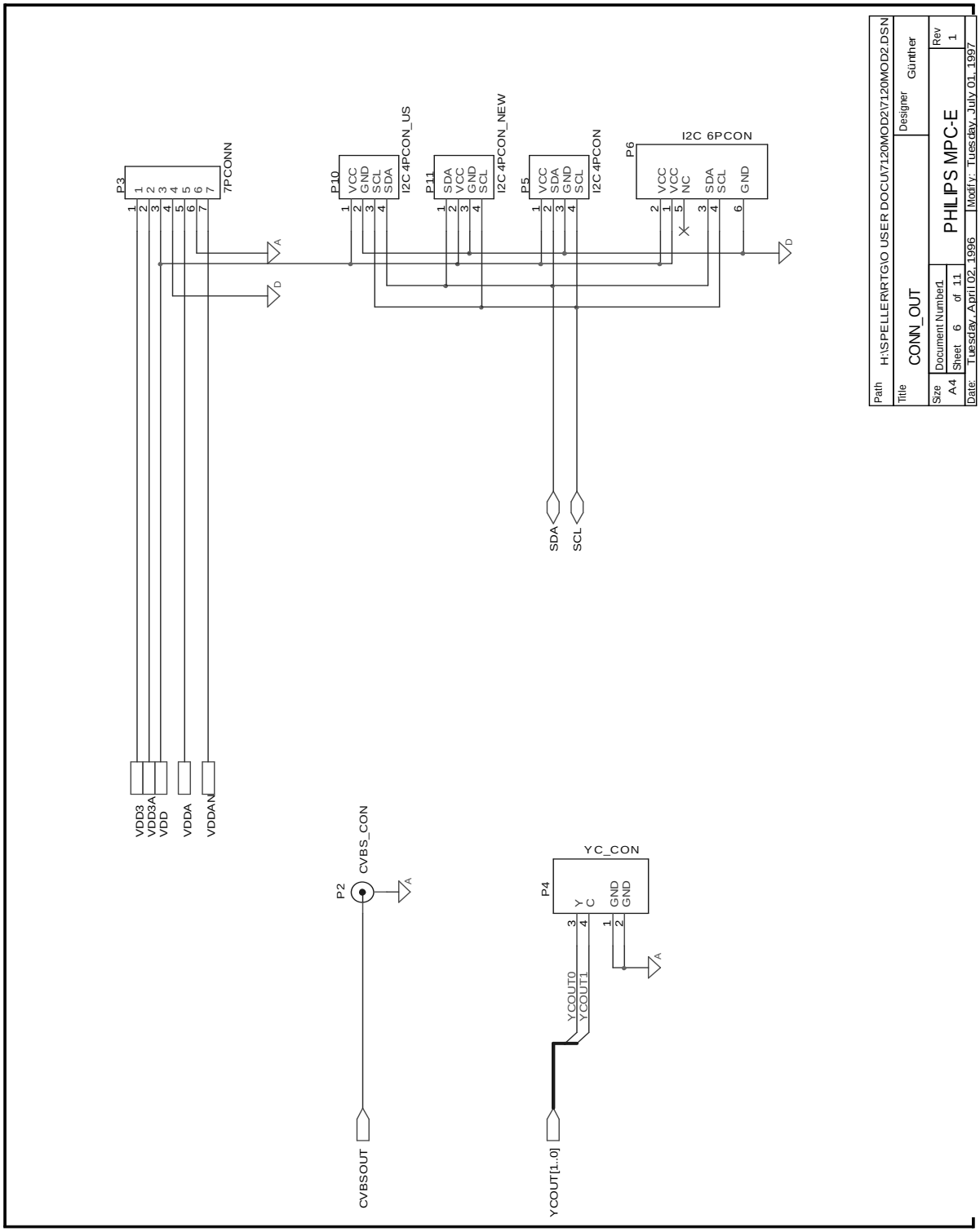
5.1.1 Top Sheet of 7120/21MOD2



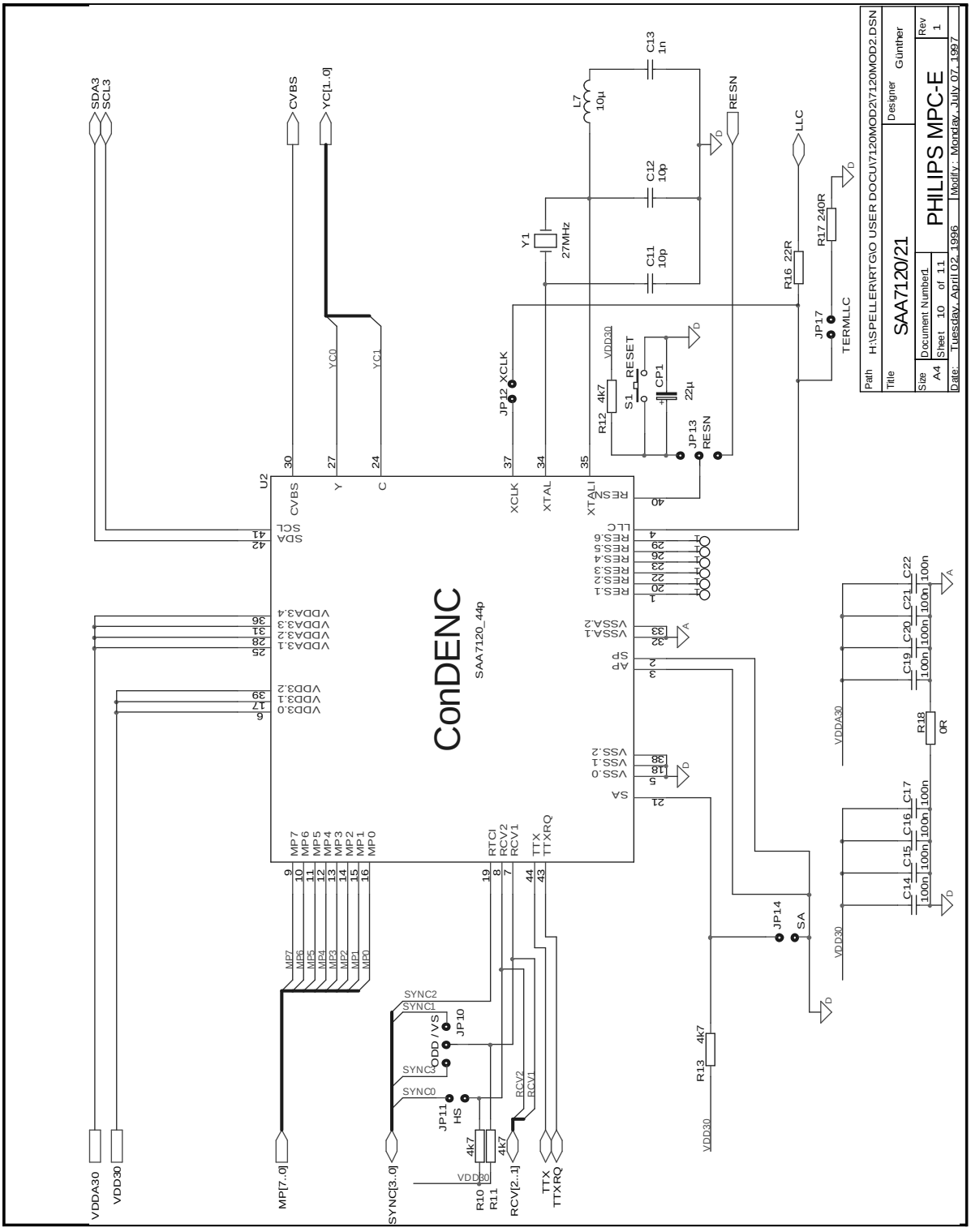
5.1.2 Connector In



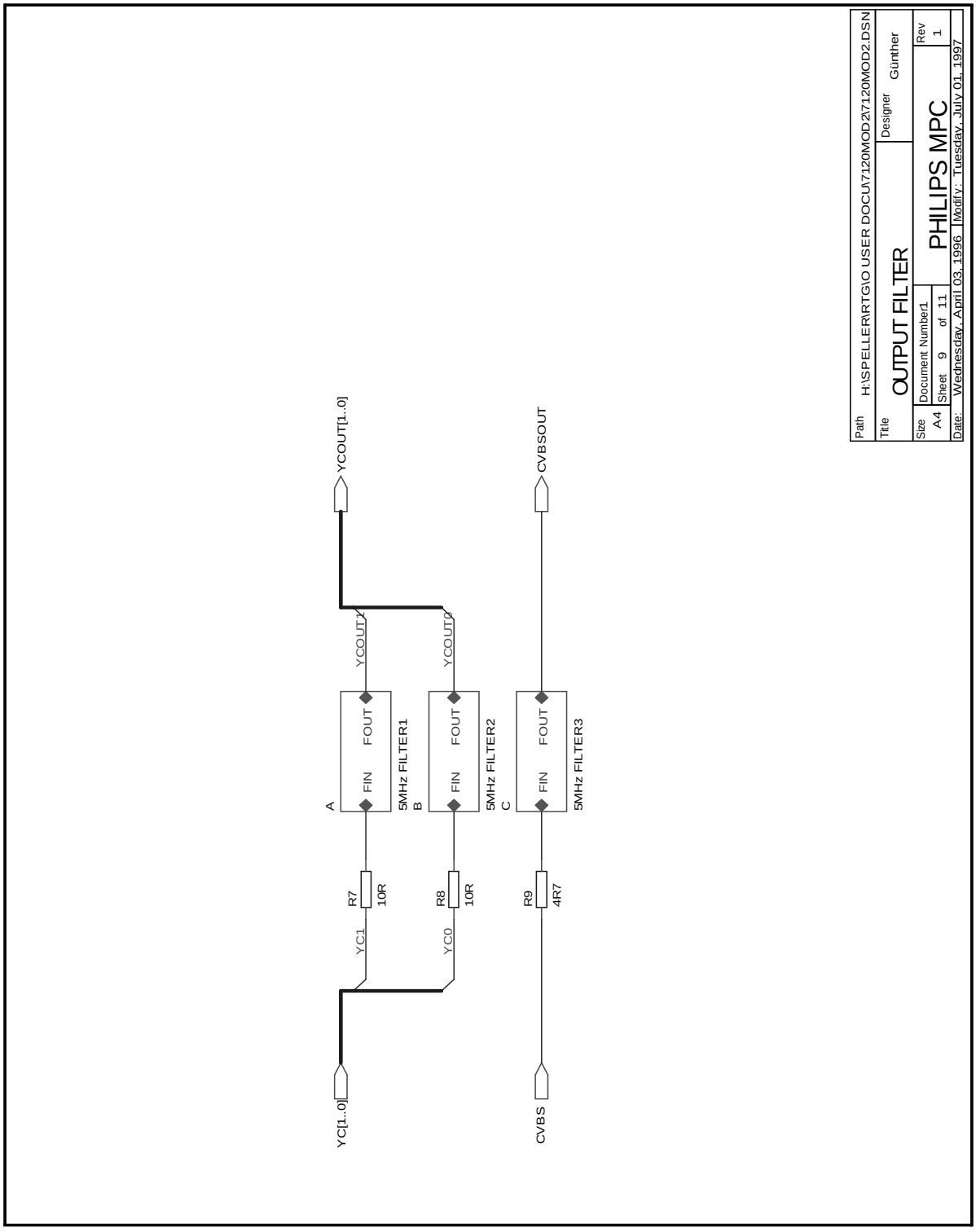
5.1.3 Connector Out



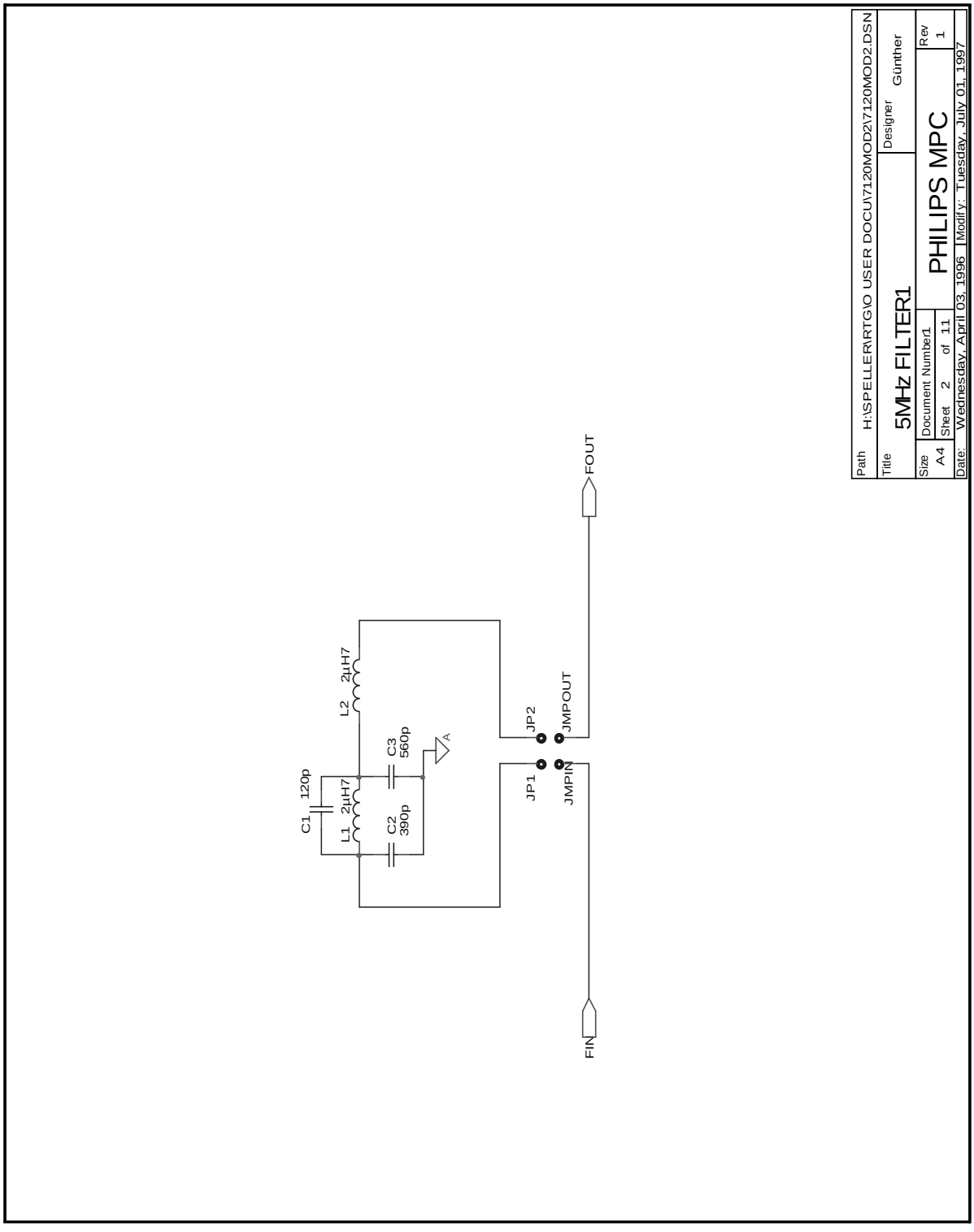
5.1.4 SAA7120/21



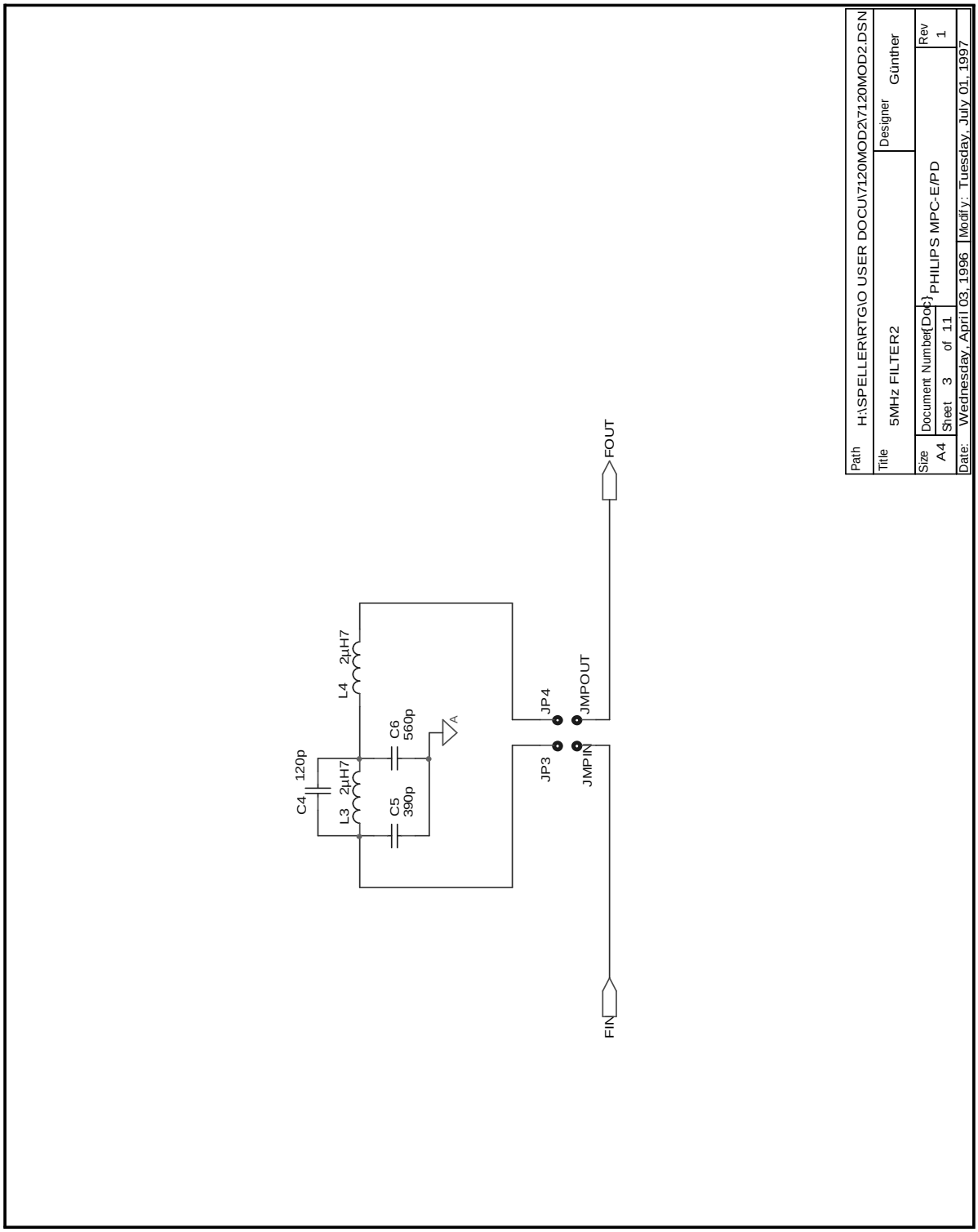
5.1.5 Output Filter



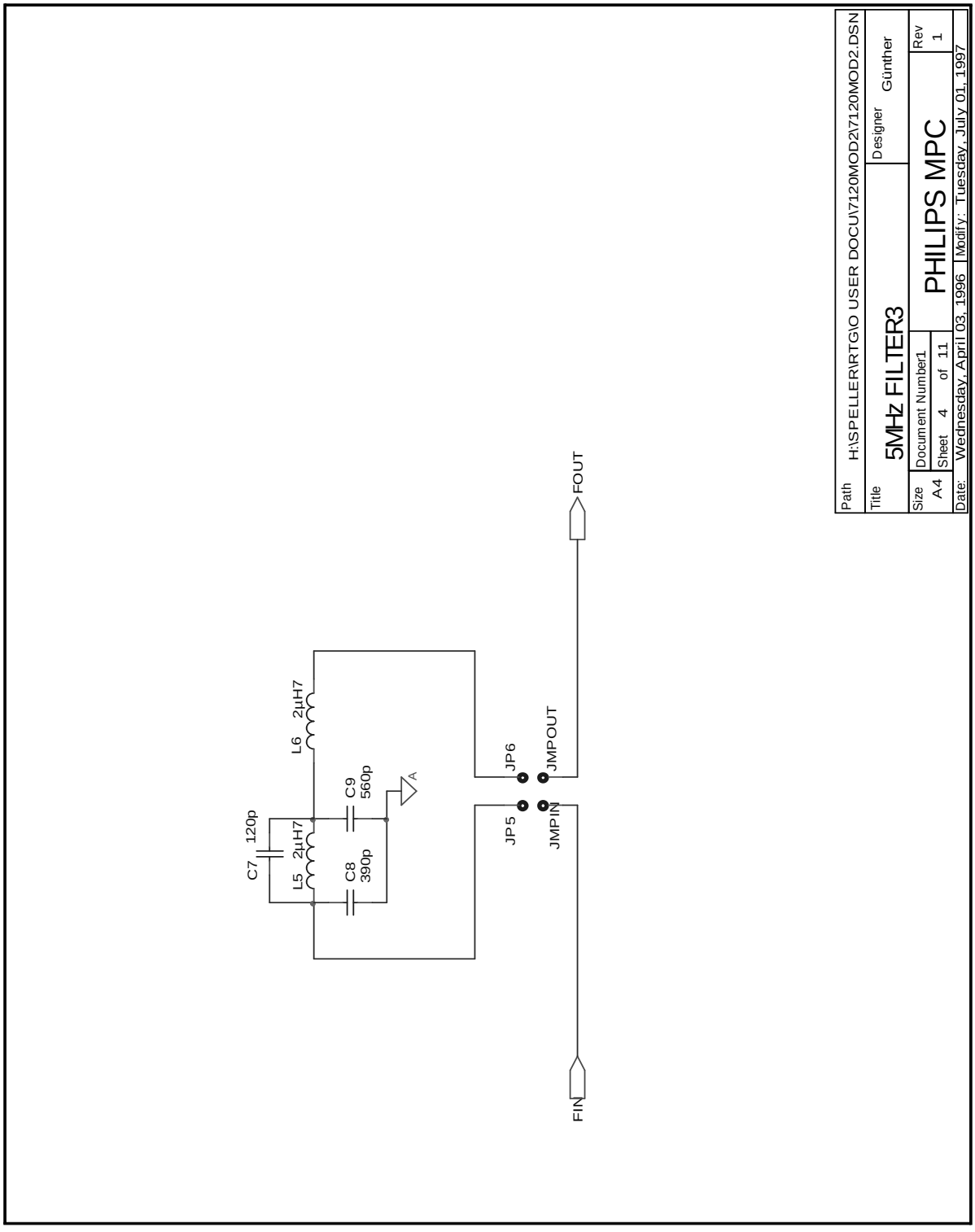
5.1.6 5MHz Lowpass Filter 1



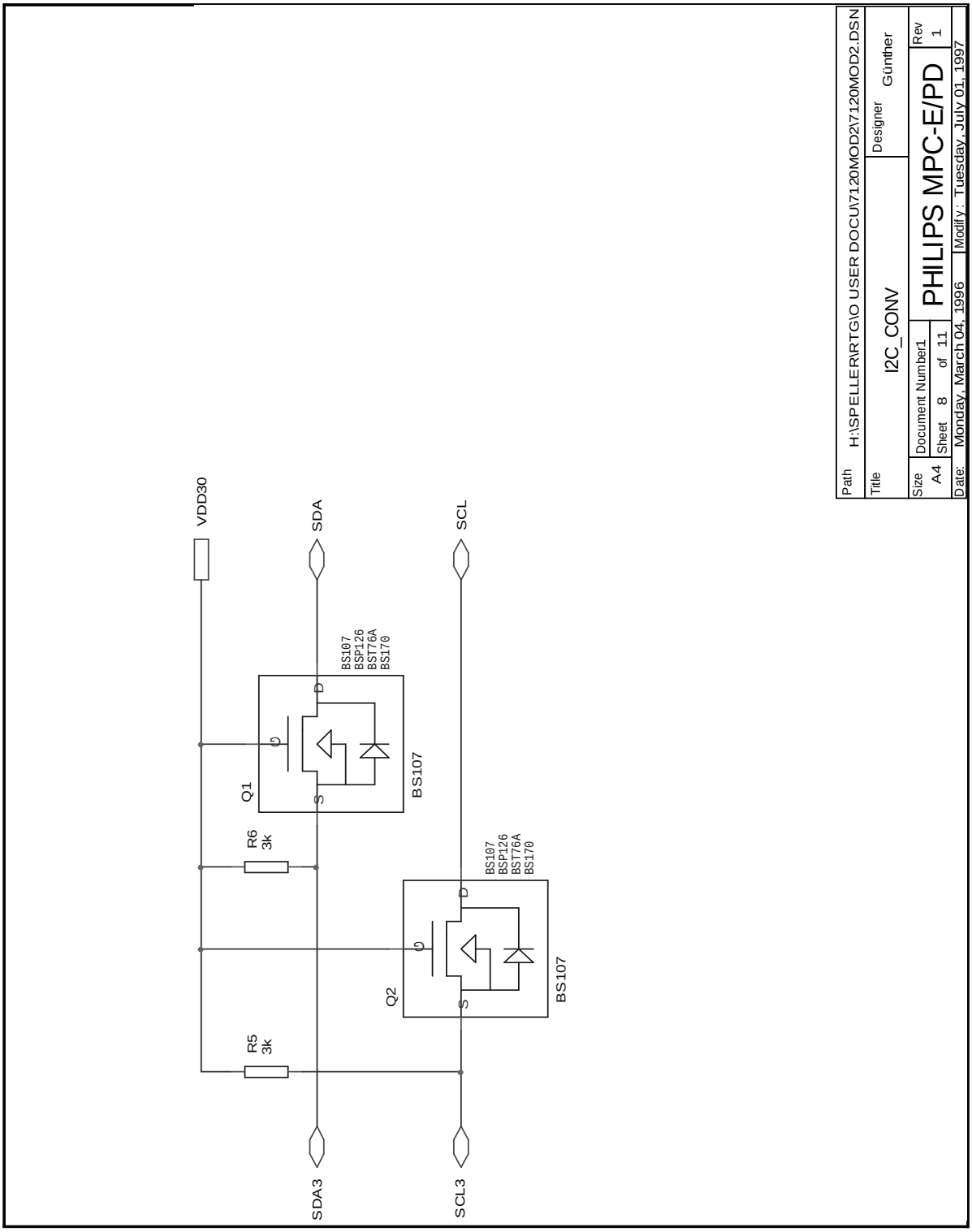
5.1.7 5MHz Lowpass Filter 2



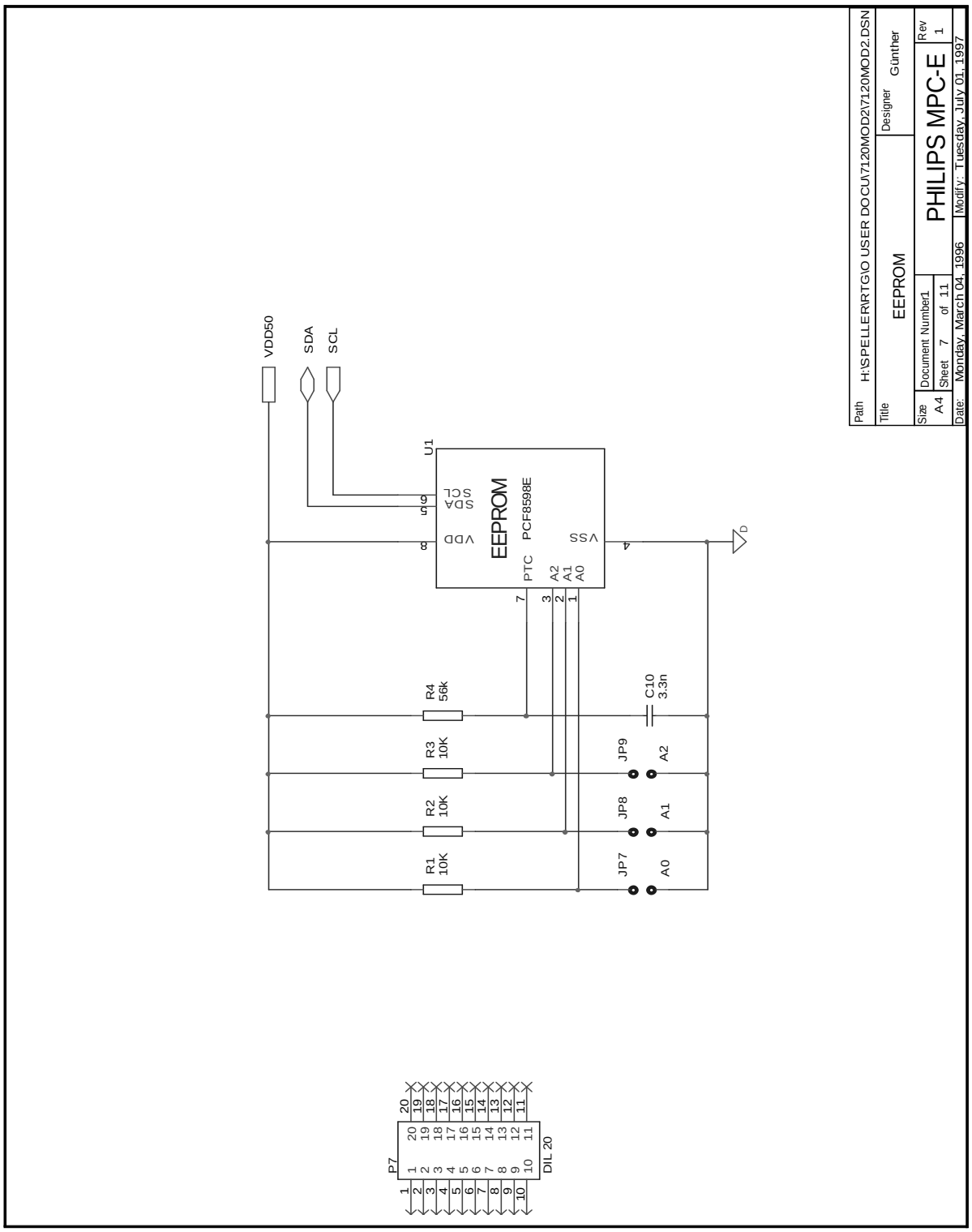
5.1.8 5MHz Lowpass Filter 3



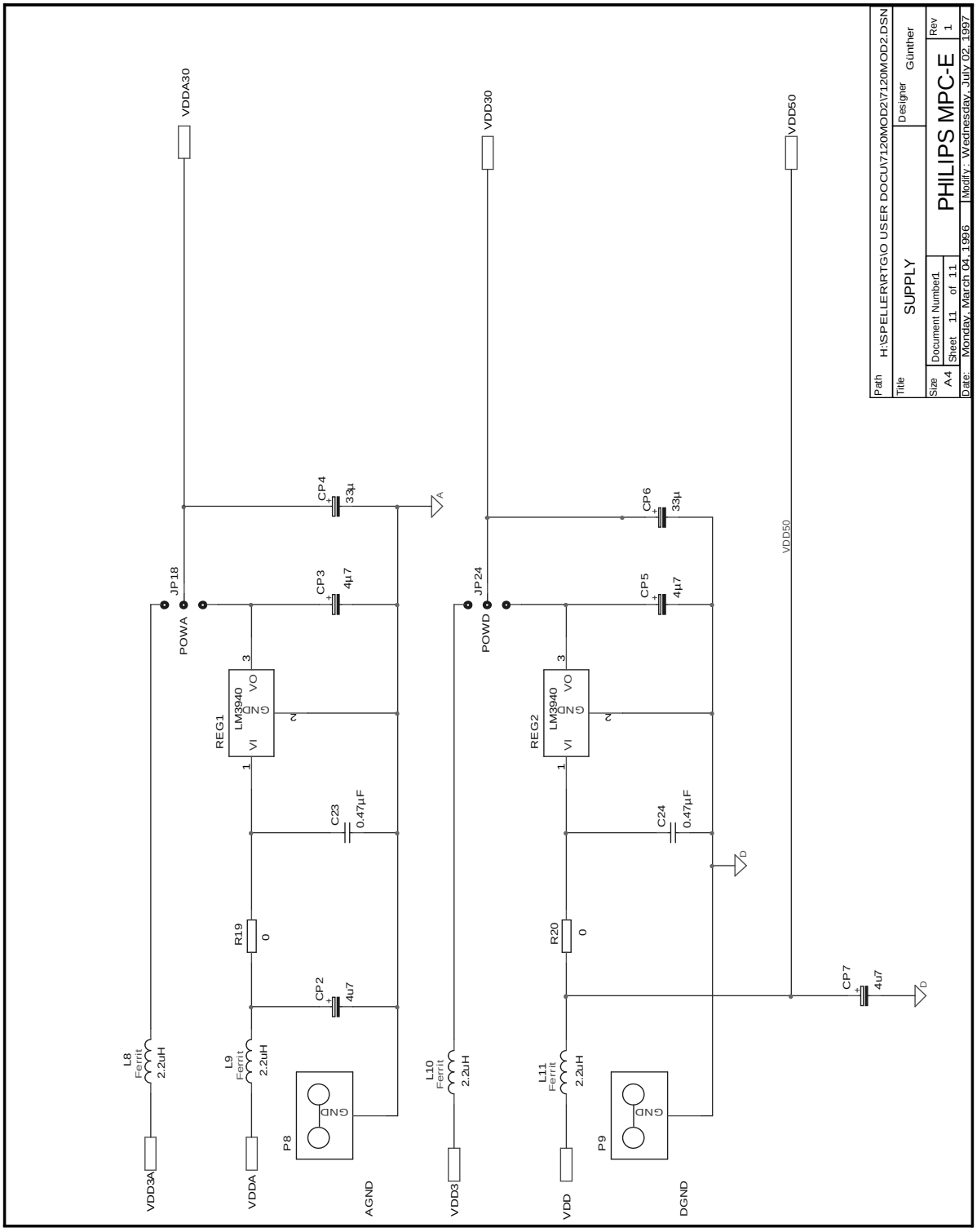
5.1.9 I²C Conversion



5.1.10 I²C EEPROM



5.1.11 Supply


VDDA30
VDD30
VDD50
JP18
POWA
JP24
POWD
CP4
33µ
CP3
4µ7
CP6
33µ
CP5
4µ7
REG1
LM3940
REG2
LM3940
C23
0.47µF
C24
0.47µF
R19
0
R20
0
CP2
4u7
CP7
4u7
L8
Ferrit
2.2uH
L9
Ferrit
2.2uH
L10
Ferrit
2.2uH
L11
Ferrit
2.2uH
P8
P9
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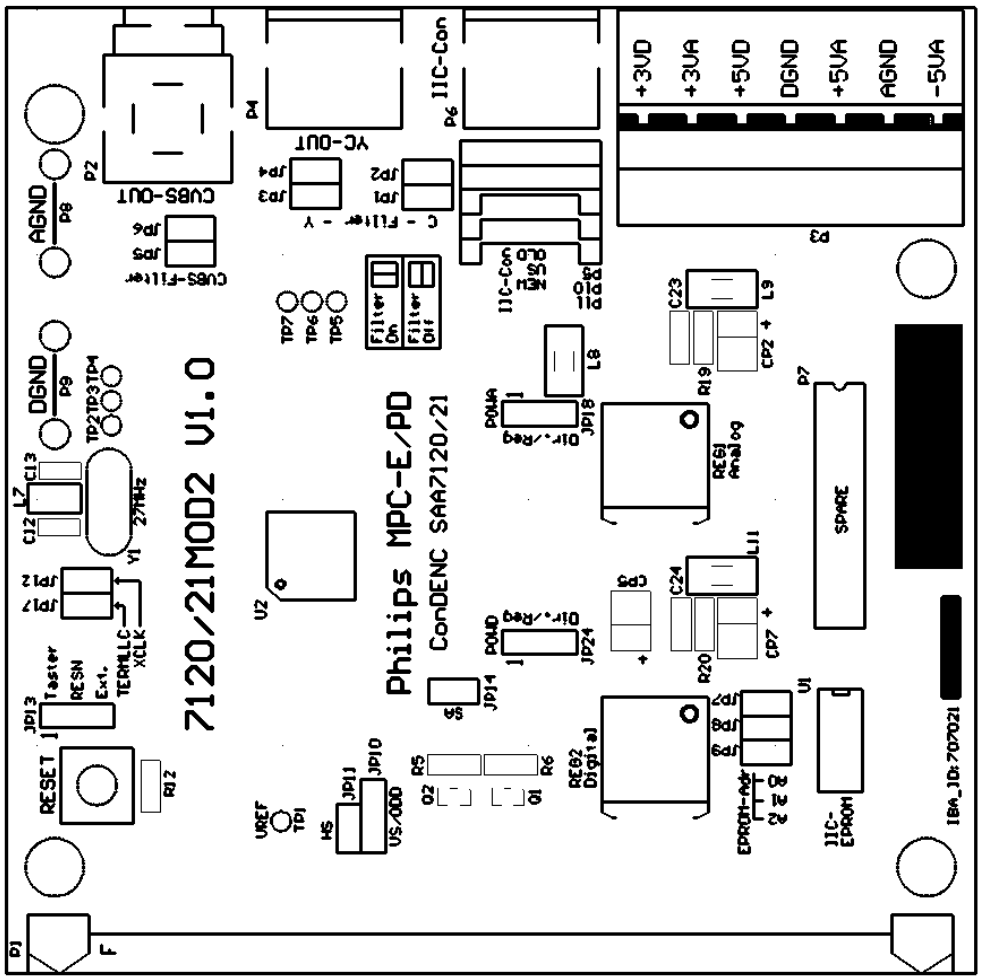
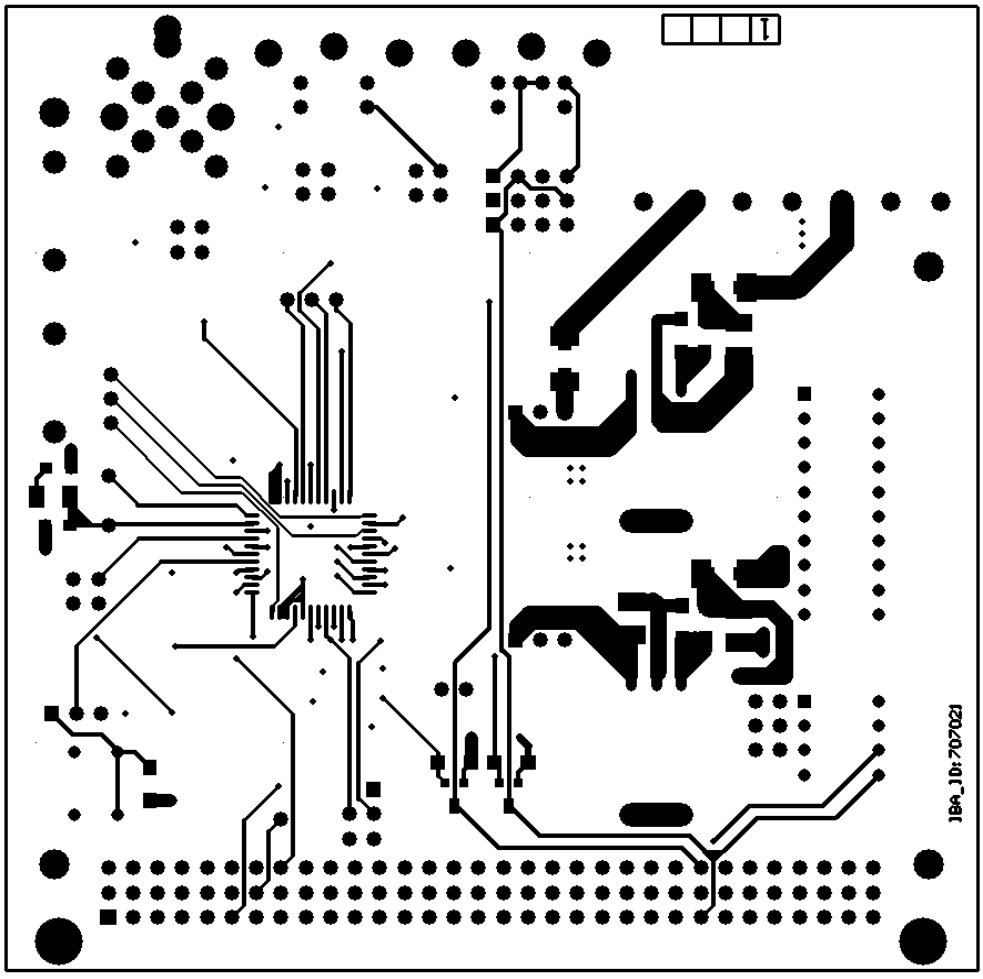
VDDA
AGND
VDD3
VDD
DGND
Path H:\SPELLER\RTG\O USER DOCU\7120MOD2\7120MOD2.DSN
Title SUPPLY
Designer Günther
Size A4
Document Number
Rev 1
Sheet 11 of 11
PHILIPS MPC-E
Date: Monday, March 04, 1996
Modify: Wednesday, July 02, 1997

5.2 Layout

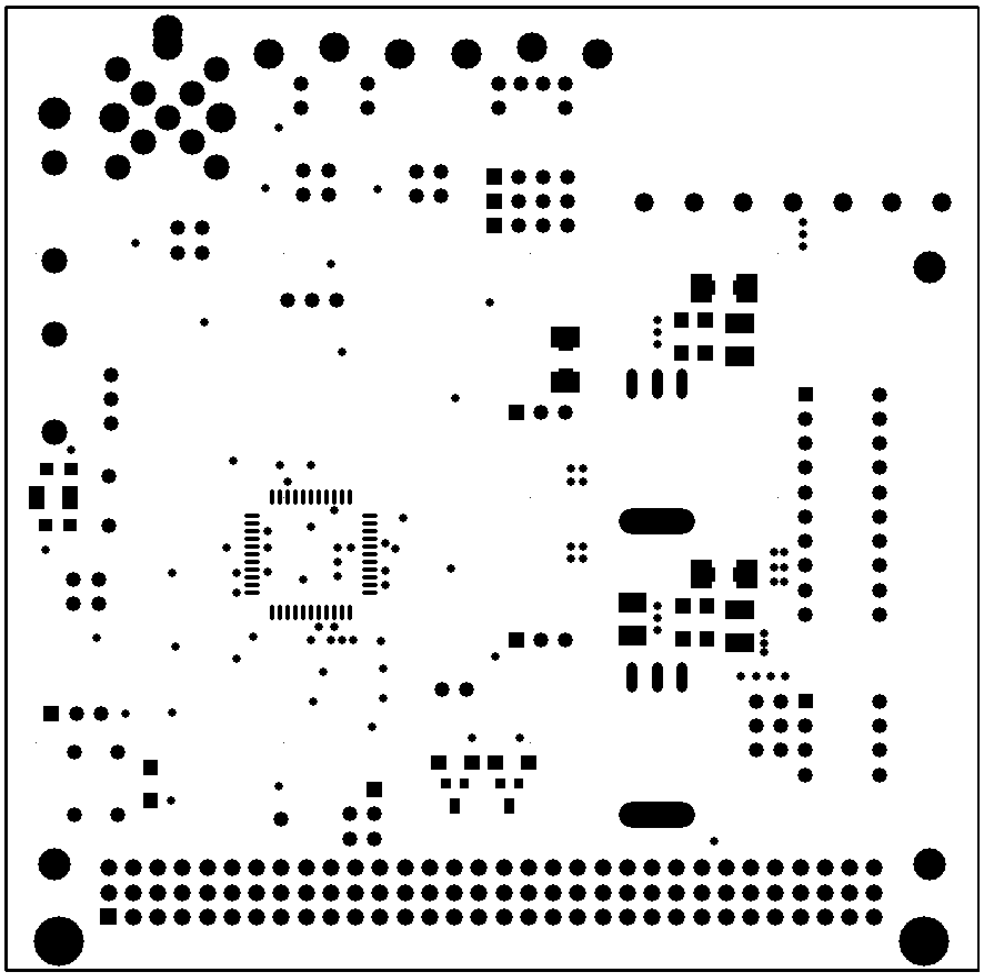
5.2.1 Top Placement of 7120/21MOD2



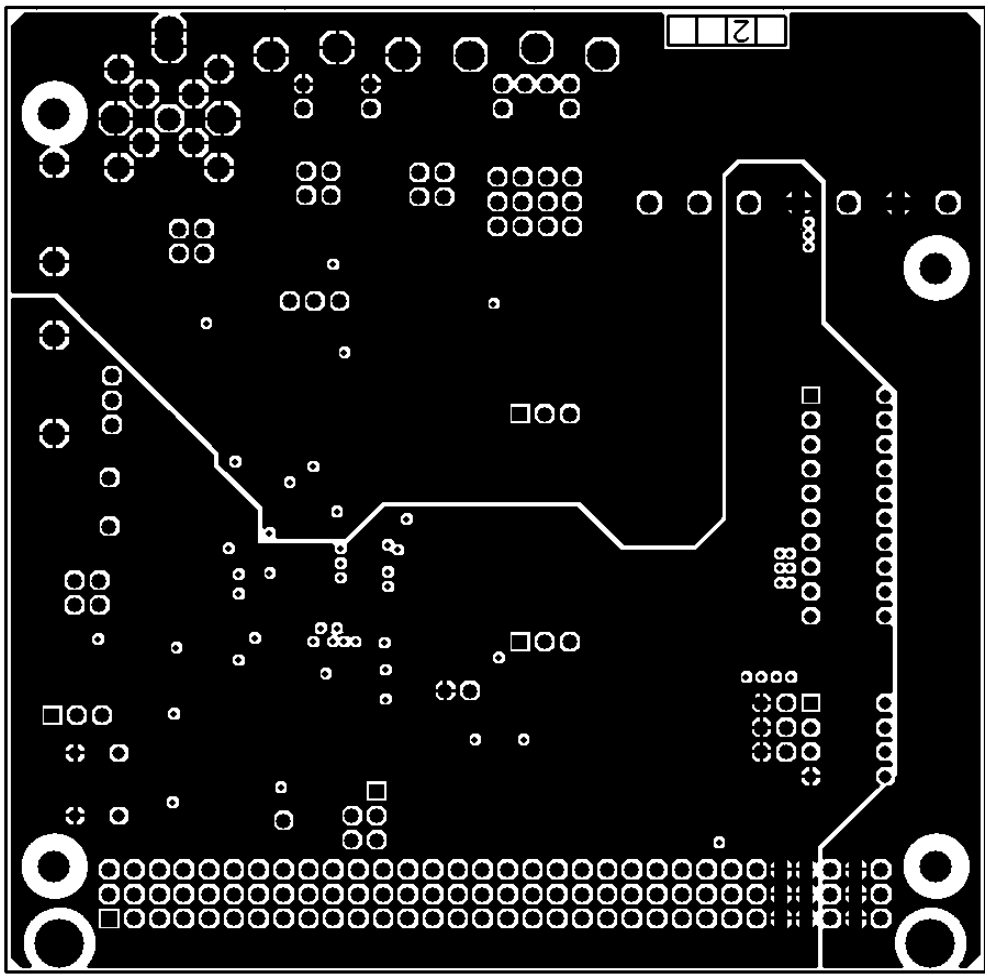
5.2.2 Routing of Top Layer of 7120/21MOD2



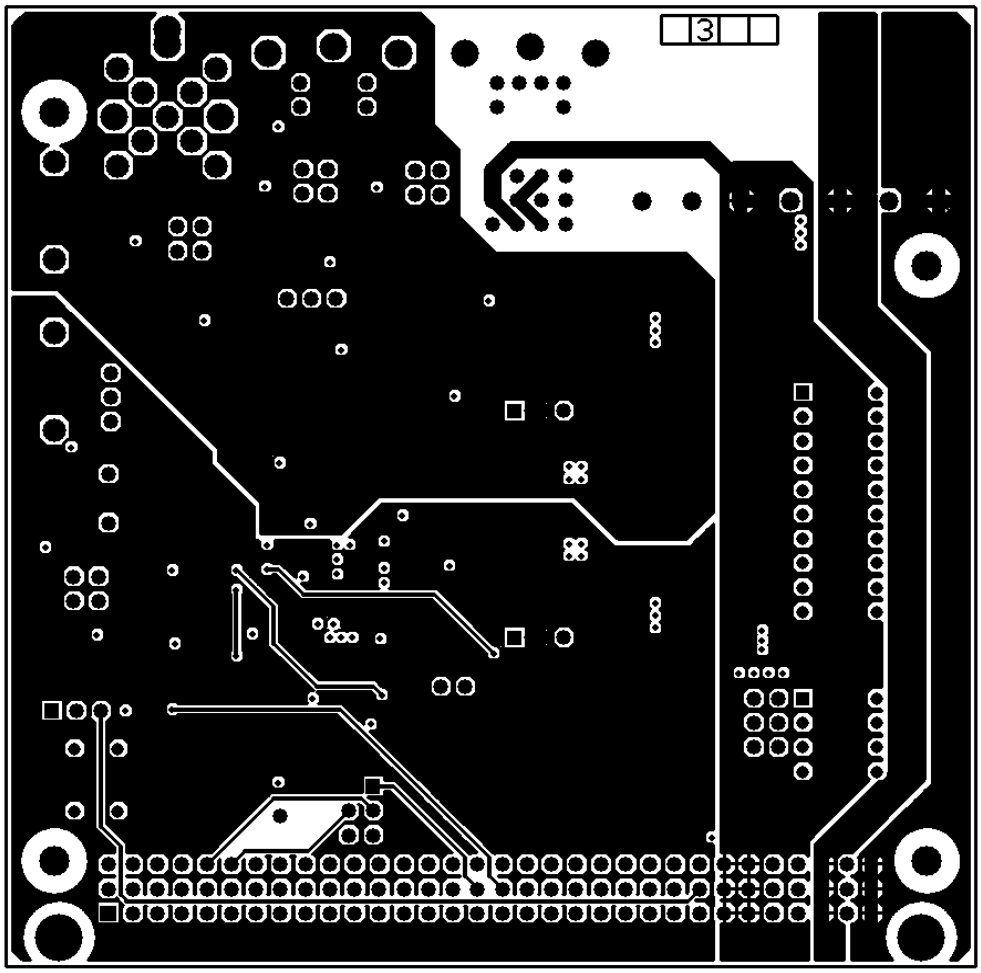
5.2.3 Top Solder Mask of 7120/21MOD2



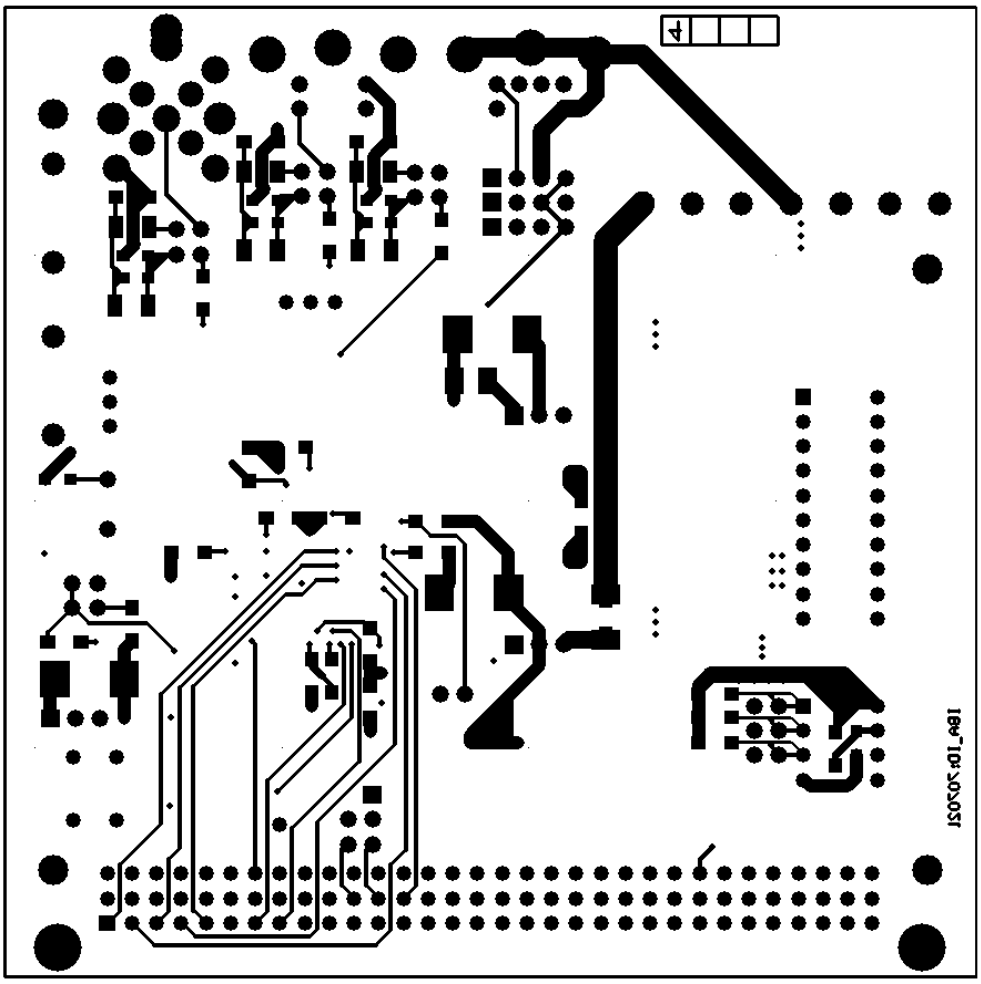
5.2.4 Ground Plane (Mid Layer 1) of 7120/21MOD2



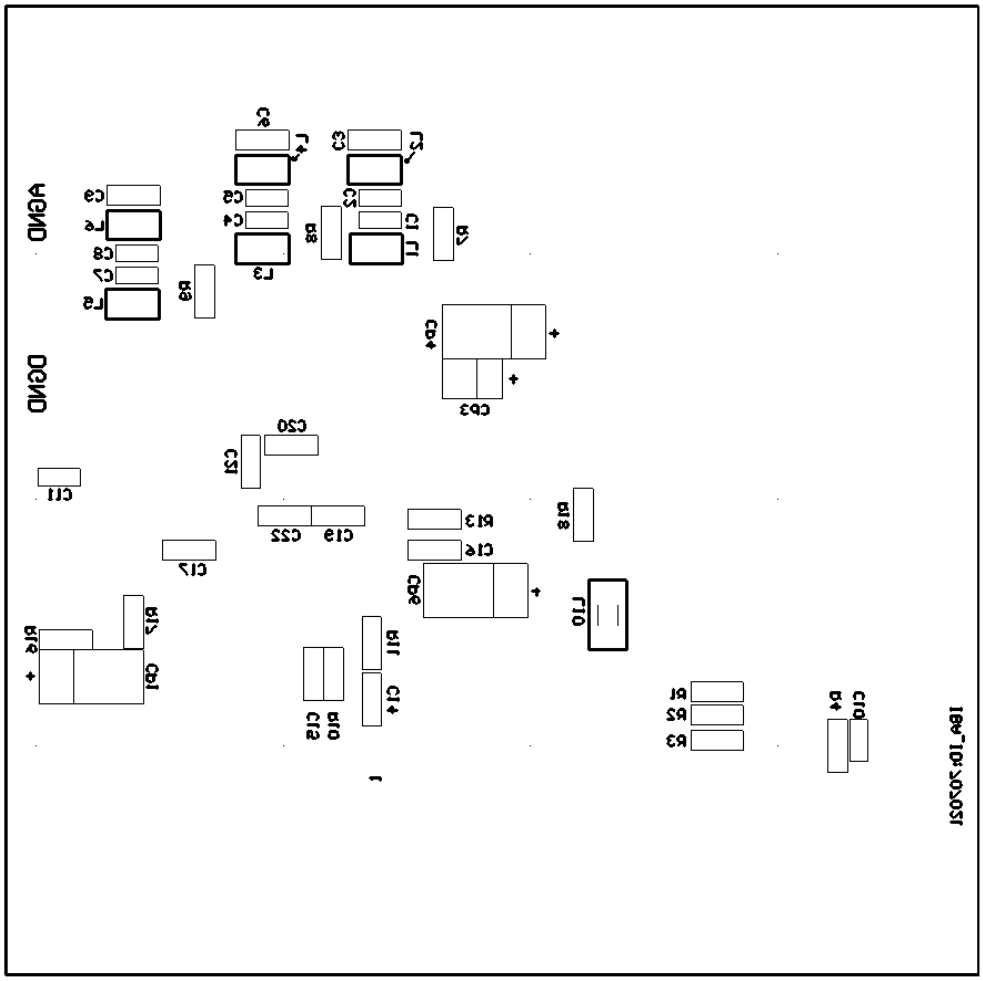
5.2.5 Supply (Mid Layer 2) of 7120/21MOD2



5.2.6 Bottom Layer of 7120/21MOD2



5.2.7 Bottom Placerment of 7120/21MOD2



5.2.8 Bottom Solder Mask of 7120/21MOD2