

APPLICATION NOTE

Digital Video Encoder Module System: 7128MOD2 AN 97085

Abstract

This application note is intended to provide application support for Philips' Digital Video Decoders and Encoders. It contains a description of one evaluation board as well as I²C-bus programming of the respective device.

The Digital Video Decoder converts an analog video input signal into a digital output signal. This signal can be processed by a wide range of applications and fed to the Digital Video Encoder, which delivers analog video signals to TV receivers or video cassette recorders.

This note gives a detailed description of the schematics and some hints how to design the PCB (Printed Circuit Board) with mixed analog and digital signal processing.

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APPLICATION NOTE

Digital Video Encoder Module System: 7128MOD2 AN 97085

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SAA7120/21
SAA7126/27
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This note gives a detailed description of the schematics and some hints how to design the PCB (Printed Circuit Board) with mixed analog and digital signal processing.

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1. Introduction

The Digital Video Decoder/Encoder Modules provide the basis to evaluate various Philips Digital Video Decoders and Encoders and give the opportunity to simply insert the modules into customized applications and systems.

On the following pages the assembly and function of a Digital Video Encoder Module is shown. The module can operate in stand alone mode (colourbar generator) as well as extension to other systems like PCI-bridges, MPEG decoders or Video input/output systems.

The module has a socket for an I²C-bus EEPROM (e.g. PCF8582, PCF8594, PCF8598, X24164) in order to store data for initialization and for simple control functionality operated by a (future) microcontroller module.

Software for IBM compatible personal computers enables access to all features and settings of the devices. It handles the I²C-bus via a printer port adaptor. This adaptor and a fitting cable is part of the accessory.

This modular concept was designed to combine different video decoders with various video encoders. Some modules (e.g. the 7128MOD2) can be configured for several devices and packages without the necessity of having a new PCB. This could be achieved by using multiple footprints for one IC and some configurational parts. For interfacing a 96-pin module connector is used.

The modules need a 5V analog and a 5V digital supply voltage. A respective power connector is placed at each backend (encoder-) module whereas frontend modules are supplied via the 96-pin module connector.

If necessary, an internal voltage regulator generates the required 3.3V onboard. Alternatively it is also possible to bypass the regulators on some encoder modules and connect 3.3V supply directly to the respective pins. You can find a fitting power connector cable as a part of the accessory as well.

2. Digital Video Encoder Module 7128MOD2

The digital encoder module 7128MOD2 contains the Philips Digital Encoder SAA7128/29, SAA7138/39, SAA7120/21 or SAA7126/27 (the even-numbered types include Macrovision Pay-per-View copy protection, while the odd-numbered types do not).

All listed encoders are CMOS 3.3V devices with 3.3V input stages but differ (among others) in following features:

SAA7128/29 PAL/NTSC/SECAM encoder with six DACs for CVBS(CSYNC), VBS(CVBS), C(CVBS), R(Cr), G(Y), B(Cb) (signals in brackets optionally) and a 54MHz double speed multiplexed D1 interface. It features also a versatile fader for fading of two data streams (at double speed port MP) against each other. QFP44 package.

SAA7138/39 PAL/NTSC/SECAM encoder with six DACs for CVBS(CSYNC), VBS(CVBS), C(CVBS), R(Cr), G(Y), B(Cb) (signals in brackets optionally) and a 54MHz double speed multiplexed D1 interface. It features also a versatile fader for fading of two data streams (at double speed port MP or through the additional port DP) against each other. QFP64 package.

SAA7120/21 PAL/NTSC encoder with three DACs for CVBS, Y, C. QFP44 package.

SAA7126/27 PAL/NTSC encoder with four DACs for CVBS(CSYNC, VBS), R(Cr, C), G(Y, VBS) and B(Cb, CVBS) (signals in brackets optionally) and a 54MHz double speed multiplexed D1 interface. QFP44 package.

The digital data is fed via the 96-pin input connector. The circuits accept CCIR compatible YUV data with 720 active pixels per line in 4:2:2 multiplexed formats, for example MPEG decoded data. For interfacing an ECL - TTL converter can be used (accessory). At a 54MHz (double speed) multiplexed D1 input port the circuits accept two CCIR compatible CbYCr data streams for example MPEG decoded data with overlay, whereas one datastream is

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latched at the rising, the other one at the falling clock edge. Therefore a special Y-module is designed (available Jan. '98). This Y-module will provide two input module connectors with multiplexer, an EPROM with CCIR 656 data and a centronic interface to generate a 54MHz interlaced data stream (see chapter 3.).

After passing the analog postfilters (to be disabled with jumper) the output signal is available simultaneously as CVBS, Y/C (and RGB) at the respective connectors (SCART for CVBS, Y/C, RGB and additionally a subclick connector for CVBS output). An adaptor from SCART to Mini Din and Cinch is part of the accessory. To prevent a wrong termination, be sure that the CVBS0 signal is not switched to the CVBS output connector and the SCART output (CVBS output or RGB-SYNC) at the same time (JP14, JP15).

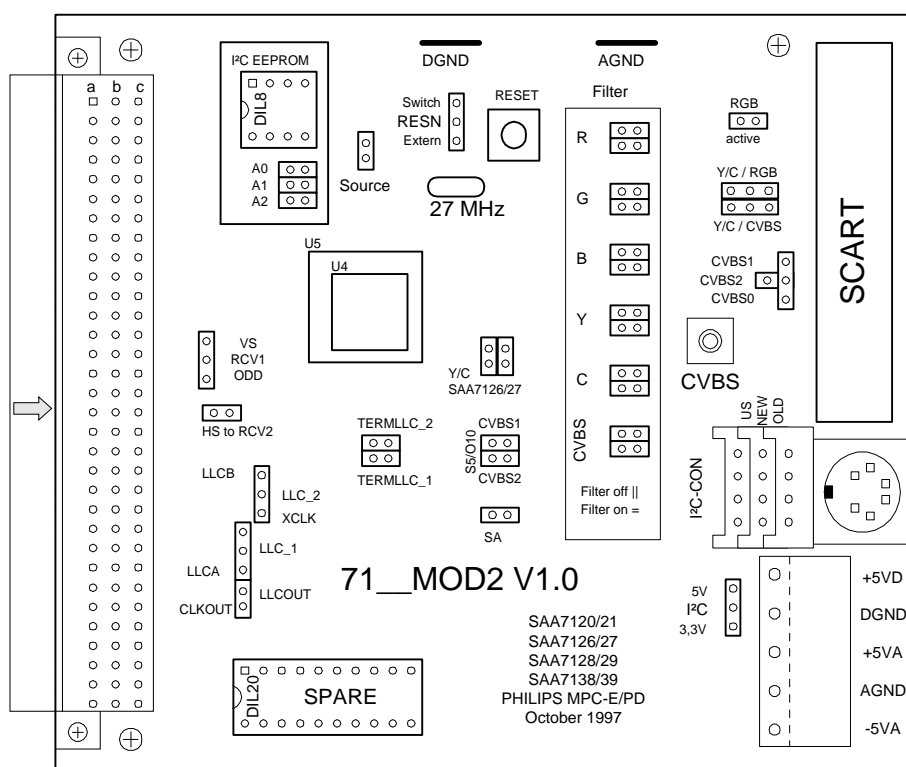


Fig.1 Location of ICs, jumpers and connectors on the 7128MOD2 PCB

Fig.1 shows the location of IC's, jumpers and connectors on the application module 7128MOD2. The function of the used connectors is described on page 10. The function of jumpers is shown in a jumper list on page 16.

2.1 Power supply

The +5V analog and digital power supply should be kept separate at the power connector. Analog and digital ground must be connected once near the power supply units.

A negative voltage (-5V) is one part of the MPC module system supply voltages but is not necessary for this application.

All supply voltages are available at the VG96 input connector according to the pinning on page 10.

2.2 Reset

There are two different ways to reset the device:

Using this module in conjunction with a MPC decoder module, preferably the 'Reset Not' generated by the decoder should be used (JP26 = Extern). Therefore a dedicated pin exists at the VG96 input connector.

In case of a stand alone operation (e.g. colourbar generator) or in conjunction with other systems the Reset push-button can be used (JP26 = Switch).

During reset (RESN = LOW) and after reset is released, all digital I/O stages are set to input mode, PAL-Blackburst on CVBS, VBS and C; all analog outputs are set to high impedance. A reset forces the I²C-bus interface to abort any running bus transfer and sets register 3A to 03H, register 61 to 06H and registers 6BH and 6EH to 00H. All other control registers are not influenced by a reset.

2.3 Input- and Output- Connectors**2.3.1 VG96 Input Connector on 7128MOD2****TABLE 1 Pinning of the VG96 module input connector (bottom view)**

IN	a	b	c
32	-5V ANALOG		
31	GND ANALOG		
30	+5V ANALOG		
29	GND DIGITAL		
28			
27	+5V DIGITAL		
26			
25	SDA	RESN	SCL
24	VP7		
23	VP6	CLKOUT*	
22	VP5		
21	VP4		
20	VP3	LLC_2*	
19	VP2		
18	VP1		
17	VP0	LLC_1	
16		ODD	
15			
14			
13		RTCI	
12		VS	
11		HS	
10		SOURCE*	
9			
8	MP7		TTXRQ
7	MP6		TTX
6	MP5		RCV2
5	MP4		RCV1
4	MP3		
3	MP2		
2	MP1		
1	MP0		

*: only for SAA7138/39

TABLE 2 Description of signals on the VG96 module input connector

Signal	Specification
SDA	I ² C-bus serial data.
SCL	I ² C-bus serial clock.
RESN	Reset Not Input (active LOW). After Reset is applied, all digital I/O's are in input mode; PAL-Blackburst on CVBS, VBS and C; RGB outputs set to lowest voltage. The I ² C-bus receiver waits for the START condition.
MP (7..0)	Double speed 54MHz MPEG port. Input for CCIR 656 style multiplexed Cb, Y, Cr data. Data are sampled at the rising and falling clock edge; data sampled on the rising edge then are sent to the encoding part of the device, data sampled on the falling edge are sent to the RGB part of the device (or vice versa, depending on programming)
DP* (7..0)	Data port input for CCIR 656 style multiplexed Cb, Y, Cr data.
LLC_1	Line-Locked clock input 1; this is the 27MHz master clock (via JP13A)
LLC_2*	Line-Locked clock input 2; this is the alternative source for the 27MHz master clock (via JP13)
CLKOUT*	Line-Locked clock output, this is the buffered output for the selected 27MHz master clock (via JP13A)
SOURCE*	Fast switch between DP and MP port. If the fader is bypassed, a HIGH selects MP port, a LOW selects DP port.
HS	Horizontal Synchronous signal for synchronization via RCV2.
VS	Vertical Synchronous signal for synchronization via RCV1 (JP9).
ODD	ODD/EVEN Field Identification, for synchronization via RCV1 (JP9).
RCV1	Raster Control 1, this pin provides or receives a VS, FS or FSEQ signal.
RCV2	Raster Control 2, this pin provides an HS pulse of programmable length or receives an HS pulse.
RTCI	Real Time Control input. If the LLC clock is provided by a digital video decoder like SAA7111A, supporting this function. RTCI should be connected to the RTCO pin of the respective decoder to get information concerning actual subcarrier, PAL-ID, and more, depending on the video decoder.
TTXRQ	Teletext Request output, indicating when the bit stream is requested.
TTX	Teletext bit stream input.

*: only for SAA7138/39

2.3.2 CVBS Subclick Connector

This is the output for the CVBS signal that passed the 5MHz LOWPASS FILTER and the JP14 (CVBS_out). This jumper selects the CVBS output (CVBS0 or optionally CVBS1,2 at Y/C lines). A simultaneous load at this connector and the SCART connector should be avoided.

2.3.3 SCART Connector

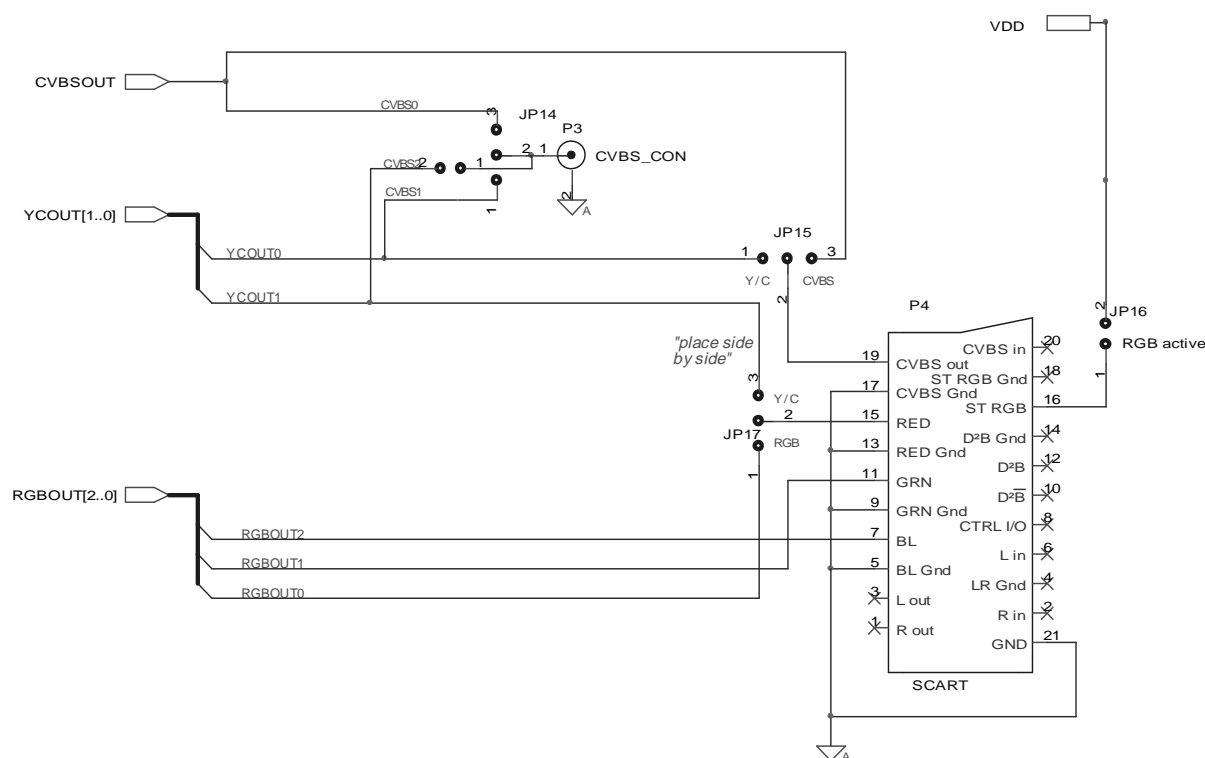


Fig.2 Output Connector

The figure above shows the analog output circuit with Subclick- and SCART- connector. The main CVBS line should not be switched to both Subclick and SCART (CVBS output or CSYNC) at the same time. The SAA7128/29 and SAA7138/39 offer additional CVBS outputs on Y and C pins as option (JP14). To enable RGB input to a SCART TV plug, close JP16. In this case JP17 must be in position 'RGB'

SAA7120/21: This device provides no other signals than CVBS and Y/C one time so the jumper configuration is JP14 = CVBS0 and JP17 = Y/C.

SAA7126/27: This device provides CVBS and Y/C or RGB signals at the respective connectors. For Y/C output JP31 and JP32 must be closed.

2.4 I²C-Bus

Two I²C-bus slave addresses are selected:

88H: LOW at pin SA

8CH: HIGH at pin SA

Systems running in a 3.3V environment probably require the same voltage for the I²C-bus. In this case, JP29 must be changed from default position to 3.3V in order to adjust the I²C supply voltage. A new Single Master Interface with the IC 74HC9114D can be used then, it replaces the former Single Master Interface with the IC 74LS05, which is only suited for 5V. The new interface operates on the I²C-bus from 1.8V to 5V.

Please note that there are no additional pullup resistors on this board, thus supply of the I²C-bus is provided once at the (single master-) I²C-bus interface.

On this backend module, two connectors can be used for I²C-bus control (alternative). The first one is a 6pin Mini DIN connector with the pinning shown on the right side of Fig.3. In order to consider different existing pinnings, the STOKO connector has a combined footprint for the standards 'Old', 'New' and 'US'. Please note that modules from the Philips Application Lab. Hamburg use the norm 'NEW' while the default configuration of the MPC module system is 'OLD'.

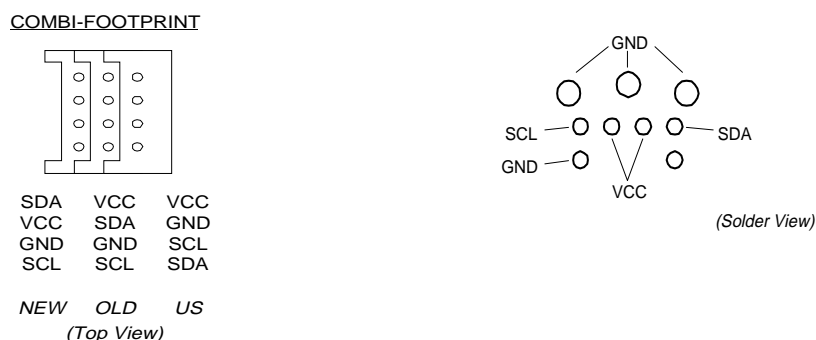


Fig.3 Pinning of I²C-STOKO and Mini-DIN connector

2.5 I²C EEPROM

A DIL 8 socket on each module is provided for adding an EEPROM with I²C interface. It can be used to store data for initialization and simple control functionality operated by a (future) microcontroller module. Several EEPROM types can be assembled depending on their memory size (e.g. PCF8582, PCF8594, PCF8598, X24164). Additionally, the I²C-bus device address can be adapted by using the jumper 1..3 (EEP-Adr).

2.6 Clock- and Synchronization signals

There are two operating modes for the encoder on this board. In master mode, V- and H- signals are output of the RCV1 and RCV2 pins in order to synchronize an external source (e.g. memory or teletext).

In slave mode the synchronization signals H and V are generated out of the frame sync code embedded into the CCIR-656 data stream or fed to the encoder via RCV1 and RCV2 (after passing JP23 and JP24). The configuration of RCV1 and RCV2 (direction, polarity etc.) is handled in Reg. 6BH (Some information about register-functions can be found on page 25). After a reset the RCV pins are programmed as inputs.

Regardless of master or slave mode operation, the system clock LLC can come from external or from the chip's own oscillator. Figures 4 and 5 show the respective jumper to configure clock direction. When an external clock is received, JP27 and JP28 allow termination of LLC_1 and LLC_2 by adding a 240R resistor to ground. In addition to this, series resistors (22R) terminate these clock lines.

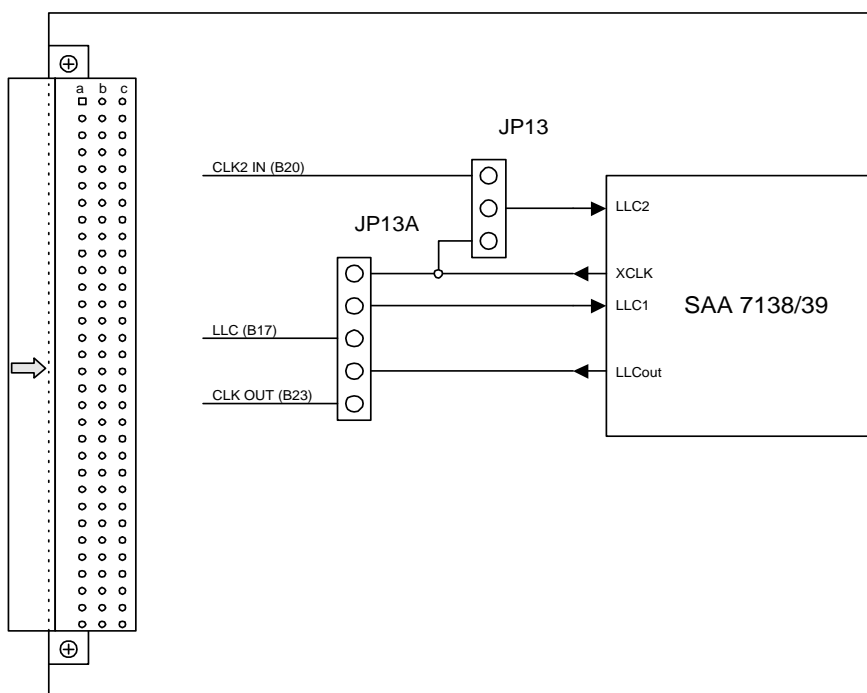


Fig.4 Clock switching for SAA7138/39

Possible applications are:

- The internal oscillator provides the master clock by connecting XCLK and LLC1 (or LLC2). The buffered clock signal at pin LLCOUT is switched to VG96 pin LLC for other circuits.
- An external oscillator can clock the device via VG96 pin CLK2_IN and JP13. Like in the first case, the buffered clock signal at pin LLCOUT is switched to VG96 pin LLC for other circuits.
- An external oscillator can clock an external device (e.g. MPEG decoder). The clock signal comes in via CLK2_IN and out via the buffered clock output LLCOUT and the VG96 pin CLKOUT.

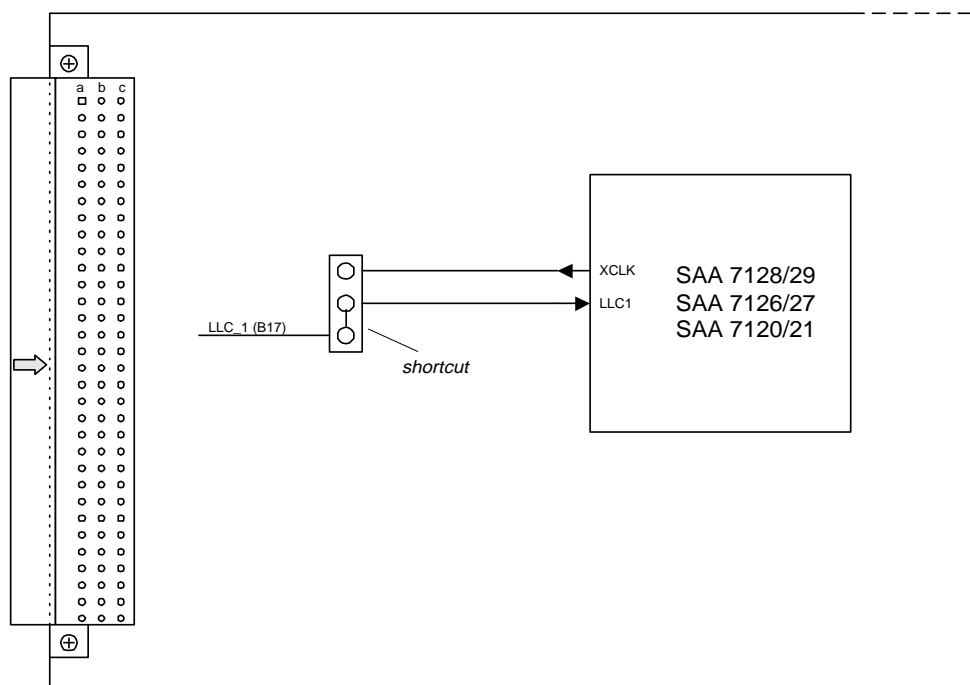


Fig.5 Clock switching for SAA7128/29 ('26/'27, '20/'21)

If types other than SAA7138/39 are being used, only jumper (JP13) is essential. In master mode the internal oscillator generates the clock at pin XCLK and jumper (JP13) is used to connect the device and external circuits via LLC_1. The shown shortcut is done by a 0R resistor.

In slave mode this jumper must be open.

2.7 Jumperlist**TABLE 3 Jumperlist 7128MOD2**

Jumper	Name	Description
JP1,2	'C'	5MHz lowpass filter 1 ON/OFF
JP3,4	'Y'	5MHz lowpass filter 2 ON/OFF
JP5,6	'CVBS'	5MHz lowpass filter 3 ON/OFF
JP7,8	'B'	5MHz lowpass filter 4 ON/OFF
JP9,10	'G'	5MHz lowpass filter 5 ON/OFF
JP11,12	'R'	5MHz lowpass filter 6 ON/OFF
JP13	XCLK/CLK2IN	Handles clock direction together with JP13A
JP 13A	CLOCK I/O	(5 pins) Handles clock directions acc. to Fig.
JP14	CVBS out	Connects default CVBS1 or opt. CVBS2,3 to SubClick
JP15	Y/C / CVBS	SCART output: CVBS0 or Y
JP16	RGB active	Activates RGB input of e.g. TV if closed
JP17	Y/C / RGB	SCART output: RED or C
JP18	A0	EEPROM address A0
JP19	A1	EEPROM address A1
JP20	A2	EEPROM address A2
JP21	S5/O10 CVBS2	Closed: CVBS2 out; open: for Y/C out (C-path)
JP22	S5/O10 CVBS1	Closed: CVBS1 out; open: for Y/C out (Y-path)
JP23	HS to RCV2	Connects HS line to RCV2 device-pin
JP24	ODD/VS	Connects ODD line or Vertical Sync to RCV1 device-pin
JP25	SA	I ² C slave address select, closed = 88H, open = 8CH
JP26	RESN	Selects source for Reset Not signal (push-b./inp.conn.)
JP27	TERMLLC_1	Termination of 1st LLC line with 240R
JP28	TERMLLC_2	Termination of 2nd LLC line with 240R
JP29	IIC 5V/3V	Supply voltage for I ² C-bus (default: 5V)
JP30	SOURCE	Fast Switch Input Port (only for SAA7138/39)
JP31	Y/C SAA7126	Y/C output from SAA7126/27 (C-path)
JP32	Y/C SAA7126	Y/C output from SAA7126/27 (Y-path)

3. Interfacing Input Data with a Y-module

The following drawings show some principal ways how to connect a Chameleon Digital Video Encoder to one or two video/overlay data sources.

Within SAA7128/29 (eventually within a device indicated here as SAA7138/39), the two video data streams can be directed separately to RGB outputs and Y/C/CVBS outputs. A hard keying or versatile chroma keying and fading is available for combining both data streams

Mode 1:

Clock LLC comes from SAA7111A (or a similar Philips Digital Video Decoder), the SAA7128/29 video encoder is slaved to the sync code (frame sync) embedded into the CCIR-656 data stream from SAA7111A. Output H - sync and V- sync from SAA7128/29 master a memory controller and memory for output of overlay data. Memory controller and associated memory can also be considered to be represented by the OSD/overlay part of an MPEG decoder.

The two data streams, one from SAA7111A, the second from the overlay generator, are multiplexed to a physical 54 MHz data stream, using LLC as a control signal for the external multiplexer.

Mode 2:

The on-chip LLC clock generator of SAA7128/29 is used to clock the MPEG decoder and the memory, providing OSD/overlay signals. Both MPEG decoder and separate overlay source are slaves of SAA7128/29 H- and V- syncs.

This seems to be a rather uncommon configuration, in practice Mode 3 will be more of interest.

Mode 3:

LLC clock is coming from the on-chip crystal oscillator of SAA7128/29, which should be able to be fine-tuned in a certain range. (LLC could also come from an external oscillator of similar properties). The MPEG decoder is slaved to SAA7128/29 w.r.t. H- sync and V- sync.

A 54 MHz multiplexed data stream, carrying e.g. video with overlay data at the rising clock edge and video without overlay data at the falling clock edge, is directly fed to the 54 MHz input port of SAA7128/29.

Mode 4:

As the device indicated here SAA7138/39 has two separate 8 bit D1 ports, 'MP' and 'VP', external demultiplexing is not necessary.

The video decoder SAA7111A is master for the video encoder w.r.t. LLC clock and H-sync and V-sync (embedded frame sync in the CCIR-656 data coming out of the video decoder and going into VP input).

The encoder-internal clock chip buffers the clock as LLCOUT for the OSD/overlay source. SAA7138/39 is sync master for the OSD/overlay source, which is sending its data to the MP input.

Again, this configuration seems to be uncommon (for test purposes, only), and Mode 5 should be focused on the more.

Mode 5:

Again, the video decoder SAA7111A is clock and sync master for SAA7138/39, providing clock LLC to clock input LLC_1, and video and sync via input port VP.

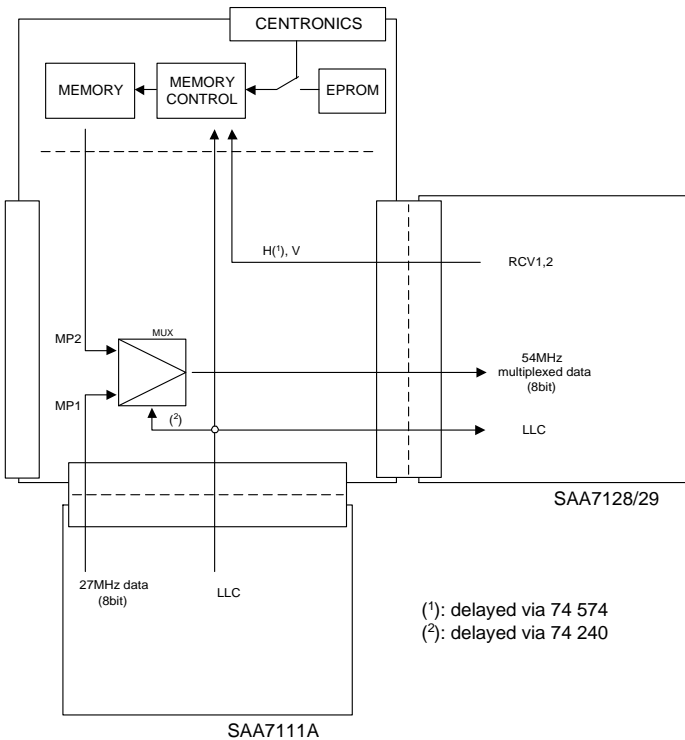
Through H- and V- sync coming out of SAA7138/39, additional OSD/overlay data can be taken from the MPEG decoder in order to overlay it to the (digitized) analog video. In this case, LLCOUT for the MPEG decoder is derived from LLC_1. The OSD/overlay data can come with the rising or falling edge of LLCOUT or with both edges.

If the active video source is MPEG video, the SAA7111A video decoder will idle, and clock for SAA7138/39 is LLCO, fed to the LLC_2 input of the encoder-internal clock multiplexer. For this operational mode, also the on-chip crystal oscillator instead of an external oscillator could be used.

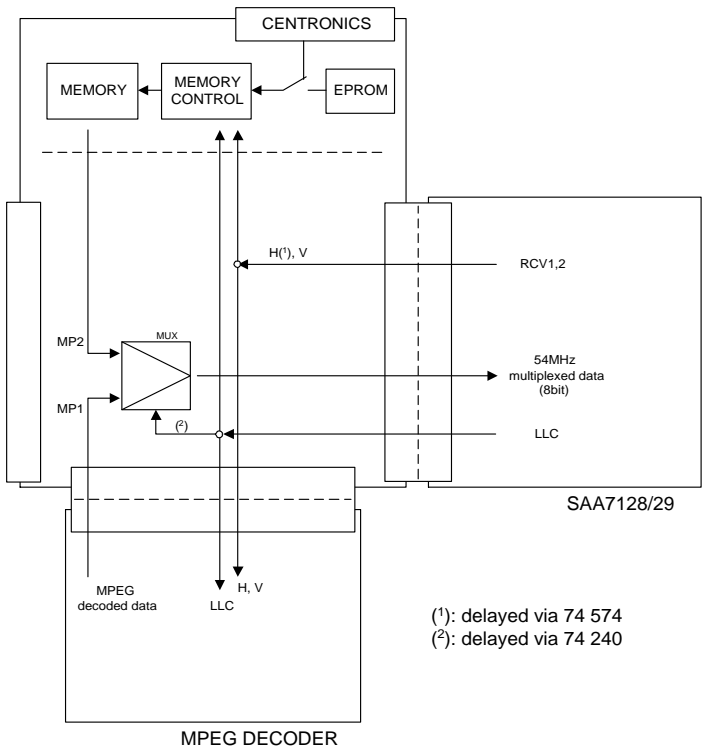
Module System: 7128MOD2

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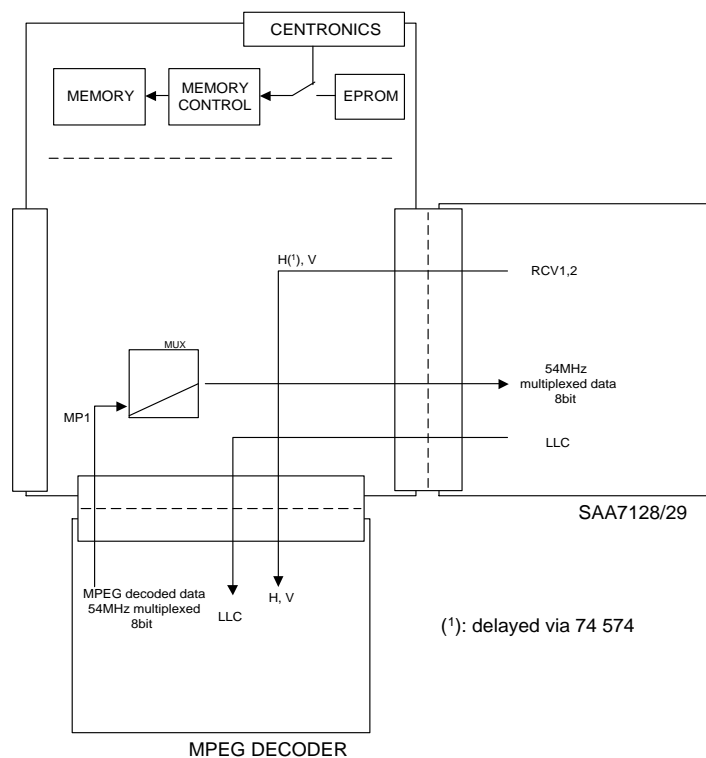
Interfacing 54MHz data via Y-module with SAA7128/29 operating as a clock slave / master (mode1 + 2)



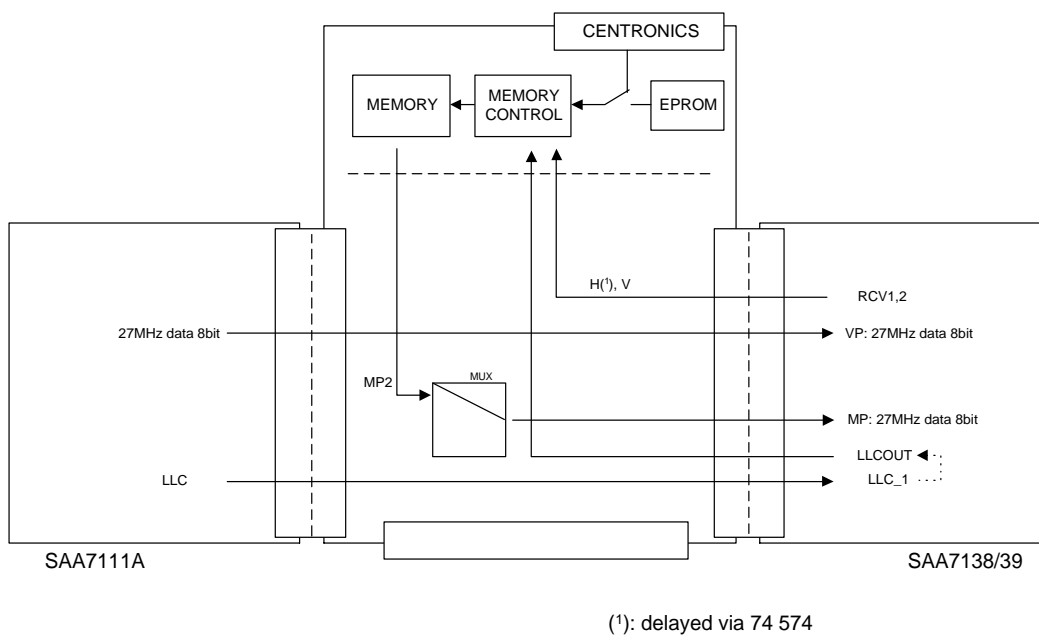
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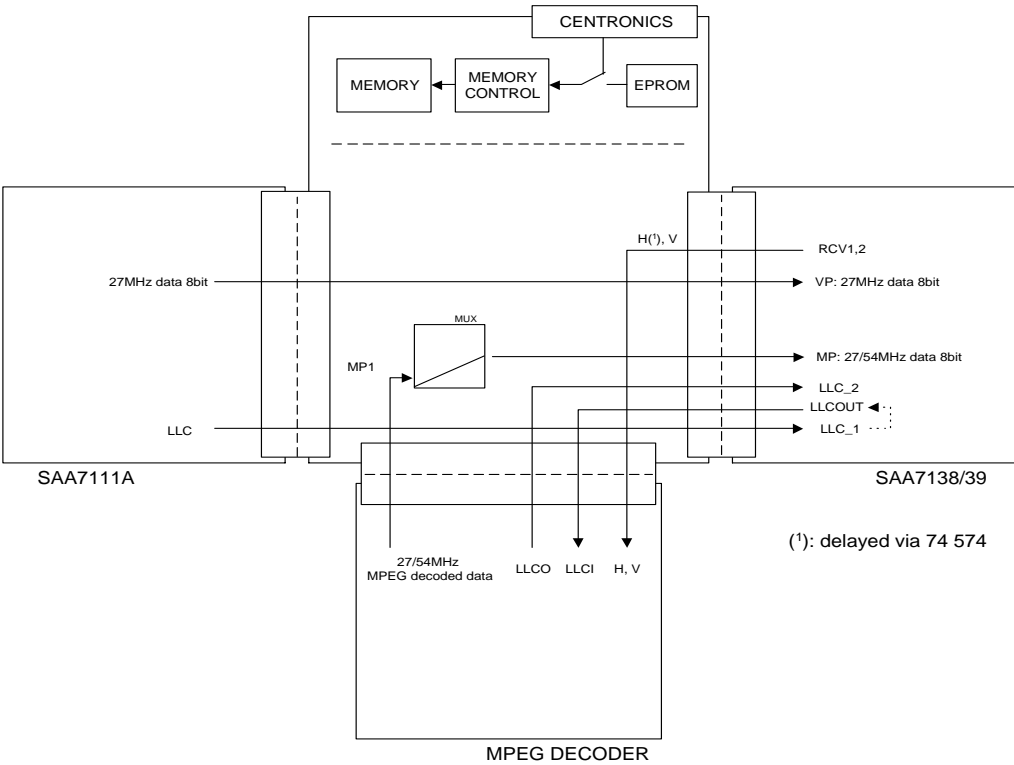
Interfacing 54MHz data via Y-module with SAA7128/29 operating as a clock master (mode 3)



Interfacing 54MHz data via Y-module with SAA7138/39 operating as a clock slave (mode 4)



Interfacing 54MHz data via Y-module with SAA7138/39 operating as a clock slave (mode 5)



4. Tips for a PCB layout

4.1 Analog and digital signal processing

- use separate ground planes for analog and digital supply in one layer (no overlapping!)
- use separate supply planes for analog and digital with the same shape (or smaller) as ground (no overlap of analog supply with digital ground and vice versa!)
- if there are different (asynchronous) clock domains, use separate ground and supply planes (place the analog areas not in a direct neighborhood; separate the clock domains)
- always use the inner layers for ground and supply planes (no signal layer in between!)
- try to keep digital signals away from analog areas
- place analog areas close to the border of a PCB
- avoid long tracks for analog signals
- place decoupling capacitors (22nF to 100nF) close to the power pins of the ICs
- prepare several provisions for connecting places for analog and digital ground on the PCB for further optimization on the final board.

4.2 IIC bus

always supply the I²C-bus with pull-up resistors, but avoid too high currents. The values of resistors R_p and R_s depend on the following parameters:

- supply voltage
- bus capacitance
- number of connected devices (input current + leakage current)

please see I²C-bus specification (e.g. chapter 10.1 in the Philips data handbook: 'Maximum and minimum values of resistors R_p and R_s ').

4.3 Application information

Application environment of all possible encoders on this board is shown at the end of the datasheet of the respective device.

5. Software

The enclosed disk contains the latest version of the Universal Register Debugger Software (URD) and some files and macros for easy debugging Philips encoders and decoders in conjunction with the I²C-bus Parallel Port adaptor.

For this module please open the file SAA7128.urd to get a default setup as described on the following page. The information will be transmitted by clicking the 'WD' (write default) push button.

To change this setting (e.g. for NTSC or SECAM encoding) there exist macros as shown on pages page 24 and following. The program is caused to perform a macro operation by clicking the push button right in front of the macro name.

For editing single values use +/- on your keyboard and then click 'WN' (write now).

You can find further details concerning the software in the doc-file on the disk.

5.1 Programming tables for SAA7128/29

SAA7128/29: init data PAL Slave: 88H or 8CH	
Sub	Data
Reg 26H	0DH
Reg 27H	00H
Reg 28H	1FH
Reg 29H	1FH
Reg 2AH	75H
Reg 2BH	3FH
Reg 2CH	06H
Reg 2DH	3FH
Reg 38H	1AH
Reg 39H	1AH
Reg 3AH	13H
Reg 42H	00H
Reg 43H	68H
Reg 44H	10H
Reg 45H	97H
Reg 46H	4CH
Reg 47H	18H
Reg 48H	9BH
Reg 49H	93H
Reg 4AH	9FH
Reg 4BH	FFH
Reg 4CH	7CH
Reg 4DH	34H
Reg 4EH	3FH
Reg 4FH	17H
Reg 50H	00H
Reg 51H	83H
Reg 52H	83H
Reg 53H	80H
Reg 54H	8CH
Reg 55H	0FH
Reg 56H	C3H
Reg 57H	06H
Reg 58H	02H
Reg 59H	80H
Reg 5AH	34H
Reg 5BH	7DH

Sub	Data
Reg 5CH	AFH
Reg 5DH	2DH
Reg 5EH	3FH
Reg 5FH	3FH
Reg 60H	7BH
Reg 61H	02H
Reg 62H	46H
Reg 63H	CBH
Reg 64H	8AH
Reg 65H	09H
Reg 66H	2AH
Reg 67H	77H
Reg 68H	41H
Reg 69H	88H
Reg 6AH	41H
Reg 6BH	12H
Reg 6CH	02H
Reg 6DH	20H
Reg 6EH	A0H
Reg 6FH	B4H
Reg 70H	41H
Reg 71H	C3H
Reg 72H	00H
Reg 73H	3EH
Reg 74H	B8H
Reg 75H	1EH
Reg 76H	15H
Reg 77H	16H
Reg 78H	15H
Reg 79H	16H
Reg 7AH	2BH
Reg 7BH	D9H
Reg 7CH	80H
Reg 7DH	00H
Reg 7EH	00H
Reg 7FH	00H

The table shows a default setup for the SAA7128/29. with following settings:

- 8-bit input data format
- working as clock slave
- detection of sync. signals (H, V) out of datastream
- Output format = PAL
- WSS, TTX and Closed Caption disabled
- Internal colour bar off (LUT's programmed to 100% colourbar)
- not listed registers must be programmed to 00H

To activate the programmable colour bar generator the MSB of register 3AH must be set to '1'.

Bold signed registers must be edited for changing the output format (NTSC, SECAM)

The most important changes e.g. concerning output format are shown in the next tables.

TABLE 4 Changes for NTSC and SECAM

SAA7182/83: changes for NTSC Slave: 88H or 8CH	
Sub	Data
Reg 5AH	
Reg 5BH	
Reg 5CH	
Reg 5DH	
Reg 5EH	
Reg 5FH	
Reg 61H	
Reg 62H	
Reg 63H	
Reg 64H	
Reg 65H	
Reg 66H	
Reg 6CH	
Reg 6DH	
Reg 6EH	
Reg 7AH	
Reg 7BH	

SAA7182/83: changes for SECAM Slave: 88H or 8CH	
Sub	Data
Reg 5AH	
Reg 5BH	
Reg 5CH	
Reg 5DH	
Reg 5EH	
Reg 5FH	
Reg 61H	
Reg 62H	
Reg 63H	
Reg 64H	
Reg 65H	
Reg 66H	
Reg 6CH	
Reg 6DH	
Reg 6EH	
Reg 7AH	
Reg 7BH	

The tables show the registers that are changed when performing a macro function.

5.2 Summary of Registerfunctions

In the following table the usage of registers is described in order to get a quick view of the most important functions and give help for programming the device. The table does not contain whole information about the function or determination of values but should give background information. The subaddress is the location according to the described function but not exclusive in every case. For further details see chapter 'Slave Receiver' in the datasheet.

TABLE 5 Registers of the SAA7128/29

Function	SubAdr	Description
Status byte (read only)	00H	
NULL	01H - 25H	Always program with 00H in order to avoid unexpected effects
Wide Screen Signal	26H - 27H	WSSON enables or disables completely the WSS encoding; for meaning of the individual bits refer to the table given in ETS-300 294
Real Time Control	28H	If RTCE is set to high, Real Time Control (RTC) of the generated subcarrier frequency is enabled. RTC should be used whenever the clock for the video encoder is generated by a digital line-locked video decoder to ensure stable encoding phase for clean colors. From a decoder supporting the new function DECCOL, a flag indicating that color was detected can be received if DECCOL=high. If DECFIS=high, the field frequency information detected by a decoder can be received.
Burst Start / End	28H - 29H	The begin and the end of the color burst can be adjusted in a certain range at an accuracy of LLC clock cycles; the suggested defaults should be used
Copy Generation	2AH - 2CH	CG19-CG0: LSB's of the respective bytes are encoded immediately after run-in, the MSB's of the respective bytes have to carry the CRCC bits, in accordance with the definition of Copy Generation Management System encoding format. CGEN set low disables the insertion.
Output Port Control	2DH	All DAC outputs can be set individually to high impedance through bits BTRI (Blue or Cb), GTR (Green or Y), RTRI (Red or Cr) YTRI (VBS or CVBS), CVBSTRI (CVBS or CSYNC). If CVBSEN0 is set low, the C signal is directed to the DAC normally used for this signal; if CVBSEN0 is set high, a CVBS signal is directed to this DAC as an alternative. If CVBSEN1 is set low, the VBS signal is directed to the DAC normally used for this signal; if CVBSEN1 is set high, a CVBS signal is directed to this DAC as an alternative.
NULL	2EH - 37H	Always program with 00H in order to avoid unexpected effects
Gain Luma and Gain Colour Diff. of RGB	38H - 39H	Common practice is to set GY=GCD in order to adjust both luminance contrast and color saturation, when RGB output mode is chosen. The suggested nominal values given in the datasheet are based on the proposed external resistor circuitry (23 Ohm series, 75 Ohm load).

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Function	SubAdr	Description
Input Port Control 1	3AH	<p>(0, 1): setting these bits high for straight binary data, inverts the MSB internally for correct processing; setting these bits low passes the data as it is.</p> <p>(2): when this bit is set low, a CVBS signal is directed to the DAC normally used for this signal; if it is set low, a composite sync only is directed to this DAC as alternative.</p> <p>(3): when this bit is set high, the color dematrix is by-passed, and video input is only up-sampled to 27 MHz data rate for output instead of RGB.</p> <p>(4): when this bit is set high, in slave mode the encoder is triggered by an embedded frame sync code within the CCIR-656 data input. If the embedded frame sync is not available, this bit must be set low and appropriate signals have to be provided at RCV1 and RCV2 inputs.</p> <p>(6): SAA7138/39 only: this bit set low enables the fader function; if it is set high, two input signals can be hard-keyed via the pin SOURCE.</p> <p>(7): setting this bit high decouples the video input and inserts a test signal defined by eight color-programmable bars, e.g. a 100/75 color bar.</p>
Key Colour	42H - 4DH	Two 24 bit (True Color) color ranges KEY1 and KEY2 are defined, which together with the weighting factors Fade1 and Fade2 determine the YUV color range of the first input signal to be blended with the second input signal.
Fade	4EH - 50H	<p>FADE1, FADE2 and FADE3 are 6 bit multipliers, defining the transparency of the two input signals. While FADE1 and FADE3 operate in the YUV color space defined through the borders of the Key Color parameters, FADE3 blends the color stored in the internal LUT against one of the input signals.</p> <p>If CFADEV is set high, the first input signal (MP1) at port MP is mixed entirely with the color stored in the internal LUT, using FADE3 as multiplier, regardless of the defined Keying range.</p> <p>If CFADEV is set high, the second input signal (MP2) at port MP is mixed entirely with the color stored in the internal LUT, using FADE3 as multiplier, regardless of the defined Keying range.</p>
Look up table for Key Colour	51H - 53H	True color value of the internal Lookup table that is used for blending if a color within color range KEY2 is detected in the first input signal.
Input Port Control 2	54H	<p>If EDGE1 set low, data of the first input signal at MP port are sampled at the rising clock edge, otherwise at the falling clock edge.</p> <p>If EDGE2 set low, data of the second input signal at MP port are sampled at the rising clock edge, otherwise at the falling clock edge.</p> <p>Only SAA7138/39: If VPSEL set low, Fader input VP is fed with data applied to DP port, if VPSEL set high, Fader input VP is fed with data applied to MP2 input.</p> <p>If DELIN set low, data at DP port are by-passing the fader; if DELIN set high, data of MP2 are by-passing the fader.</p> <p>If RGBIN set low and DELIN set low, data to the RGB processor come from the DP port; if RGBIN set low and DELIN set high, data to the RGB processor are MP2 data;</p> <p>If RGBIN set high, the output of the fader is fed data to the RGB processor.</p>

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Function	SubAdr	Description
Video Programming System Data Insertion	54H - 59H	VPSEN set to high enables the insertion of data for Video Programming System. Five bytes VPS5, VPS11, VPS12, VPS13, and VPS14 can be loaded acc. to the specification of VPS
Chroma Phase	5AH	This register defines the absolute subcarrier phase w.r.t. the synchronization pulse scheme. Although in practice the absolute subcarrier phase is almost never relevant, values for the most common standards NTSC-M and European PAL are given. Please note that the value is different when the internal color bar function is active.
Gain_U, Gain_V	5BH - 5EH	These registers directly influence the amplitude of the internal color difference baseband signals and thus of the generated subcarrier for quadrature modulated standards (for SECAM, the frequency deviation is influenced!) Usually, the nominal settings given in the datasheet should be used; in case that an analog post filter contributes noticeable attenuation around the subcarrier frequency, both GAINU and GAINV should be enlarged accordingly. Note that the sign bit (0=positive, 1=negative) is located in 5DH for GAINU and in 5EH for GAINV.
Black Level	5DH	This parameter adds a certain offset to the luminance signal w.r.t. to the sync tip, but leaves the peak-peak amplitude unaffected.
Real Time Control	5DH - 5EH	IF DECOE=high, the odd/even information can be received from a decoder supporting this function. If DECPH=high, a subcarrier oscillator phase reset initiated on the decoder side will reset the phase of the encoder oscillator.
Blanking Level	5EH - 5FH	This parameter adds a certain offset to the luminance blanking level w.r.t. the sync tip. Note that this parameter has to be set twice, i.e. outside (5EH) and inside (5FH) the vertical blanking interval. Usually, both blankings are identical.
NULL	60H	Always program with 00H in order to avoid unexpected effects
Standard Control	61H	(0): configures the internal pixel counter either to 858 pixels/line (high) or 868 pixels/line (low) (1): this bit set to high enables the PAL specific process of inverting the V color difference component line by line. (2): usually set to high for standard-compliant chroma bandwidth; in some cases (e.g. for best S-Video quality), it can be set to low. (3): this bit set to high enables the SECAM processing; it overrides bit PAL (4): this bit selects one of two possible gain factors for the luminance black-to-white amplitude; when set to high, luminance is adjusted for 92.5 IRE output amplitude, and when set to low for 100 IRE output amplitude. (5): only relevant when RTCE bit is high; usually set to low. (6): if set to high, internally a constant code corresponding to the lowest possible output voltage at the DACs for CVBS, Y/C is applied. (7): if set to high, internally a constant code corresponding to the lowest possible output voltage at the DACs for R, G, B is applied.

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Function	SubAdr	Description
Real Time Control Enable	62H	If RTCE is set to high, Real Time Control (RTC) of the generated subcarrier frequency is enabled. RTC should be used whenever the clock for the video encoder is generated by a digital line-locked video decoder to ensure stable encoding phase for clean colors.
Burst Amplitude	62H	These registers directly influence the amplitude of the color burst for quadrature modulated standards (for SECAM, the amplitude of the color burst cannot be modified!) Usually, the nominal settings given in the datasheet should be used; in case that an analog post filter contributes noticeable attenuation around the subcarrier frequency, this parameter should be enlarged accordingly.
Subcarrier Frequency	63H - 66H	The subcarrier frequency is synthesized by a 32 bit Discrete Time Oscillator; all four bytes are fully programmable
Line 21 Encoding	67H - 6AH	Closed Caption and Extended Data Service bytes to be downloaded including parity bit at the MSB position of each byte.
RCV-Port Control	6BH	Handles input- or output signal of RCV1 and RCV2 pins (see corresponding table in the datasheet). Although the usual definition for master mode stands for trigger I/O's to be switched to output, the device allows for a kind of mixed mode as to be slaved by a frame sync applied to pin RCV1 and simultaneously to output a horizontal pulse on pin RCV2.
H-Trigger Control	6CH - 6DH	Sets the Horizontal Trigger phase related to signal on RCV1 or RCV2. If a vertical sync is applied to RCV1, an additional horizontal sync at RCV2 is needed to adjust the position of video horizontally.
V- Trigger Control	6DH	Sets the Vertical Trigger phase related to the input signal on RCV1; value VTRIG - counting half lines - should be even, only.
Field Length Control	6EH	Interlaced operation or two different non-interlaced modes are selectable for 525/60 signals or 625/50 signals.
Luma Delay	6EH	depending on LDEL1 and LDL0 bits, an extra delay of the luminance signal portion (for VBS or CVBS) can be added in order to compensate for group delay distortions of the analog post filter.
Phase Reset Mode of the colour subcarrier generator	6EH	These two bits should exactly be set acc. to the table in the datasheet. For NTSC signals, both 'two-line reset' or 'four-field reset' are possible.
BLCKON	6EH	this bit set to low ensures normal operation, while set to high forces the all signals to blanking level.
V-Blanking Definition	6EH	setting this bit to low will define the Vertical Blanking Interval by the values loaded into registers FAL and LAL; if this bit is set to high, the Vertical Blanking Intervall is forced acc. to CCIR-624 (50Hz) or acc. to RS170A (60Hz)
Individual Line 21 Encoding	6FH	Two bits enabling field-dependent insertion of Closed Caption/ Eextended data.
Teletext Enable	6FH	For any line with Teletext insertion, this bit must be set to high, as it is a master switch. The actual selection for activated Text lines is made below.

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Function	SubAdr	Description
Line Select for Closed Caption or extended data	6FH	This parameter selects one out of 32 possible position for Closed Caption encoding; usually it is line 21 for NTSC corresponding to 11h.
Start / End RCV2	70H - 72H	These registers define start and end of a pulse repeating at line frequency: Note that if 'Start' is greater than 'End', the pulse will be inverted.
Start / Delay TTXRQ	73H - 74H	Every high-state of the signal at pin TTXRQ - depending on the chosen Text format - initiates the transfer of a new Teletext bit stream bit; as this bit stream must match to the internal pixel counter, the start of the first request pulse is programmable by TTXHD to accommodate to individual latencies of the bit stream source. TTXHS is an internally needed parameter and should be taken as given in the datasheet.
VSYNC shift	75H	In master mode (RCV1 and RCV2 as outputs), sometimes the phase of the horizontal pulse on RCV2 must be shifted against the phase of the vertical sync pulse on RCV1 in steps of 27 MHz clock cycles. This can be accomplished with this parameter in 3 steps.
CSYNC advanced	75H	In order to compensate for shorter propagation of RGB signals through a TV SCART input, the alternative CSYNC signal on the (usually) CVBS DAC can be advanced up to 31 LLC clock cycles.
TTX odd / even request VS/VE	76H-79H, 7CH	For the odd and even field, the lines to carry Teletext information can be determined individually. Note that it is possible to nearly use the complete inactive and the complete active fields for Teletext insertion instead of video.
First / Last Active Line	7AH - 7CH	These parameters define the Vertical Blanking Interval if bit SBLBN = low. Main purpose is to widen the range for active video input, as the input data are ignored during the lines that are dedicated to belong to the Vertical Blanking Interval. E.g., Time code could be inserted through the video input port when FAL is programmed to start before the normal first active line.
TTX mode	7CH	TTXO set to low enables the universal TTX protocol: At every rising edge of TTXRQ a single TTX bit is requested. TTXO set to high enables the older TTX protocol for compatibility reasons: The encoder provides a high state window of TTXRQ, and the length of the window depends on the chosen Text standard. Depending on the selected field frequency (Bit FISE), the Teletext standard is being selected through TTX60
NULL	7DH	Always program with 00H in order to avoid unexpected effects
Disable TTX Line	7EH - 7FH	Starting with line line 8, ending with line 23 inclusive, each of these lines can be disabled for Teletext insertion (the respective bit set to high), although enabled by the global window definitions for Teletext. This can be useful in order to allow e.g. other information entering through the video input to be inserted between lines containing Teletext.

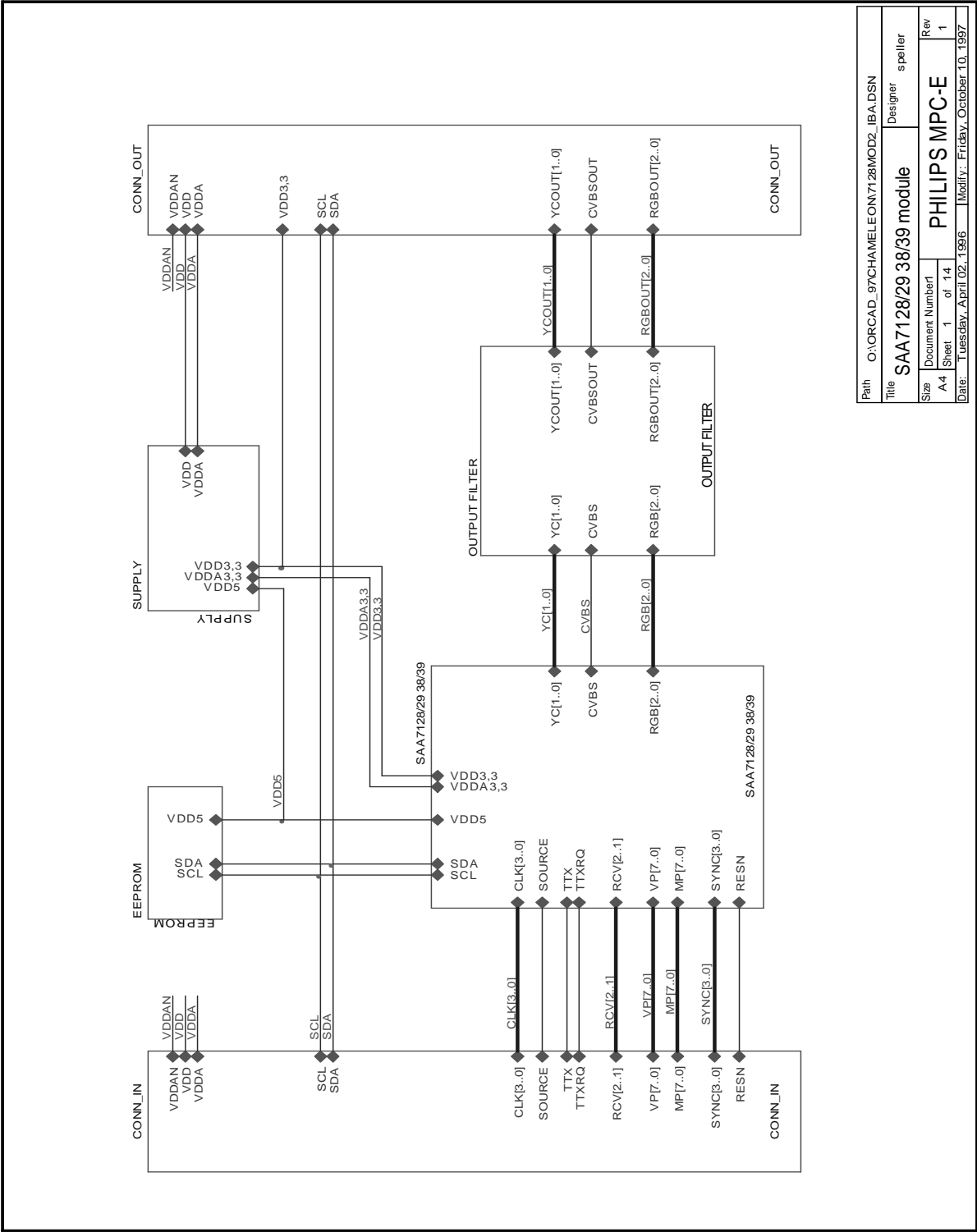
6. Appendix: Schematics and Layout

The schematics (made in ORCAD) can be delivered on request.

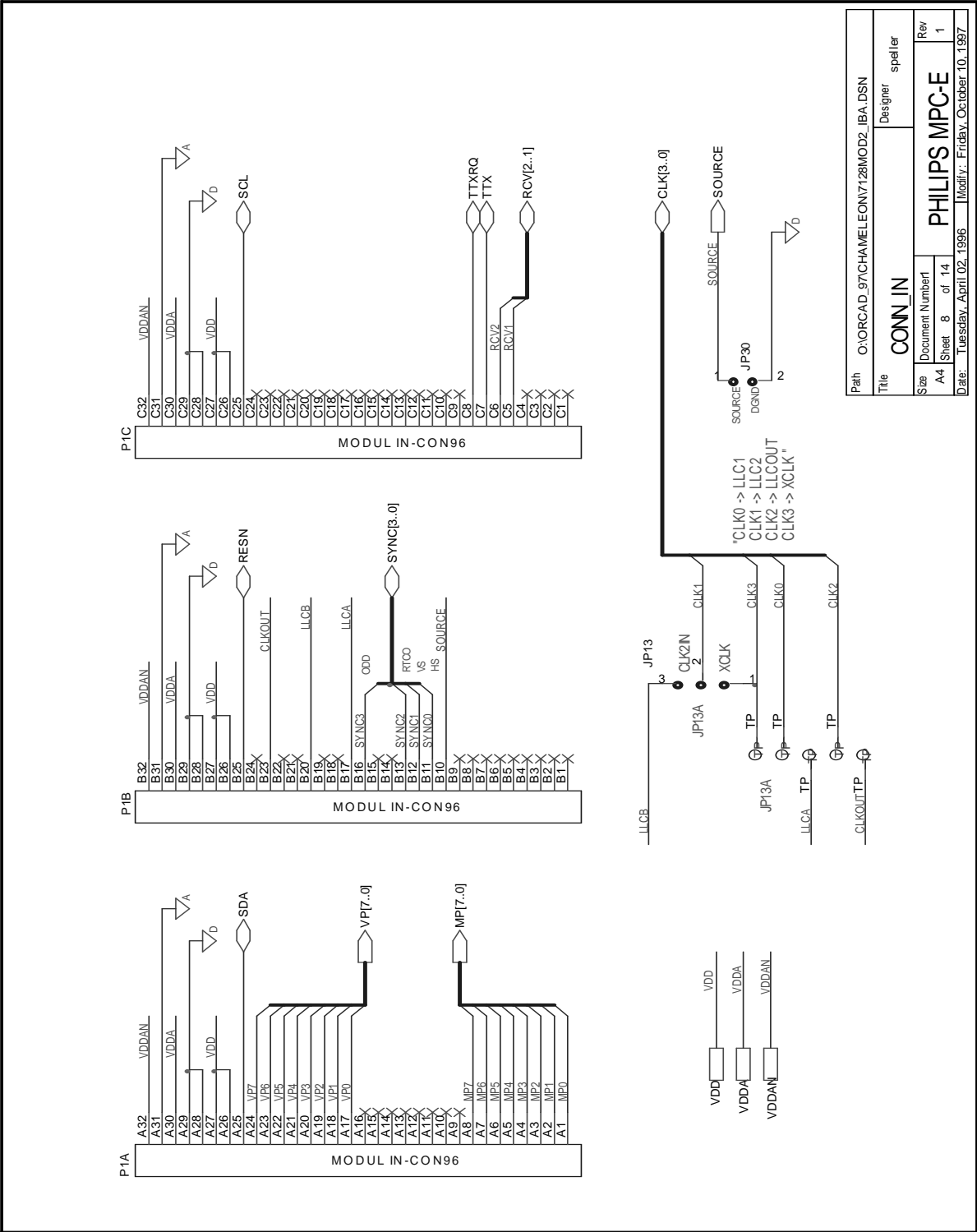
For a board layout GERBER files are available.

6.1 Schematic

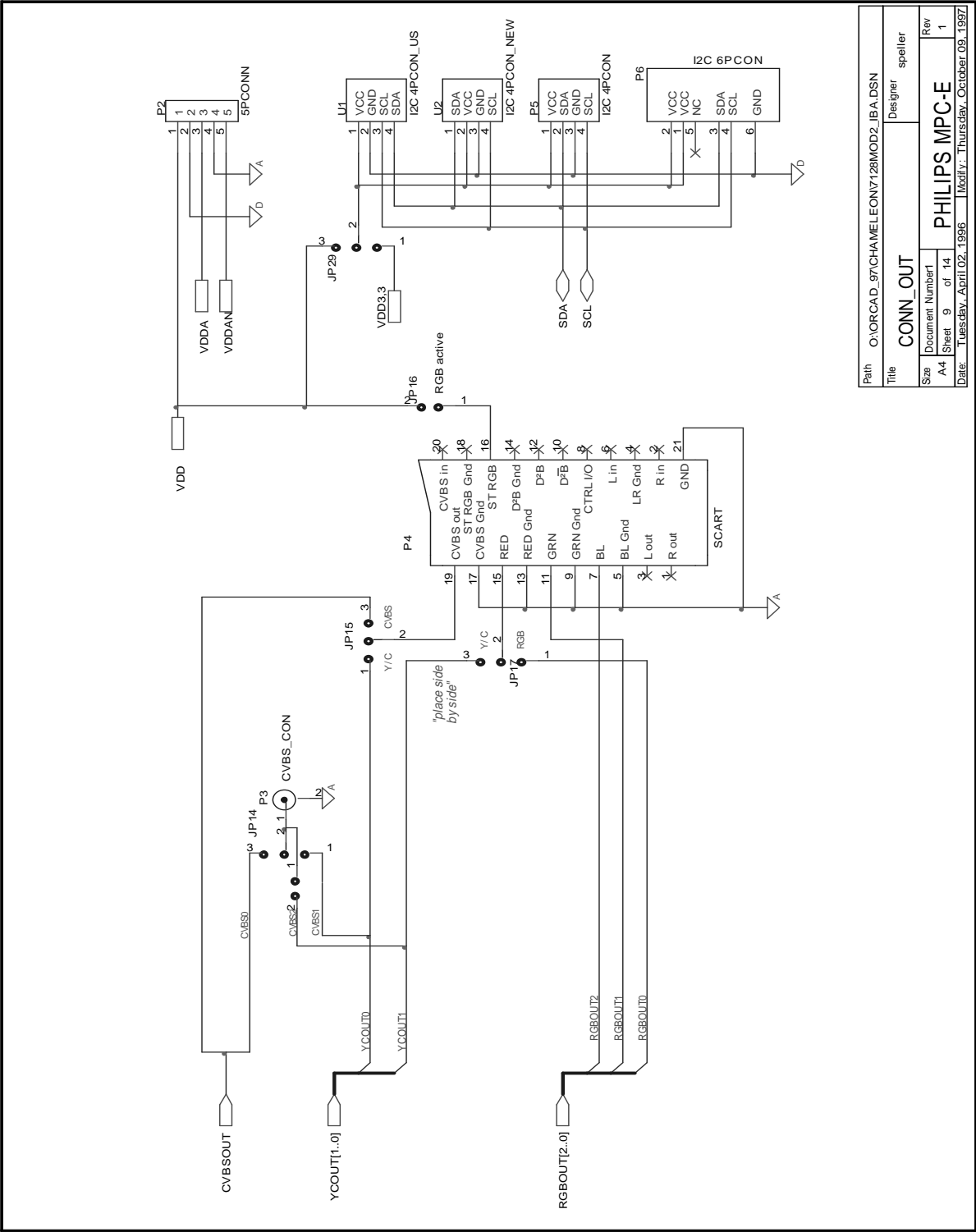
6.1.1 Top Sheet of 7128MOD2



6.1.2 Connector In



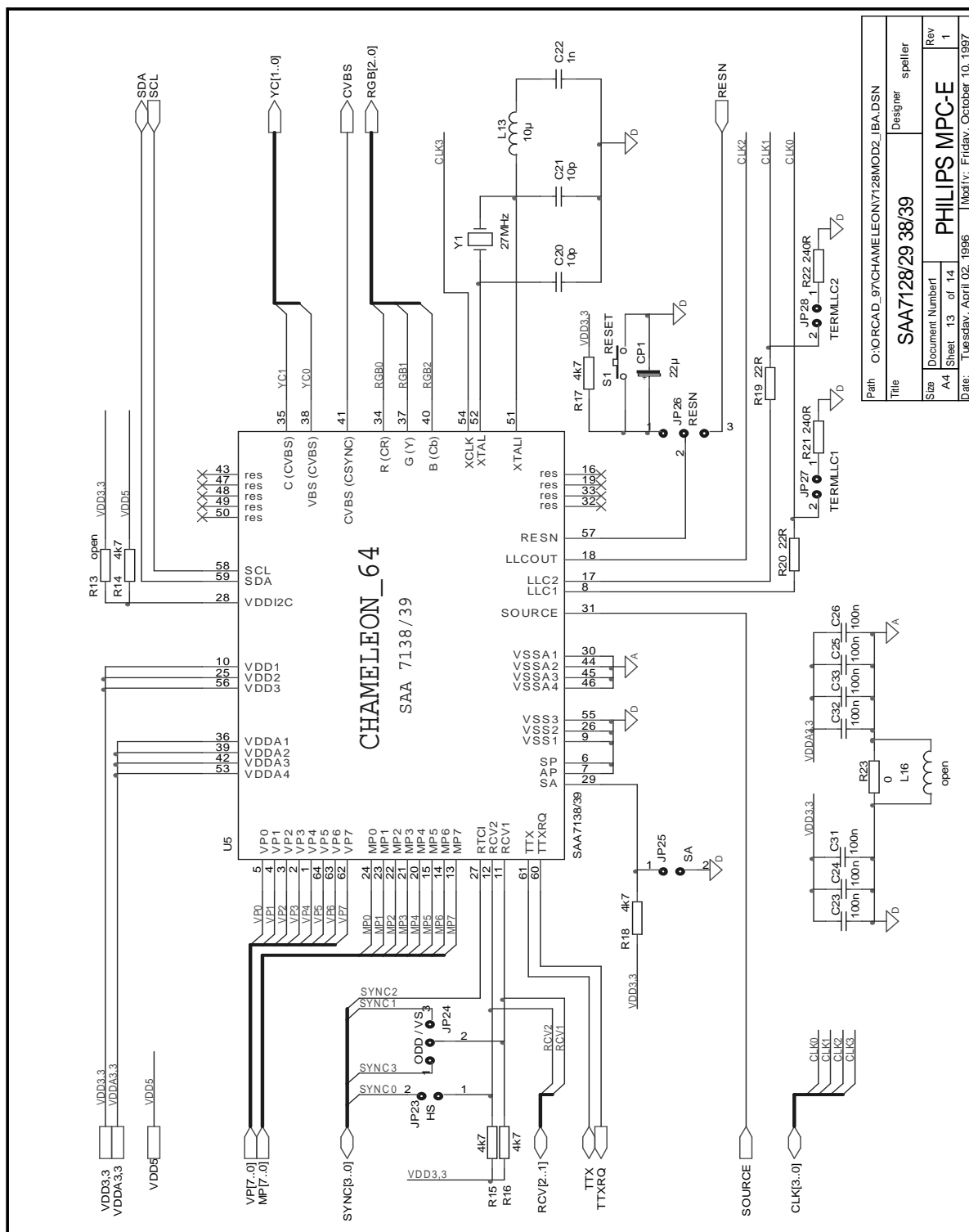
6.1.3 Connector Out



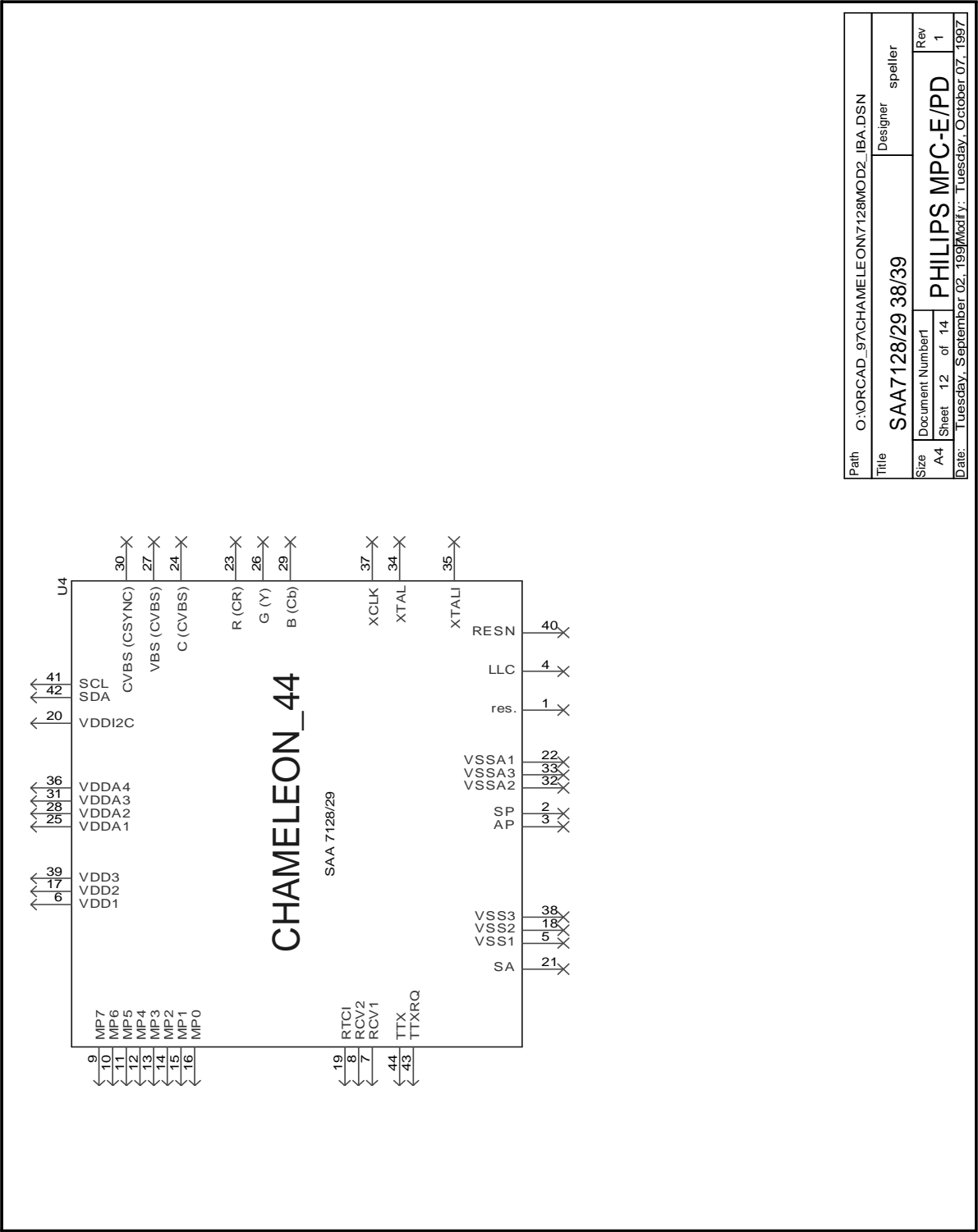
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Size	Document Number	Designer	spell
A4	Sheet 9 of 14		
Date	Tuesday, April 02, 1996	Modify: Thursday, October 09, 1997	

Rev	1
PHILIPS MPC-E	

6.1.4 SAA7138/39

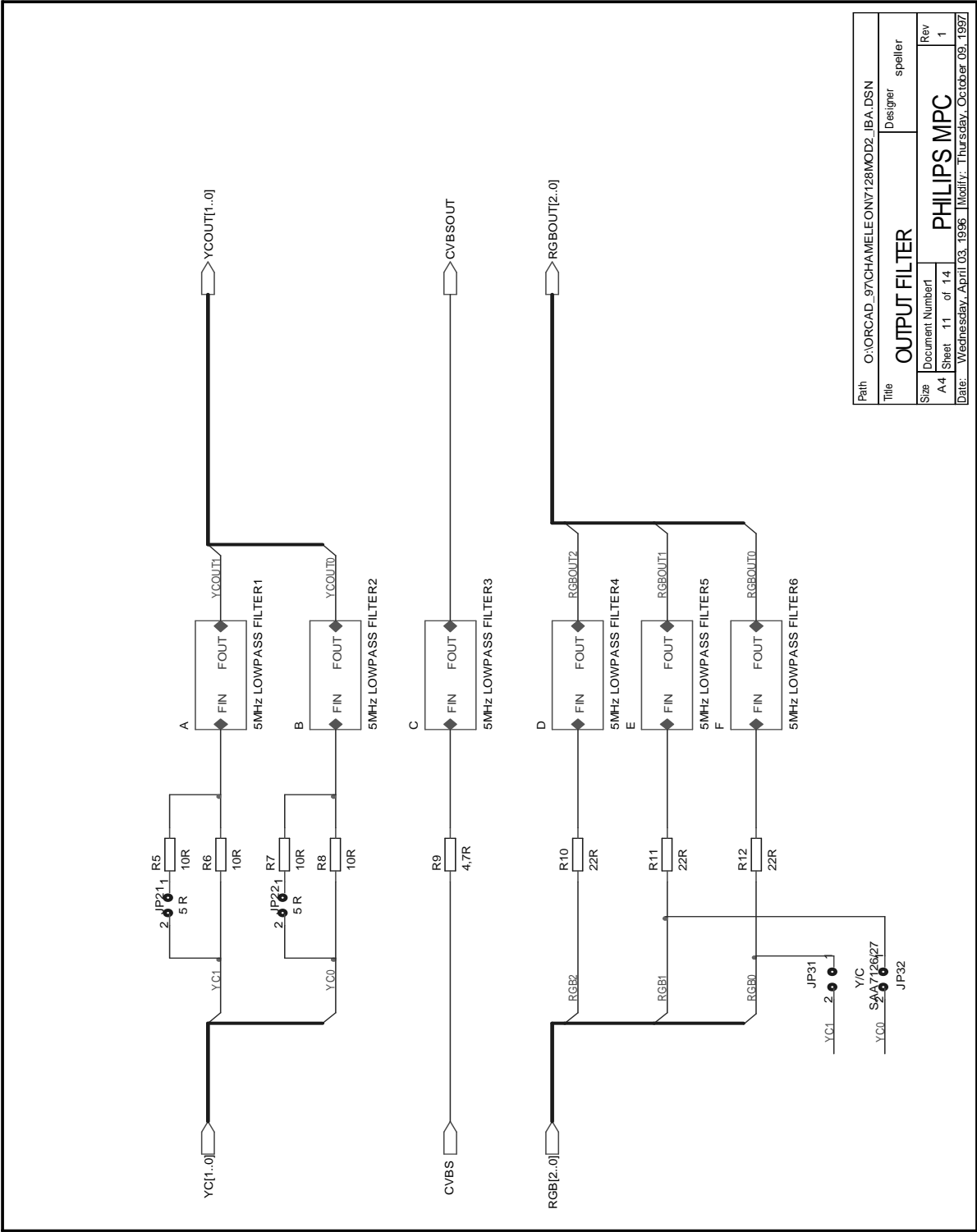


6.1.5 SAA7128/29



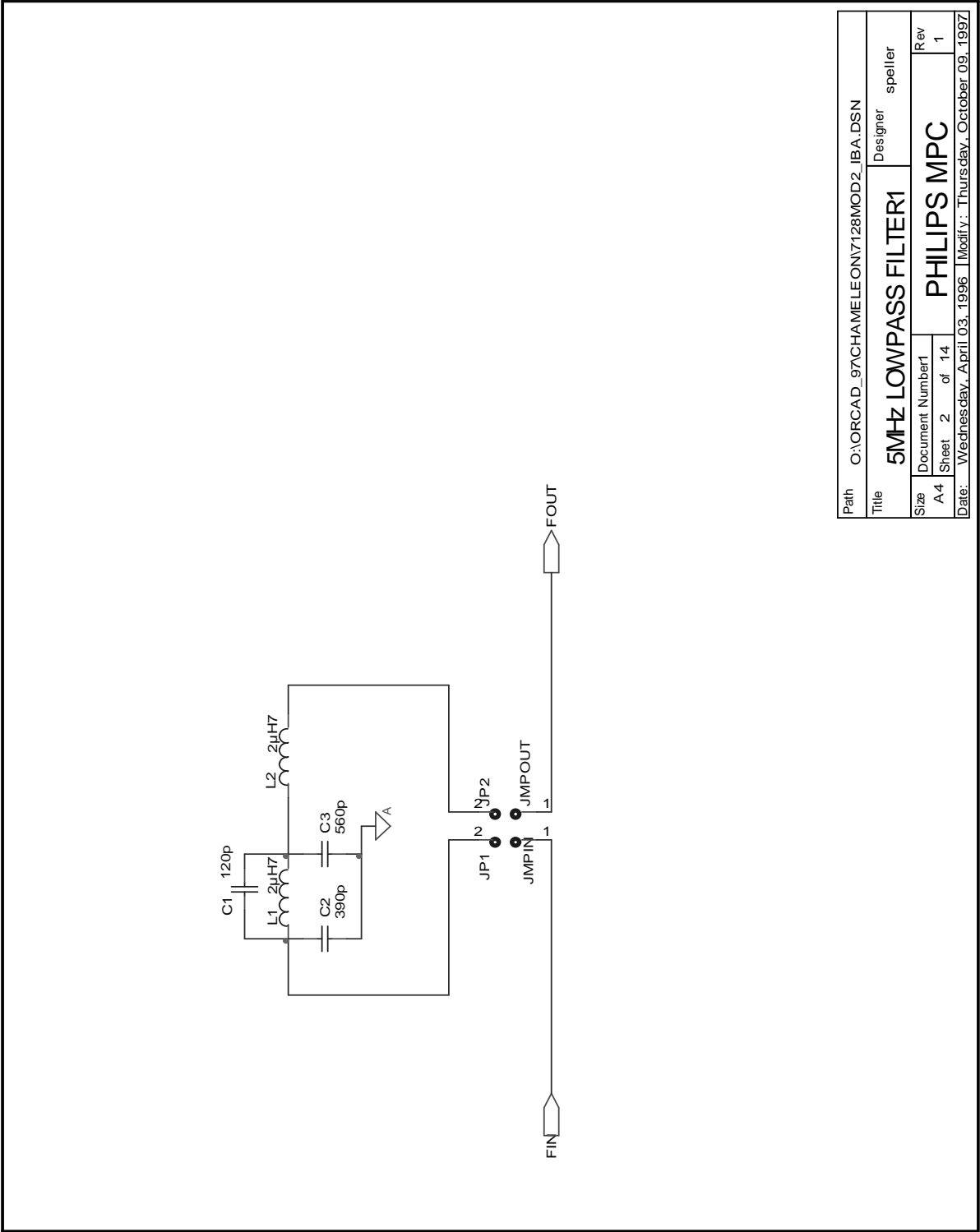
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Modify: Tuesday, October 07, 1997	

6.1.6 Output Filter 1..6

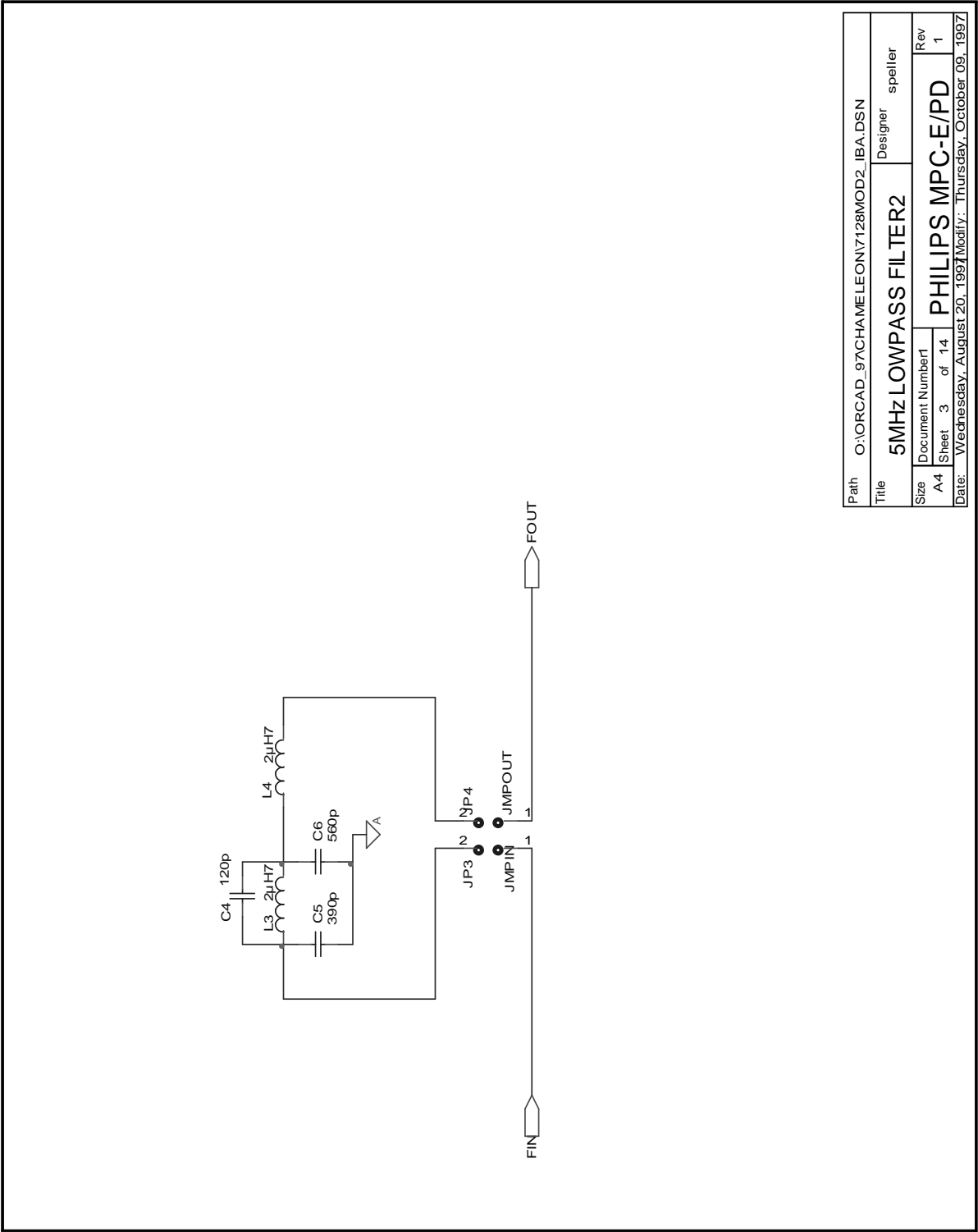


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Rev		1	
Rev		1	
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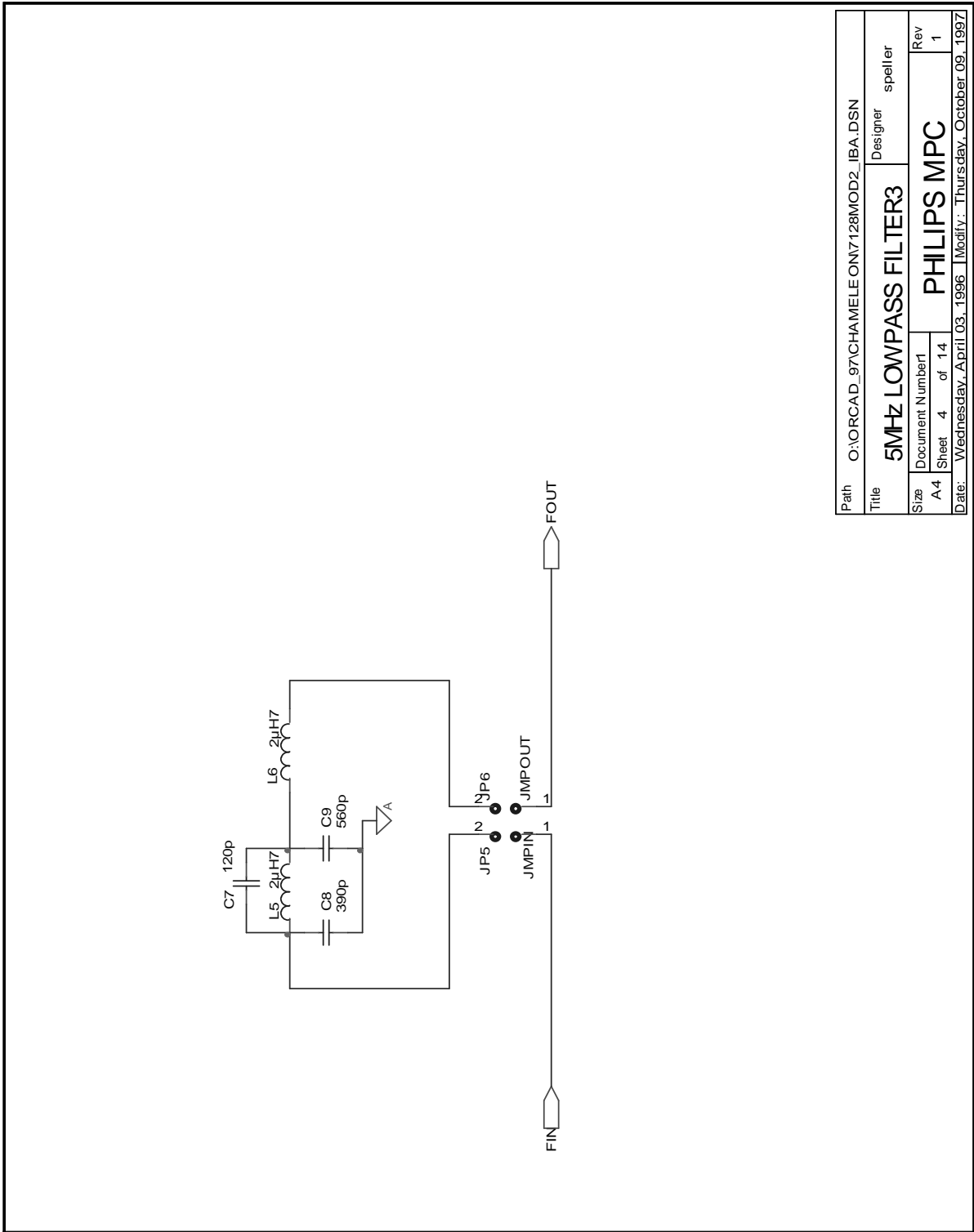
6.1.7 5MHz Lowpass Filter1



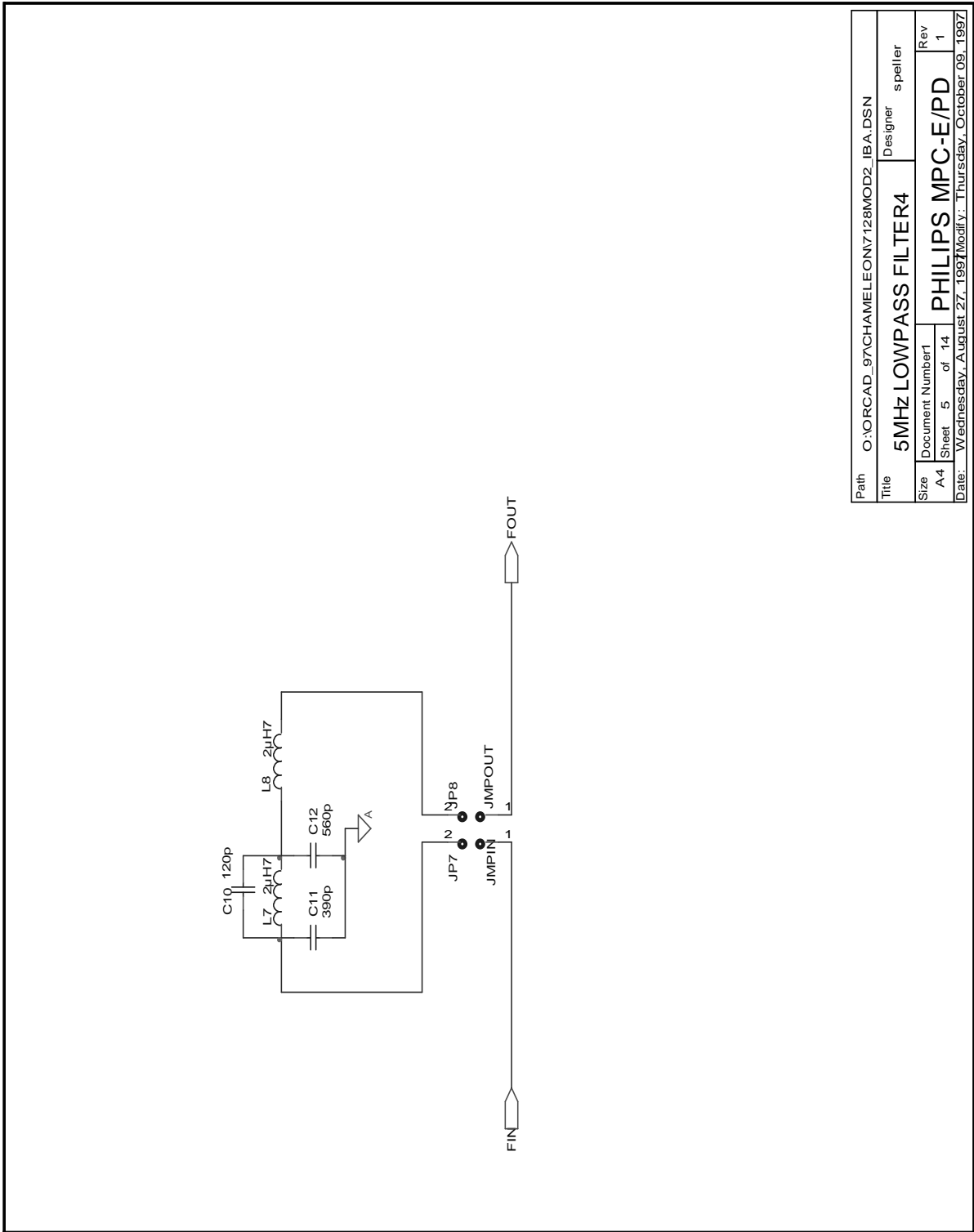
6.1.8 5MHz Lowpass Filter2



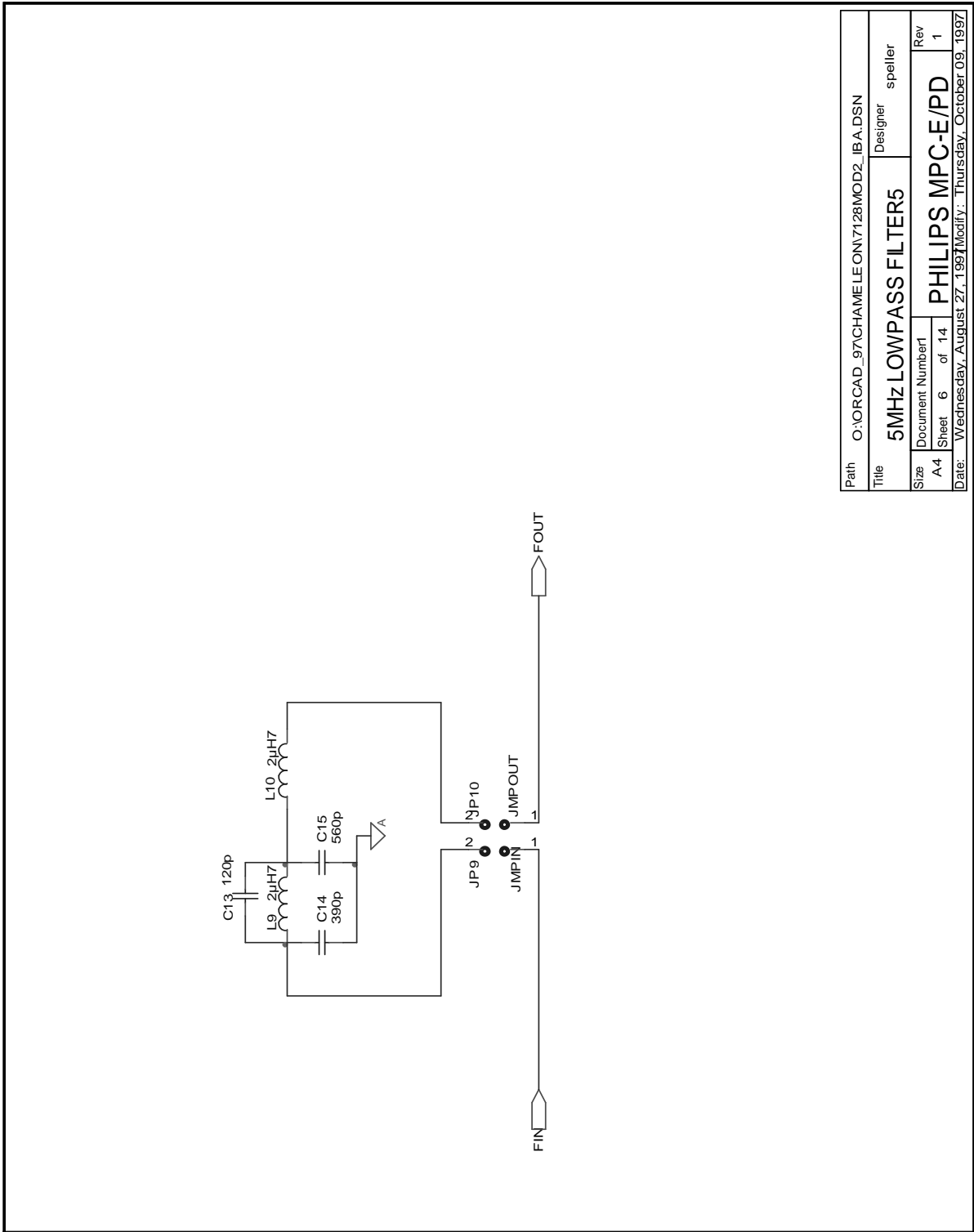
6.1.9 5MHz Lowpass Filter3



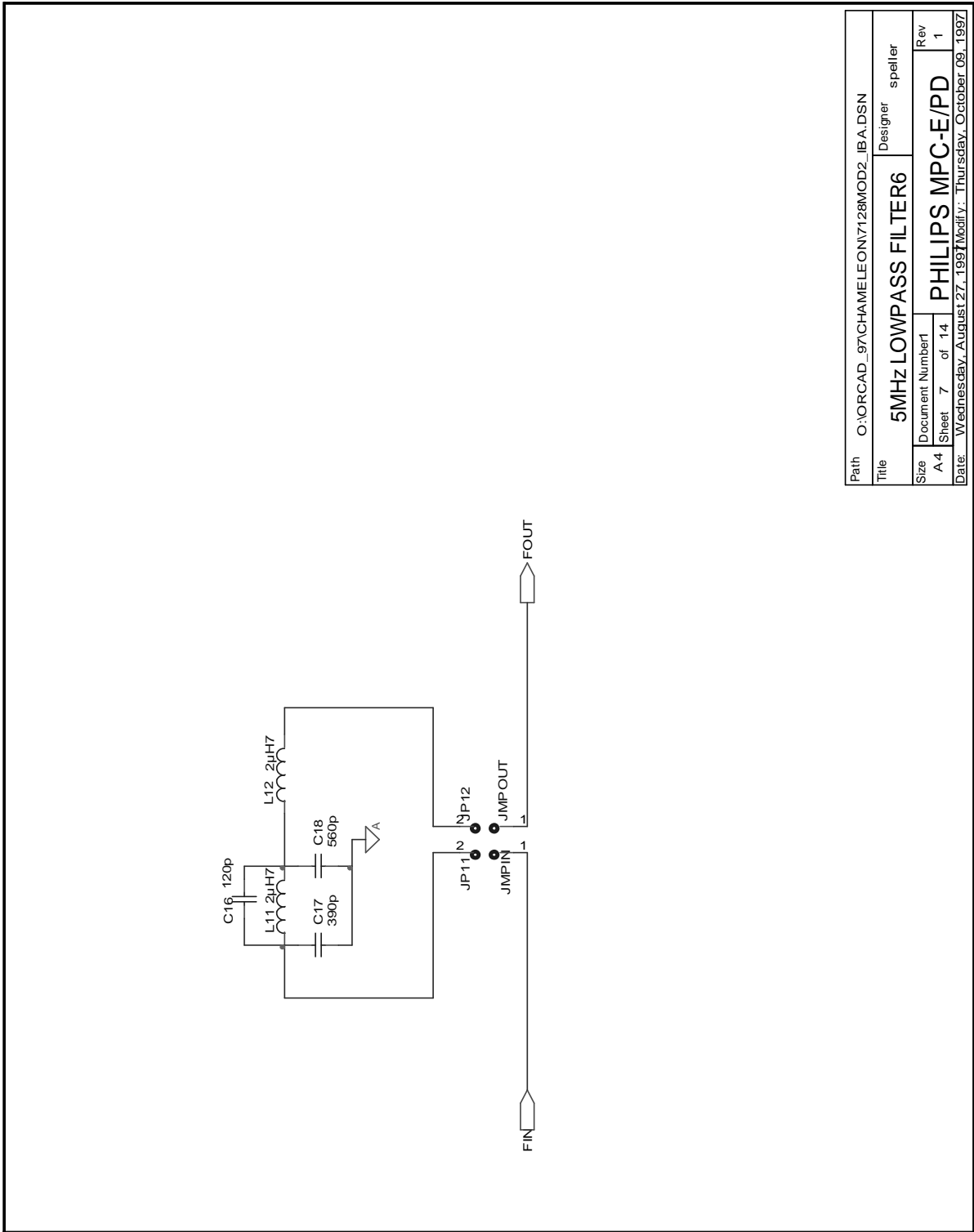
6.1.10 5MHz Lowpass Filter4



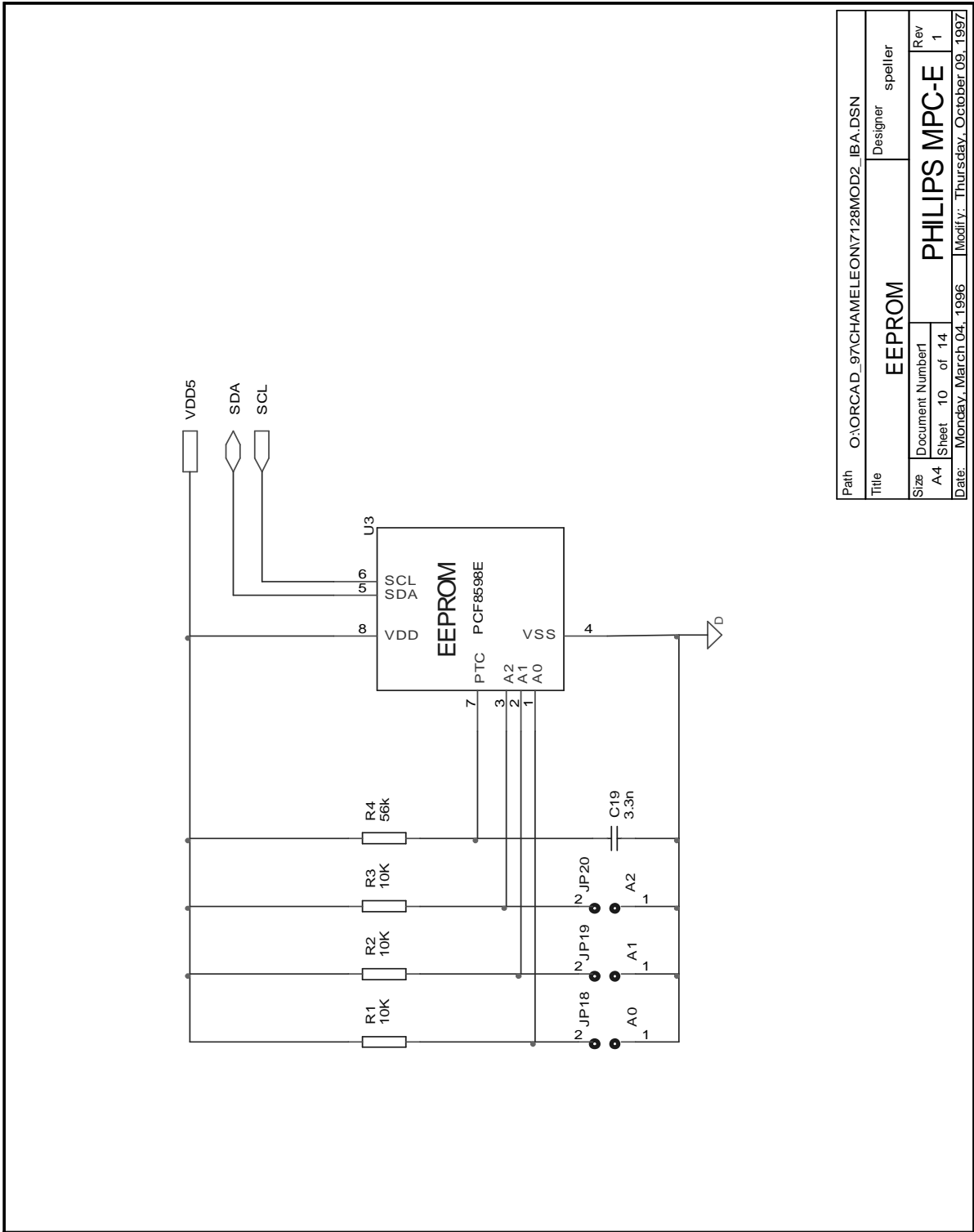
6.1.11 5MHz Lowpass Filter5



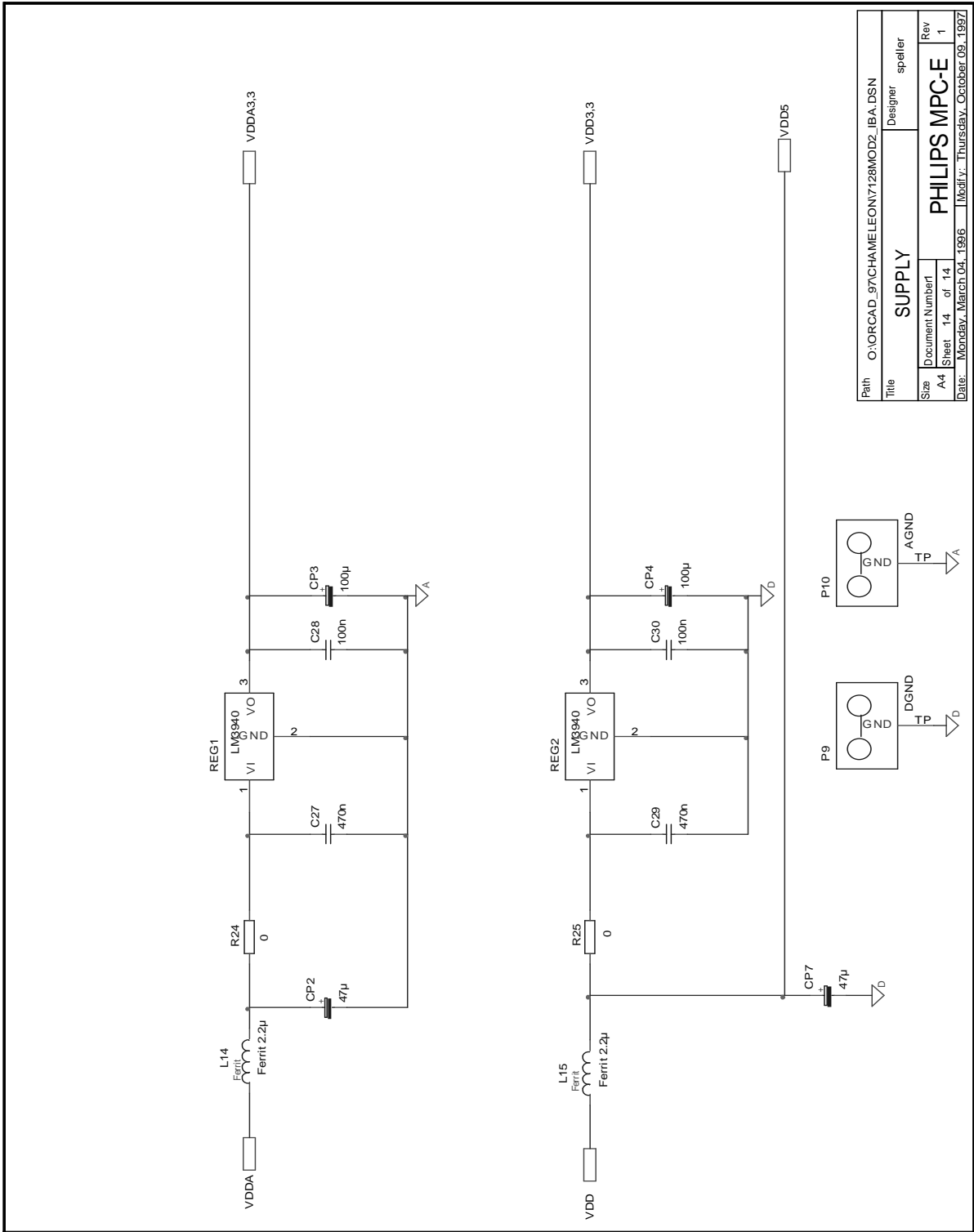
6.1.12 5MHz Lowpass Filter6



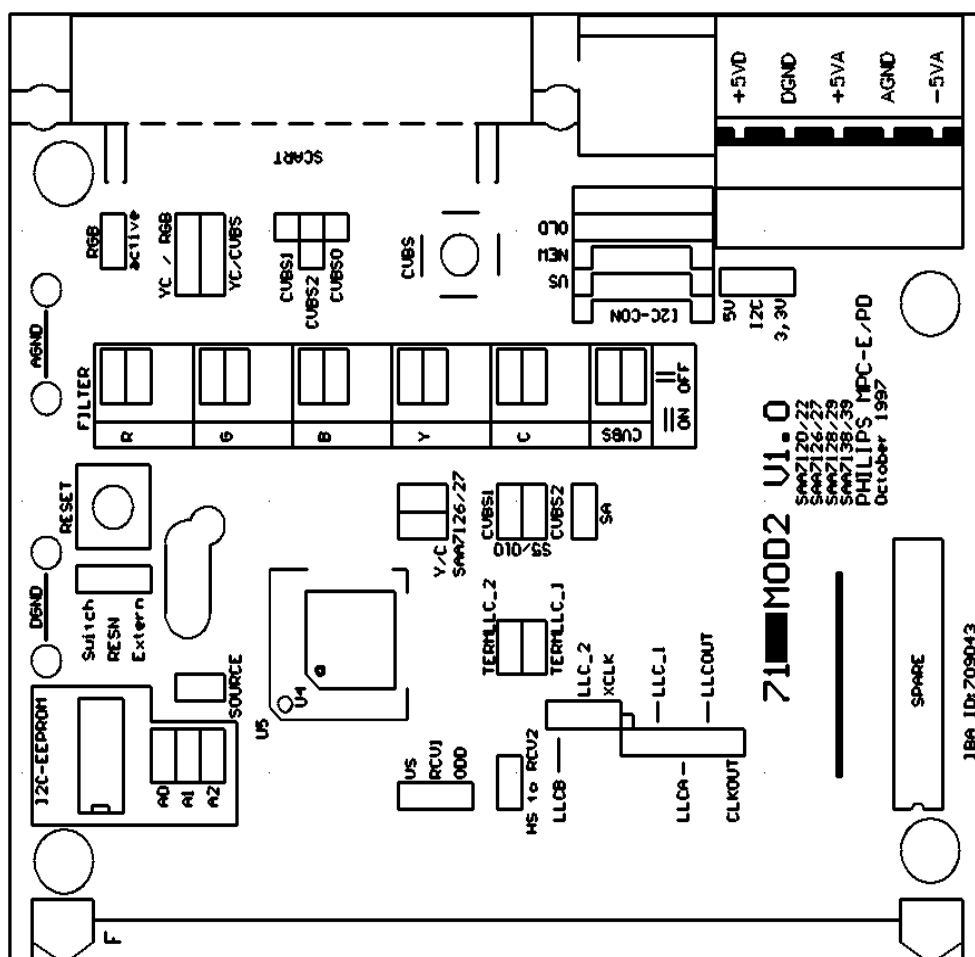
6.1.13 I²C - EEPROM



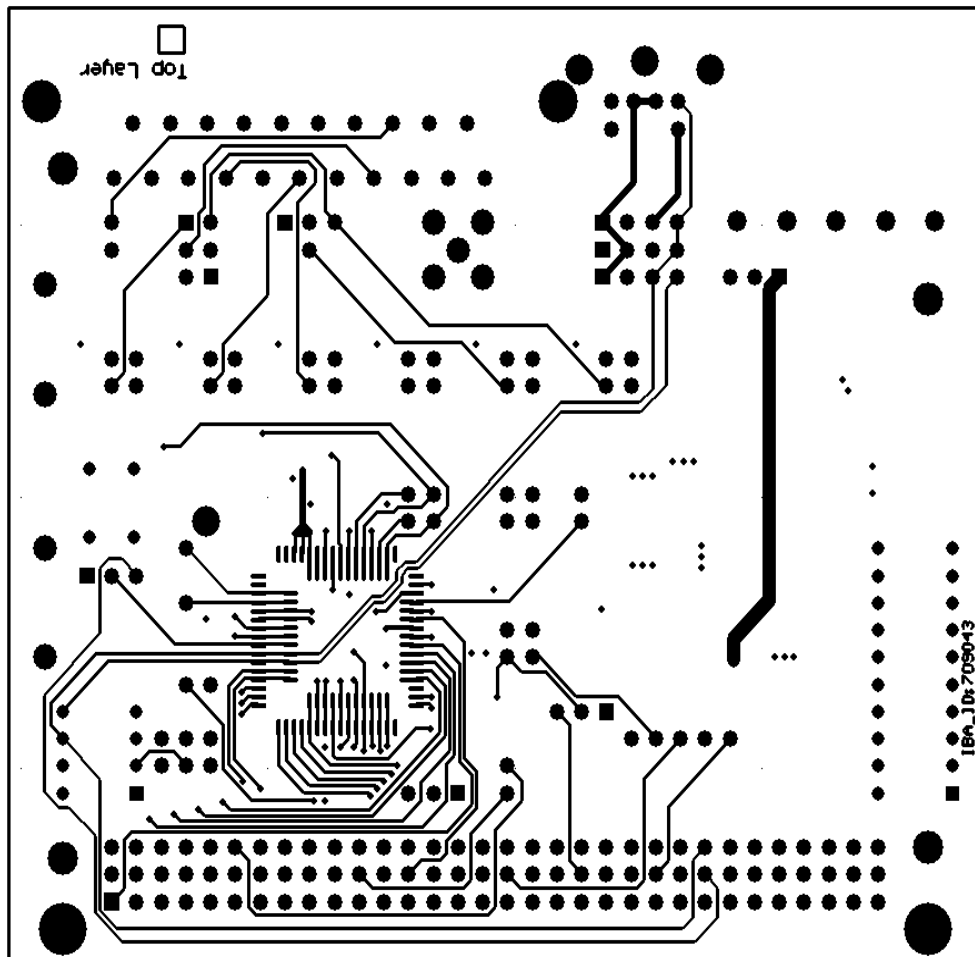
6.1.14 Supply



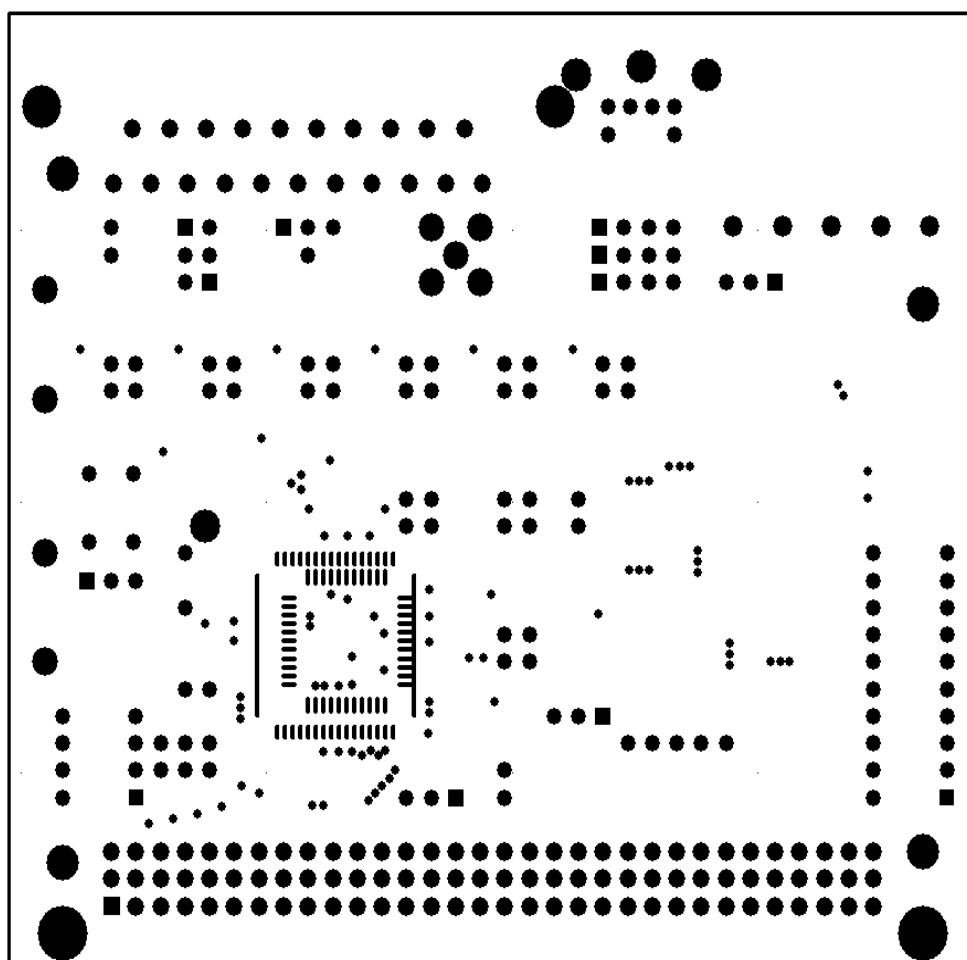
6.2.1 Top Placement of 7128MOD2



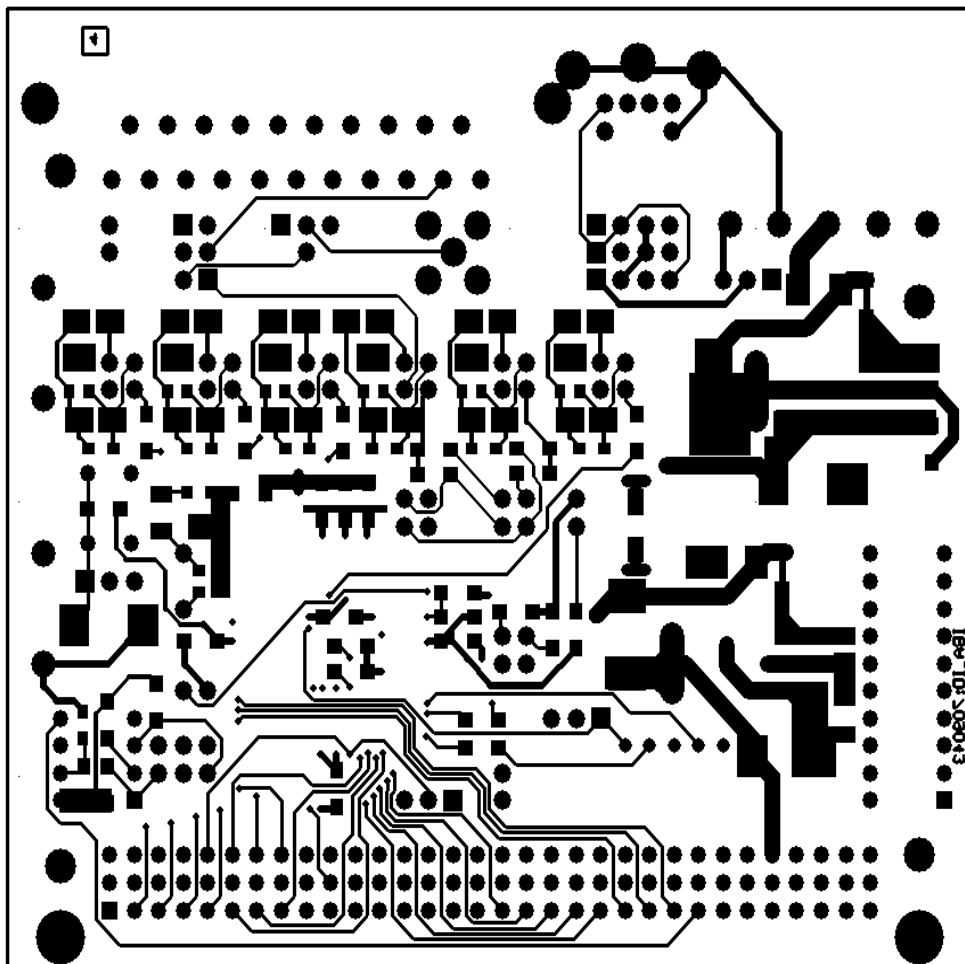
6.2.2 Routing of Top Layer of 7128MOD2



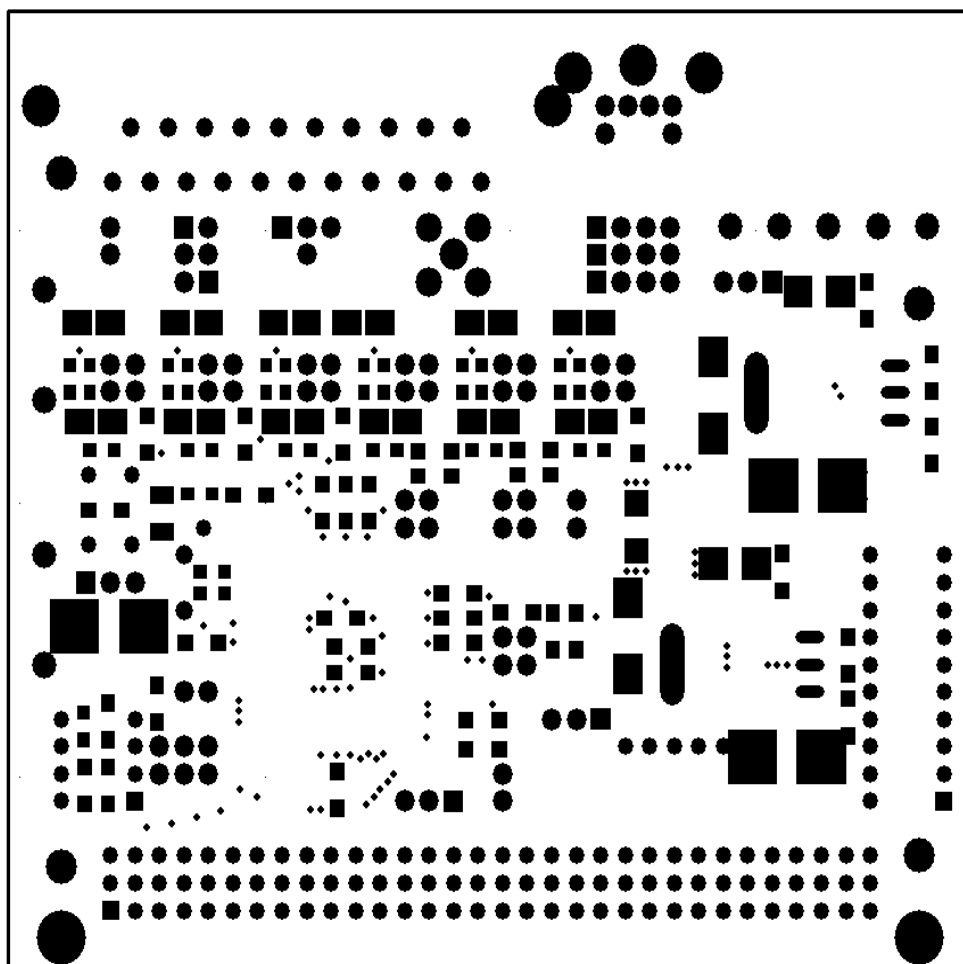
6.2.3 Top Solder Mask of 7128MOD2



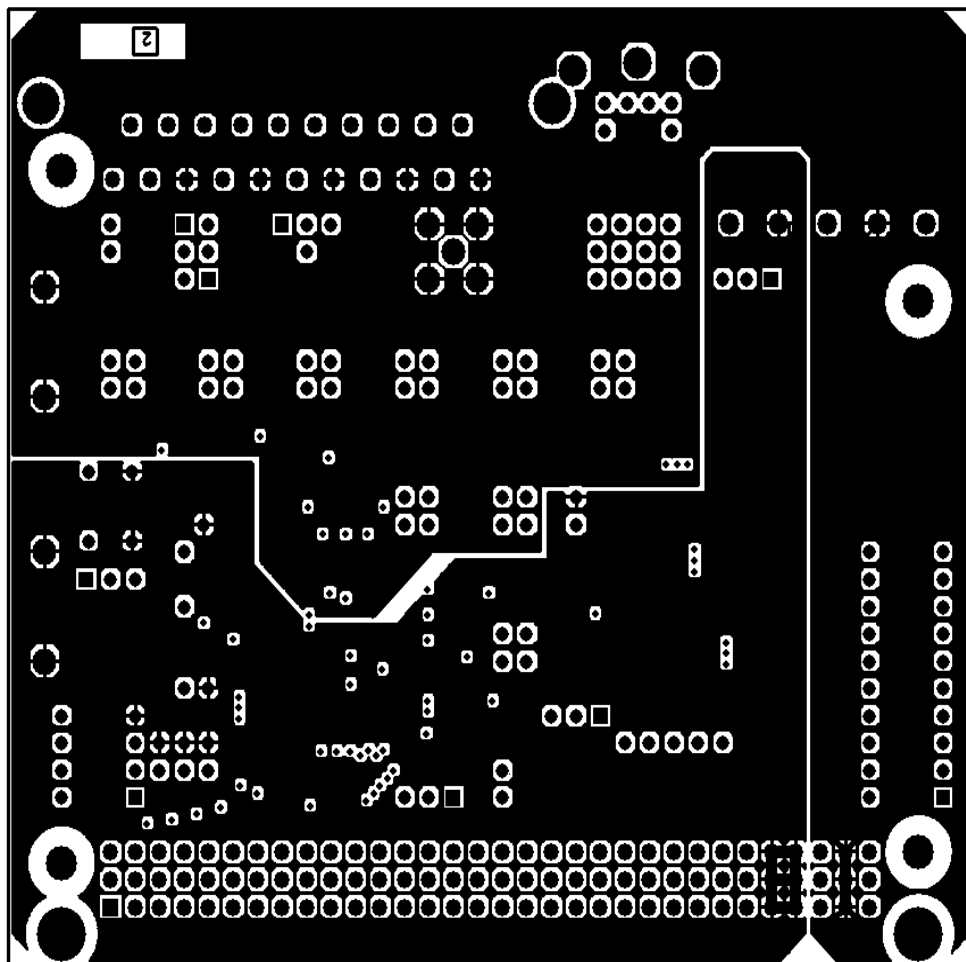
6.2.5 Bottom Layer of 7128MOD2



6.2.6 Bottom Solder Mask of 7128MOD2



6.2.7 Ground plane layer of 7128MOD2 (Mid Layer1)



6.2.8 Routing of Power Supply Layer of 7128MOD2 (Mid Layer2)

