APPLICATION NOTE

Application of the UBA1710M modulator for GaAs power amplifiers

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Abstract

The UBA1710M is a monolithic silicon modulator for transmission GSM/DCS/PCS applications.
This report contains a description of the device and the mode of operation in association with a GaAs power amplifier .

APPLICATION NOTE

APPLICATION OF THE UBA1710M MODULATOR

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Summary

This report is intended to provide support for designing the power control in use for GSM/DCS/PCS applications with GaAs power amplifier.

It contains a general description of the circuit as well as a more in-depth analyse of the different blocks implemented in the controller .

An application example of the UBA1710M is given by means of the board description for testing the performances.

Some additional informations concerning the optimisation of the modulator when this one is used under GSM/DCS/PCS standards are also available in this document .

CONTENTS

LIST OF FIGURES

1. INTRODUCTION

This note describes the application of monolithic silicon devices in plastic SMD packages for DCS/PCS power control of GaAs amplifiers.

Their main features are:

-low cost

-100% SMD

-high performance

-low Rdson for the MOS switches

-Negative voltage on board

-Power management and idle mode

-Wide bandwidth for the feedback loop amplifier

-4.8 V operation

2. PINNING

The pinning is shown in Fig.1.

SYMBOL	PIN	DESCRIPTION
NC3P	1	charge pump tank capacitor
NC3N	2	charge pump tank capacitor
VN	3	negative bias voltage
Vcc	4	analog. supply voltage
GND	5	ground
TC1N	6	charge pump tank capacitor
Vdd	7	digital supply voltage
TC1P	8	charge pump tank capacitor
TC2N	9	charge pump tank capacitor
TC2P	10	charge pump tank capacitor
Vp	11	positive tripler voltage
BUFI	12	buffer input
S1A	13	power MOS 1 source A
S1B	14	power MOS 1 source B
D1A	15	power MOS 1 drain A
D1B	16	power MOS 1 drain B
S2	17	power MOS 2 source
D2	18	power MOS 2 drain
Rext	19	external resistor for VN
STB	20	stand by input (active high)

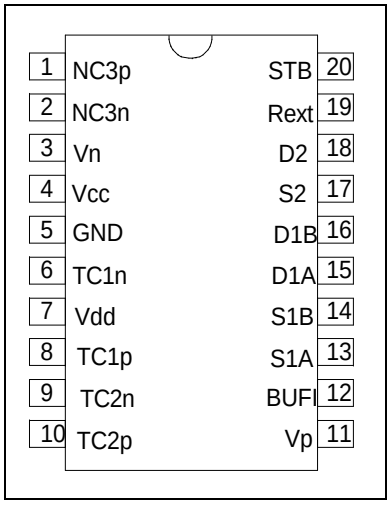

Fig. 1 Pin configuration

3. CIRCUIT DESCRIPTION

3.1 General block diagram

As described in fig.2. the controller has a built in double power MOS to switch on and off the drain voltages applied to the power amplifier in order to control the power level of the transmit path .

These MOS power devices can be connected in parallel or separately to the power amplifier output and driver stages drain circuits .

As we use N MOS transistors for switching , a buffer is used to drive these ones . The buffer output voltage capability is much higher than the battery voltage in order to saturate and turn on the power MOS at the rated maximum output power level with minimum insertion losses .

A voltage tripler is used to supply the buffer . This voltage converter is necessary to allow high positive voltage swing at the buffer output to drive the power MOS devices .

A negative voltage is also built in to bias the gates of the GaAs power amplifier . This negative voltage can be adjust externally with a resistor . As the tripler voltage and the negative bias use charge pump circuits , an internal clock/oscillator drives simultaneously these two blocks .

The power management block disables the input control ramp applied to the buffer as long as the negative bias is not available .

Finally a stand by circuit can set the circuit in an idle mode when activated .

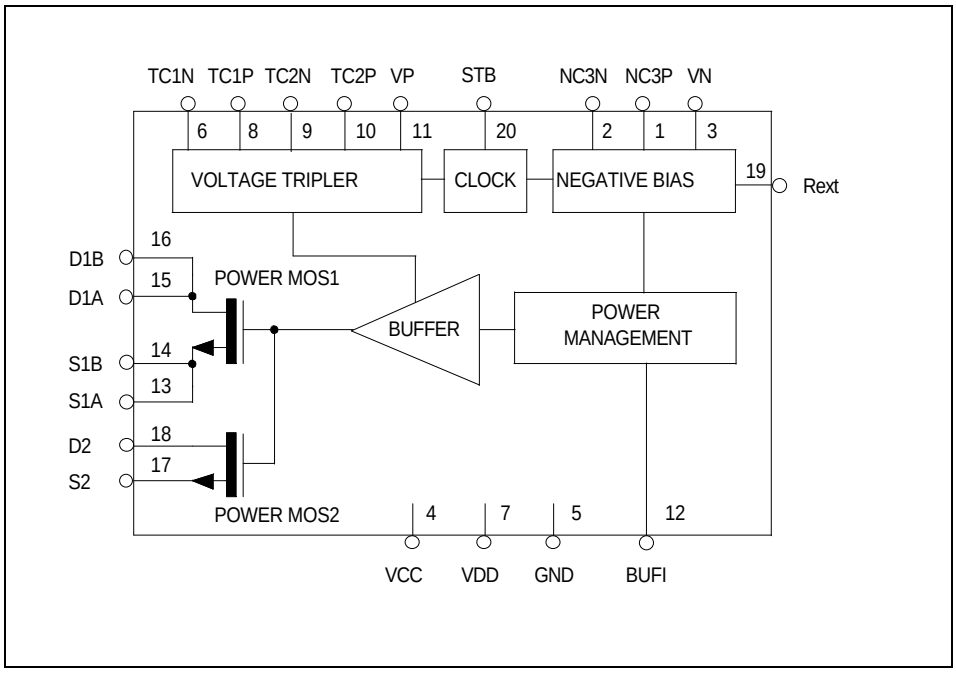

Fig. 2 General block diagram

3.2 Voltage tripler circuit

The voltage tripler is described in fig.3.

The circuit works on the basis of charge pump circuits with transferred charges from a capacitor to an other one .

In a first step , the switches S1 to S4 are closed (while S5 to S7 are opened) ,C1 is charged to Vbat .Then switches S5 to S7 are closed (S1 to S4 opened) and C1 is discharged in C2 with an additional voltage Vbat applied .The peak voltage across this capacitor is then 2*Vbat .

In a third step ,S1 to S4 are closed once more (with S5 to S7 opened) and now C2 discharges in C3 with an additional V bat applied to the previous peak voltage present across C2 (2*Vbat). This new voltage appearing across C3 is now 3*Vbat .

The group of switches are operated alternately through a switches control block as long as the Vtriple has not reached the value given by the ratio : [(R1+R2)/R2]*Vbg .

Vbg is the band gap voltage applied to the non inverting port of the comparator .

When this voltage value is reached the output level of the comparator goes to zero ,disabling the switches control and in turn stopping the capacitors charging/discharging process .

Theorically Vtriple is 3*Vbat , but practically the voltage is regulated at a constant level of 11.8V .

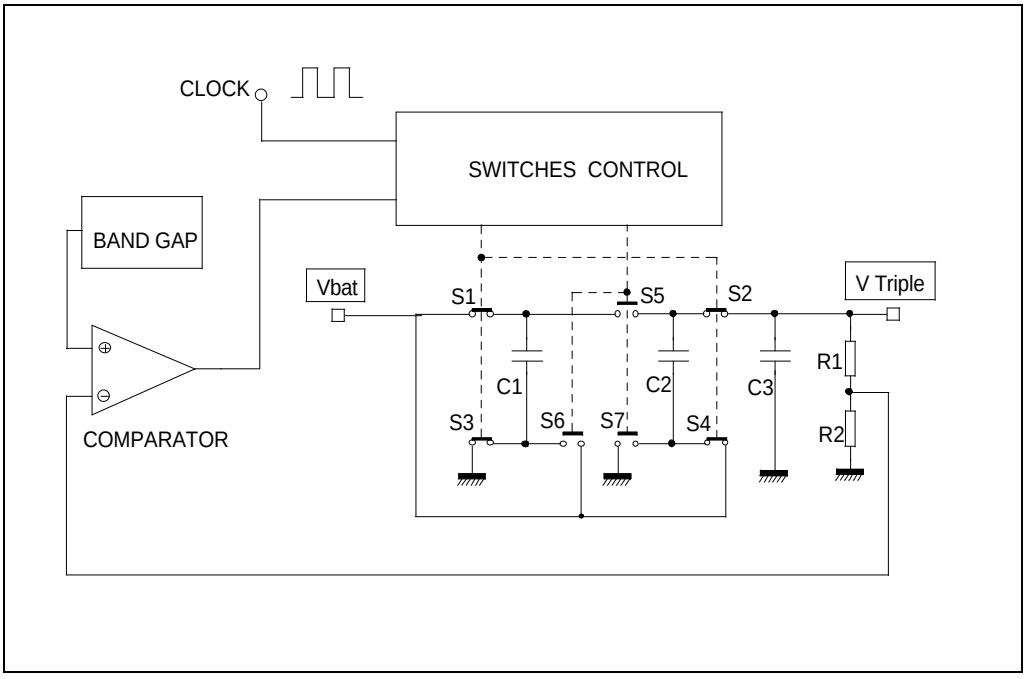

Fig. 3 Voltage tripler

3.3 Negative voltage

The negative voltage block diagram is given in fig.4.

As for the voltage tripler , the process in use is a charge pump circuit using diodes as switches .

At the starting point the negative voltage is zero and the voltage output level of the comparator is high ,

enabling the clock pulses to charge the capacitors C1 and C2 .

The voltage at the inverting port of the comparator is gradually pulled down as Vneg is decreasing toward negative values .When the voltage become zero ,the output of the comparator goes to zero , and in turn the pulses from the clock no longer charge the capacitors of the charge pump circuit and Vneg stabilises to a value determined by the band gap voltage and the resistors bridge .

The value of Vneg is given by the formula : Vneg = -[R2*Rext/R1(R2+Rext)]Vbg with R2 = 60kΩ ,R1 = 38.4kΩ and Vbg = 1.28 V .

As we can see the negative voltage can be adjust by mean of the external resistor Rext , and the range lies between -2 V for Rext = ∞ and 0 V for Rext = 0Ω .

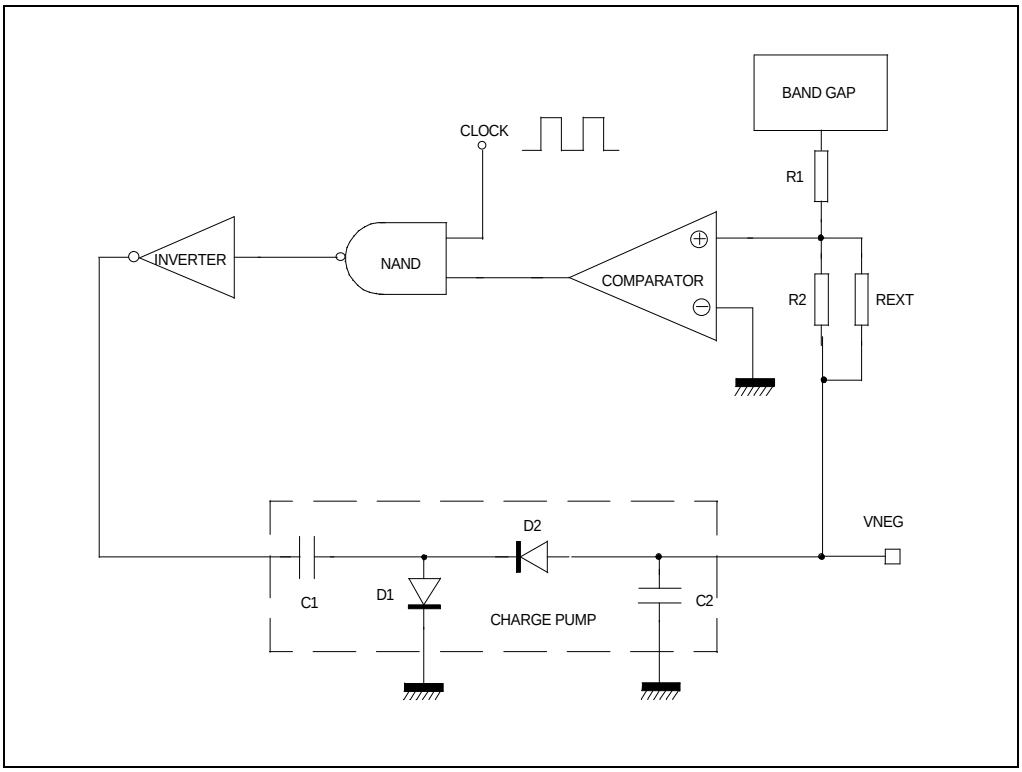

Fig. 4 Negative voltage circuit

3.4 Power management

The schematic of the power management circuit is given in fig.5.

The aim of this circuit is to prevent any signal from being applied to the buffer as long as the negative voltage is not at least -1 V .

In fact this does not allow any drain voltage to be applied to the power amplifier if the negative voltage is not low enough to prevent this one from excess of drain current .

For this purpose , a comparator in association with two MOS switches is used .

When the UBA1710M is turn on , Vneg is close to zero and a positive voltage is applied to the non inverting port of the comparator .The output voltage level of this one is high and the MOS switches SW1 /SW2 are respectively in off and on states .This situation prevent any control signal to be present at the buffer input .

When Vneg goes negative , the voltage at the comparator is pulled down and when this voltage is zero or less, SW1 /SW2 are on and off ,enabling the control signal to switch on the drain voltage .

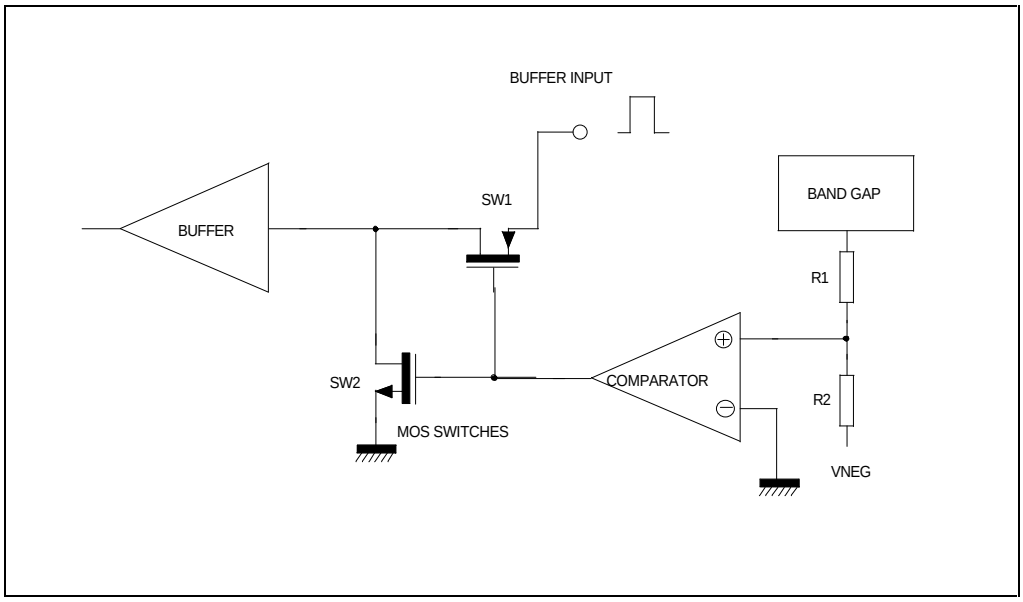

Fig. 5 Power management

3.5 Shut down circuit

When the UBA1710M modulator is not operating (within the bursts for example), and to avoid any unnecessary consumption ,the circuit can be set in an idle mode .

The circuit described in fig.6 ,comprises a MOS switch inserted between the battery and the rest of the modulator .

When a positive voltage (+Vbat) is applied to the stand by pin ,the modulator is in an idle state while this one is active with zero volt applied .

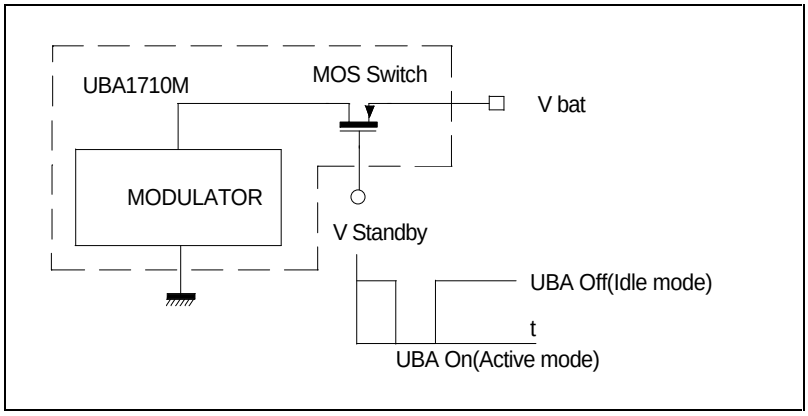

Fig. 6 Shut down circuit

3.6 Power MOS switch and buffer

In order to improve the bandwidth and the dynamic range of the association power MOS and buffer , a negative feedback is introduced by means of two resistors .The block diagram is given in fig.7.

The feedback ratio ,equal to R2/(R1+R2) is sufficient to insure a 2 MHz bandwidth minimum with an input signal ranging from 1.2 to 3.4 V .These values are important if the modulator has to be used in a control loop .

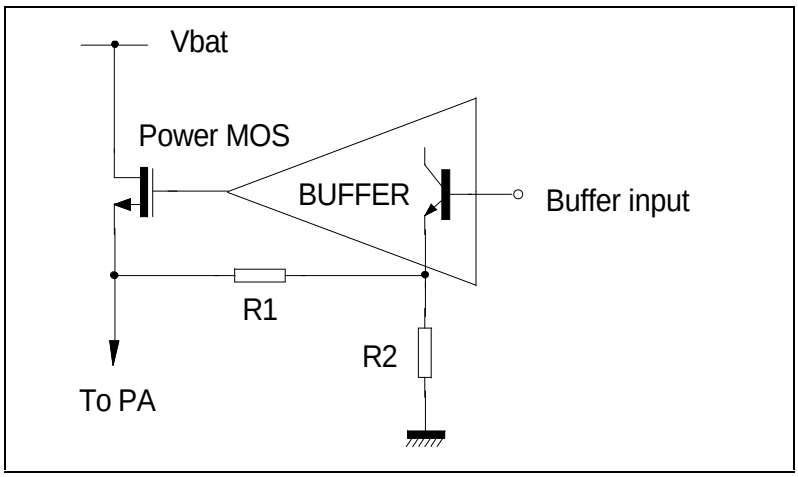

Fig. 7 Power switch and buffer

3.7 Oscillator

The oscillator (clock) in use in the UBA1710M is a source coupled CMOS multivibrator. The schematic is given in fig.8.

The oscillation frequency is 600 kHz and this one is given by the formula : F=I/(4*C*Vc) ,where I is the current source value ,C the coupling capacitor value and Vc is the voltage across the capacitor .

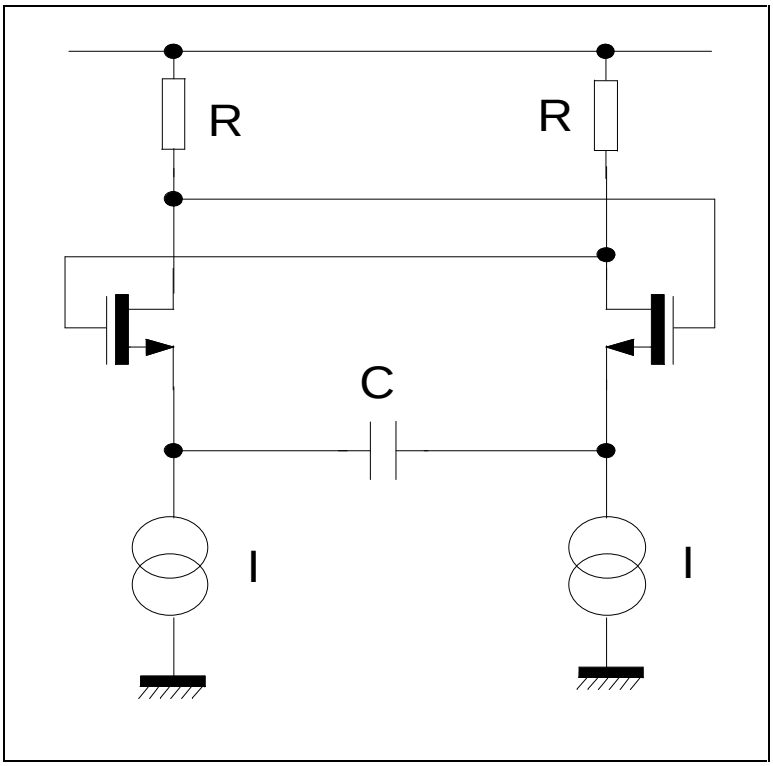

Fig. 8 Oscillator

4. MODE OF OPERATION

The device must be operated under pulse conditions with a power MOS driving current capability not exceeding 2.5 A peak (MOS1 and MOS2 connected in parallel) with a maximum duty cycle of 10% and a pulse width of 1 mS .

5. GENERAL CHARACTERISTICS

VDD=4.8V;Tamb=25°C; unless otherwise specified .

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
Supplies						
Icc=Idd	peak supply current	power-up mode; PA on	-	12	-	mA
		power-down mode; PA off	-	5	-	mA
Istb	standby current	standby mode	-	0.1	1	µA
Power MOS1						
Rdson1	on resistance	Ids=1.3A	-	0.18	-	Ω
Power MOS2						
Rdson2	on resistance	Ids=0.4A	-	0.5	-	Ω
Clock circuit						
fclk	clock frequency		-	600	-	kHz
Voltage tripler						
Vpo	output voltage	with Ipo=2 mA	11.4	11.8	12.3	V
Vr(p-p)	amplitude ripple (peak-to-peak value)	with Ipo=2 mA C1=C2=100 nF; Cp=100 nF	-	20	-	mV
ton	turn-on-time		-	100	-	µS
Negative DC/DC converter						
Vno	output voltage	with Ino=250 µA; Rext=470kΩ	-1.5	-1.8	-2.0	V
Vr(p-p)	amplitude ripple (peak-to-peak value)	with Ino=250 µA, C3=100 nF; Cn=100 nF	-	2	-	mV
ton	turn-on-time		-	280	-	µS
MOS buffer amplifier						
Vil	LOW level input voltage		-	1.2	-	V
Vih	HIGH level input voltage		-	3.4	-	V
tsw	switching time from 0 to 4.5 V		-	1	-	µS

6. CIRCUIT DIAGRAM AND RECOMMENDATIONS FOR USE

6.1 Circuit diagram

With the circuit diagram given in fig.9 , we make use of a GaAs power amplifier for DCS/PCS applications as active device to be controlled by the modulator UBA1710M .

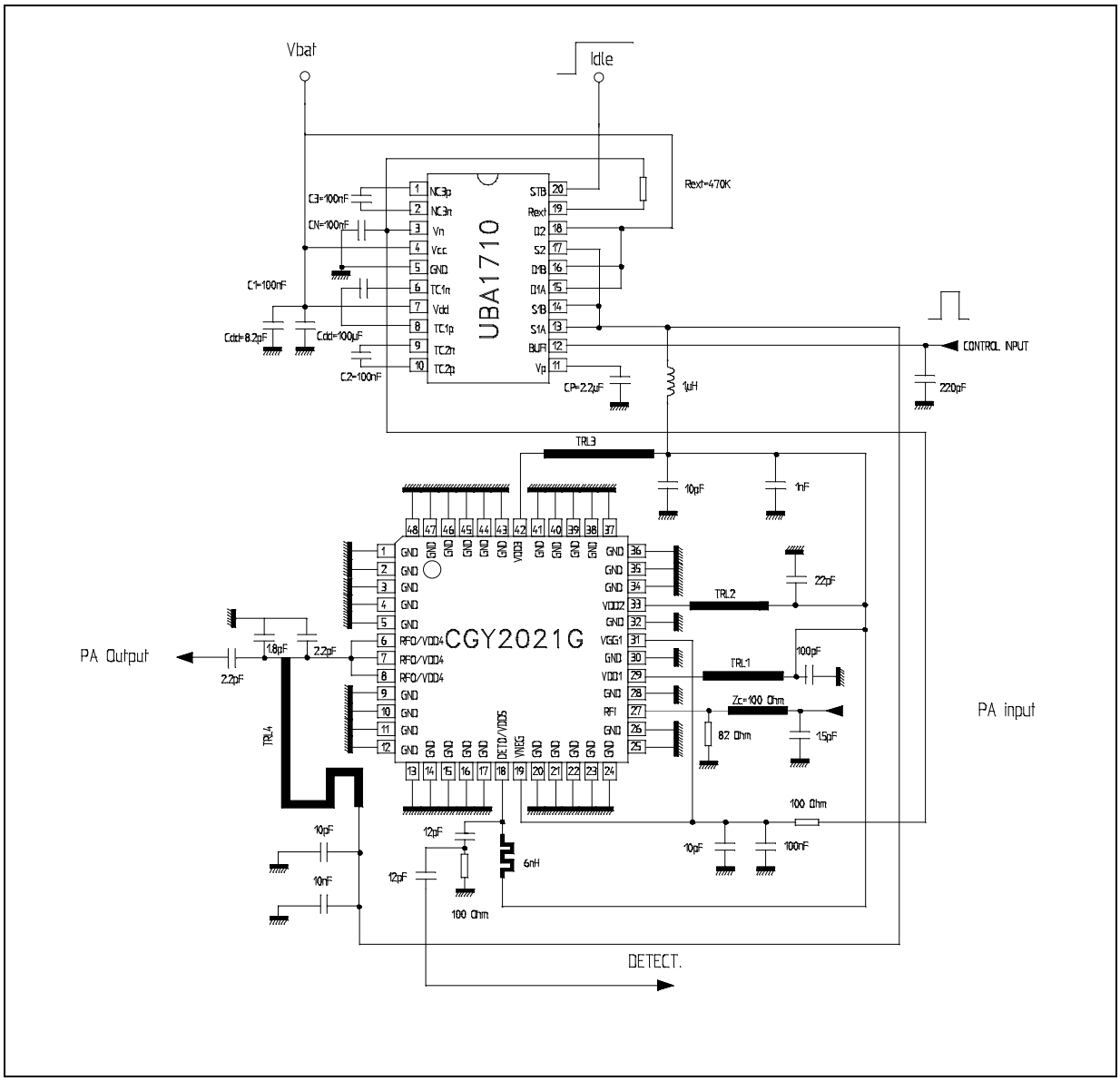

Fig. 9 Circuit diagram

6.2 Recommendations for use

When the modulator is associated with power amplifier for DCS/PCS applications , we know that the standards in use are rather difficult to fulfil ; this is particularly critical for the time and frequency masks .

Some attention must be paid with the decoupling and filtering around the UBA1710M to avoid any unwanted spurious , or noise to be amplified by the transmit path . For that reason , when looking at the circuit diagram in fig.9 ,low and high frequency decouplings are used at Vgs and Vcc (pin 7 and 4) locations as close as possible to the circuit connection . The values of these capacitors are 100 µF and 8.2 pF .

An other important decoupling is the 2.2 µF connected at the terminal pin of the voltage tripler (pin 11) . The third important filtering is the 1 µH inductor inserted between the source pins (pin 17,14,13) and the drains of the power amplifier first three stages .

All other capacitors used around the circuit for the charge pump are 100 nF .

7. PRINTED CIRCUIT BOARD LAYOUT-LIST OF COMPONENTS

7.1 Circuit layout.

The demoboard layout using the layout describes in fig. 7 is not optimised for noise and spurious ,but the aim of it is to demonstrate the dynamic behaviour of the modulator UBA1710M in association with a power amplifier CGY2021G.
The characteristics of the substrate in use for the PCB are as follows:
-substrate type:FR4 double clad
-Relative permetivity:εr=4.7
-Thickness:H=0.8mm
-Size:35x42mm

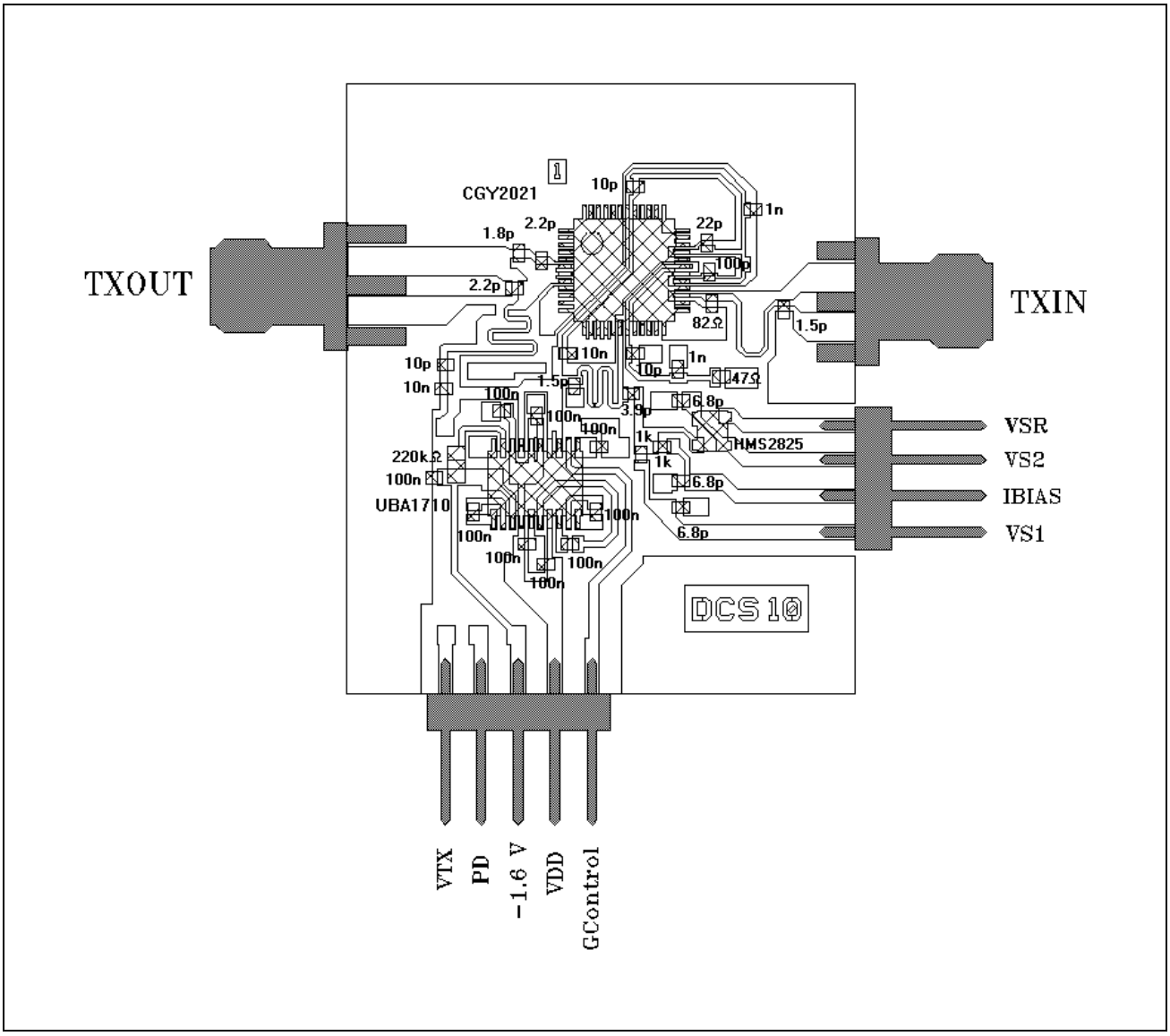

Fig. 10 Circuit layout

7.2 Part list DCS power amplifier with UBA1710

CAPACITORS (Size:0603)	
VALUE	**NUMBER**
1.5 pF	2
1.8pF	1
2.2pF	2
3.9 pF	1
6.8 pF	3
10 pF	3
22 pF	1
100 pF	1
1 nF	2
10 nF	2
100 nF	9

RESISTORS (Size:0603)	
VALUE	**NUMBER**
47 Ω	1
82 Ω	1
1kΩ	2
220kΩ	1

ACTIVE COMPONENTS	
CGY2021G	1
UBA1710M	1
HMS2825	1

8. ELECTRICAL CHARACTERISTICS

8.1 Control curve

The control curve is the one given for the association of a power and the modulator .The output power of the amplifier is plotted versus the control voltage applied to the modulator buffer input (see fig.11).

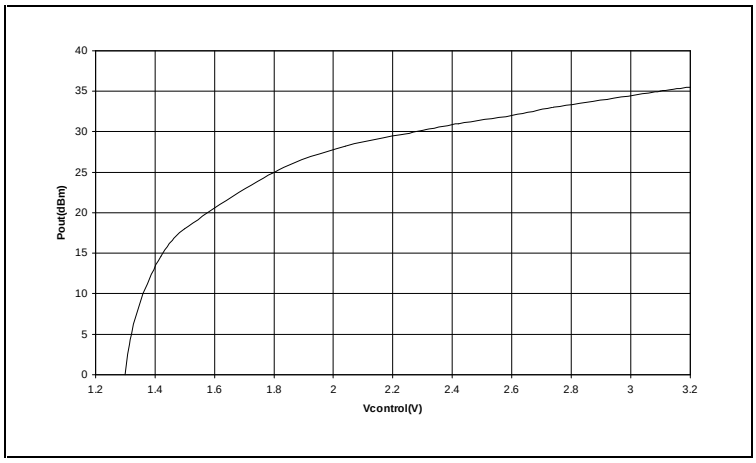

Fig. 11 Control curve

8.2 Turn-on time (tripler and negative voltage)

The turn-on time is the delay that the voltages take to establish to the nominal values when the modulator is switched on .This is an important parameter as the modulator is periodically shut down to the idle mode in order to reduce the overall consumption .These parameters are plotted in fig.12 and fig.13 .

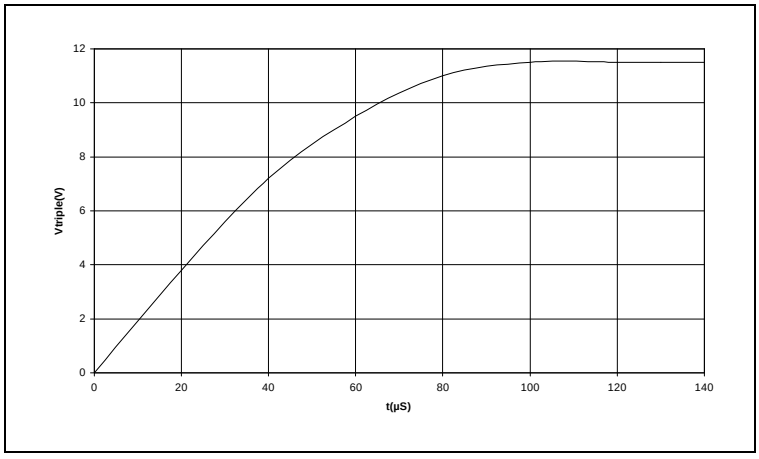

Fig. 12 Tripler turn-on time

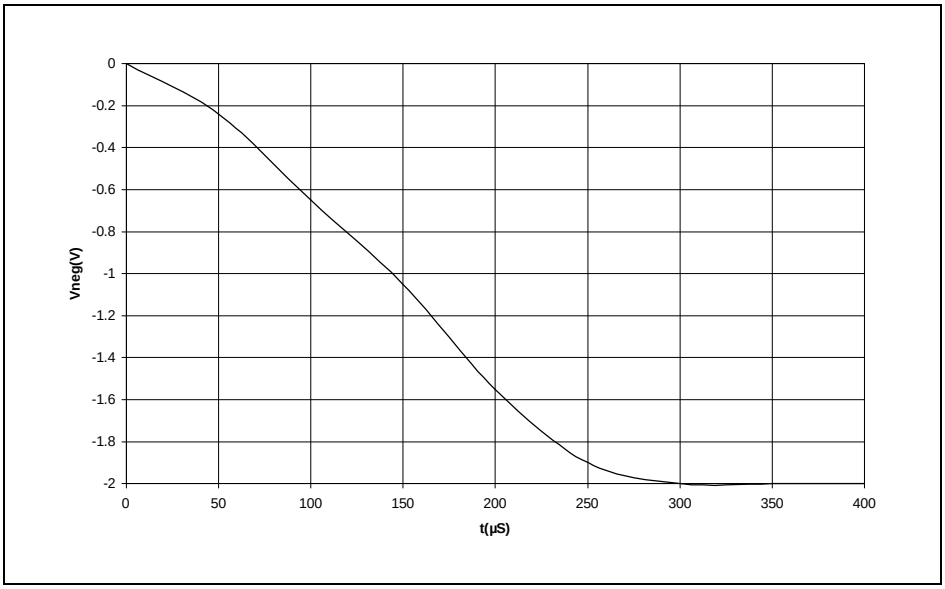

Fig. 13 Negative voltage turn-on time

8.3 Rdson versus Vcc (power MOS switches)

Rdson is also an important parameter as its value will influences the overall efficiency of the association modulator/power amplifier at the rated maximum power output level .

A plot of Rdson versus the voltage applied to the drain is shown in fig.14 and fig.15 for both MOS1 and MOS2 .

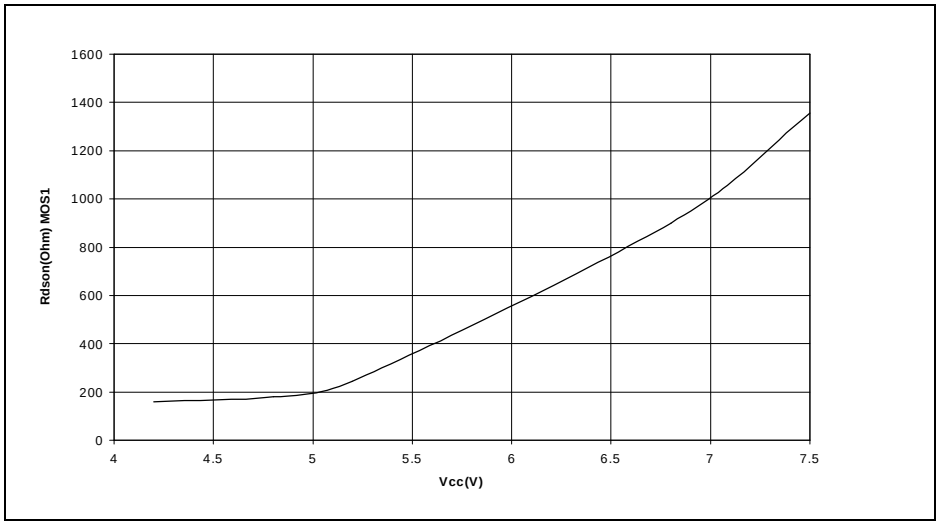

Fig. 14 MOS1 Rdson

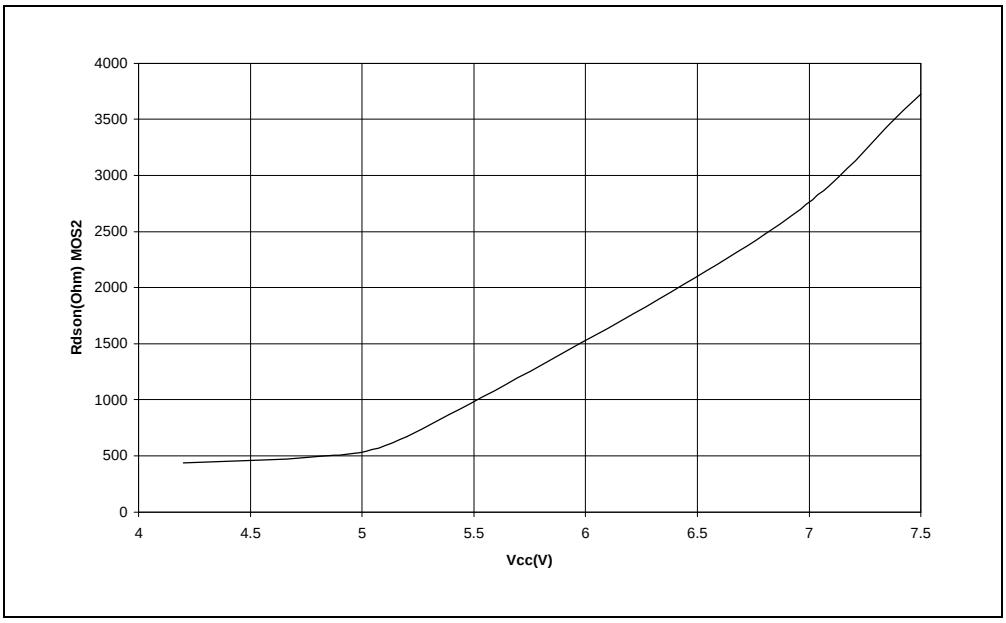

Fig. 15 MOS2 Rdson

8.4 Buffer bandwidth

The buffer bandwidth is measured between the input of the buffer and the sources of the power MOS for a given quiescent control voltage of 2.2 V .The result of this measurement is shown in fig.16 .

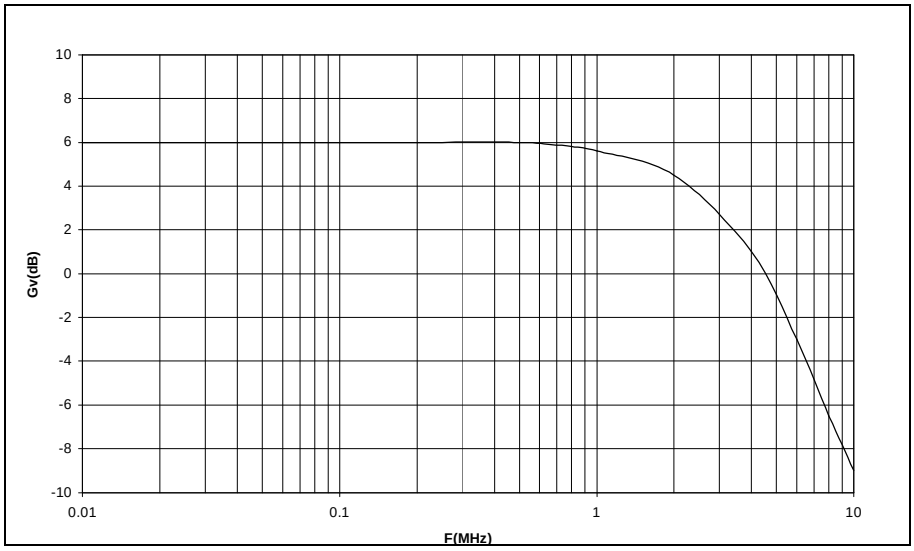

Fig. 16 Buffer bandwidth

8.5 Switching time /settling time

The switching time or settling time is characterised in terms of rise and fall times at the output port of a power amplifier using a UBA1710M as modulator .The rise/fall times are plotted versus the power level at the output of the amplifier (see fig.17) .

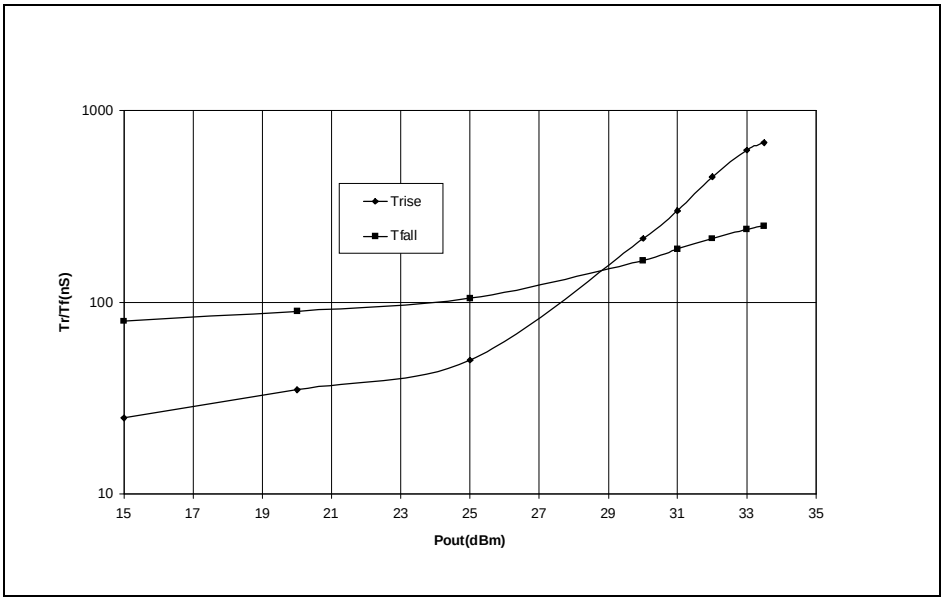

Fig. 17 Switching time/settling time