APPLICATION NOTE

Image Rejecting Front-Ends UAA207X family

AN96106

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Abstract

The UAA2072M, UAA2073M, UAA2073AM, UAA2077AM, UAA2077BM and UAA2077CM are low power integrated front-ends with on-chip image rejection. This further integration level permits to reduce significantly radio designs cost and time.

This report contains background information related to image rejection, a detailed description of the ICs, a worked-out application example and measurement results.

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APPLICATION NOTE

UAA2072M, UAA2073M and UAA2073AM Image Rejecting Front-Ends for GSM applications

UAA2077AM, UAA2077BM and UAA2077CM 2 GHz Image Rejecting Front-Ends

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Summary

This report is intended to provide application support for designing image rejecting front-ends with the UAA2072M, UAA2073M, UAA2073AM, UAA2077AM, UAA2077BM and UAA2077CM integrated circuits from Philips Semiconductors.The first of the line, the UAA2072M, has been developed for GSM applications. The UAA2073M and UAA2073AM are derivatives from the UAA2072M and hence closely related. The UAA2077AM, UAA2077BM and UAA2077CM are based on the same structure but are intended for use in 2 GHz applications. They permit low power applications and eliminate the need for an external bulky ceramic filter required for image rejection.They contain a receiver front-end and a high frequency transmit mixer (not on the UAA2077AM).

Chapter 1 covers complete theoretical background of image rejection. Chapters 2 and 3 contain a general and functional description of these ICs. Chapter 4 gives useful equations, which have been utilized for impedance matching. A worked-out application example, based on the UAA2077BM is given in Chapter 5. The related schematics, layout and assembly drawings can be found in Chapter 7. Matching results, image rejection, IP3 and all relevant RF characteristics of the circuits are included in Chapter 6, to aid in proper circuit design.

Since it was not possible to give, for each topic, the features of the all 6 ICs, it was decided to take into account only one circuit at a time as an example.

CONTENTS

1. BASIC THEORY OF IMAGE REJECTION

In a conventional heterodyne receiver, the incoming signal is amplified with a single stage of tuned RF amplifier and mixed with an adjustable local oscillator (LO) to produce a signal at a fixed intermediate frequency (IF). A selective RF filter is then needed to attenuate all frequencies outside the band of interest.

Let's consider the case of the following reception : the LO frequency is lower than the RF wanted frequency.

A simple application for the 935 to 960 MHz GSM band is shown below. Assuming that the IF frequency is chosen equal to 70 MHz, this leads to the values of 865 to 890 MHz for the LO frequency. The image frequency band, placed at 140 MHz away from the desired band is at 795 to 820 MHz. The signal at LO-IF frequency, presented at the RF input has to be rejected while the signal at LO+IF must go through the reception chain. On the same way, the lower side band can be also rejected.

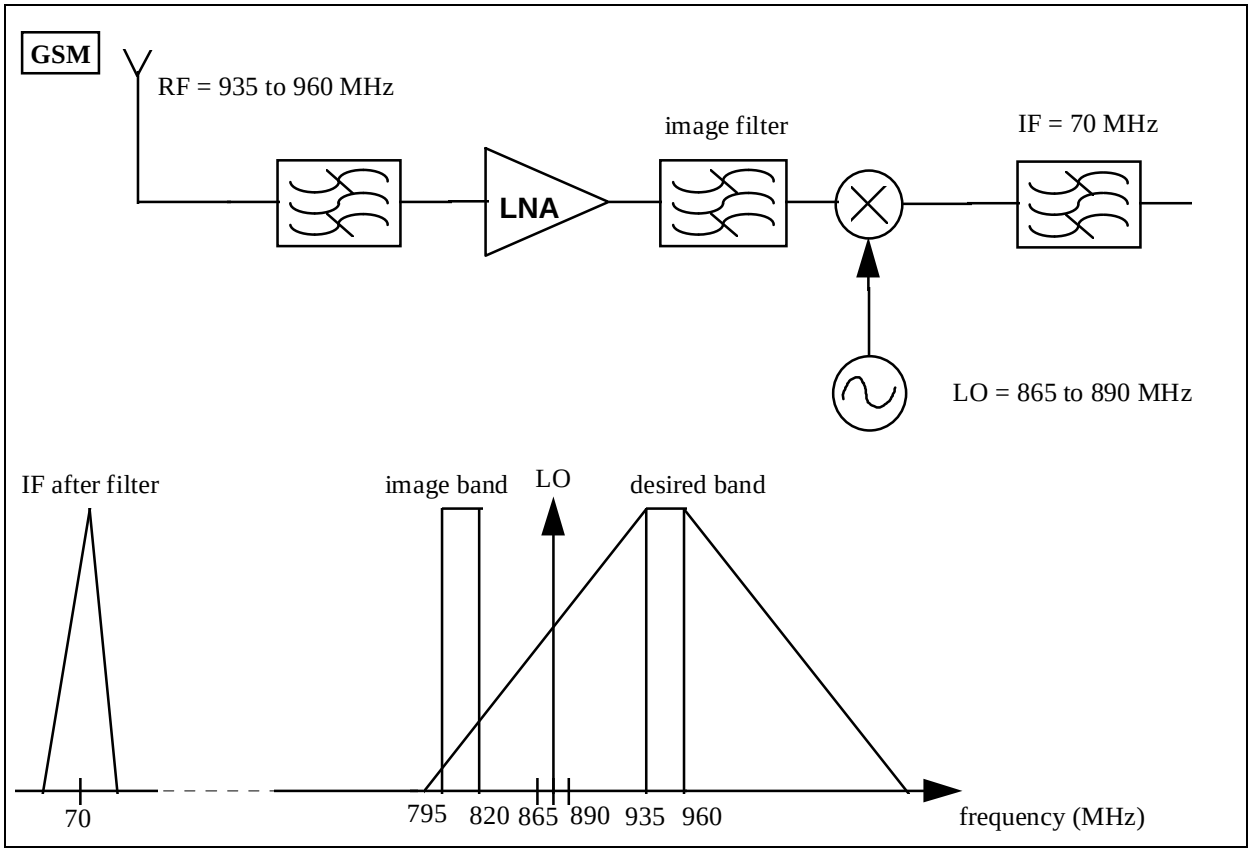


Fig. 1 Heterodyne radio receiver and frequency plan

Another way to suppress response at the image frequency is to use an image reject mixer. The basic principle is to use phase cancellation instead of frequency selective attenuation. The basic circuit consists of a pair of mixers, driven from a quadrature LO source, a 90° phase shifter and a power combiner, as shown below :

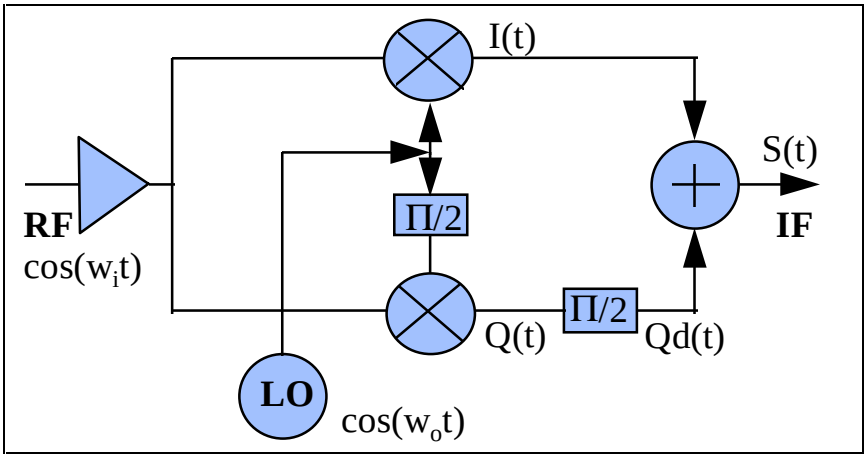


Fig. 2 Image reject mixers

To understand how the process of image rejection with this circuit is done, let's follow the mathematics equations behind that :

The signal **I(t)**, corresponding to the in-phase mixer product is equal to :

$I(t) = \cos(\omega_i t) * \cos(\omega_o t) = 1/2\ (\cos(\omega_i - \omega_o)t + \text{sum frequency}) = 1/2 \cos(\omega_d t)$

with $\omega_d = \omega_i - \omega_o > 0$, considering the case of the RF wanted signal above the LO signal.

The signal **Q(t)**, related to the quadrature mixer product is :

$Q(t) = \cos(\omega_i t) * \cos(\omega_o t - 90°) = 1/2 \cos(\omega_d t + 90°) = -1/2 \sin(\omega_d t)$

The quadrature shifter, introduced in one path, produces a signal $\mathbf{Q_d(t)}$ such as :

$Q_d(t) = -1/2 \sin(\omega_d t - 90°) = 1/2 \cos(\omega_d t)$

The signal **S(t)** , after summing the in-phase and quadrature signals is :

$S(t) = Q_d(t) + I(t) = \cos \omega_d t$, provided that ω_i is the RF frequency and $\omega_d = \omega_i - \omega_o > 0$

Now, assume that $\omega_d = \omega_i - \omega_o < 0$ ω_i is the image frequency

$I(t) = 1/2 \cos(-\omega_d t) = 1/2 \cos(\omega_d t)$

$Q(t) = 1/2 \cos(-\omega_d t + 90°) = 1/2 \sin(\omega_d t)$

$Q_d(t) = 1/2 \sin(\omega_d t - 90°) = -1/2 \cos(\omega_d t)$

Sum I(t) and $Q_d(t)$: $S(t) = 1/2 \cos(\omega_d t) - 1/2 \cos(\omega_d t) = 0$

2. INTRODUCTION TO THE IMAGE REJECTING FRONT ENDS

This chapter provides an overview of this IC family and follows with detailed description, specific to each circuit.

The UAA2072M was the first IC in the image rejection family. To satisfy the need of the emerging digital mobile communications equipment, a family of image rejecting front-end IC's based around the UAA2072M has been developed : the UAA2073M and UAA2073AM dedicated for GSM and the UAA2077AM, UAA2077BM and UAA2077CM dedicated for 2 GHz applications. A simplified block-diagram, representing the main common functionalities of these circuits is shown in Fig. 3. The IC is divided into three main blocks : the receive, transmit and local oscillator sections. The transmit block is not integrated in the UAA2077AM.

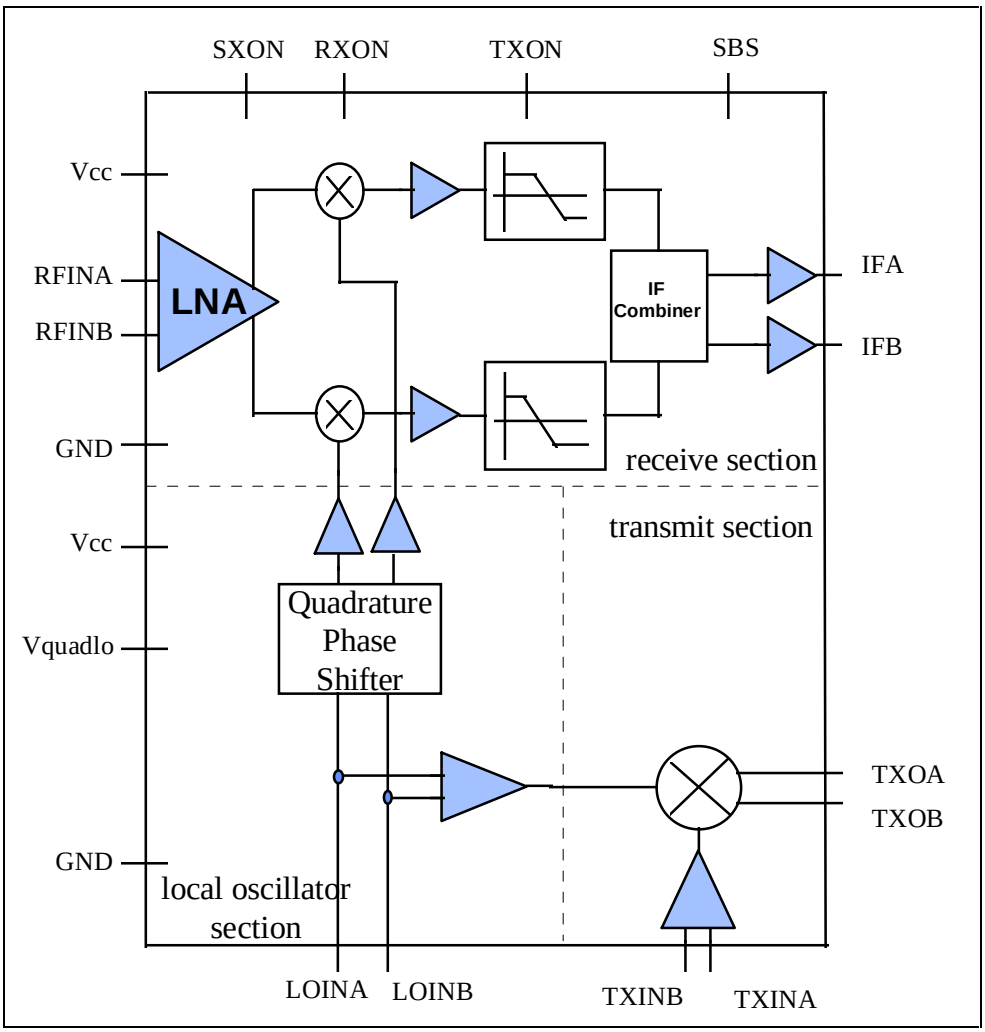


Fig. 3 Block-diagram

The circuits present the following common features :

2.1 Common Features

- low-noise, wide dynamic range amplifier
- double balanced image reject mixing
- integrated Rx and Tx blocks
- IF I/Q combiner
- on-chip quadrature network
- low-power consumption
- very low-noise figure
- small package SSOP20
- very small application (no image filter)

All relevant parameters are summed up in the following table :

Table 1 Quick reference data
Typical values are indicated

	UAA2072M	**UAA2073M**	**UAA2073AM**	**UAA2077AM**	**UAA2077BM**	**UAA2077CM**
Vcc (V)	4.5 to 5.3	3.6 to 5.5	3.6 to 5.3	3.15 to 5.3	3.6 to 5.3	3.6 to 5.3
Iccrx (mA)	31.5	26	26	27	27	36
RX Noise Figure (dB)	4	3.25	3.6	4.3	4.3	4.0
Gain (dB)	26	23	22	20	20	23
IP3 (dBm)	-15	-15	-15	-17	-17	-17
CP1 (dBm)	-24.5	-23	-23	-23	-23	-24
Image Rejection (dB)	35	37	45	32	32	38
IF frequency (MHz)	program.	71 (nominal)	175 (nominal)	110 (nominal)	188 (nominal)	188 (nominal)
Application	GSM	GSM	GSM	DECT	DCS1800	DCS1800/ PCS1900

All these circuits comprise an LNA and an image reject mixer. In the previous equipment designs generation, this RF part was composed of discrete LNA, mixer and image filter. This higher integration level reduces variation of RF performance in production. Therefore, high frequency radio manufacturability is eased so that reliability and reproducibility are thus improved.

The image reject mixer gives typically over 30 dB of image rejection (see Table 1). This means little RF input filtering is necessary, enabling the use of only one low-cost RF input filter. Moreover, the removal of the bulky expensive ceramic image filter enables smaller phone designs.

The performance is such that all critical RF parameters are stable over the entire temperature and voltage ranges.

Particularities of each circuit are described below.

2.2 the UAA2072M

Its supply voltage ranges from 4.5 to 5.3 V ; it is intended to be used in the GSM cellular telephones. To adjust for maximum image rejection performance at a given IF, a control logic programmable via the 3-wire serial bus interface is provided. This permits indeed compensation for process spreads and trimming for the chosen IF frequency and the LO band center frequency. The power-up of the transmit, receive and LO buffers as well as the selection of sideband rejection are also programmable by the 3-wire serial bus.

2.3 the UAA2073M and UAA2073AM

The UAA2073M is the second generation front-end for 900 MHz applications. It offers better performance than the UAA2072M.

The supply voltage range is lower, from 3.6 to 5.3 V with a typical 3.75 V supply. The power consumption has been improved to 26 mA typically in receive mode. The whole control block for tuning image rejection has been suppressed. The image rejection is optimum when the IF frequency is equal to 71 MHz.

The UAA2073AM is a derivative of the UAA2073M, with an IF frequency equal to 175 MHz. The image frequency rejection has been improved to 45 dB but at the expense of a reduced range of possible IF frequencies.

2.4 the UAA2077AM, UAA2077BM and UAA2077CM

In order to meet the rapidly increasing demand for mobile radio 1800 MHz equipment, the UAA2077AM, the UAA2077BM and UAA2077CM have been developed and have become the new generation of image rejection ICs.

The UAA2077AM is intended for use in the digital cordless system DECT, the UAA2077BM and UAA2077CM in the digital cellular systems DCS1800 and PCS1900. One particularity of the UAA2077AM is that it doesn't include a transmit block. One the other hand, the voltage supply can be reduced up to 3.15 V for temperature from 0 to 70 °C. This offers the possibility to connect directly the chip to an unregulated 3-cell battery supply. The UAA2077BM has been designed for DCS1800 applications. The UAA2077CM, a derivative of that IC, was designed initially to address the stringent requirements of PCS1900 applications but is also suitable for DCS1800 applications.

3. FUNCTIONAL DESCRIPTION

3.1 Power-down modes

The UAA2072M is the only one of this ICs' family to feature software power-down modes. For the five other circuits, several power-down modes are exclusively controlled by hardware input pins. Let's take the example of the UAA2073M. According to the block-diagram, 3 different functional areas are defined:

- the receive section
- the transmit section
- the local-oscillator section

For minimizing the pulling effect on the external VCO when entering in the receive or transmit modes, a special mode of operation has been created : the synthesizer-ON (synthon) mode . This mode is used to power-up the buffering on the LO inputs. The whole local oscillator section is thus turned **on**; this includes the quadrature phase shifter and buffers.

When the transmit mode is active, the down conversion mixer and the low-noise amplifier, including in the transmit section are turned **on**. The LO buffer (from the LO section) is also needed to drive the transmit IF down conversion mixer and has to be powered-on.

For the receive mode, the whole receive section is turned **on**, just as the quadrature phase shifter and the LO buffer on the path.

For example, a typical cellular transceiver would first assert SXON, to power-up LO buffers and allow VCO to stabilize, followed some time later by RXON being asserted just before the wanted signal arrives. At the end of the receive burst, RXON only is de-activated to power-down the receiver. The circuit is left in SX mode, as following slots will be used for example for transmitting. The circuit will enter TX mode when TXON is asserted. When the complete transceiver re-enters IDLE mode (no active call), the IC is returned to power down mode by de-activating SXON, RXON and TXON.

The different modes of operation are then defined as follows:

- the RX mode : the receive section and LO buffers to RX are **on**
- the TX mode : the transmit section and LO buffers to TX are **on**
- the Synthon mode : the complete LO section is **on**
- the SRX mode : the receive section is **on** and the Synthon mode active
- the STX mode : the transmit section is **on** and the Synthon mode active

The control of these different power status is done by hardware, with the pins TXON, RXON and SYNTHON.

Different logical combinations allow a selection of all the modes defined above (see Table 2).

Table 2 Control of power status

EXTERNAL PIN LEVEL			**CIRCUIT MODE OF OPERATION**
TXON	**RXON**	**SYNTHON**	
LOW	LOW	LOW	power-down mode
LOW	HIGH	LOW	RX mode
HIGH	LOW	LOW	TX mode
LOW	LOW	HIGH	Synthon mode
LOW	HIGH	HIGH	SRX mode
HIGH	LOW	HIGH	STX mode
HIGH	HIGH	LOW	receive and transmit sections on; specification not guaranteed
HIGH	HIGH	HIGH	receive and transmit sections on; specification not guaranteed

Figure 4 shows these modes of operation.

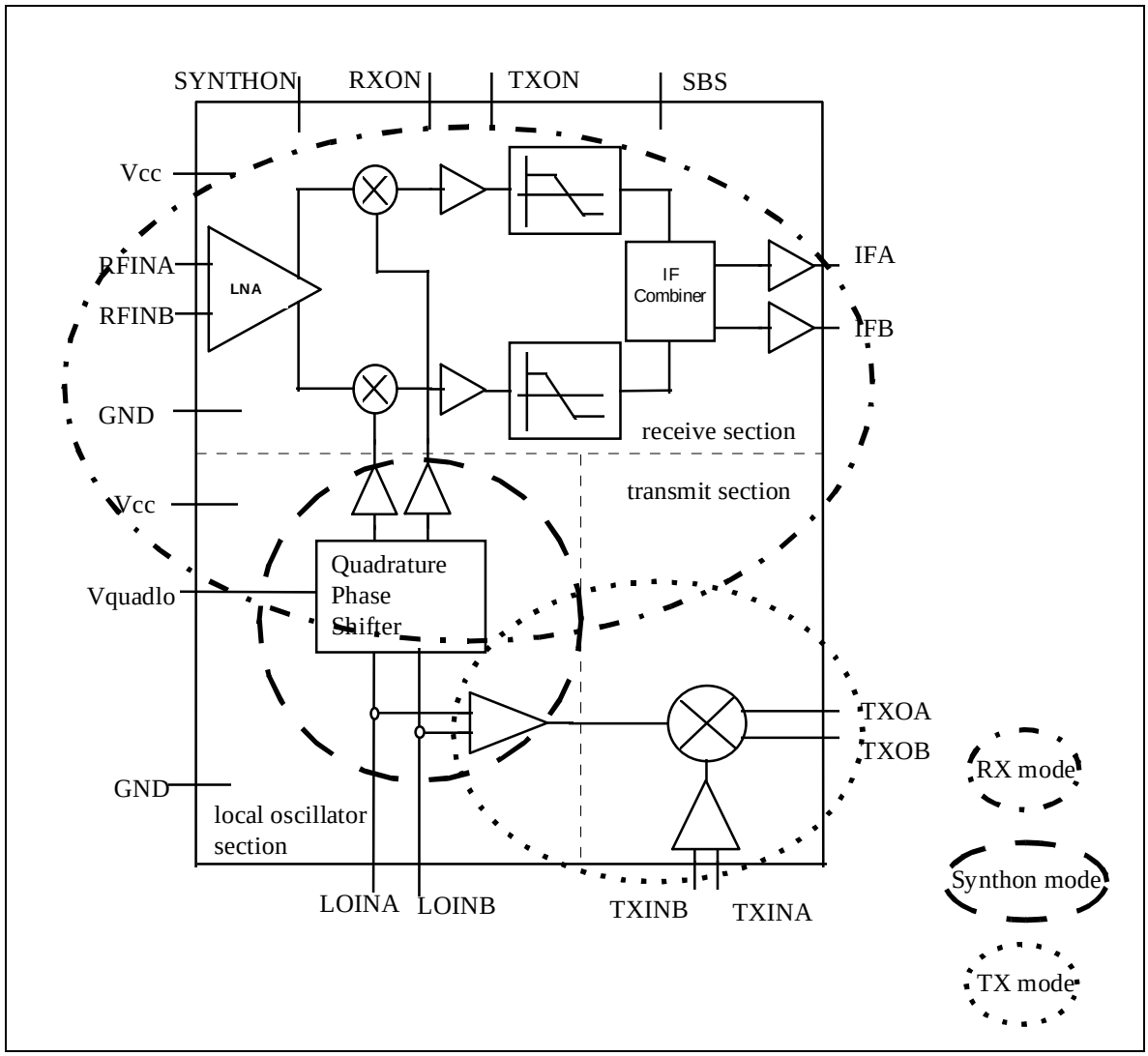


Fig. 4 Power-down modes

Power-down modes for the UAA2077AM/BM/CM operate in the same way. The SYNTHON pin is named in that case the SXON pin and refers to the SX mode (instead of Synthon).

3.2 Pin function diagram

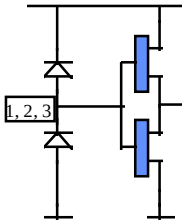
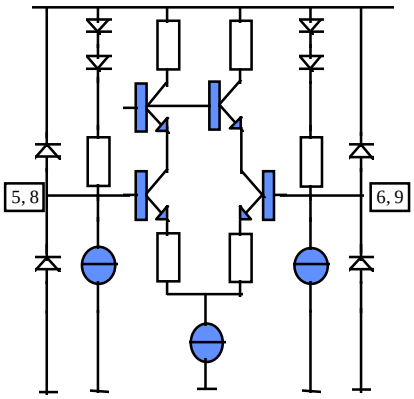
The following table shows the equivalent circuit per pin for the UAA2072M. An analogy can be made for the pins functions diagrams of the UAA2073M/AM and UAA2077AM/BM/CM.

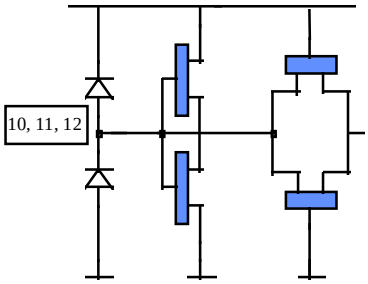
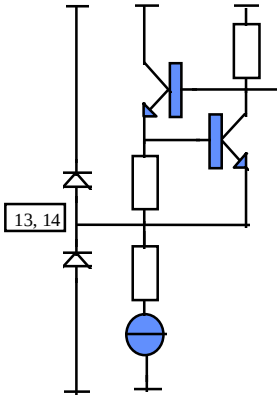
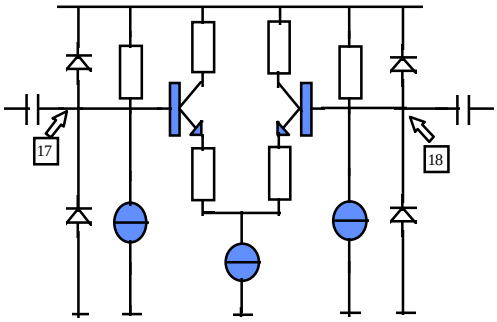
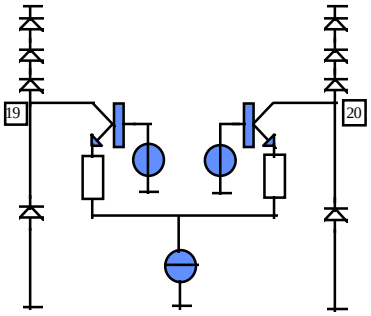
- the equivalent circuits related to the LO, RF, TX inputs and IF outputs are common for all ICs.

- the TX output on the UAA2077BM/CM is identical to the IF output on the UAA2072M.

- the TX output of the UAA2073M/AM is identical to the TX output of the UAA2072M.

- the TXON, RXON and SXON pin diagrams on UAA2073M/AM and UAA2077AM/BM/CM are similar to the CLK, DATA and $\overline{E}$ ones on the UAA2072M.

PIN N°	PIN MNEMOMIC	DCV	EQUIVALENT CIRCUIT
1	CLK		
2	DATA		
3	$\overline{E}$		
5	RFINA	+ 2.1	
6	RFINB	+ 2.1	
8	TXINA	+ 2.2	
9	TXINB	+ 2.2	

PIN N°	PIN MNEMOMIC	DCV	EQUIVALENT CIRCUIT
10	TEST		
11	RXON		
12	TXON		
13	TXOIFB	+ 2.9	
14	TXOIFA	+ 2.9	
17	LOINB	+ 4.8	
18	LOINA	+ 4.8	
19	IFB	+ 2.5	
20	IFA	+ 2.5	

3.3 Phase shifter

The principle of phase shifting, implemented in the image rejecting front-ends is based on all-pass filters.

The basic cell is then as follows :

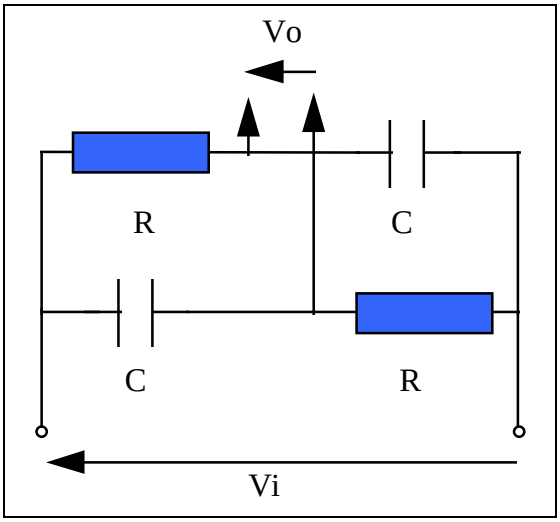


Fig. 5 All-pass filter

From the equations associated with the circuit, it can be easily deduced that :

$$|Vo| = |Vi|$$

$\Delta\phi$ = -2arctan(RCω)

For the LO quadrature phase shifter, two cells of such type are used, one set to 45 ° and the other to 135 ° and work in their linearity zone. Graphs of simulated LO phase shift are given so that exact quadrature phase can be obtained for a given LO frequency (see Fig. 6 and Fig. 7).

The design procedure for phase-shifting on the I and Q channels is similar.

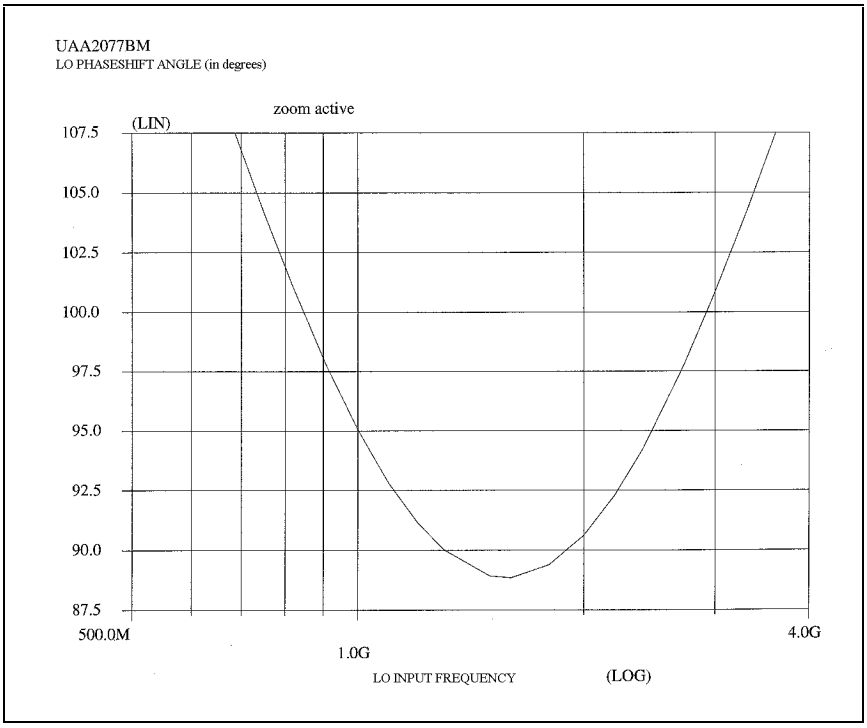


Fig. 6 Simulated LO phase shift versus LO input frequency

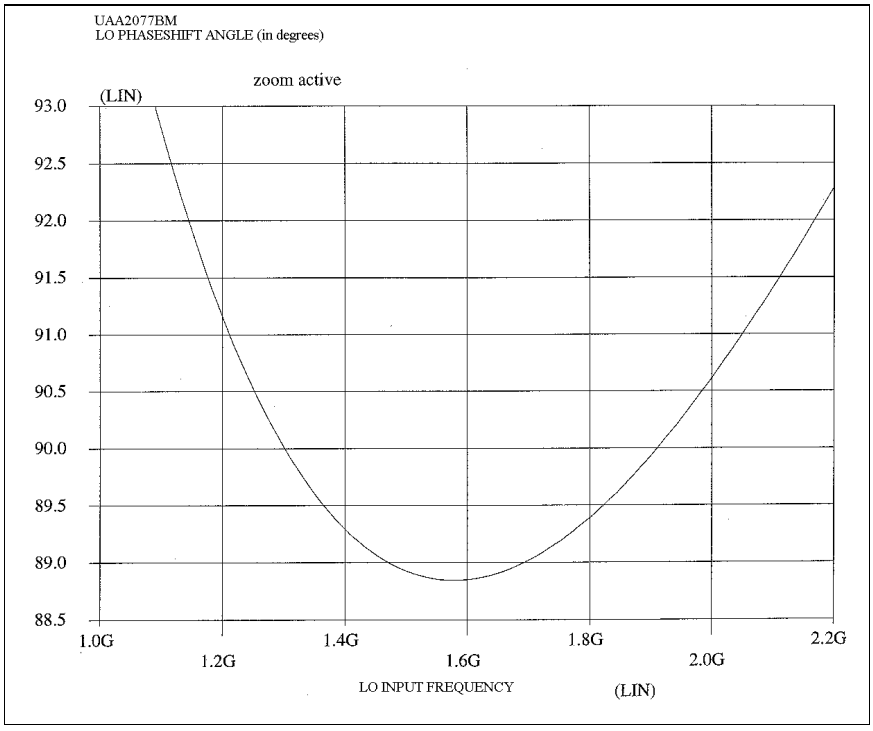


Fig. 7 Simulated LO phase shift versus LO input frequency (magnified around 1.6 GHz)

4. IMPEDANCE MATCHING CONSIDERATIONS

4.1 Introduction

Transfer of power between a source and its load must be done with a minimum of loss, particulary if the originated signal is already very low. Therefore, special care must be taken for impedance matching when designing a RF circuit. The aim is indeed to enable a maximum of power transfer.

4.2 Impedance Matching

Let's assume first that the source and load impedances are purely resistive equal to R_S and R_L. A matching can be easily done with a L-network design, shown below . It is the simplest and most widely used circuit as a matching circuit :

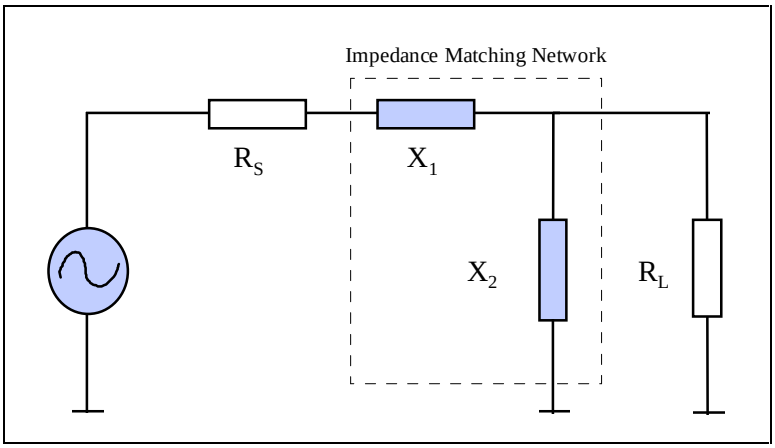


Fig. 8 L-network circuit

R_S : source resistance

R_L : load resistance

X_1 : series reactance

X_2 : parallel reactance

Let's now introduce the equations, which can be used to design this network.

Dealing with the quality factor Q, the following equations provide a simple and quick solution.

Determine the Q factors from

$$Q_1 = Q_2 = \sqrt{\frac{R_L}{R_S} - 1}$$

Determine X_1 and X_2 from

$Q_1 = X_1 / R_S$ $Q_2 = R_L / X_2$

Since there are 2 possible arrangements of the L and C components, X_1 and X_2 can be either capacitive or inductive reactance; it depends on the configuration required, low-pass or high-pass.

In most cases, the impedance is rarely purely resistive. Source and load impedances are almost always complex, i.e. they contain both resistive and reactive components. Therefore, it is also necessary to handle these stray reactances.

Two basic approaches can be used : the stray reactances present in the source and load can be absorbed in the matching network when the stray element values are smaller than the calculated element values. If not, they can be resonated with an equal and opposite reactance. This is the basic of any matching design, to make the source drive its complex conjugate as a load impedance The reactive parts thus cancel each other and leave only R_S and R_L . If R_S and R_L are equal, maximum power transfer is achieved.

4.3 Balun Design

A balun is a device for matching an unbalanced line (e.g. a coax) to a balanced load (e.g. an antenna).

The standard configuration of all baluns utilized in our application is depicted in Fig. 9.

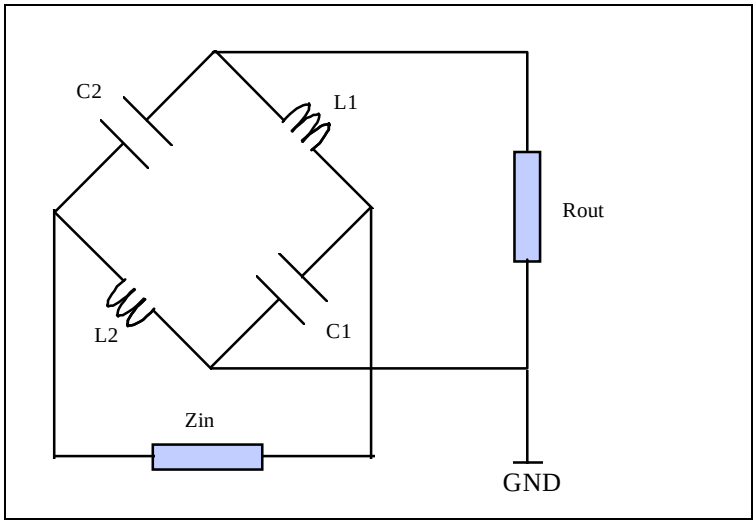


Fig. 9 Balun circuit

Since Rout represents the output impedance of the generator, it is always resistive (e.g. 50 Ω). Zin represents the differential input impedance of the circuit. In order to simplify the balun design, let's assume that Zin is also resistive, equal to Rin.

Therefore, L1 = L2

C1 = C2

The mathematics associated with the circuit give the following results; the balun parameters, depending on the input / output resistances and frequency are :

$$L = \frac{\sqrt{Rin * Rout}}{\omega} \qquad \text{and } C = \frac{1}{\omega * \sqrt{Rin * Rout}}$$

To get more information on printed balun design, please refer to the "OM5045 Dect radio design" application note (see references).

5. TYPICAL APPLICATION CIRCUITS

5.1 Worked Examples

In this chapter, a design example, based around the UAA2077BM for DCS1800 applications is given. The circuit is typically connected as shown in Fig. 26. All values related to input / output impedances are mentioned in the product datasheet (dated from 9 Jan 96). The input impedance parameters are always specified in parallel configuration.

Multilayer ceramic capacitors with NPO dielectric have been used for general coupling/decoupling aspects :

- a value of 8.2 pF for decoupling 2 GHz frequencies (C1, C3, C17, C18, C19, C29 for AC-coupling; C6 to C9, C27, C30 for supply voltage decoupling).

- a value of 100 pF for decoupling 100-200 MHz frequencies (C11, C23 for AC-coupling; C5, C31 for supply voltage decoupling)

This choice results in a compromise between a high capacitive value needed for decoupling and the effect of parasitic inductance (self resonance frequency) appearing when dealing with high frequencies.

5.1.1 RF input

R_p, the real part of the parallel impedance is equal to 60 Ω

C_p, the imaginary part of the parallel impedance is equal to 1 pF

f_i , the RF input frequency is equal to 1850 MHz

The balun component values are then calculated at 1850 MHz with Rin = 60 Ω and Rout = 50 Ω

L = 4.7 nH On the demo board, L6 = L1 = 5.6 nH

C = 1.6 pF On the demo board, C2 = C14 = 1.2 pF

The difference found between calculated and real values are due to PCB parasitic effects. An optimization has also been done in order to get a noise figure as small as possible.

Now, let's resonate C_p with an equal and opposite reactance at 1850 MHz :

$LC_p\omega^2 = 1$ hence L = 7.4 nH On the demoboard, L15= 6.8 nH.

5.1.2 TX input

R_p, the real part of the parallel impedance is equal to 65 Ω

C_p, the imaginary part of the parallel impedance is equal to 1 pF

f_i , the RF input frequency is equal to 1750 MHz

This yields to the following values :

L = 5.2 nH L7 = L8 = 4.7 nH

C = 1.6 pF C15 = C16 = 1.8 pF

5.1.3 IF output

According to the pin function diagram, the IF output is of the open-collector type. It can also be deduced that the voltage output can not be greater than $V_{cc}+3V_{be}$.

It is decided to proceed in 2 stages :

- a first matching from 1.2 kΩ to 50 Ω in single-ended mode that means on each IF output

- a second matching using a balun in order to provide from both IF ouputs, IF_A and IF_B (100 Ω differential) one terminal single ended output IF_O at 50 Ω.

Matching

The need for a DC path between V_{CC} and the output pin dictates the need for an inductor in the shunt leg of the matching network.

Z_{LRX}, the typical application IF output load impedance is equal to 1kΩ in balanced configuration. C_{IF}, the typical internal capacitance, measured on the demo board is equal to 4 pF.

The application is then for 1 kΩ load in differential mode i.e. 1 kΩ on each single-ended IF output.

For our application, C_L is equal to 4 pF

R_L is chosen equal to 1.2 kΩ

R_S = 50 Ω

f_{IF} = 188 MHz

Following the basic design procedure from paragraph 4.2 yields :

$$Q_1 = Q_2 = \sqrt{\frac{1200}{50} - 1} = 4.8$$

$X_1 = Q_1 * R_S = 50 * 4.8 = 240$

$X_2 = R_L / Q2 = 1200 / 4.8 = 250$

$X_1 = 1 / C\omega \quad \Rightarrow C = 1 / X_1 \omega = 1 / (240 * 2\pi * 188.10^6) = 3.5$ pF

On the schematic, C22 = C24 = 3.9 pF

$X_2 = L\omega \quad \Rightarrow L = X_2 / \omega = 250 / (2\pi * 188.10^6) = 212$ nH

The matching for the reactive part of the load, C_L = 4 pF, leads to the following value for L' :

$L'C\omega^2 = 1 \quad \Rightarrow L' = 1 / (4.10^{-12} * (2\pi * 188.10^6)^2) = 1.79.10^{-7}$

The resultant inductance is :

$L // L' = 97*10^{-9} = 97$ nH

On the schematic, L11 = L12 = 100 nH

Balun

Rin = 100 Ω

Rout = 50 Ω

L = $\sqrt{100 * 50}$ / (2π*188*10^6)= 59.8 nF L13 = L14 = 56 nH

C = 1 / ($\sqrt{100 * 50}$ *2π*188.10^6) = 11.9 pF C25 = C26 = 12 pF

6. MEASUREMENTS and RESULTS

6.1 Matching results

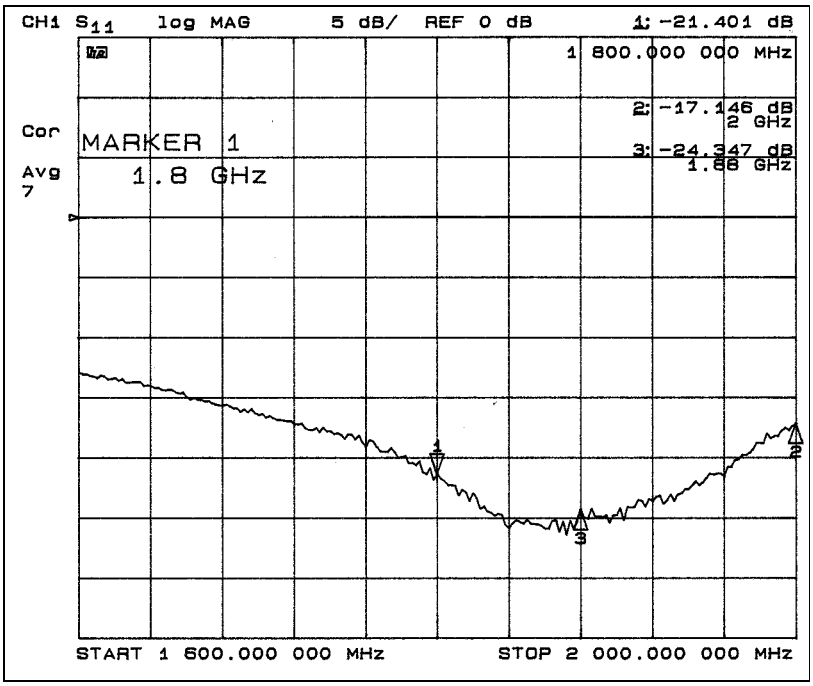


Fig. 10 Matching at RF input

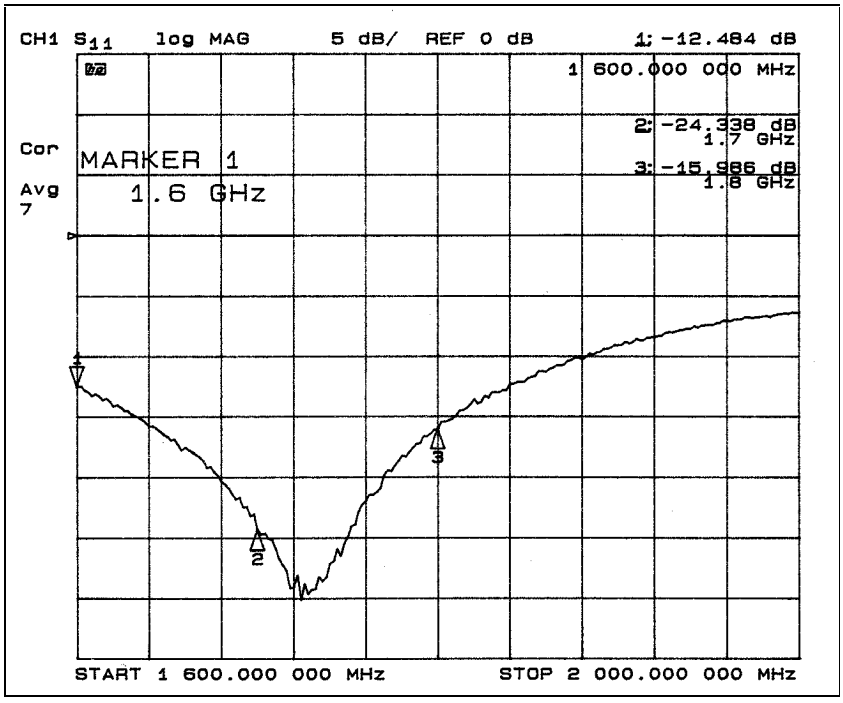


Fig. 11 Matching at TX input

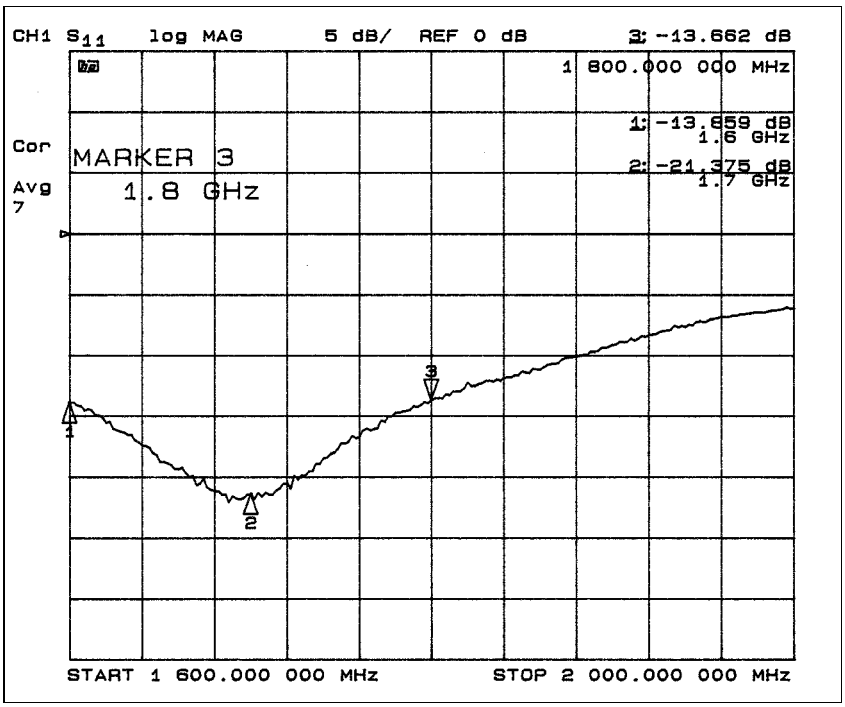


Fig. 12 Matching at LO input

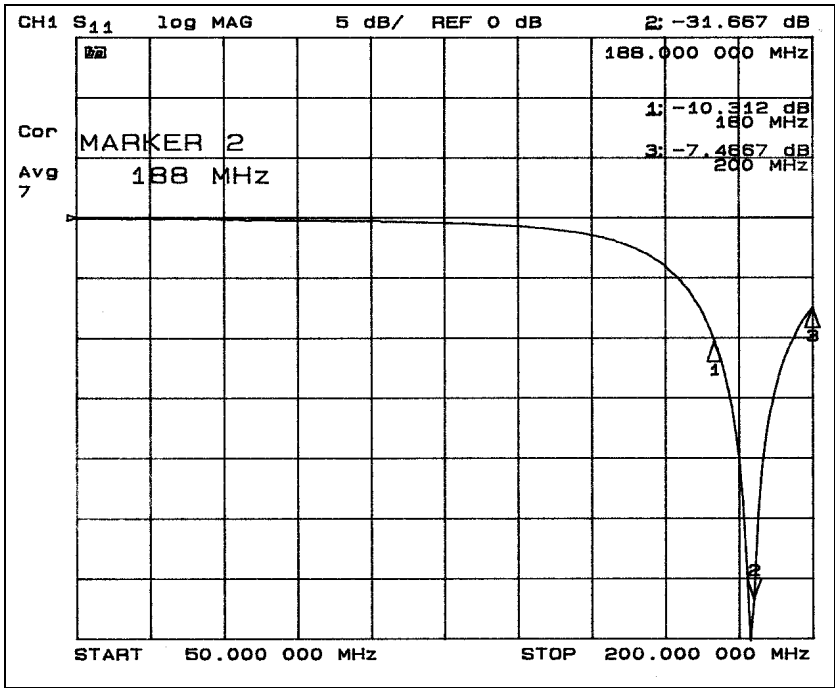


Fig. 13 Matching at IF output

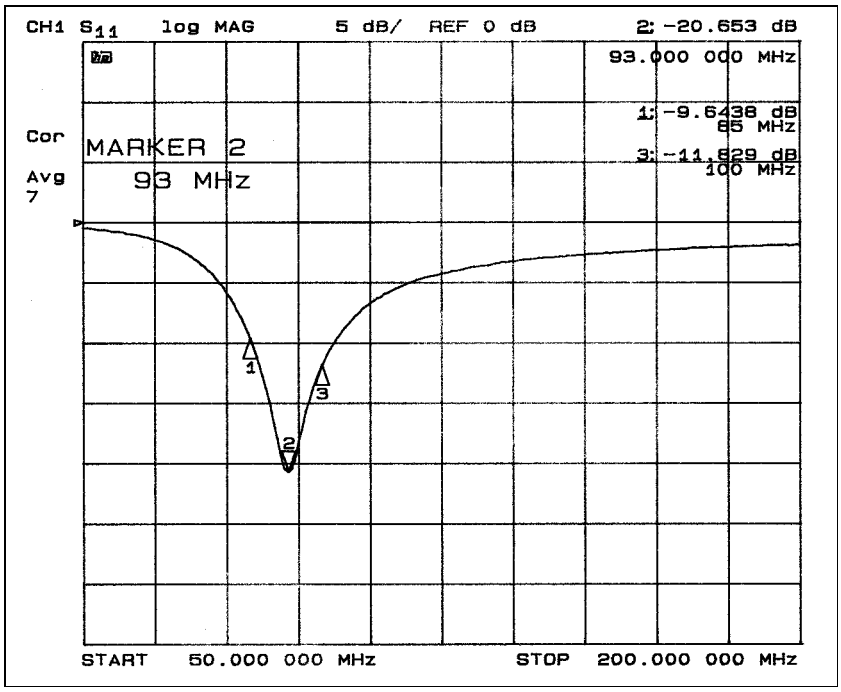


Fig. 14 Matching at TX output

6.2 Linearity / spurious response

In Fig. 15 is depicted the setup used for measuring the spurious response . Two separate measurements have been done :

- the RF frequency sweeps from RF - 4IF to RF + IF with a variable step of IF/(3∗4∗5) in order to reach the 2nd, 3rd, 4th and 5th harmonics.

- the RF frequency sweeps from IF to 22 IF with a fixed step equal to IF/5

In both cases, the LO frequency is fixed and the network analyzer always looks at a fixed IF frequency.

The results are shown on Fig. 16 and Fig. 17.

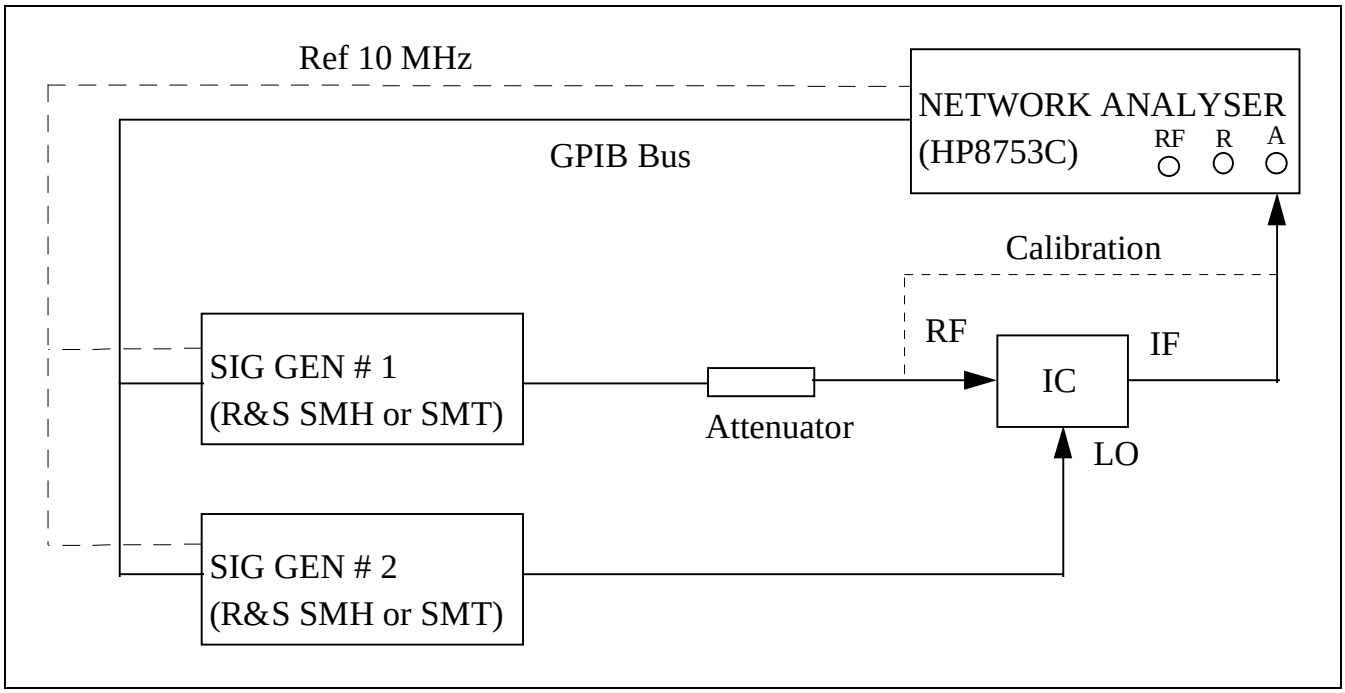


Fig. 15 Spurious response measurement setup

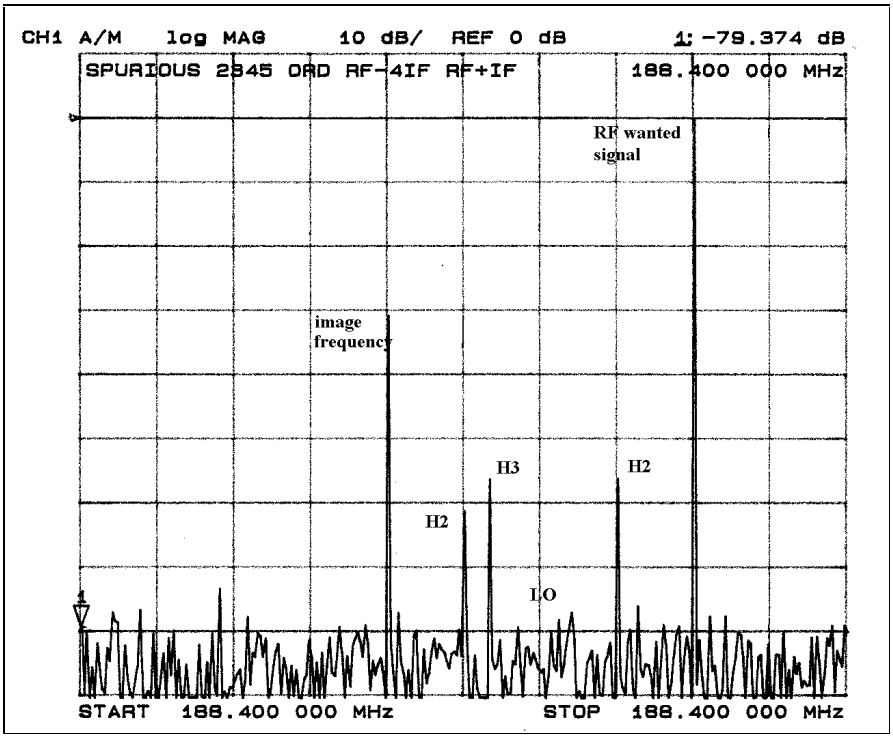


Fig. 16 UAA2077BM spurious response

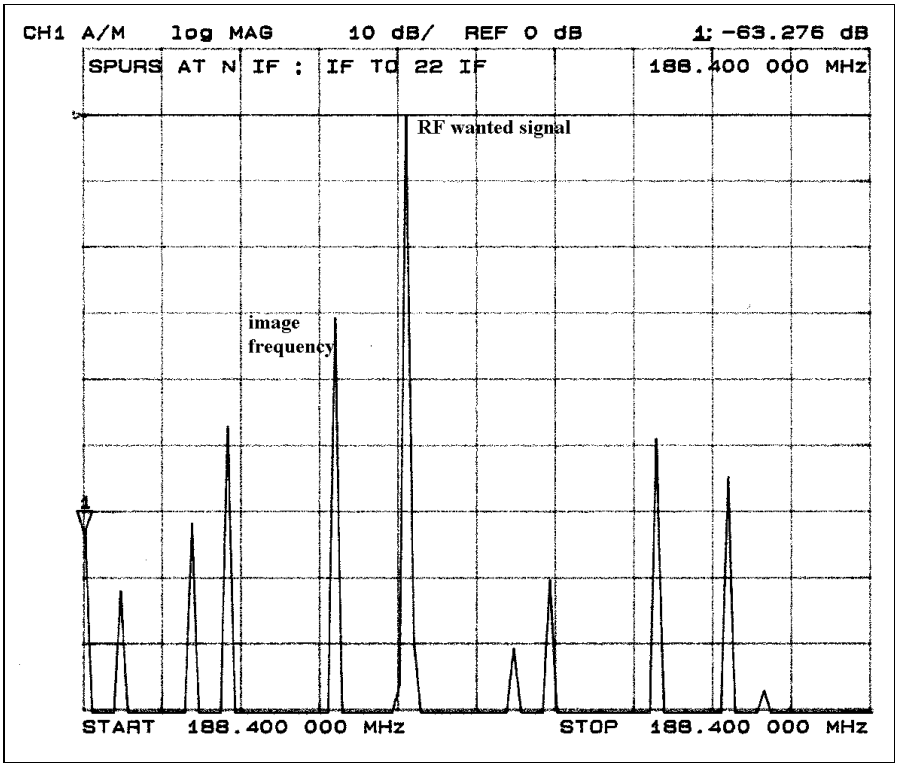


Fig. 17 UAA2077BM spurious response

6.3 Image rejection

Image rejection measurements have been proceeded in varying 2 different parameters :

- the image rejection is given versus the IF frequency with a fixed LO . The RF signal is swept. The appropriate set-up is depicted on Fig. 18. Results are shown on Fig. 19 and 20.

- the image rejection is given versus the RF frequency with a fixed IF. Both RF and LO input signals are swept. The set-up, in that case, is identical to the one used for spurious response measurement (see Fig. 15). The results are shown on Fig. 21.

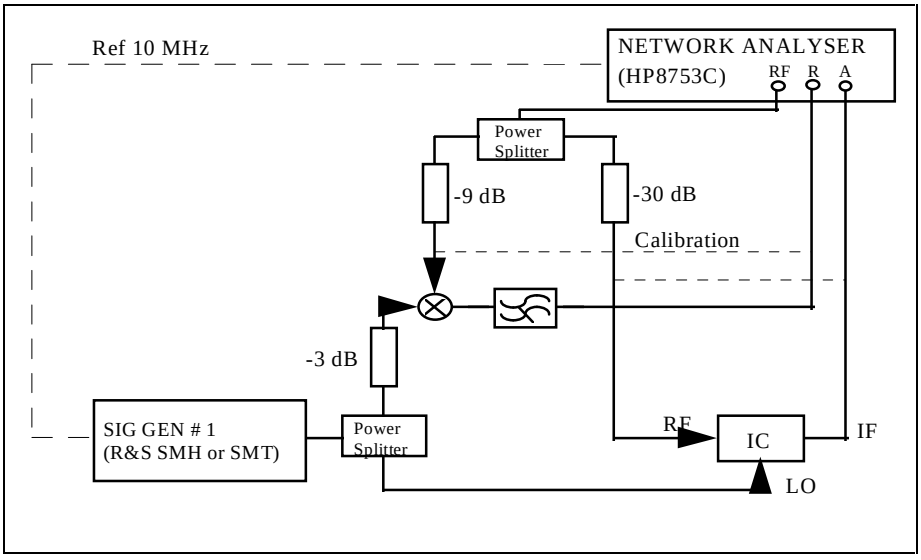


Fig. 18 Image rejection measurement setup with a fixed LO frequency

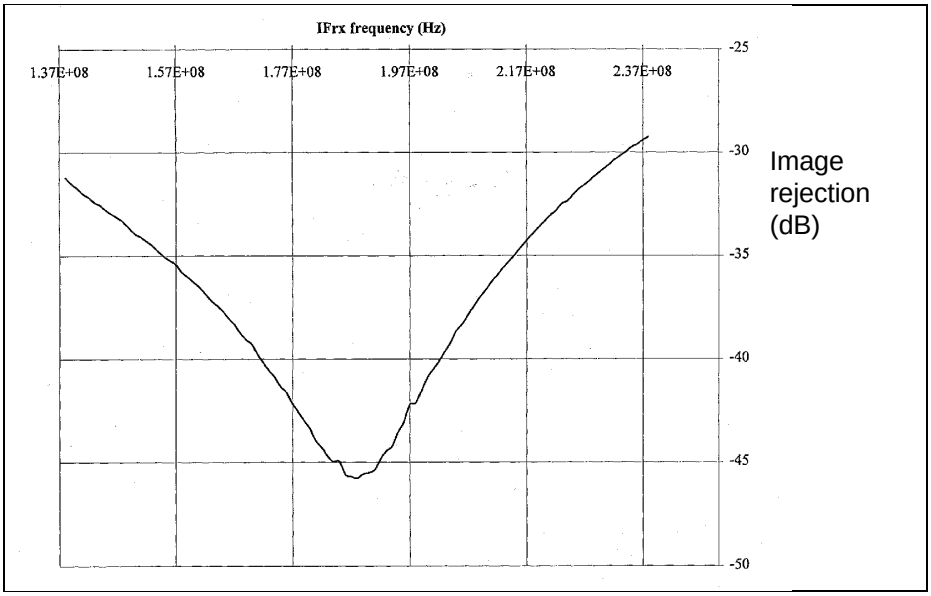


Fig. 19 UAA2077CM Image rejection versus IF frequency for f_{RF} wanted > f_{LO}

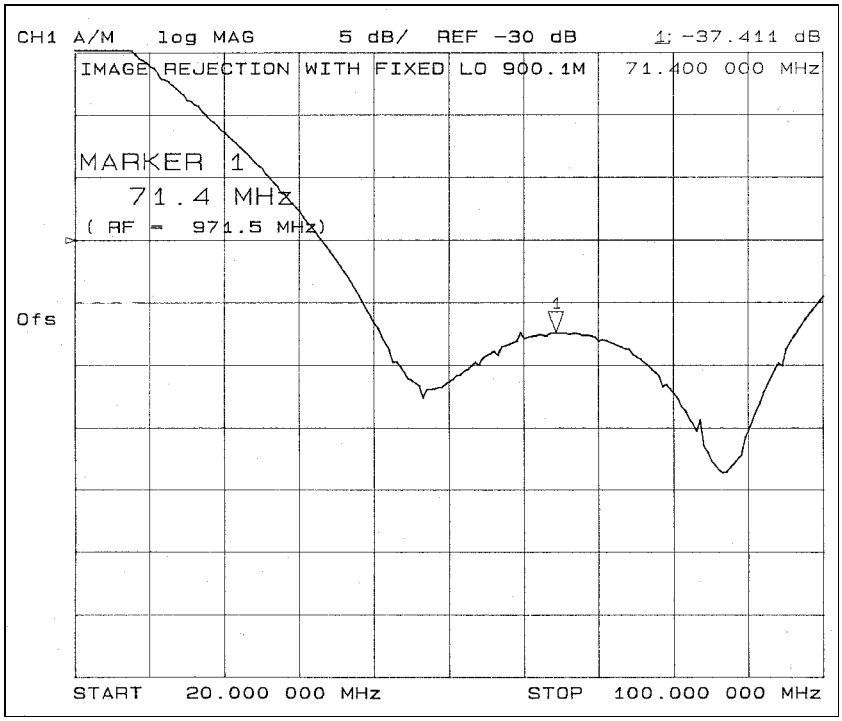


Fig. 20 UAA2073M Image rejection versus IF frequency

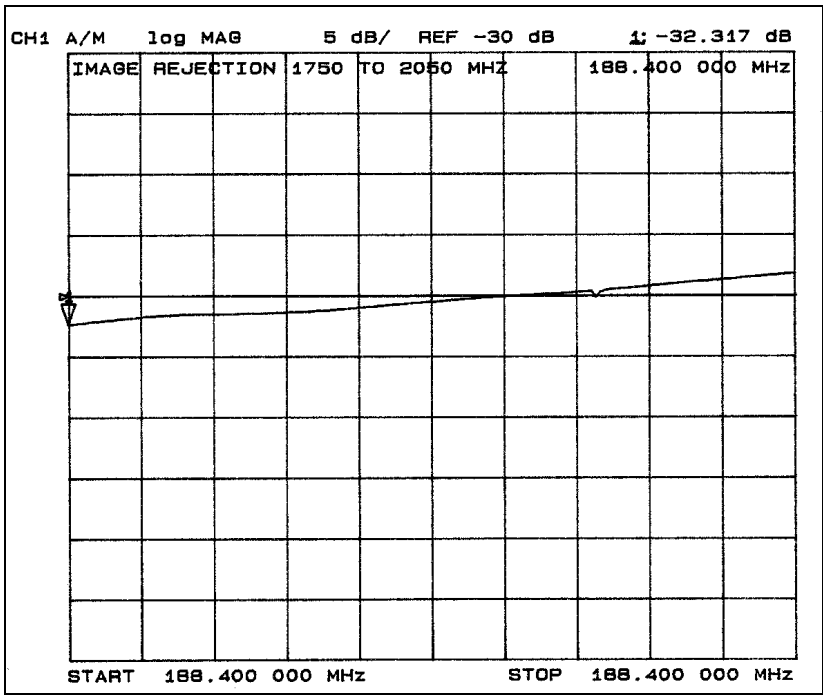


Fig. 21 UAA2077BM Image rejection versus LO frequency

6.4 Gain, compression point and IP3

The gain presented on Fig. 23 has been measured for a fixed IF frequency with a RF swept from 1.75 to 2.05 GHz. The set-up utilized in that case is the same as the one shown on Fig. 15.

The 1 dB compression point has been measured following the test set-up depicted on Fig. 20.

The set-up shown on the following figure enables a measurement of the 3rd order intercept point parameter.

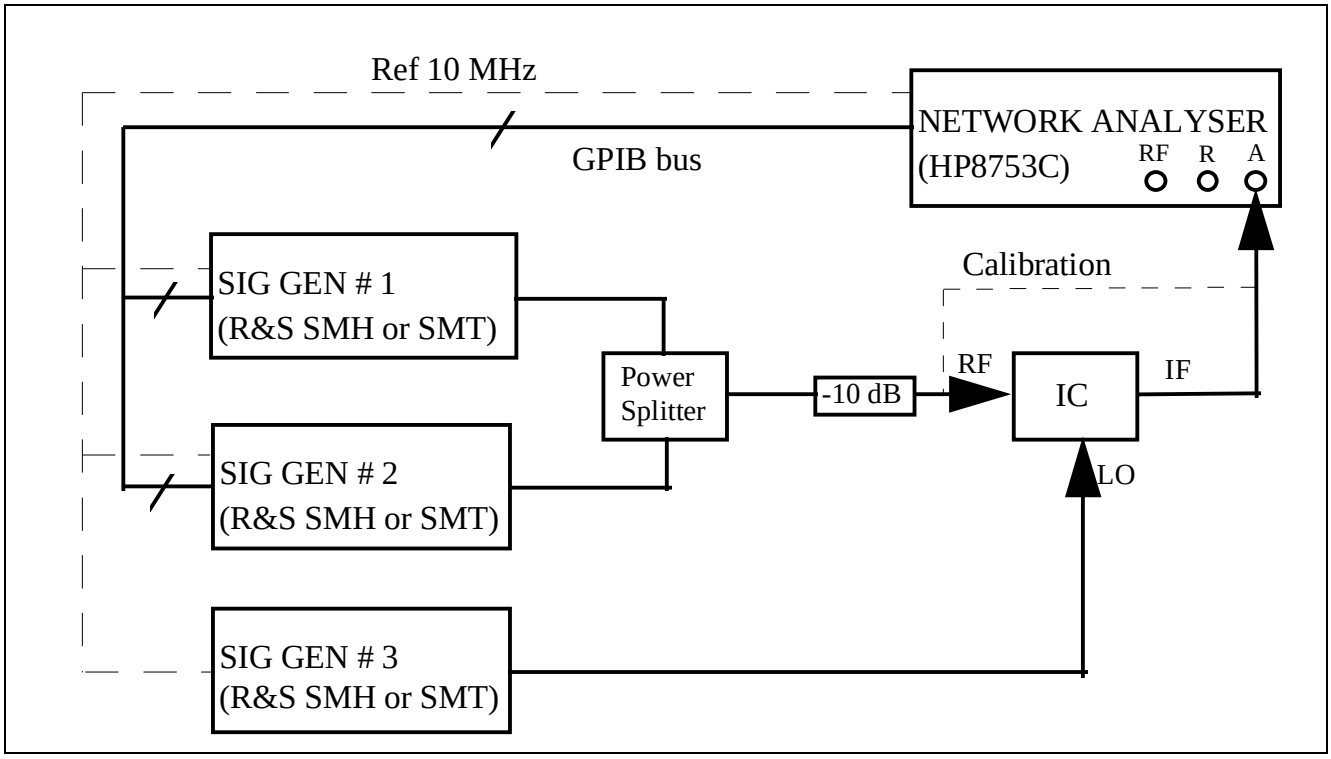


Fig. 22 Third order Intercept Point set-up

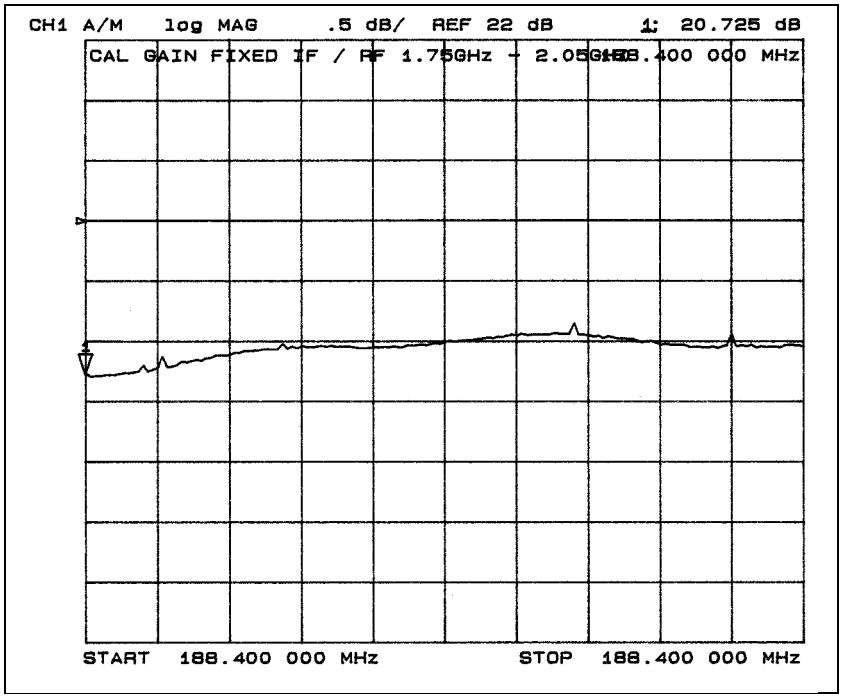
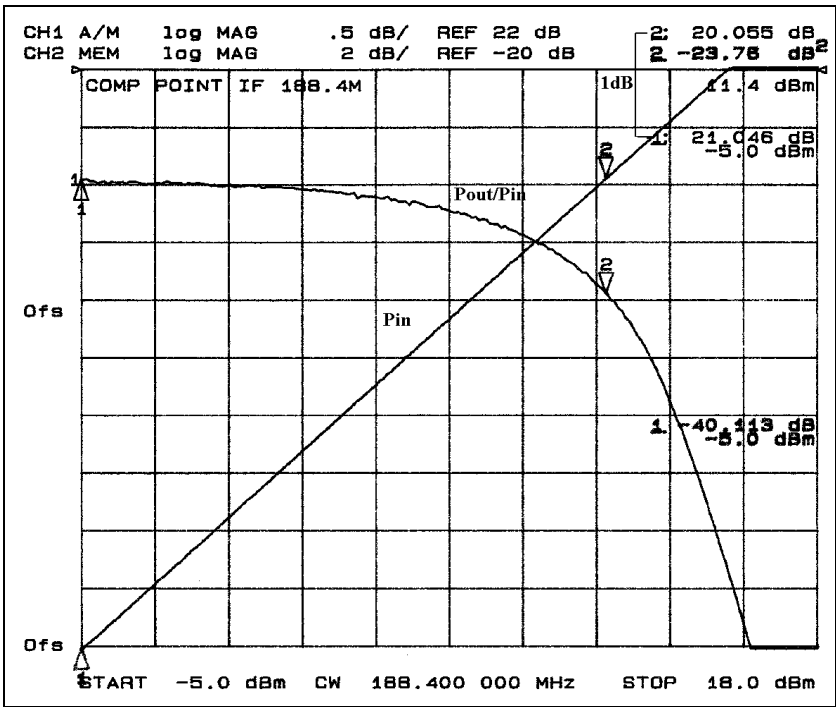


Fig. 23 UAA2077BM gain versus input frequency (from 1.75 to 2.05 GHz)



CPin = -23.75 dBm

Fig. 24 UAA2077BM 1 dB Compression Point

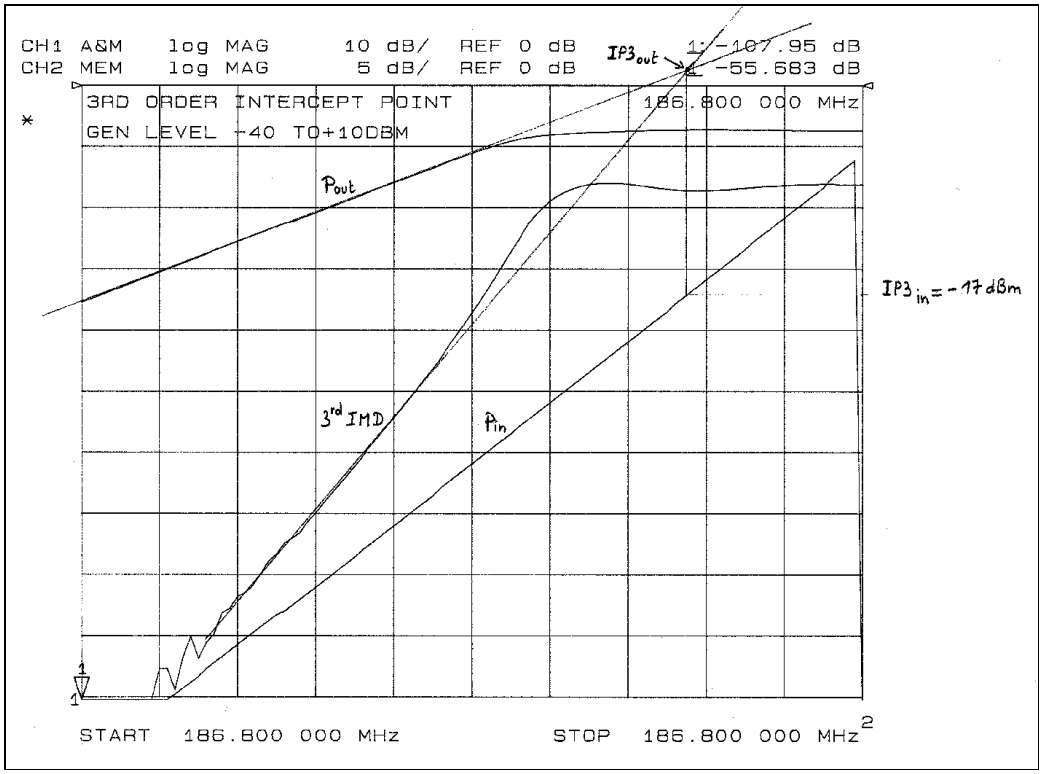


Fig. 25 UAA2077BM 3rd order Intercept Point

7. DEMONSTRATION BOARD

Two different kinds of board have been designed, one related to the UAA2073XM ICs, the other one to the UAA2077XM ICs.The UAA2077BM and the UAA2073M have been taken as an example for both families.

7.1 Schematic drawings

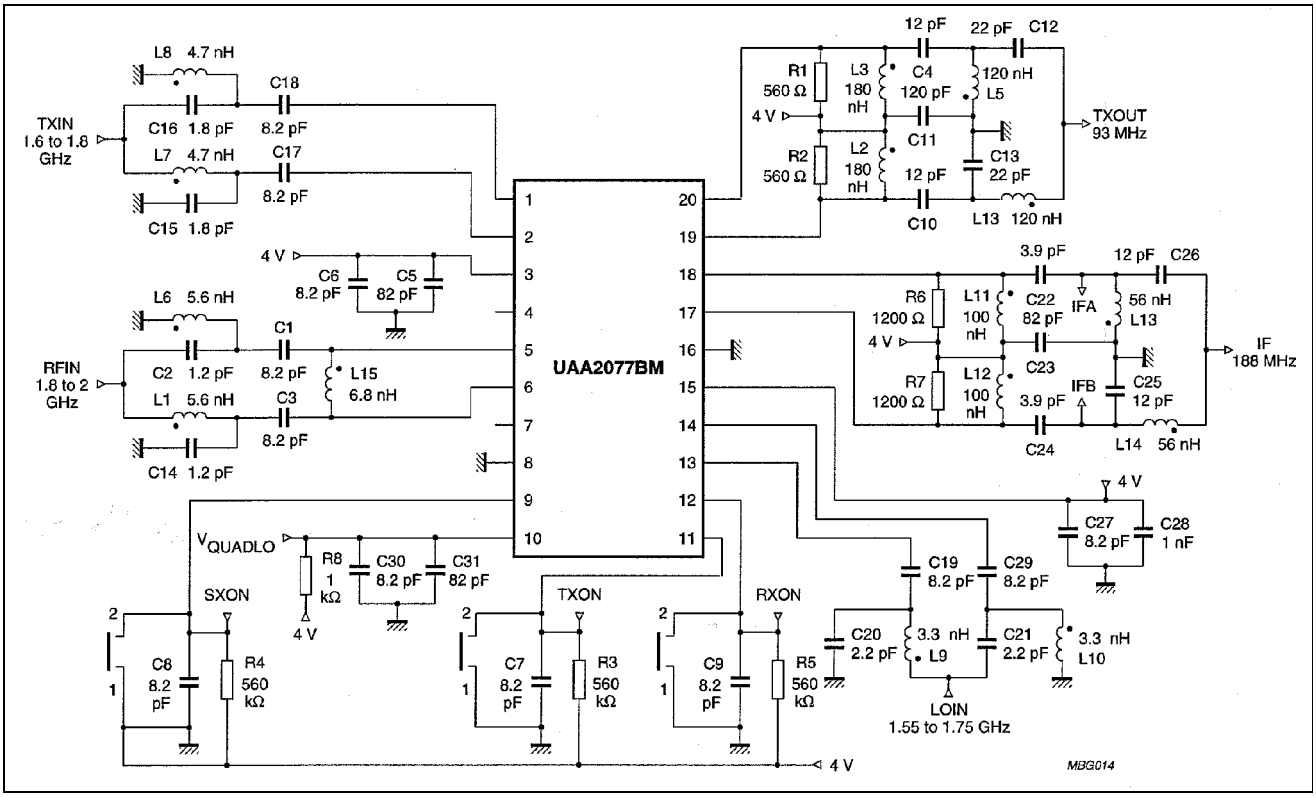


Fig. 26 UAA2077BM application diagram

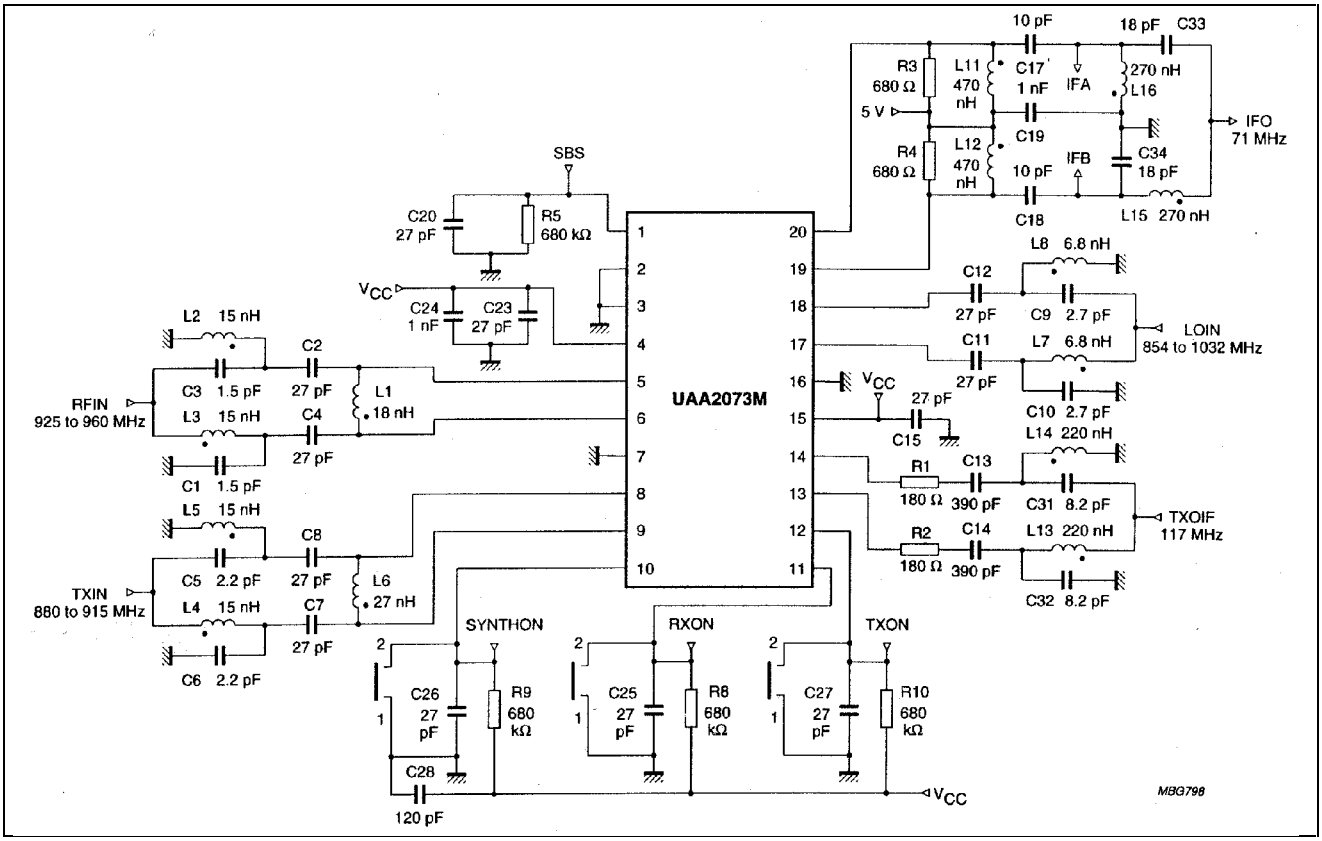


Fig. 27 UAA2073M application diagram

7.2 Component lists

Component values for the UAA2077BM demoboard are indicated below.

Table 3 Demo board Component List

Reference	Value	Type / Size	Reference	Value	Type / Size
L1	5.6 nH	0603 SMD	C13	22 pF	0805 SMD
L2	180 nH	0805 SMD	C14	1.2 pF	0603 SMD
L3	180 nH	0805 SMD	C15	1.8 pF	0603 SMD
L4	120 nH	0805 SMD	C16	1.8 pF	0603 SMD
L5	120 nH	0805 SMD	C17	8.2 pF	0603 SMD
L6	5.6 nH	0603 SMD	C18	8.2 pF	0603 SMD
L7	4.7 nH	0603 SMD	C19	8.2 pF	0603 SMD
L8	4.7 nH	0603 SMD	C20	2.2 pF	0603 SMD
L9	3.3 nH	0603 SMD	C21	2.2 pF	0603 SMD
L10	3.3 nH	0603 SMD	C22	3.9 pF	0805 SMD
L11	100 nH	0805 SMD	C23	82 pF	0805 SMD
L12	100 nH	0805 SMD	C24	3.9 pF	0805 SMD
L13	56 nH	0805 SMD	C25	12 pF	0805 SMD
L14	56 nH	0805 SMD	C26	12 pF	0805 SMD
L15	6.8 nH	0603 SMD	C27	8.2 pF	0805 SMD
C1	8.2 pF	0603 SMD	C28	1 nF	1206 SMD
C2	1.2 pF	0603 SMD	C29	8.2 pF	0603 SMD
C3	8.2 pF	0603 SMD	C30	8.2 pF	0805 SMD
C4	12 pF	0805 SMD	C31	82 pF	0805 SMD
C5	82 pF	0805 SMD	R1	560 Ω	0805 SMD
C6	8.2 pF	0805 SMD	R2	560 Ω	0805 SMD
C7	8.2 pF	0805 SMD	R3	560 k Ω	0805 SMD
C8	8.2 pF	0805 SMD	R4	560 k Ω	0805 SMD
C9	8.2 pF	0805 SMD	R5	560 k Ω	0805 SMD
C10	12 pF	0805 SMD	R6	1.2 k Ω	0805 SMD
C11	120 pF	0805 SMD	R7	1.2 k Ω	0805 SMD
C12	22 pF	0805 SMD	R8	1 k Ω	0805 SMD

Component values for the UAA2073M demoboard are indicated below.

Table 4 Demo board Component List

Reference	Value	Type / Size	Reference	Value	Type / Size
R1	180 Ω	0805 SMD	C20	27 pF	0805 SMD
R2	180 Ω	0805 SMD	C23	27 pF	0805 SMD
R3	680 Ω	0805 SMD	C24	1 nF	0805 SMD
R4	680 Ω	0805 SMD	C25	27 pF	0805 SMD
R5	680 kΩ	0805 SMD	C26	27 pF	0805 SMD
R8	680 kΩ	0805 SMD	C27	27 pF	0805 SMD
R9	680 kΩ	0805 SMD	C28	120 pF	0805 SMD
R10	680 kΩ	0805 SMD	C31	8.2 pF	0805 SMD
C1	1.5 pF	0805 SMD	C32	8.2 pF	0805 SMD
C2	27 pF	0805 SMD	C33	18 pF	0805 SMD
C3	1.5 pF	0805 SMD	C34	18 pF	0805 SMD
C4	27 pF	0805 SMD	L1	18 nH	0805 SMD
C5	2.2 pF	0805 SMD	L2	15 nH	0805 SMD
C6	2.2 pF	0805 SMD	L3	15 nH	0805 SMD
C7	27 pF	0805 SMD	L4	15 nH	0805 SMD
C8	27 pF	0805 SMD	L5	15 nH	0805 SMD
C9	2.7 pF	0805 SMD	L6	27 nH	0805 SMD
C10	2.7 pF	0805 SMD	L7	6.8 nH	0805 SMD
C11	27 pF	0805 SMD	L8	6.8 nH	0805 SMD
C12	27 pF	0805 SMD	L11	470 nH	1008 SMD
C13	390 pF	0805 SMD	L12	470 nH	1008 SMD
C14	390 pF	0805 SMD	L13	220 nH	0805 SMD
C15	27 pF	0805 SMD	L14	220 nH	0805 SMD
C17	10 pF	0805 SMD	L15	270 nH	1008 SMD
C18	10 pF	0805 SMD	L16	270 nH	1008 SMD
C19	1 nF	0805 SMD			

7.3 Layout and assembly drawings

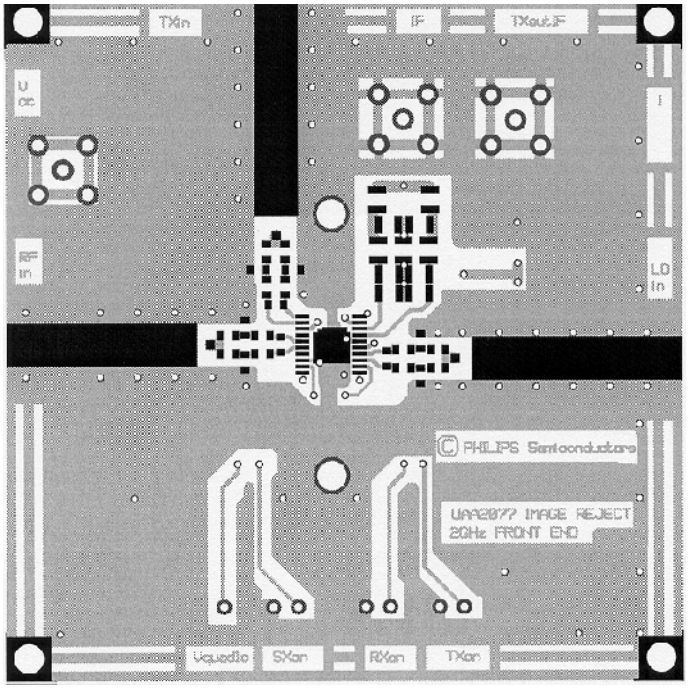


Fig. 28 UAA2077XM Demo board - Layer 1

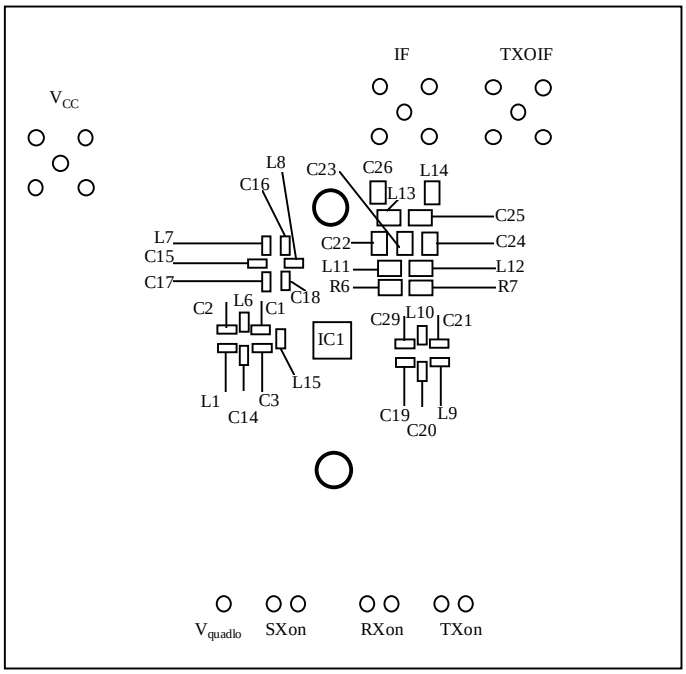


Fig. 29 UAA2077XM Demo board - Layer 1 Assembly

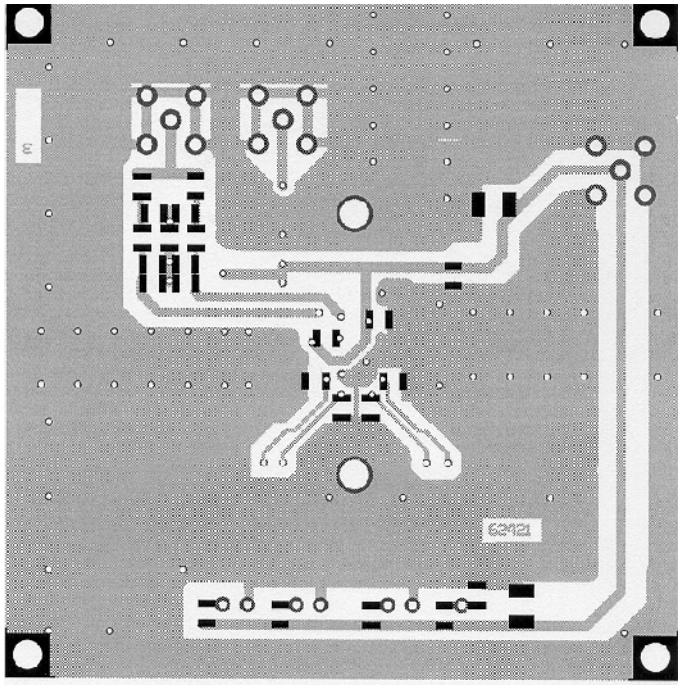


Fig. 30 UAA2077XM Demo Board - Layer 2 Layout

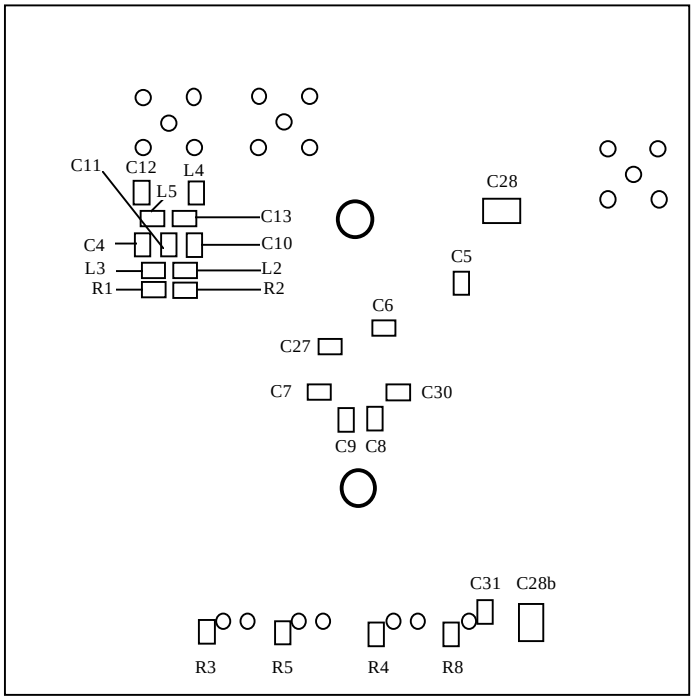


Fig. 31 UAA2077XM Demo Board - Layer 2 Assembly

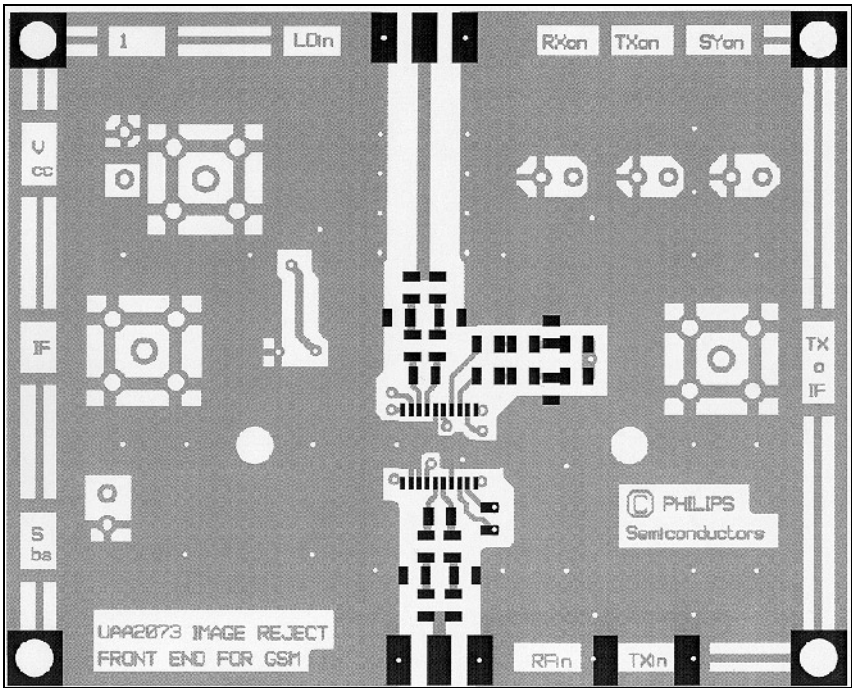


Fig. 32 UAA2073XM Demo Board - Layer 1 Layout

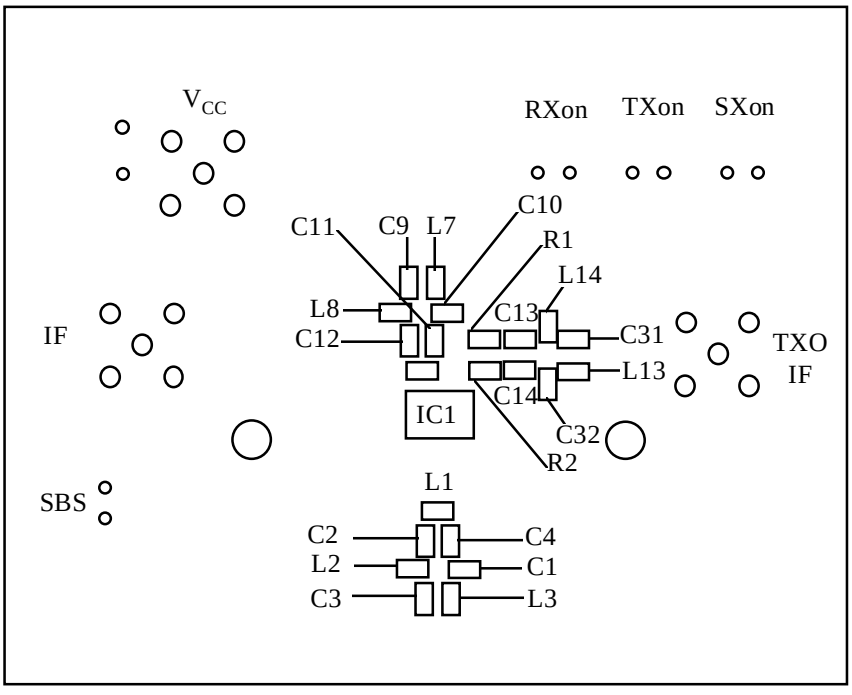


Fig. 33 UAA2073XM Demo board - Layer 1 Assembly

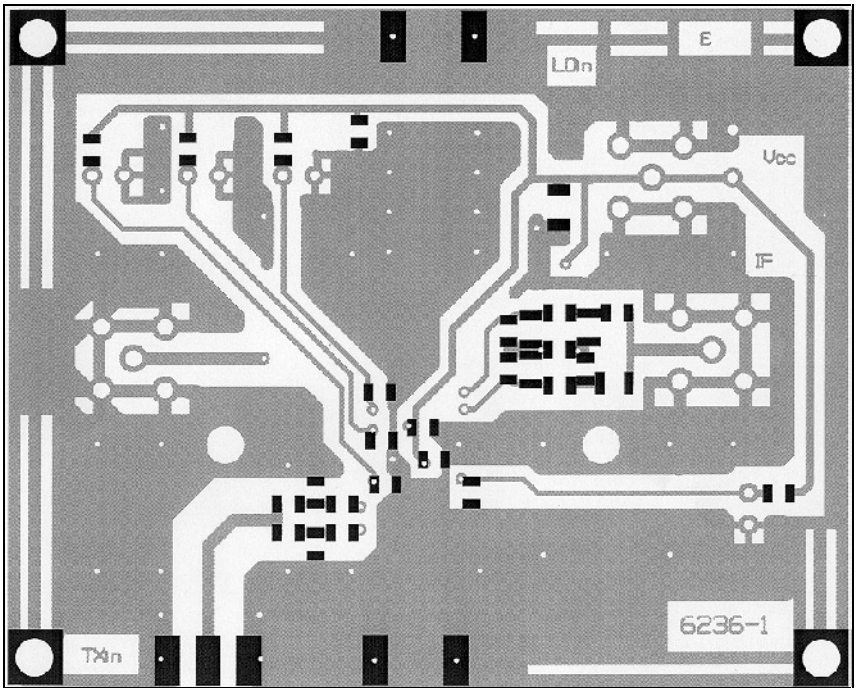


Fig. 34 UAA2073XM Demo Board - Layer 2 Layout

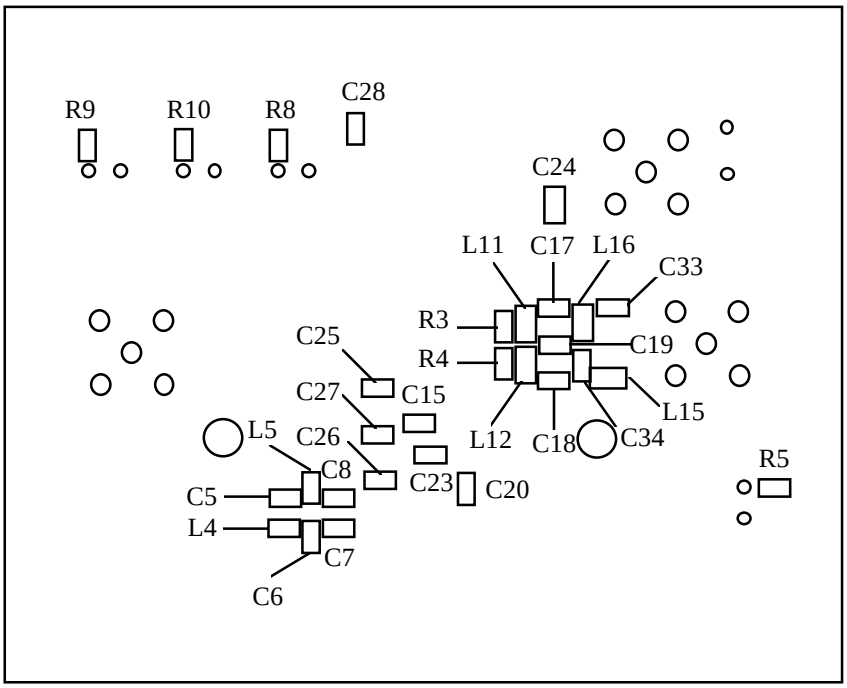


Fig. 35 UAA2073XM Demo Board - Layer 2 Assembly

8. REFERENCES

[1] UAA2072M Image rejecting front-end for GSM applications
Datasheet - November 94

[2] UAA2073M Image rejecting front-end for GSM applications
Datasheet - 07 December 95

[3] UAA2073AM Image rejecting front-end for GSM applications
Datasheet

[4] UAA2077AM Image rejecting front-end for DECT applications
Datasheet -04 July 96

[5] UAA2077BM 2 GHz Image rejecting front-end
Datasheet - 09 January 96

[6] UAA2077CM 2 GHz Image rejecting front-end
Datasheet

[7] OM5045 DECT Radio Design
Application note (report n°AN95096) - 31 October 1995