APPLICATION NOTE

Application of the CGY2030M power amplifier

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Abstract

The CGY2030M is a monolithic GaAs power amplifier for transmission DECT applications.
This report contains a description including the power amplifier ,the switching circuit and the operation modes.

APPLICATION NOTE

APPLICATION OF THE CGY2030M POWER AMPLIFIER

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Summary

This report is intended to provide support for designing power amplifier for DECT applications.

It contains a description of the power amplifier as well as a brief overview of interstage and input /output matching .

An application example of the CGY2030M is given by means of board description for testing ,recommendations for use ,measurement results ,and performances.

Some explanations concerning the self biasing specificity of this circuit are also available in the document.

CONTENTS

LIST OF FIGURES

1. INTRODUCTION

This note describes the application of RF monolithic GaAs device in plastic SMD packages for DECT power amplifier.

Their main features are:

-low cost

-100% SMD

-high performance

-low voltage operation

-possible operation without negative bias for the gates

2. PINNING

The pinning is shown in Fig.1.

SYMBOL	PIN	DESCRIPTION
VGG2	1	fourth stage gate bias input voltage
GND	2 to 4	ground
VDD2	5	drain second stage and supply
GND	6 and 7	ground
VDD1	8	drain first stage and supply voltage 1
RFI	9	PA input
VGG1	10	first second and third stages gate bias input voltages
GND	11 and 12	ground
VDD3	13	drain third stage and supply voltage 3
GND	14 and 15	ground
RFO/ VDD4	16	PA output and supply voltage 4

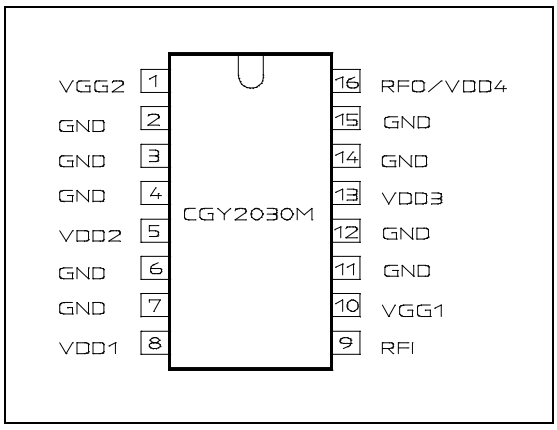

Fig. 1 Pin configuration

3. CIRCUIT DESCRIPTION

3.1 Power amplifier

The amplifier is based on a monolithic integrated four stages device using GaAs FET technology in a plastic package.
This device is able to deliver 27 dBm with 3.2 V drain operation.
As briefly described in Fig.2. this device exhibits inter stage matching circuits implemented simultaneously both on board and in the package on chip.Each matching consists of a series,parallel combination of elements.The series elements are generally capacitive (MIM capacitors on chip) while the parallel ones can be inductive or capacitive.Further more the parallel matching networks include a bias path for the drains of the different stages.
The input and output matching circuits are implemented on board.
When built on a low cost printed circuit board ,the amplifier is associated with a switching circuit for pulsed applications.This one provides the suitable ramping and switching time for DECT applications.

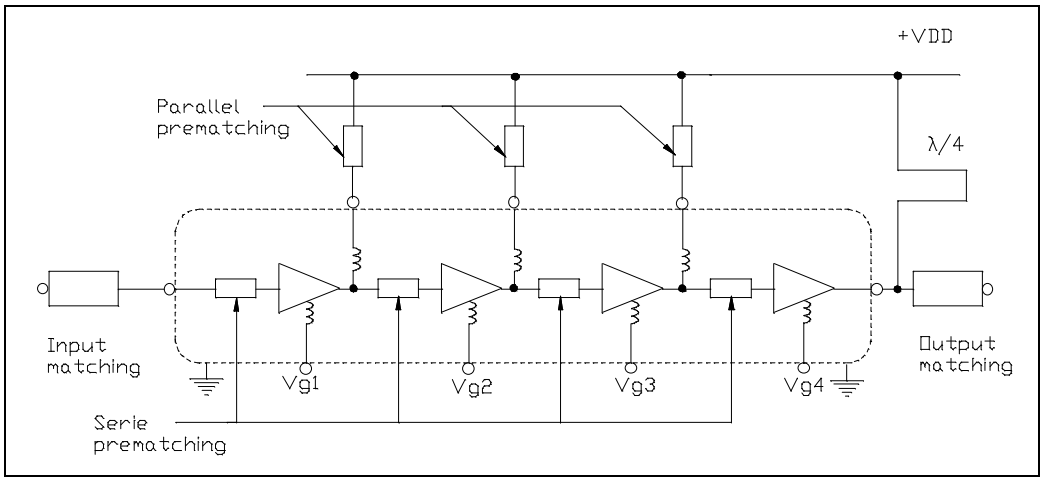

Fig. 2 Power amplifier

3.2 Interstage matchings

The general philosophy used for interstage matching is described when looking at the Fig.3.

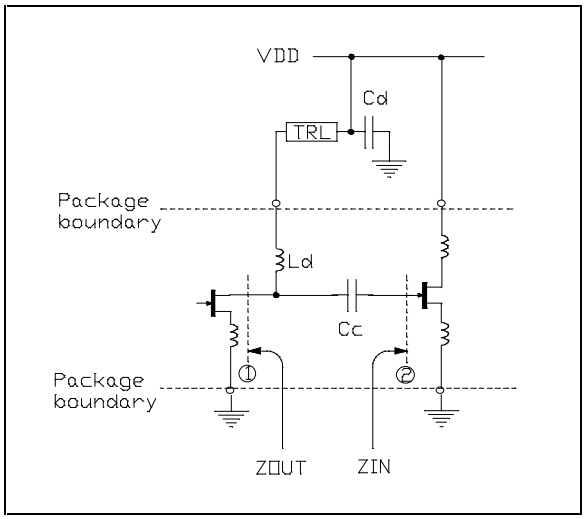

Fig. 3 Interstage matching

The aim is to match the input impedance Zin from a stage in the reference plane 2 to the output impedance Zout of the previous one in the reference plane 1.
This can be accomplished with the interstage coupling capacitor Cc(MIM) on chip ,the bonding wire between the drain and the package lead ,the external transmission line TRL and the decoupling capacitor Cd.
The only parameters that can be tuned are external to the package because Ld (bonding wire) and Cc are fixed values that cannot be adjusted.
As Zin ,Zout are known by simulation with enough accuracy ,it is relatively easy to adjust Cd and TRL (width and length) for a perfect matching between Zin and Zout.

3.3 Drain switching circuit

When used in DECT applications the power amplifier needs to be switched on and off by means of external series bipolar or MOS transistors.
For this purpose we use a double switch as described in Fig.4.

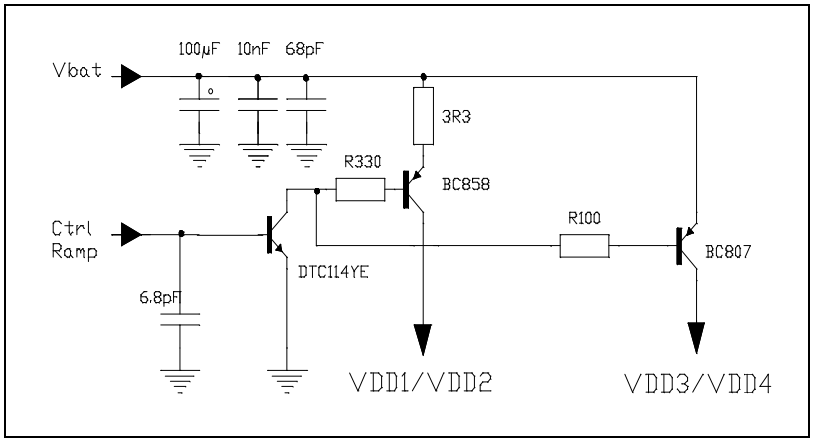

Fig. 4 Drain switching circuit

The reason why we use two PNP bipolar transistors (one for the first two stages and one for the last two ones) is that ,in order to avoid transient high peak current and to insure smooth power ramp-up , the two last stages must be switched on with some delay with respect to the first two ones.
This is accomplished with separated switches and with different time constants for the first and second stages on one hand and for the third and fourth stages on the other hand.
To understand how this delay can be introduced ,let's consider the equivalent circuit of one switch in Fig.5

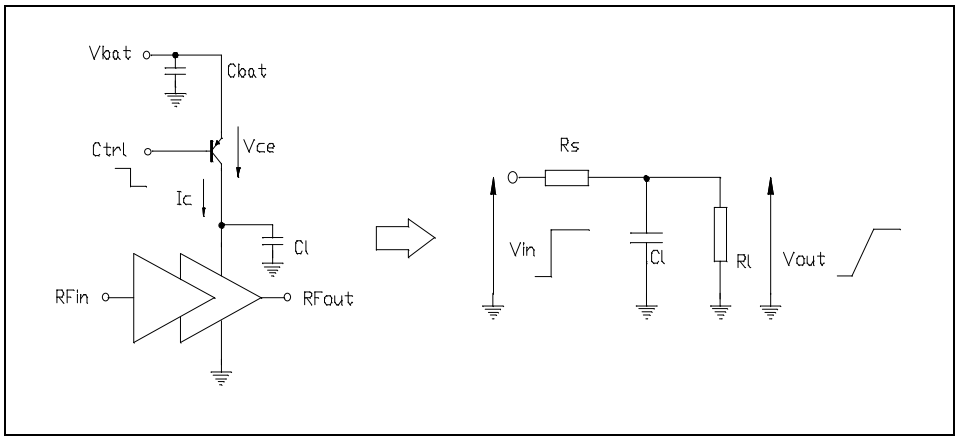

Fig. 5 Drain switching equivalent circuit

-Rl is the non linear load resistance induced by two stages of the power amplifier when these ones are switched on.
The instantaneous value of Rl (versus time) depends on the ratio V/I present on the drains of this stages.
In a first approach we will only consider the final values of V and I for calculations.
-Rs is also a non linear source resistance introduced by the switch and is approximately the ratio between Vce and I.
We will also consider the final values Vcesat and I for calculations.
-Cl is the integrating capacitor introducing the different time constants between the two last stages and the first ones.
As Rl is much larger than Rs ,we can consider that td≅(tr2-tr1)≅2.2(Cl2-Cl1) where td is the time delay to establish the drain voltage ;tr1 ,tr2 are the rise times and Cl1 ,Cl2 the integrating capacitors of the two parts of the amplifier.In that way td is approximately 22 nS.
This time delay is high enough to get the last stages already self biased before their supply voltage has reached its steady state value and in turn no extra peak current or any power overshoot can take place within the ramp-up.
A simpler drain switching circuit can be used if the amplifier is operated with negative bias at pins VGG1 and VGG2.

4. MODE OF OPERATION

Two operation modes are possible depending on the nature of the power control.

4.1 Mode 1:without negative bias

In this mode the four stages of the power amplifier are self biased with the incoming RF signal (see Fig.6).

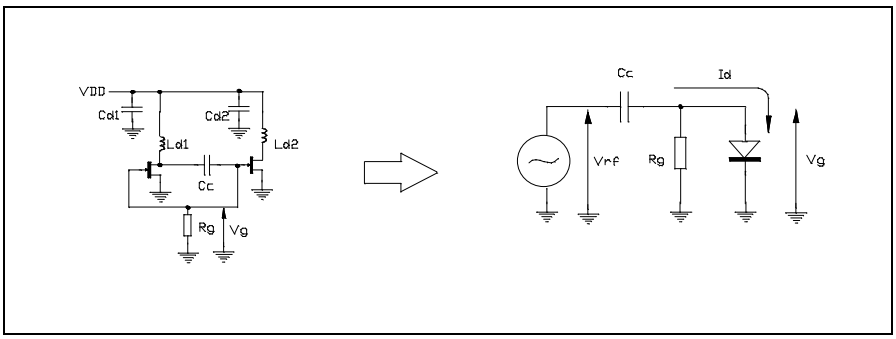

Fig. 6 Self biasing equivalent circuit

As the gates are return to ground via resistors ,when a RF signal is applied ,and if the level of this one is high enough ,a DC detected current takes place in the gate source junction.This current charges the interstage coupling capacitor Cc and in turn a DC average voltage will appear gradually across the gate source junction ,starting from zero to a negative value within the few first periods of the RF signal.When the absolute maximum value of the signal (RF+DC) is less than 0.7V (Vgson) a steady state is established because ,as the detected signal is no longer existing ,the coupling capacitor stops charging.
Once the steady state is reached ,the DC component of the signal at the gate terminal will bias negatively this one and his value will depend on the time constant Rg*Cc and the RF level.
As the power control cannot be achieved by any supply variations ,this mode of operation is only suitable for applications where power control is not required such as DECT.

4.2 Mode 2:with negative bias

This mode of operation is possible when a negative bias is available.
In that case ,adequate negative bias are applied to gates via pins VGG1 and VGG2.
Generally VGG1 biases the first three stages more in class A while VGG2 bias the last one more in class AB for a better compromise between power gain and efficiency.
This mode of operation is necessary when higher level of linearity is required.
As the internal bias no longer depends on the incoming RF level the power control is now possible by variation of the supply voltage.

5. GENERAL CHARACTERISTICS

CONDITIONS:

VDD=3.2V-F=1900MHz-Tamb=25°C-Pulse width=2.5mS-Duty cycle=25%-Pin=0dBm

CHARACTERISTICS	MIN	TYP	MAX	CONDITIONS	UNITS
Measured in mode 1 ;without negative bias-VGG1 and VGG2 connected to ground					
Supply current		400	500		mA
Rf output power	26	27	28.5		dBm
DC to RF efficiency		40			%
Output RF leakage in off state		-40		VDD=0V	dBm
Harmonic level		-35			dBc
Spurious level		-60		Load VSWR=6:1 through all phases	dBc
Load mismatch	No degradation			Pload=27dBm VSWR=6:1	
Measured in mode 2 ;with negative bias at pins VGG1 and VGG2 ;VGG1=-1.2V-VGG2=-2V					
RF output power	25.5	26	28		dBm
DC to RF efficiency		35			%
Output Rf leakage in off state		-50		VDD=0V	dBm
Total gate current	-1		1		mA

6. CIRCUIT DIAGRAM AND RECOMMENDATIONS FOR USE

6.1 Circuit diagram

The circuit diagram used for testing is described in Fig.7

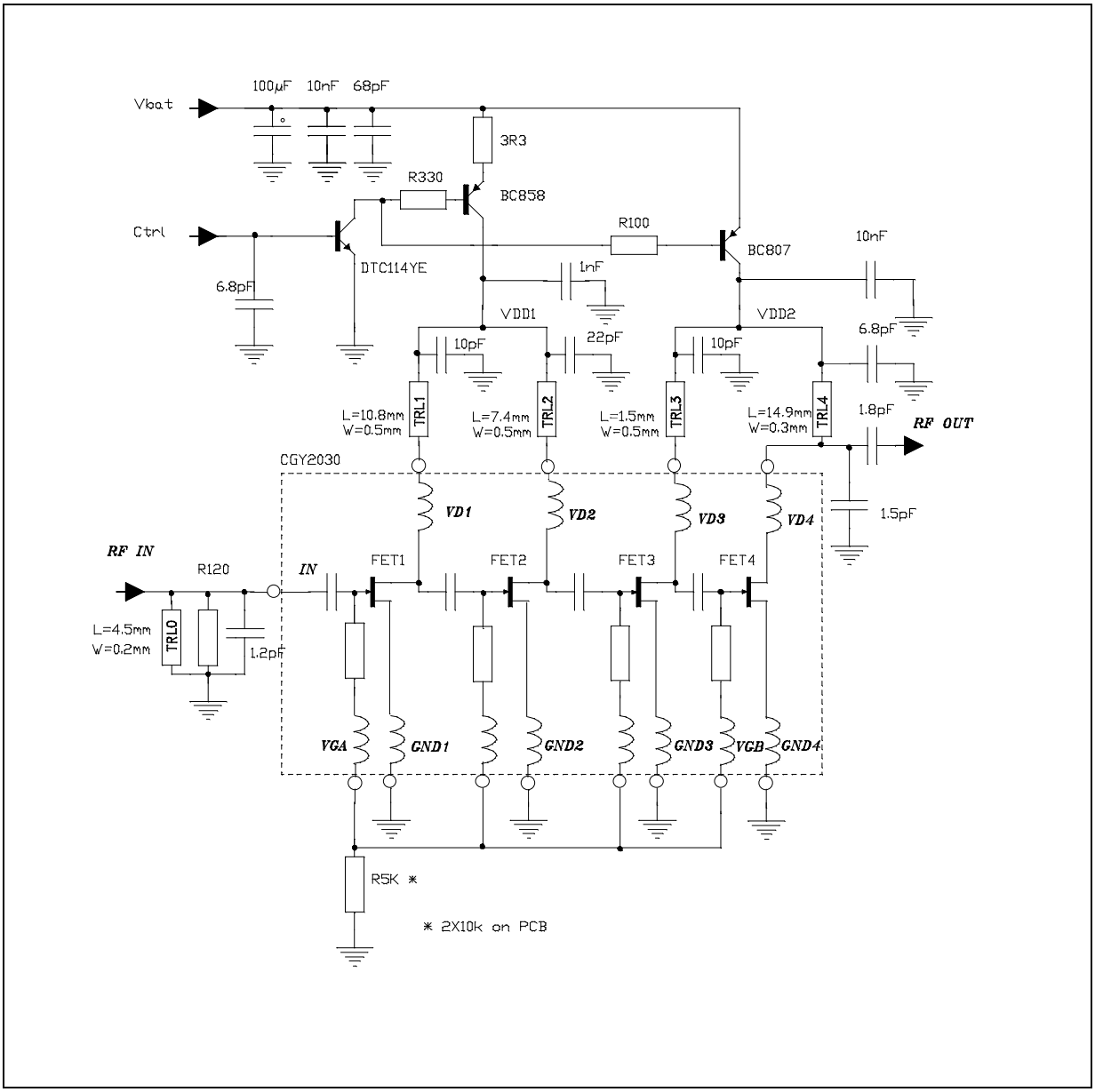

Fig. 7 Circuit diagram

6.2 Recommendations for use

Mode1 operation:
When used without negative biasing voltage applied on pin VGG1 and VGG2 ,the power amplifier is self biased with the incoming signal.
In order to prevent the device from destruction ,apply first the RF signal to pin Rfin ,then apply the switching signal to pin Ramp once Vbattery is present.

Mode2 operation:
When negative biasing is used ,apply first the negative voltages to VGG1 (typically -1.2V) and to VGG2 (typically -2V) prior the drain voltage.

7. PRINTED CIRCUIT BOARD LAYOUT-LIST OF COMPONENTS

7.1 Circuit layout.

The demoboard layout is given in Fig.8.
The characteristics of the substrate in use for the PCB are as following:
-substrate type:FR4 triple clad (the central layer is used as the reference ground plane).
-Relative permetivity:εr=4.7
-Thickness:H=2x0.8mm
-Size:40x45mm

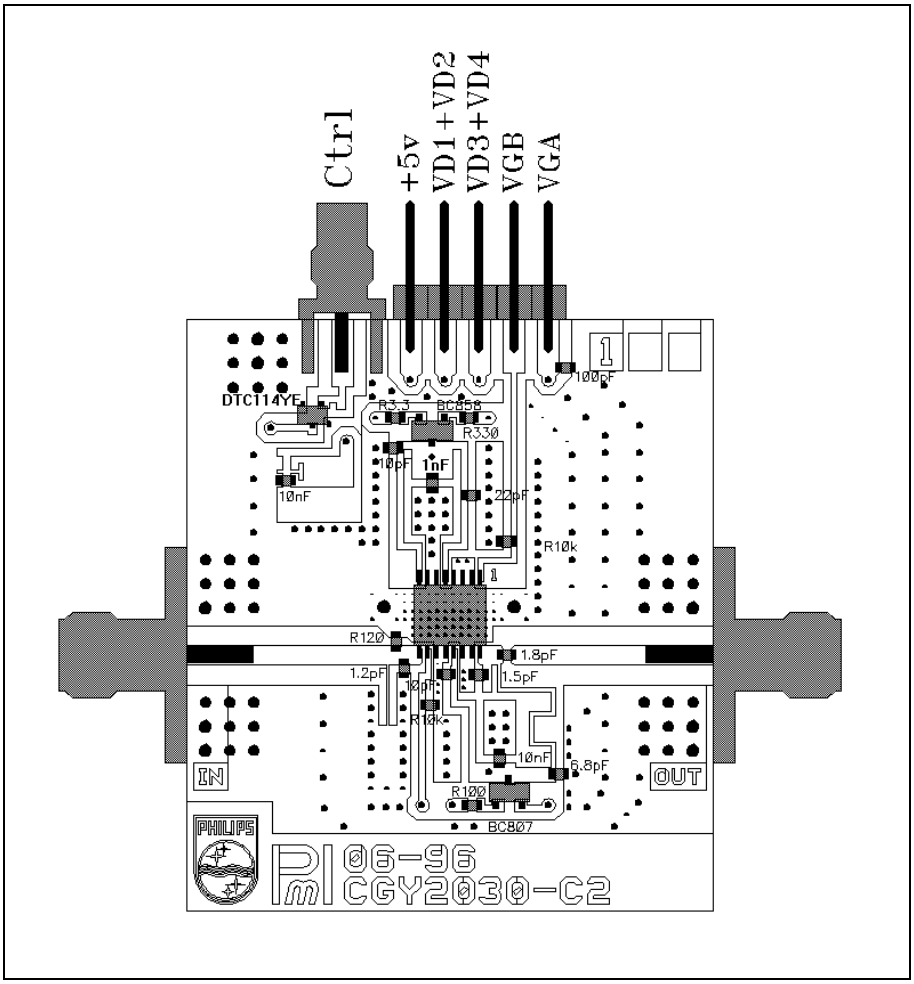

Fig. 8 Circuit layout

7.2 Part list DECT power amplifier.

CAPACITORS (Size:0603)	
VALUE	**NUMBER**
1.5 pF	1
1.2pF	1
1.8 pF	1
6.8 pF	3
10 pF	2
22 pF	1
68 pF	1
1nF	1
10 nF	2
100 µF	1

RESISTORS (Size:0603)	
VALUE	**NUMBER**
3.3 Ω	1
100Ω	1
120	1
330Ω	1
10kΩ	2

TRANSISTORS	
TYPE	**NUMBER**
DTC114YE	1
BC807	1
BC858	1

TRANSMISSION LINES (PCB)		
NAME	**WIDTH(µm)**	**LENGTH(µm)**
TRL0	200	4500
TRL1	500	10800
TRL2	500	7400
TRL3	500	1500
TRL4	300	14900

8. THERMAL CHARACTERISTICS/POWER DISSIPATION CONSIDERATIONS

8.1 Thermal Characteristics

The device is capable of a maximum average power dissipation of Ptot= 400 mW up to a channel temperature not exceeding Tch= 150°C
The thermal resistance from channel to ambient in free air is typically Rth j-a= 145 K/W.
In consequence ,as the formula to calculate the channel temperature is Tch= (Pl/Eff-Pl) x δ x Rth j-a + Tamb we can determine the channel temperature Tch, knowing all other parameters

8.2 Channel temperature calculation /Maximum duty cycle

If we want to calculate Tch with the following parameters:
Ptot = 400 mW
Eff = 40%
Pl = 500 mW
δ = 10%
Rtlj-amb= 145 kW
Tamb= 50°C
With formula we get:
Tch= (0.5/0.4 -0.5) X 0.1 X 145 + 50
Tch= 60.88 C°
In a same way, using the formula, we can determine what is the maximum duty cycle allowed for not exceeding the maximum channel temperature of 150°C for a given ambient temperature.

8.3 Power derating curve

For safety and reliability reason we can draw a derating curve concerning the power dissipation versus ambient temperature (See Fig 9).

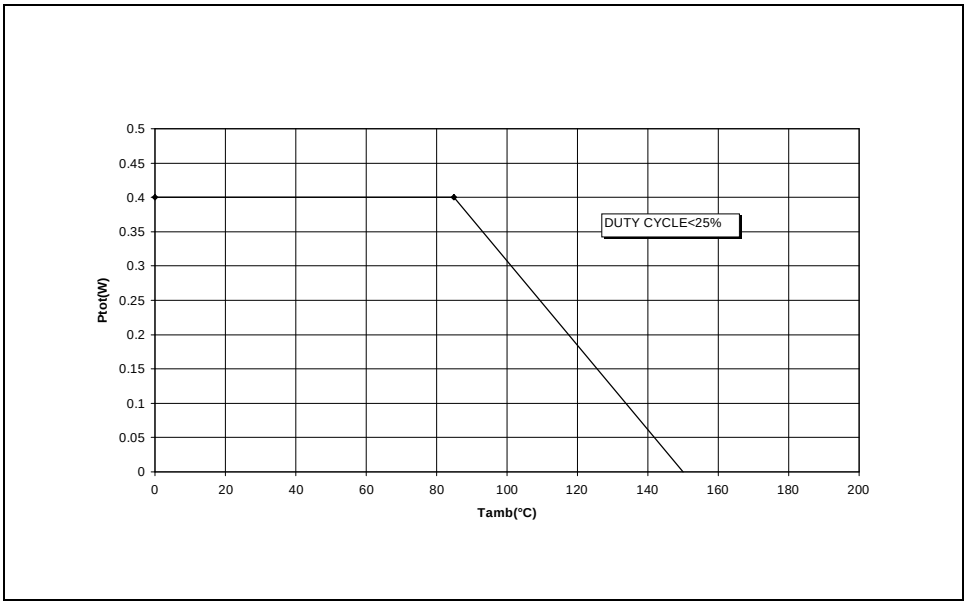

Fig. 9 Power derating

9. ELECTRICAL CHARACTERISTICS

9.1 Output power and efficiency as a function of drain voltage

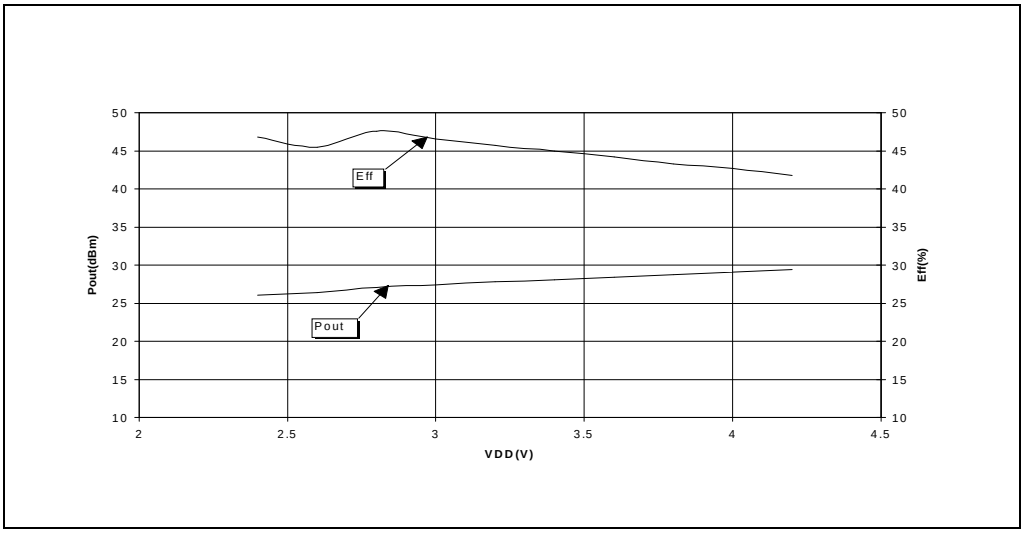

Fig. 10 Output power/efficiency versus drain voltage

9.2 Output power and efficiency as a function of frequency

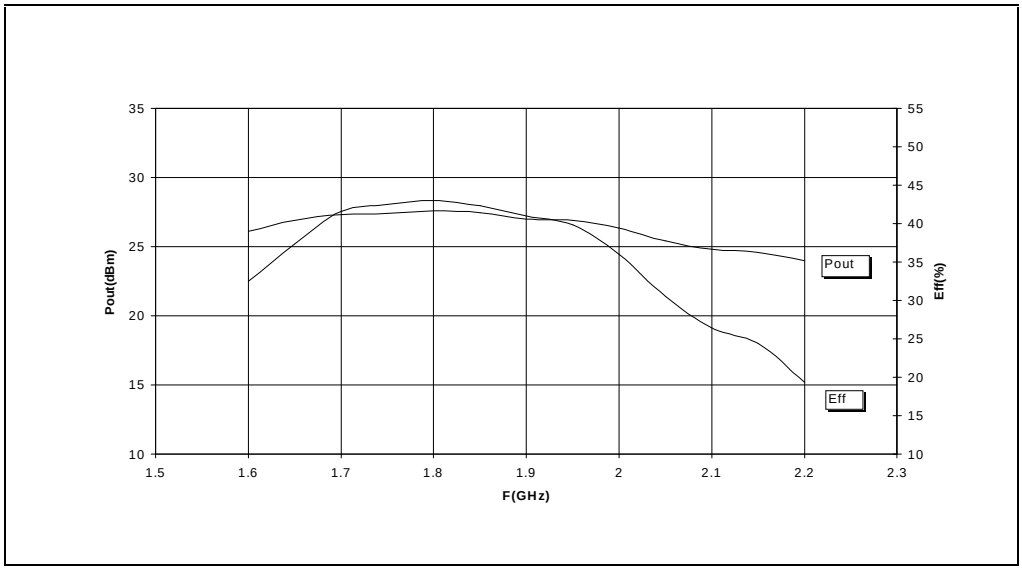

Fig. 11 Output power/efficiency versus frequency

9.3 Harmonics

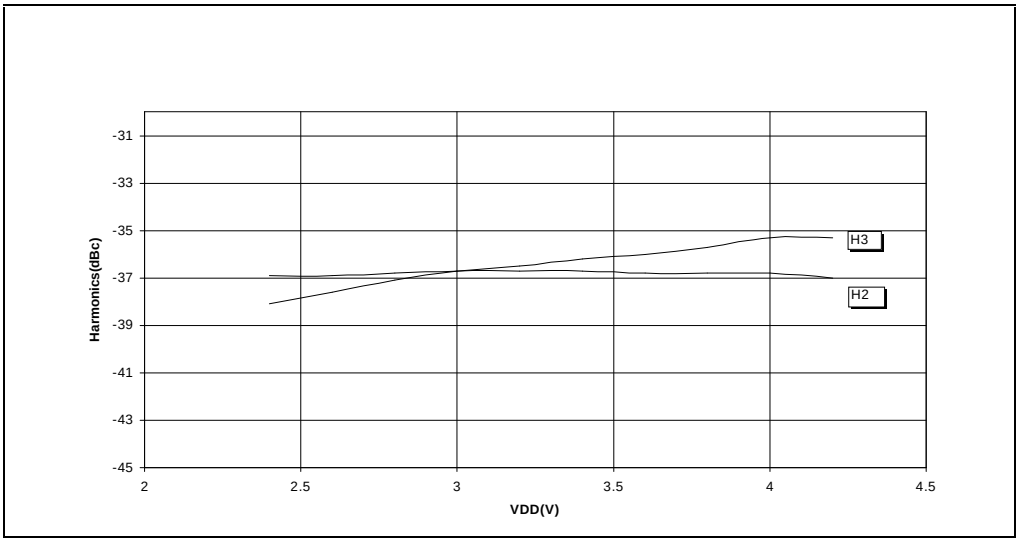

Fig. 12 Harmonics versus drain voltage

9.4 Temperature dependency

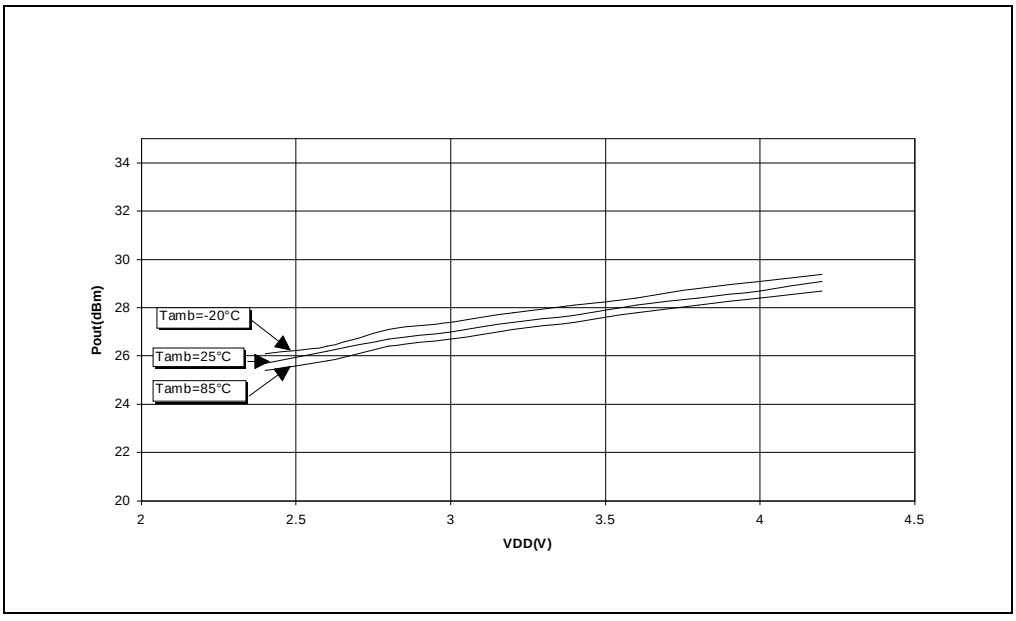

Fig. 13 Temperature dependency