APPLICATION NOTE

Fiber optic transceiver demo board STM16 OM5801

AN96051

Philips
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Application Note

Abstract

The STM16 fiber optic frontend chipset is capable of transmitting and receiving 32 digital channels simultaniously over one fiber optic link. The low side datarate is 78 Mbps, the high side datarate is 2448 Mbps.

The chipset consists of a multiplexer, laserdriver, transimpedance amplifier, main amplifier, clock recovery, clock multiplier and demultiplexer. The main advantage of the chipset is the use of Current Mode Logic interface for the high rate channels. This guarentees low power consumption combined with high interference immunity. Furthermore the chipset has a built in loop capability: received signals can directly be fed to the laser driver, and multiplexed signals can directly be demultiplexed. This feature simplifies testing during production and maintenance.

The demoboard can be used for system and IC evaluation. Additional guard circuits for operational conditions have been implemented.

INTRODUCTION

This application note describes the use of the Philips' STM16 chipset. First general items are discussed, interfaces are described. After this, the functional blocks are discussed. Finally the evaluation results of key characteristics of the board are given. The schematics, layout, partslist, manufacturer data and the lenghts of critical lines are given in the appendices. Also the use of Current Mode Logic is explained in an appendix.

Contents

1. General

1.1 Goal

The demoboard has been designed to demonstrate the capability of the Philips' STM16 chip set, designed for SDH or SONET systems, bitrate: 2.5 Gbps. The board has been set up such that individual evaluation of each IC is possible, with an exception for the transimpedance amplifier.

No attempts have been made to design advanced *peripheral* circuitry:

- The power supplies are therefore simple, discrete DC voltage regulators.
- Standard a temperature stabilized laser must be mounted. A Peltier temperature stabilizing loop is included. Modulation control is a fixed setting.
- A laser bias control is included.
- A simple 2 state photo diode guard circuit is included in the board.
  The transition voltage and -current can be adjusted.

1.2 Acronyms

- If a text is placed between quotes, this text is placed on layer 1 (top) of the demoboard.
- On all places where STM16 (SDH) also OC48 (SONET) can be read
- 19 MHz 19,440 kHz
- 19 Mbps 19,440 kbps
- 2.5 GHz 2,488,320 kHz
- 2.5 Gbps 2,488,320 kbps
- 2G5 2.5 GHz
- 39 MHz 38,880 kHz
- 39 Mbps 38,880 kbps
- 78 MHz 77,760 kHz
- 78 Mbps 77,760 kbps
- AGC Automatic Gain Control
- AGC Automatic Gain Control, signal output
- AGCDC Automatic Gain Control, reference output
- ALS Automatic Laser Shutdown
- APD Avalanche Photo Diode
- BTL Backplane Transceiver Logic
- BW Bandwidth
- Buf Buffer
- CLK Clock
- CML Current Mode Logic
- CREF Reference clock
- Conv Converter (for conversion of 622 MHz clock to 2.5 GHz)
- Cu Copper

- DCR Data and Clock Recovery
- EL Electrical
- EXT External
- ITU International Telecommunication Union
- JUMA Jumper A
- JUMB Jumper B
- JUMC Jumper C
- LAB Buffered laser output
- LAQ Inverted laser output
- LDR Laser driver
- LOS Los Of Signal (main amplifier), signal output
- LOSDC Los Of Signal (main amplifier), reference output
- MS Microstrip
- MUX Multiplexer
- N4V5 -4.5 Volt
- N6V5 -6.5 Volt
- OP Optical
- Op1 Optical connector no. 1 (Output)
- Op2 Optical connector no. 2 (Input)
- P3V3 +3.3 Volt
- P5V +5 Volt
- PCB Printed Circuit Board
- PLL Phase Locked Loop
- PRBS Pseudo Random Bit Sequence
- RCV Receiver
- REF Reference
- RF Radio Frequency, in this document 2.5 Gbps data 2.5 GHz clock signals
- SDH Synchronous Digital Hierarchy
- SMD Surface Mount Devices
- SONET Synchronous Optical Networks
- STM16 Synchronous Transport Module no. 16
- TRL Transmission Lines
- TTI Transistor buffered Transimpedance output
- TTL Transistor Transistor Logic
- Te Ternary
- Transimp Transimpedance
- bps bits per second

1.3 Layout considerations

- The layout for the demoboard is designed on a 8 layer PCB. The layers are 35 micrometer thick, the space between two layers is 0.2 ± 0.02 mm, the thickness of a carrier layer is 0.2 ± 0.038 mm. The material is FR4, with a relative dielectric constant is 4.3. No buried vias are used. The used layout process has an underetching for all but outer layers of 20 micrometer. The use of layers is ordered as follows:

layer 1	Signal; Microstrip transmission lines (Single ended: 1 mm width; Coupled: 0.35 mm width / 0.15 mm spacing)
layer 2	Signal; Local ground; Where microstrip transmission lines are placed on layer 1: nothing
layer 3	Global ground. At RF parts no thermal releases are used
layer 4	VEE (N4V5); Signal; Where triplate transmission lines are placed on layer 5: nothing
layer 5	Triplate transmission lines (Single ended: 0.3 mm; Coupled: 0.25 mm width / 0.25 mm spacing)
layer 6	VCC (P5V; P3V3). Where triplate transmission lines are placed on layer 5: nothing
layer 7	Global ground. At RF parts no thermal releases are used
layer 8	Signal

  A schematic view is drawn on the next page.

- The microstrip transmission lines and triplate transmission lines are guarded with vias, to enhance interference immunity. The spacing is 1 mm minimum between line and via. No thermal releases were made in this vias.
- All positive power lines and ground are 1 mm wide. All negative power lines 2 mm.
  The width has also been used for those lines on layer 1 and 8.
- The RF decoupling capacitors are placed as close as possible to the ICs.
- The loading of the ICs has been layed out as symmetrical as possible.
- Whenever necessary the 50 ohms lines were placed in the triplate layer.
- The SMA connectors have been placed with a 20 mm centre distance apart from each other.
  This gives enough space to properly connect the SMA connectors with a torque key.

1.4 Optical components

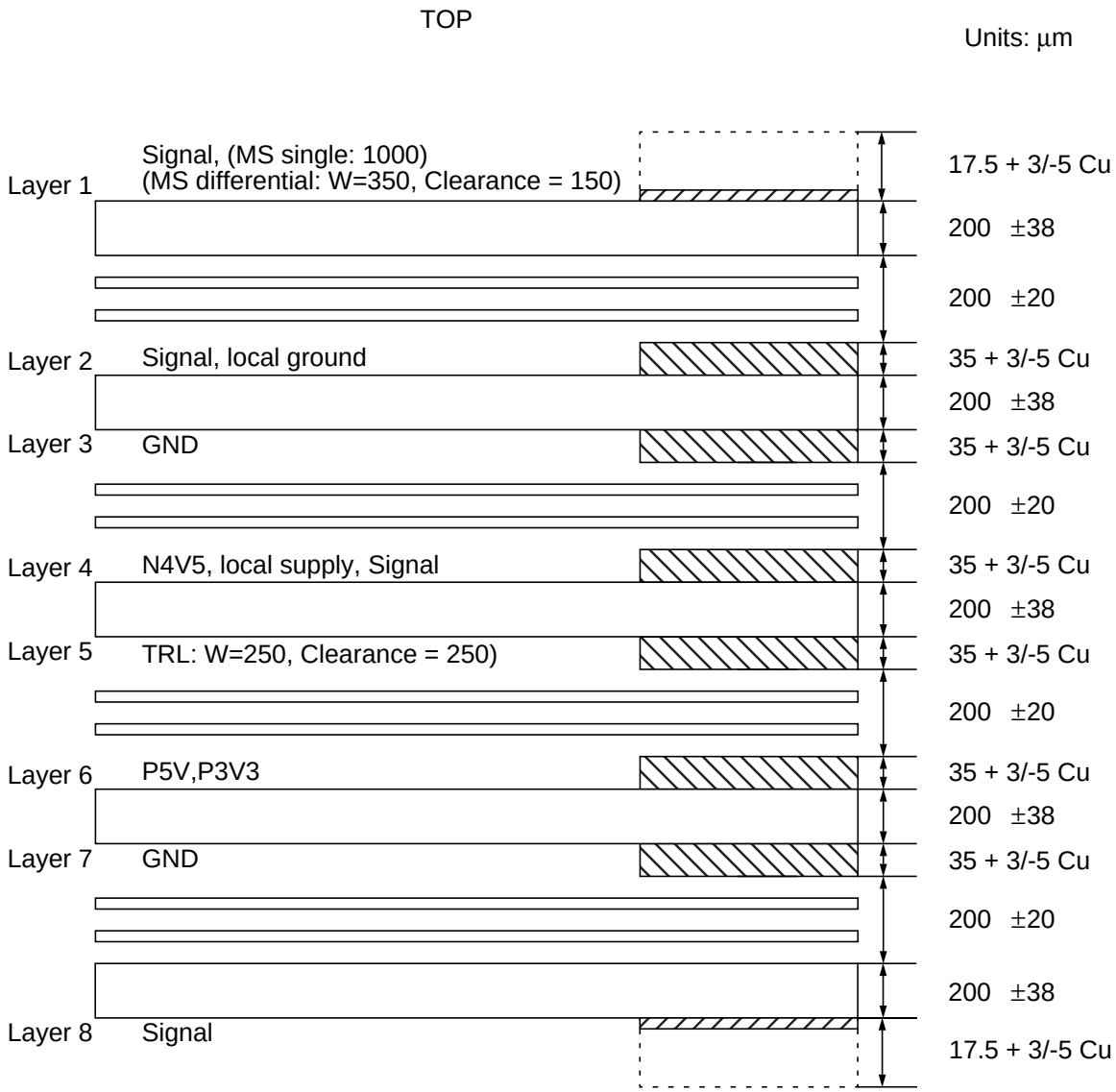
Standard, the board is delivered with a 1550 nm Distribueted Feedback (DFB) Laser and Ternary avalanche diode. The manufacturer and type numbers are:

Laser: Philips Optoelectronics Centre - CQF910/D
Diode: ATT- ATT 127E

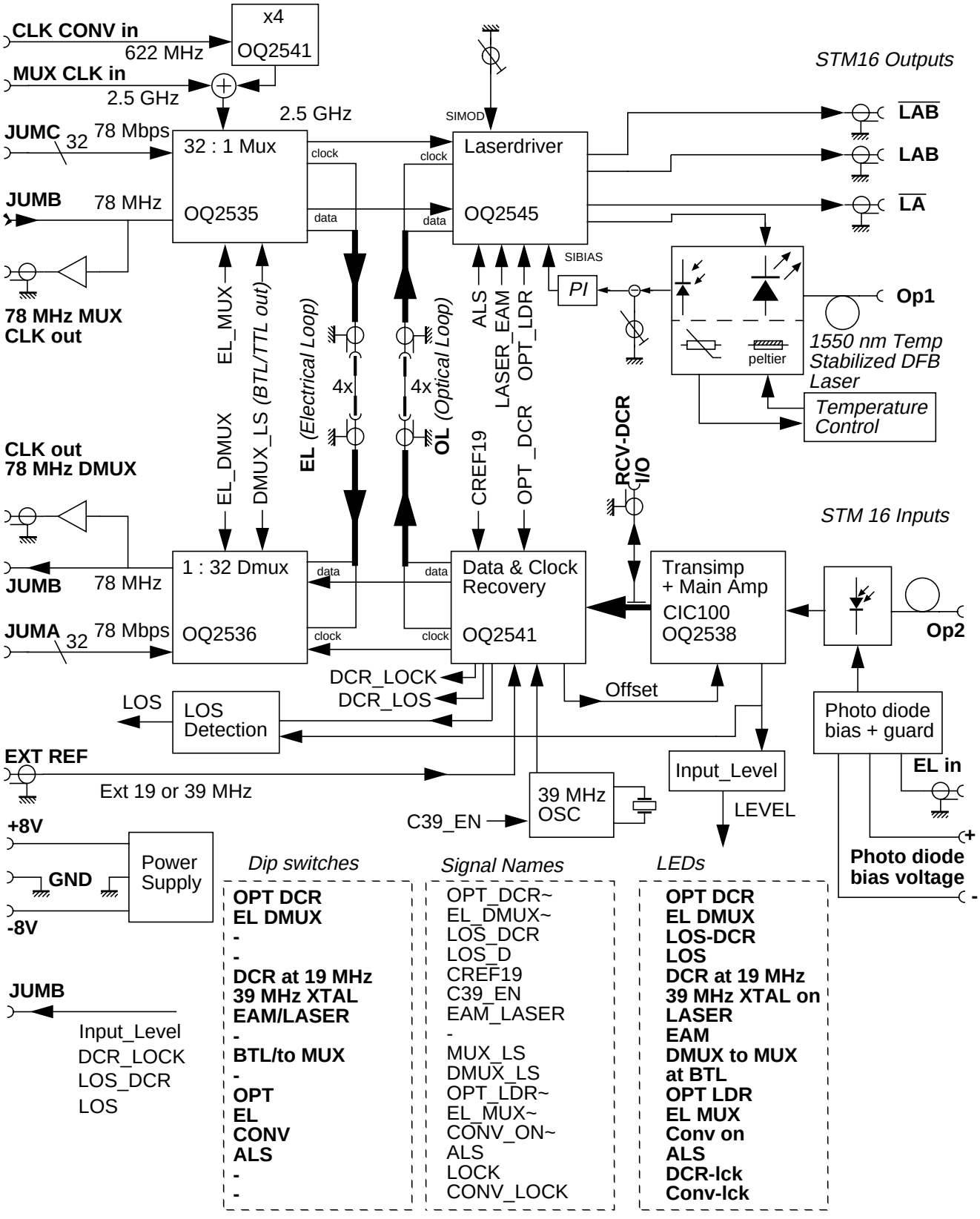
1.5 ITU recommendations

ITU recommendations G.957 and G.958 apply to the chipset described in this document.

Build up of multilayer PCB



FUNCTIONAL BLOCK DIAGRAM STM16 DEMOBOARD Application Note



2. Interface

2.1 Interface description list

TABLE 1 SMA Connectors

Name	Portno.	Netname	I/O	Description
EL-CLK-OUT	ST621	EL_CLK_OUT	O	Electrical loop clock output, CML
$\overline{\text{EL-CLK-OUT}}$	ST622	EL_CLK_OUT~	O	Electrical loop clock output, CML, inverted
EL-DATA-OUT	ST623	EL_DATA_OUT	O	Electrical loop data output, CML,
$\overline{\text{EL-DATA-OUT}}$	ST624	EL_DATA_OUT~	O	Electrical loop data output, CML, inverted
EL-CLK-IN	ST625	EL_CLK_IN	I	Electrical loop clock input, CML
$\overline{\text{EL-CLK-IN}}$	ST626	EL_CLK_IN~	I	Electrical loop clock input, CML, inverted
EL-DATA-IN	ST627	EL_DATA_IN	I	Electrical loop data input, CML
$\overline{\text{EL-DATA-IN}}$	ST628	EL_DATA_IN~	I	Electrical loop data input, CML, inverted
OL-CLK-OUT	ST631	OL_CLK_OUT	O	Optical loop clock output, CML
$\overline{\text{OL-CLK-OUT}}$	ST632	OL_CLK_OUT~	O	Optical loop clock output, CML, inverted
OL-DATA-OUT	ST633	OL_DATA_OUT	O	Optical loop data output, CML
$\overline{\text{OL-DATA-OUT}}$	ST634	OL_DATA_OUT~	O	Optical loop data output, CML, inverted
OL-CLK-IN	ST635	OL_CLK_IN	I	Optical loop clock input, CML
$\overline{\text{OL-CLK-IN}}$	ST636	OL_CLK_IN~	I	Optical loop clock input, CML, inverted
OL-DATA-IN	ST637	OL_DATA_IN	I	Optical loop data input, CML
$\overline{\text{OL-DATA-IN}}$	ST638	OL_DATA_IN~	I	Optical loop data input, CML, inverted
I/O	ST642	RCV_DCR_I_O	I/O	Attenuated path signal-path RCV-DCR
$\overline{\text{I/O}}$	ST641	RCV_DCR_I_O~	I/O	Attenuated path signal-path RCV-DCR
$\overline{\text{LA}}$	ST651	LA~	O	Inverted laser driver output
LAB	ST652	LAB	O	Buffered laser driver monitor output
$\overline{\text{LAB}}$	ST653	LAB~	O	Buffered laser driver monitor output, inverted
78 MHz DMUX CLK out	ST661	C78R_BTL	O	Received 78 MHz clock - 50 ohm source
78 MHz MUX CLK out	ST662	C78T_BTL	O	Transmit 78 MHz clock - 50 ohm source (Derived from Mulitplexer/converter clock)
EXT REF	ST671	CREF	I	External 19 MHz or 38 MHz reference clock for DCR
EL in	ST672	EL_IN	I	Electrical input
Conv in	ST673	CLK_CONV_IN	I	Converter clock(622 MHz)
MUX CLK in	DT674	CMUX_IN	I	Multiplexer clock (2.5 GHz)

TABLE 2 Dipswitches and LEDs

Dipswitch	Line	LED no	LED name	Colour	Description
OPT DCR	OPT_DCR~	OT611	OPT DCR	Yellow	DCR in optical loop mode
EL DMUX	EL_DMUX~	OT612	EL DMUX	Yellow	DMUX in electrical loop mode
-	LOS_DCR	OT622	LOS-DCR	Red	LOS detected by DCR
-	LOS_D	OT621	LOS	Red	LOS detected by main RCV
DCR at 19 MHz	CREF19	OT632	DCR at 19 MHz	Yellow	DCR is in 19 MHz reference clock mode

TABLE 2 Dipswitches and LEDs

Dipswitch	Line	LED no	LED name	Colour	Description
39 MHz XTAL	C39_EN	OT631	39 MHz XTAL on	Yellow	Board crystal oscillator is on
EAM/LASER	EAM_LASER	OT642	LASER	Yellow	LDR in in Laser mode
-	-	OT641	EAM	Yellow	LDR is in EAM mode
BTL/to MUX	MUX_LS	OT651	DMUX to MUX	Yellow	Enables MUX/DMUX communication possiblitie (amplitude only, needs extra level shift)
	DMUX_LS	OT652	at BTL	Yellow	DMUX is in 'BTL' mode
OPT	OPT_LDR~	OT601	OPT LDR	Yellow	LDR is in optical loop mode
EL	EL_MUX~	OT602	EL MUX	Yellow	MUX is in electrical loop mode
CONV	CONV_ON~	OT603	Conv on	Yellow	Clock converter is enabled
ALS	ALS	OT604	ALS	Yellow	Automatic Laser shutdown is enabled
-	LOCK	OT623	DCR lck	Green	DCR is in lock
-	CONV_LOCK	OT624	Conv lck	Green	Clock convertor is in lock

TABLE 3 I/O Jumpers

Name	Portno	Line	Level	Description
JUMA1	ST601	D_C78RBUS	BTL	Received data, bits 0-7
JUMA2	ST602	D_C78RBUS	BTL	Received data, bits 8-15
JUMA3	ST603	D_C78RBUS	BTL	Received data, bits 16-23
JUMA4	ST604	D_C78RBUS	BTL	Received data, bits 24-31
JUMB	ST609	LEVEL LOS_DCR LOS_D LOCK C78TB C78RB	Analog TTL TTL TTL TTL TTL	Input level detektor (main amp) output signal. Buffered Loss of signal from DCR Loss of signal from RCV Lock output DCR 78 MHz transmitted data clock 78 MHz received data clock
JUMC1	ST605	D_C78TBUS	TTL	Transmitted data, bits 0-7 (threshold input comperators 1.5 V)
JUMC2	ST606	D_C78TBUS	TTL	Transmitted data, bits 8-15 (threshold input comperators 1.5 V)
JUMC3	ST607	D_C78TBUS	TTL	Transmitted data, bits 16-23 (threshold input comperators 1.5 V)
JUMC4	ST608	D_C78TBUS	TTL	Transmitted data, bits 24-31 (threshold input comperators 1.5 V)

TABLE 4 Control jumpers/PADs

Portno	Name	Description
ST212	RCV-DCR bias	Closing this jumper will close the bias loop of RCV and DCR. ST202 should be left open.
ST213	RCV bias	Closing this jumper will close the bias network at the receiver. ST201 should be left open.
ST281	5V Diode bias	5V bias enabling Enables the use of 5 V for photo diode bias. The APD bias voltage input pins should be left open

TABLE 4 Control jumpers/PADs

Portno	Name	Description
R820	Laser bias	Laser bias adjustment. By adding a resistor to this point, the laser bias current can be controlled
R857	Laser modulation	Laser modulation adjustment. By adding a resistor to this point, the laser modulation current can be controlled.

TABLE 5

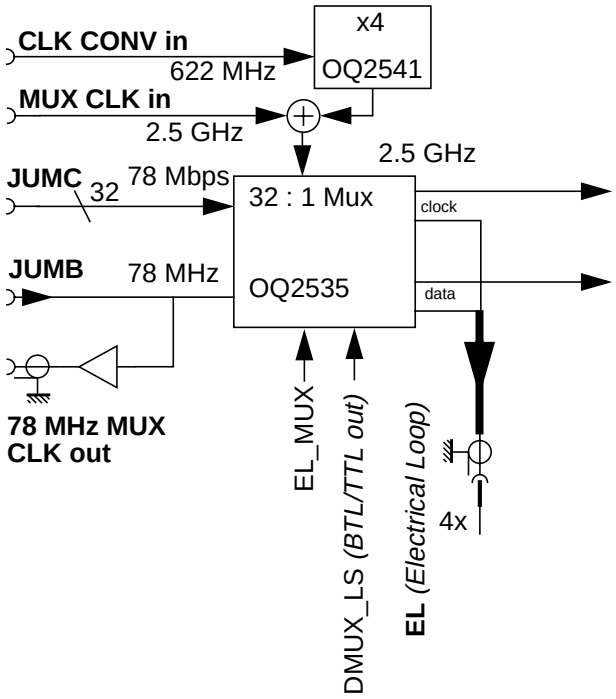
M-no.	Voltage, signal	Description
M1	P8V	+8 V
M2	N8V	-8 V
M11	P5V	+5 V
M12	P5V	+5 V
M13	P5V	+5 V
M14	P5V	+5 V
M15	P8V	+8 V
M21	P3V3	+3.3 V
M22	P3V3	+3.3 V
M24	P3V3	+3.3 V
M25	P8V	+8 V
M31	N4V5	-4.5 V
M32	N4V5	-4.5 V
M33	N4V5	-4.5 V
M34	N4V5	-4.5 V
M35	N4V5	-4.5 V
M41	N6V5	-6.5 V
M42	N6V5	-6.5 V
M43	N6V5	-6.5 V
M44	N6V5	-6.5 V
M45	N6V5	-6.5 V
M202		REF (pin 21) Main Amplifier
M203		IC202 (pin 1), differential amplifier output LOS detector
M204		IC203 (pin 5), switch level LOS detector
M206	MC_VREF	Reference voltage
M207		IC203 (pin 7), output level of LOS dectector
M209		LEVEL detector output signal (equal to JUMB, pin 1)
M210		IC204 (pin 7), differential amplifier output LEVEL detector
M211		DC voltage a offset
M241	UPH_KAP	DC bias voltage of photo diode
M242	EL_IN	Electrical input
M303	U_PH	Photo diode bias voltage, after guard circuit
M343		IC304 (pin 6), guard circuit voltage measurement opamp output

TABLE 5

M-no.	Voltage, signal	Description
M401		IC400 (pin 32), demultiplexer, Diode-anode
M207		IC400 (pin 33), output level of LOS dectector
M403		IC400, (pins 13,14,36,37,63,85,86), demultiplexer VTT input
M504		-3.3 V supply voltage Data and Clock recovery
M508		IC400 (pin 48), AREF, (0.5 x output level voltage) DCR
M516	LOCK	IC400 (pin 12), LOCK, (VCO is at 2488320 kHz)
M517		IC400 (pin 37), PC, power supply control signal
M592	VEE_DCR	IC400, VEE, -3.3 V
M594		Input voltage power supply regulator, IC400, DCR
M595		Input voltage power supply regulator, IC400, DCR
M596		T551 emitter voltage (power supply regulator, IC400, DCR)
M598		T552 emitter voltage (power supply regulator, IC400, DCR)
M701		IC701 (pin 74), diode-anode
M751		Converteroutput signal
M752		Converter output signal, inverted
M754		IC751 (pin 48), AREF, (0.5 x output level voltage) Conv
M755		IC751, -3.3 V
M758	CONV_LOCK	IC751 (pin 12), LOCK, (VCO is at 2488320 kHz)
M831		Laser bias alignment, signal side
M832		Laser bias alignment, reference side
M834		- input PI control opamp laser bias loop
M835		Laser driver temperature monitor (diode), anode side.
M901	P8V	+8 V
M902	P8V	+8 V
M903	P8V	+8 V
M904	N8V	-8 V
M905	N8V	-8 V
M906	N8V	-8 V

3. Multiplexer

3.1 Block diagram



3.2 Circuit setup

The multiplexer block consists of the following circuits:

-Multiplexer, OQ2535A, (IC701)
-Clock converter OQ2541C3 (IC751).
-78 MHz clock buffer

The multiplexer and clock converter are drawn on schematics page “OTM/1.drw”, the buffer is drawn on page “CONNECTORS/2.drw”. The schematics can be found in appendix 1, “Schematics”.

The multiplexer is connected as in the datasheet. The boundary scan inputs are not used, and are pulled up internally. The input level threshold can be modified slightly by sinking current out of pin 38. This possibility can be turned on by turning T719 on through MUX_LS. The signal is controlled by switch S635-4,5 “BTL/to MUX”. LED OT651 “DMUX to MUX’ will light up when active. The data inputs are directly connected to connectors JUMC1..4. The selection of the output path (either “normal” or “Electrical loop”) is done by signal EL_MUX~ (active low). EL_MUX~ is controlled by switch S601-7,2 “EL”. When enabled, OT602 “EL-MUX” will light up. Mind that the same control switch is used to modify the demultiplexer output voltages. Selection which ICs will be controlled is implemented by mounting a FET on the appropriate place. Either T719 (multiplexer) or T459 (demultiplexer).

The multiplexer needs a 2.5 GHz clock. The clock can either be applied to connector ST674, “MUX CLK in” as a 2.5 GHz signal, or as 622 MHz signal to connector ST673, “CONV in”. The 622 MHz signal is multiplied by 4 in IC751, a OQ2541C3 setup in transmit mode. In order to avoid transport of the clock signal over a jumper, a combiner has been used for the selection of the signal source. Therefore, only one clock source should be active at the same time. The layout details of the combiner are shown on the next page.

The power supply filtering is so dimensioned that the quality factor of the used components is low. This guarentees no oscillation when the transmitted data contains frequency components at the resonance frequency of the power supply filters..

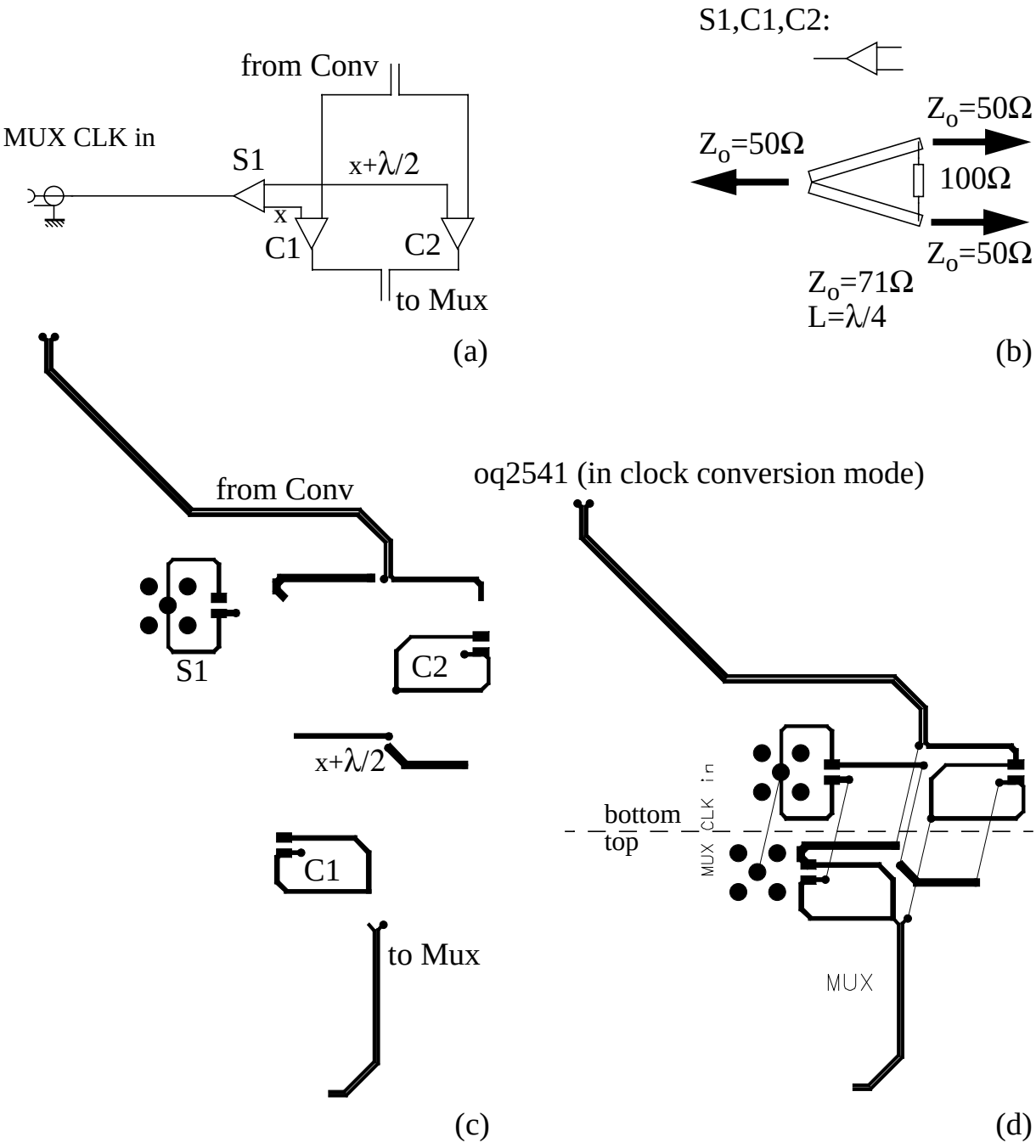


Fig.1 Used splitter circuits and layouts. The 2.5 GHz Multiplex clock signal can be taken from either the MUX CLK in connector or the converted 622 MHz signal. In order to avoid transport of the clock signal over a jumper, a combiner has been used for the selection of the signal source. Therefore, only one clock source should be active at the same time.The two signals are combined in two Wilkinson combiners C1 and C2. The 2.5 GHz signal is made differential by splitting it in a Wilkinson splitter and delaying one branche λ/4. The circuit is shown in (a), the splitter circuit in (b). The several individual layouts in (c) and the complete layout in (d).

The multiplexer has a high frequency input clock. The data is triggered by the low frequency clock. This clock has TTL level. To be able to drive 50 ohm, two buffers are used. First, the TTL signal is buffered by IC671 (74ABT244). After this, it is boosted by 1/2 IC 681 (3205). Three outputs have been connected via resistors R671, R672 and R673, in order to sink enough current to reach TTL level. The networks R674-C674 and R676-C676 have been added to compensate for overshoot

3.3 Layout

The following considerations have been taken into account in the generation of the layout:

- The multiplexer IC has an extra ground plane on layer 1 and 8. This plane is not a must, but it helps reducing interference.
- The TTL lines (from JUMC1..4, bus D_78TBUS) are thin lines (0.3 mm). The lines are kept short, to reduce the load capacitance.
- The clock combiner circuit is shown in the figure on the previous page.
- The lines to the clock inputs of both multiplexer and clock converter are symmetrical 50 ohm microstrips.
- The transmission lines for the clock have been placed on layer 1.
- The transmission lines for the electrical loop signals have been placed on layer 5.
- The spacing between the electrical loop - SMA connectors depicts the distance between multiplexer and demultiplexer. The SMA connectors have been distributed equally between multiplexer and demultiplexer. The lines to the SMA connectors are symmetrical triplate lines.
- IC671 is placed close to the multiplexer. This is done to keep the unbuffered clock line short. The booster IC681 is placed near JUMB.
- Lengths of transmission lines to laserdriver and demultiplexer are shown in appendix 5, “Critical line lengths”.

3.4 Operational information

The input stage of the multiplexer consists of the circuit shown below.

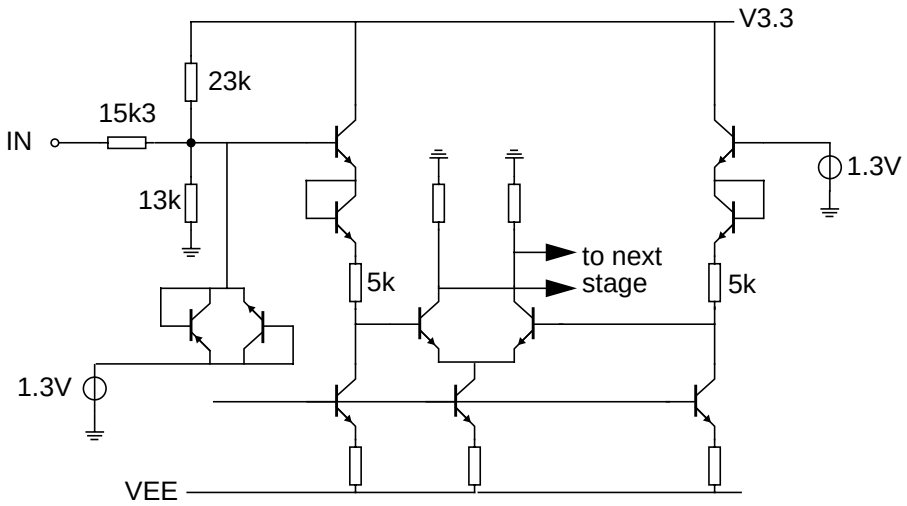
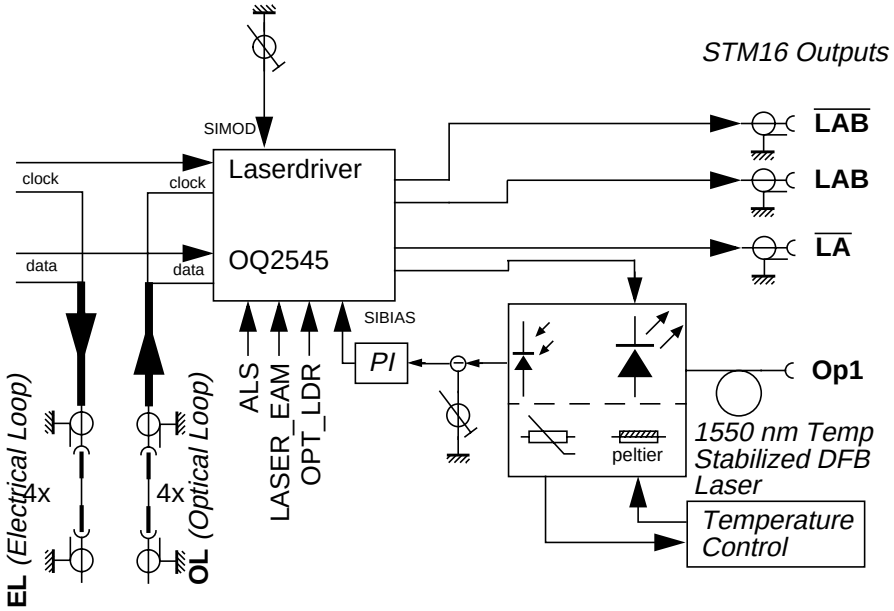


Fig.2 Input stage of multiplexer.

4. Laserdriver

4.1 Block diagram



4.2 Circuit setup

The laserdriver circuit consists of the following subcircuits:

-Laserdriver
-Temperature stabilized laser, with control circuit
-Control circuitry for the bias- and modulation current of the laserdriver

The circuit of the laserdriver is drawn on schematics page “OTM/2.drw”. The temperature control of the laser is drawn on page “OTM/3.drw”.The schematics can be found in appendix 1, “Schematics”.

The laserdriver has two inputs: the ‘normal’ signal from the multiplexer (TRANS_BUS) and the optical loop signals (OL_BUS). The selection is done by signal OPT_LDR~ (active low). OPT_LDR is controlled by switch S601-8,1 “OPT”. When enabled, OT601 “OPT LDR” will light up.

To the adjustment pins AMPADJ (16) and EFADJ (15) a current can be applied. This has been prepared with pads for resistors R802, R803, R807 and R808. On the boards, only R802 is mounted.

In the demoboard no modulation control loop has been implemented. The user can set a DC current with adjusting R857 “Laser mod setting”. R857 is mounted on the bottom of the board.

The bias current is controlled by a loop consisting of the monitor photo diode, IC820 and T831. The output power is monitored and converted to voltage with 1/2 2904 (IC820, pins 1,2,3). This voltage is fed to the integrator around the other half of IC820 (pins 5,6,7). The bias setting can be adjusted by R820 “Laser bias setting”.

The Automatic Laser Shutdown (ALS) signal from switch S601-4,5 “ALS” controls LED OT604 “ALS” . It is fed to the laserdriver and the integrator. This guarentees a soft start of the laser after automatic laser shutdown.

The polarity of the output signal can be changed by switching the laserdriver in “Laser” or “Electro Absorbing Modulator” (EAM) mode. This can be done by switch S631-3,6 “EAM/LASER”. LED OT641 “EAM” or LED OT642 “LASER” will indicate the mode. The control signal EAM_LASER is connected to pin 17.

The temperature control for the laser consist of a resistor bridge around the lasers’ NTC resistor (R954, R955 and R956), a differential integrator (1/2 2904, IC951) and a booster (T958 and T958).

The unused output ($\overline{LA}$) is terminated with 50 ohms and made available at connector ST651 “LA”. For proper functioning of the laserdriver this connector should be terminated with 50 ohms. This guarentees an equal load of 25 ohm on LA and $\overline{LA}$ output of the laserdriver. When problems occur, the path can be disconnected by removing R810. Termination R811 should then changed to 25 ohm. The laser buffer outputs are available at connectors ST652 “LAB” and ST653 “$\overline{LAB}$”.

4.3 Layout

The following considerations have been taken in the generation of the layout:

- The laserdriver is mounted on layer 8. This is to minimize line lengths to the laser and to have space for the cooling fins.
- The corner pins have been enlarged to copper planes to work as heat spread. The corner pins are in the package connected with the die.
- A -6.5V copper plane has been made on layer 1 and 4 to enhance heat transport from the IC to the heat spreader of the laser.
- An extra ground plane has been placed at layer 2 to enhance heat transport from the IC to the heat spreader of the laser.
- On layer 1 and 2 planes have been added. No thermal releases were made in the vias in the area between laserdriver and laser.
- No signals were placed on top of the input pins of the laserdriver.
- The components around the laserdriver were placed as close as possible to the laser.
- The driving line, to the laserdiode is a 25 ohm line. (The laser diode has an input impedance of 25 ohm). The lines from the multiplexer to the laserdriver have equal length and are 50 ohm coupled transmission lines.
- The lines to the buffer outputs are differential 50 ohm lines on layer 8.
- The termination of the output $\overline{LA}$ is done as close to the laserdriver as possible.
- Lengths of data and clock lines from multiplexer and data and clock recovery are shown in appendix 5, “Critical line lengths”.

4.4 Alignment procedure

The alignment procedure adjusts the control circuitry to the used laser. The bias is set first, with modulation current = 0. (R857 not yet mounted)

- The used optical connectors are cleaned and checked.

4.4.1 Bias setting

- The output power at the laser connector is applied to an optical power meter.
- A resistor decade is connected to pad R820 “Laser bias setting”.
- The resistor value is adjusted until the optical power is 1 mW.
- R820 is chosen within 1% of the found resistor value (nearest E96 resistor value).

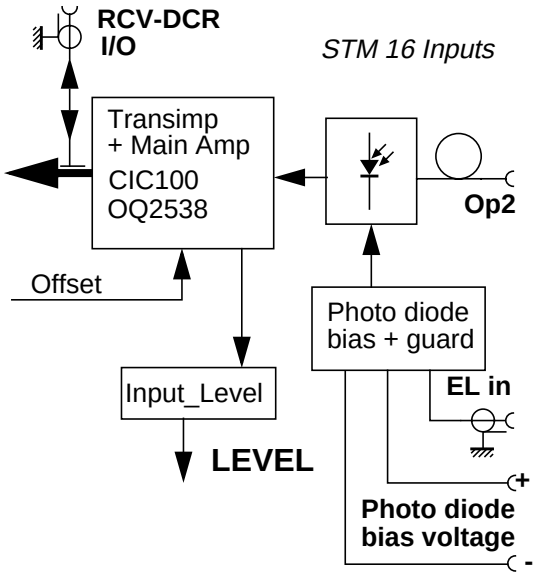
4.4.2 Modulation setting

According to ITU recomendation G.957 (03/93) section 3.2.4, “Measurement methods for the extinction ratio” are under study. The board has been aligned with the following procedure:

- The laser is modulated with a 2^7-1 Pseudo Random Bit Sequence (PRBS).
- A resistor decade is connected to pad R857 “Laser mod setting” (bottom of board).
- The output signal is fed via a O/E transducer and STM16 filter to an oscilloscope.
- A histogram of the Y value is made.
- The highest peak around optical 0 and 1 are taken as mean values.
  (If not one real maximum can be found, the average between the two highest peaks is taken).
- The resistor value is adjusted until the extinction ratio (Low/High) is 10%.
- R852 is chosen within 1% of the found resistor value (nearest E96 resistor value).

5. Receiver

5.1 Block diagram



5.2 Circuit setup

The receiver circuit consists of the following subcircuits:

-Photo diode bias monitor and guard
-Electrical input. This can only be used when the photo diode is not mounted. A resistor of 4.7 kohm needs to be mounted between input pin and M242 (see appendix 6)
-Photo diode. This can be a PIN diode or an APD
-Transimpedance amplifier
-Main amplifier
-Offset control loop/offset adjustment

The circuit of the transimpedance- and main amplifier is drawn on schematics page “ORM/1.drw”, the LOS and Level detect circuits on page “ORM/2.drw” and the guard circuit is drawn on page “PDCM/1.drw”. The schematics can be found in appendix 1, “Schematics”.

5.2.1 Photo diode bias monitor and guard

In order to guard a mounted avalanche photo diode from voltage breakdown, a simple guard circuit has been implemented on the board. The principle is based on the following assumptions:

- Voltage breakdown occurs only when the photo diode bias voltage is high. This means a high avalanche multiplication factor. Still, the total photo current will be low. So a high photo diode bias voltage will cause a low current limit.

- When the photo diode bias voltage is low, it means that the avalanche multiplication factor is also low. Thus for a low bias voltage a high current limit will be taken.

The guard circuit measures the photo diode voltage and current. The current limit is dependent on the measured voltages. If the current limit is reached, the photo diode bias voltage is shorted by a MOSFET. The current limits and transition voltages can be adjusted. A Matlab program is given to calculate the set values.

The photo diode bias circuit is secured to misconnection by diode GR301.

The current monitor is build up around 1/2 IC304 (pins 1,2,3). The photo current causes a positive voltage at the output of the transimpedance amplifier. This voltage is compared with the reference voltage at the output of analog switch IC305.

The selection of the reference voltage is done by comparing the photo diode bias voltage with a set value. This is achieved via voltage divider R306, R305 (photo diode voltage) and R391, R392 (set voltage). The set voltage can be changed for different diodes by adding resistors on pads R379 and R378. The ratiod photo diode voltage is buffered by 1/2 IC301 (pins 1,2 and 3) and compared by the rest of IC301 (pins 5,6 and 7) in a Schmitt trigger. The output voltage is clamped between -0.2 and 5 volt with R394 and GR321.

The current limit is determined from voltage MC_VREF (4.04V) by voltage dividers R377,R376 and R375,R374.

The bias voltage line is filtered with RC combinations R203,C261,C262, R263,C201 and R202,C202.

If a PIN diode is used, the bias guard can be left open. Closing jumper ST264 will bias the photo diode. GR264 has been added for safety measures, if the jumper has been left closed. The photocurrent can be measured at ST264. For accurate measurements prevent current flow in guard circuit by removing R203.

5.2.2 Calculations for photo diode bias guard

Voltage ratio photo diode bias voltage:

$$V_{PDMeas} = \frac{R306}{R306 + R305} \cdot V_{PD} \quad (1)$$

$$V_{PDMeas} = \frac{R391//R379}{R392//R378 + R391//R379} \cdot V_{MC\_VREF} \quad (2)$$

Transition voltage input from high to low:

$$V_{PDMeas} = \frac{R388 + R380}{R388} \cdot \frac{R391//R379}{R392//R378 + R391//R379} \cdot V_{MC\_VREF} - \frac{R380}{R388} \cdot V_{P5V} \quad (3)$$

Transition voltage input from low to high

$$V_{PDMeas} = \frac{R388 + R380}{R388} \cdot \left(\frac{R391//R379}{R392//R378 + R391//R379} \cdot V_{MC\_VREF}\right) - \frac{R380}{R388} \cdot V_{PN4V5} \quad (4)$$

Equations 3 and 4 can be expressed in terms of V_{PD}, giving:

$$V_{PD,HtoL} = \left(\frac{R388 + R380}{R388} \cdot \frac{R391//R379}{R392//R378 + R391//R379} \cdot V_{MC\_VREF} - \frac{R380}{R388} \cdot V_{P5V}\right) \cdot \frac{R305+R306}{R306} \quad (5)$$

Transition voltage input from low to high

$$V_{PD,LtoH} = \left(\frac{R388 + R380}{R388} \cdot \frac{R391//R379}{R392//R378 + R391//R379} \cdot V_{MC\_VREF} + \frac{R380}{R388} \cdot V_{PN4V5}\right) \cdot \frac{R305+R306}{R306} \quad (6)$$

Gain of transimpedance amplifier:

$$A_{TransImp} = R351 \tag{7}$$

High photo diode voltage, bias current limit voltage:

$$V_{Lim,VPDHigh} = \frac{R377}{R377 + R376} \cdot V_{MC\_VREF} \tag{8}$$

Low photo diode voltage, bias current limit voltage:

$$V_{Lim,VPDLow} = \frac{R375}{R375 + R374} \cdot V_{MC\_VREF} \tag{9}$$

The current limit is equal to the voltage limit divided by the transimpedance gain:

High photo diode voltage, bias current limit:

$$I_{Lim,VPDHigh} = \frac{R375}{R375 + R374}\frac{1}{R351} \cdot V_{MC\_VREF} \tag{10}$$

Low photo diode voltage, bias current limit:

$$I_{Lim,VPDLow} = \frac{R377}{R377 + R376} \cdot \frac{1}{R351} \cdot V_{MC\_VREF} \tag{11}$$

The values can be calculated with the given Matlab program. The program is shown on the next pages, followed by the calculated values.

5.2.3 Matlab program

```
% Matlab program for calculation of transition voltages
% and current limit, determined by resistor settings
%
% Used variables
%
% Set values
R305 = 1e6; % Photo diode voltage divider
R306 = 34.8e3;
R378 = 110e3;% Lower part Schmitt trigger voltage divider
R392 = 38.3e3;
R379 = 1e99;% Higher part Schmitt trigger voltage divider
R391 = 10e3;
R380=  10e3;% Smitt trigger input resistor
R388 = 1e6;% Smitt trigger feedback resistor
R376 = 4.64e3;% Photo diode bias current high limit
R377 = 8.25e3;
R375 = 1e3;% Photo diode bias current low limit
R374 = 10e3;
R351 = 3.32e3;% Transimpedance gain
%
R392a=1/(1/R392 + 1/R378);
R391a=1/(1/R391 + 1/R379);
% Voltages
N4V5 = -4.5;
P5V = 5;
V_MC_VREF=4.05;
%
RatioPD = R306/(R306+R305);
Hysteresis=R380/R388;
Vmin_Smitt=(R391a/(R392a+R391a))*V_MC_VREF;
V_PD_HtoL=(((R388+R380)/R388)*Vmin_Smitt-Hysteresis*P5V)/RatioPD;
V_PD_LtoH=(((R388+R380)/R388)*Vmin_Smitt-Hysteresis*N4V5)/RatioPD;
RatioHighCurrentLim=R377/(R377+R376);
RatioLowCurrentLim=R375/(R375+R374);
I_Lim_VPDHigh=RatioLowCurrentLim*(1/R351)*V_MC_VREF;
```

```
I_Lim_VPDLow =RatioHighCurrentLim*(1/R351)*V_MC_VREF;
% printout of values
Outfile=fopen('/home/lb_mge/PCALE/sdh_sonet/usermanual/4STM/Matlab/guard.txt','w');
fprintf(Outfile,'Photo diode bias guard settings\n');
fprintf(Outfile,'Set values of resistors are\n');
fprintf(Outfile,'\t R305 = %g \t[ohm] \t Photo diode voltage divider\n',R305);
fprintf(Outfile,'\t R306 = %g \t[ohm] \t Photo diode voltage divider\n',R306);
fprintf(Outfile,'\t R378 = %g \t[ohm] \t Lower part Schmitt trigger voltage divider\n',R378);
fprintf(Outfile,'\t R392 = %g \t[ohm] \t Lower part Schmitt trigger voltage divider\n',R392);
fprintf(Outfile,'\t R379 = %g \t[ohm] \t Higher part Schmitt trigger voltage divider\n',R379);
fprintf(Outfile,'\t R391 = %g \t[ohm] \t Higher part Schmitt trigger voltage divider\n',R391);
fprintf(Outfile,'\t R380 = %g \t[ohm] \t Smitt trigger input resistor\n',R380);
fprintf(Outfile,'\t R388 = %g \t[ohm] \t Smitt trigger feedback resistor\n',R388);
fprintf(Outfile,'\t R376 = %g \t[ohm] \t Photo diode bias current high limit\n',R376);
fprintf(Outfile,'\t R377 = %g \t[ohm] \t Photo diode bias current high limit\n',R377);
fprintf(Outfile,'\t R375 = %g \t[ohm] \t Photo diode bias current low limit \n',R375);
fprintf(Outfile,'\t R374 = %g \t[ohm] \t Photo diode bias current low limit \n',R374);
fprintf(Outfile,'\t R351 = %g \t[ohm] \t -Transimpedance gain\n',R351);
fprintf(Outfile,'\n');
fprintf(Outfile,'Results\n');
fprintf(Outfile,'\n');
fprintf(Outfile,'\t\t %g \t\t Division ratio photo diode bias voltage \n',1/RatioPD);
fprintf(Outfile,'\t %g\t [V]\t Transition voltage current limit selection, High to low \n',V_PD_HtoL);
fprintf(Outfile,'\t %g\t [V]\t Transition voltage current limit selection, Low to High \n',V_PD_LtoH);
fprintf(Outfile,'\t %g\t [mA]\t Current limit at high voltage \n',I_Lim_VPDHigh*1000);
fprintf(Outfile,'\t %g\t [mA]\t Current limit at low  voltage \n',I_Lim_VPDLow*1000);
fprintf(Outfile,' \n');
fprintf(Outfile,'\t %g\t [V]\t Voltage at high current limit \n',RatioHighCurrentLim*V_MC_VREF);
fprintf(Outfile,'\t %g\t [V]\t Voltage at low  current limit \n',RatioLowCurrentLim*V_MC_VREF);
fprintf(Outfile,'\t %g\t [V]\t Voltage at (-) input Smitt trigger \n',Vmin_Smitt);
fprintf(Outfile,' \n');
fprintf(Outfile,' \n');
fclose(Outfile);
```

5.2.4 Matlab program output

Photo diode bias guard settings

Set values of resistors are

R305 = 1e+06	[ohm]	Photo diode voltage divider
R306 = 34800	[ohm]	Photo diode voltage divider
R378 = 110000	[ohm]	Lower part Schmitt trigger voltage divider
R392 = 38300	[ohm]	Lower part Schmitt trigger voltage divider
R379 = 1e+99	[ohm]	Higher part Schmitt trigger voltage divider
R391 = 10000	[ohm]	Higher part Schmitt trigger voltage divider
R380 = 10000	[ohm]	Smitt trigger input resistor
R388 = 1e+06	[ohm]	Smitt trigger feedback resistor
R376 = 4640	[ohm]	Photo diode bias current high limit
R377 = 8250	[ohm]	Photo diode bias current high limit
R375 = 1000	[ohm]	Photo diode bias current low limit
R374 = 10000	[ohm]	Photo diode bias current low limit
R351 = 3320	[ohm]	-Transimpedance gain

Results

	29.7356	Division ratio photo diode bias voltage
30.1815	[V]	Transition voltage current limit selection, High to low
33.0064	[V]	Transition voltage current limit selection, Low to High
0.110898	[mA]	Current limit at high voltage
0.780761	[mA]	Current limit at low voltage
2.59213	[V]	Voltage at high current limit
0.368182	[V]	Voltage at low current limit
1.05445	[V]	Voltage at (-) input Smitt trigger

5.2.5 Example setting APD guard

The APD mounted on board 01 has the following specifications:

Device:	ATT InGaAs Avalanche Photodetector	
Product:	127E	
Device#:	18867	
Wafer-ID:	qe2899b1-93	
Vbr:	69.6 V	Breakdown voltage
V(12)	64.2 V	Voltage at M=12
V(4)	53.6 V	Voltage at M=4

V(2.7)	47.9 V	Voltage at M=2.7
Mmax	38	Maximum gain
Idp	1.8 nA	Primary dark current
id(12)	31 nA	Dark current at M=12
Id(0.9V)	26 nA	Total dark current at 0.9 Vbr
F(12)	4.9	Excess noise factor at M=12
F(17)	6.4	Excess noise factor at M=17
A	65 V	Gain coefficient
BW(2.7)	2401 Mx	Bandwidth at M=2.7 in MHz
BW(12)	2059 Mx	Bandwidth at M=12 in MHz
TEMP(C)	27.9	Measurement temperature
M(0.9Vbr)	9.34	Calculated value of A, from value at 0.1 Vbr
R	0.85	Responsivity at 1550 nm

The temperature coefficient of the photodiode has the following temperature dependency:

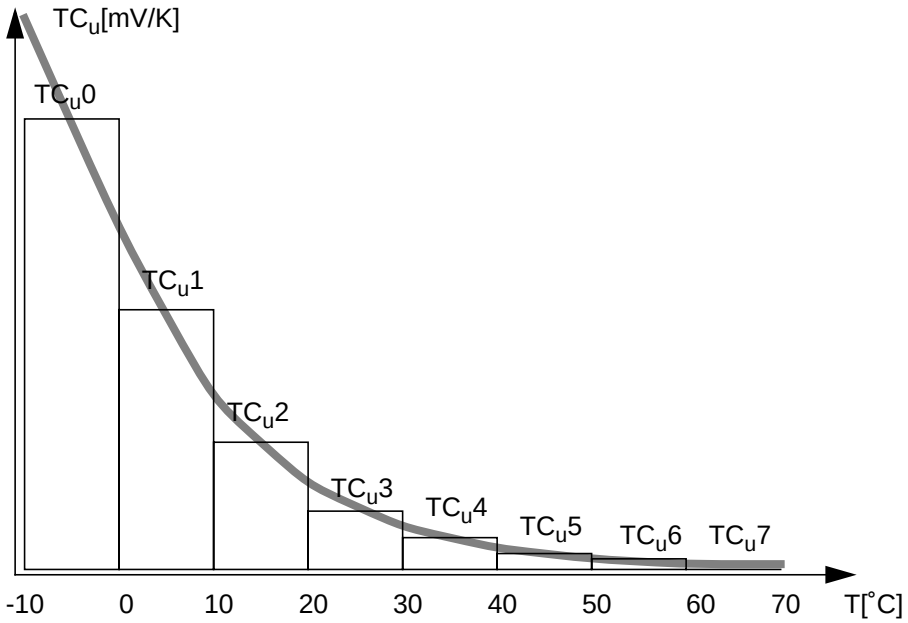


Fig.3 The temperature coefficient TC_u versus temperature. The curve can be approximated by a constant for 10 ˚ C intervals.

To calculate the breakdown voltage at a set temperature, the following equation must be taken into account:

$$V_{br}(T) = V_{br}(T_0) + B_n + (T - T_0)TC_un \quad (12)$$

The offset B_n and temperature coefficient TC_un can be taken constant in 10 ˚C intervals. For the temperature range -10 ˚C .. 70 ˚C, the values for the used photodiode are given in the table below.

TABLE 6 Temperature behaviour of APD type ATT127E,

Temperature	-10..0	0..10	10..20	20..30	30..40	40..50	50..60	60..70	**˚C**
n	0	1	2	3	4	5	6	7	**-**
B_n	0.163	0.085	0.029	0	0	0.048	0.145	0.318	**V**
$TC_u n$	195.4	192.3	188.6	182.8	177.9	172.6	168.7	163.8	**mV/K**

Filled in, with the data of the mounted diode, gives for the photodiode at board 01 the following breakdown voltages:

$V_{br}(-10^{\circ}C)=69.6+0.163+(-10-27.9) \bullet 0.1954 = 62.01$ V

$V_{br}(+70^{\circ}C)=69.6+0.318+(+70-27.9) \bullet 0.1638 = 76.52$ V

The settings for the guard circuit must be set at Vmax < 62.01 V.

To find the value at which the photo diode should be biased, the photobias is varied, with optical input power constant. The optical power is chosed such that the bit errors are in the range 1E-10 .. 1E-4. The result is shown below.

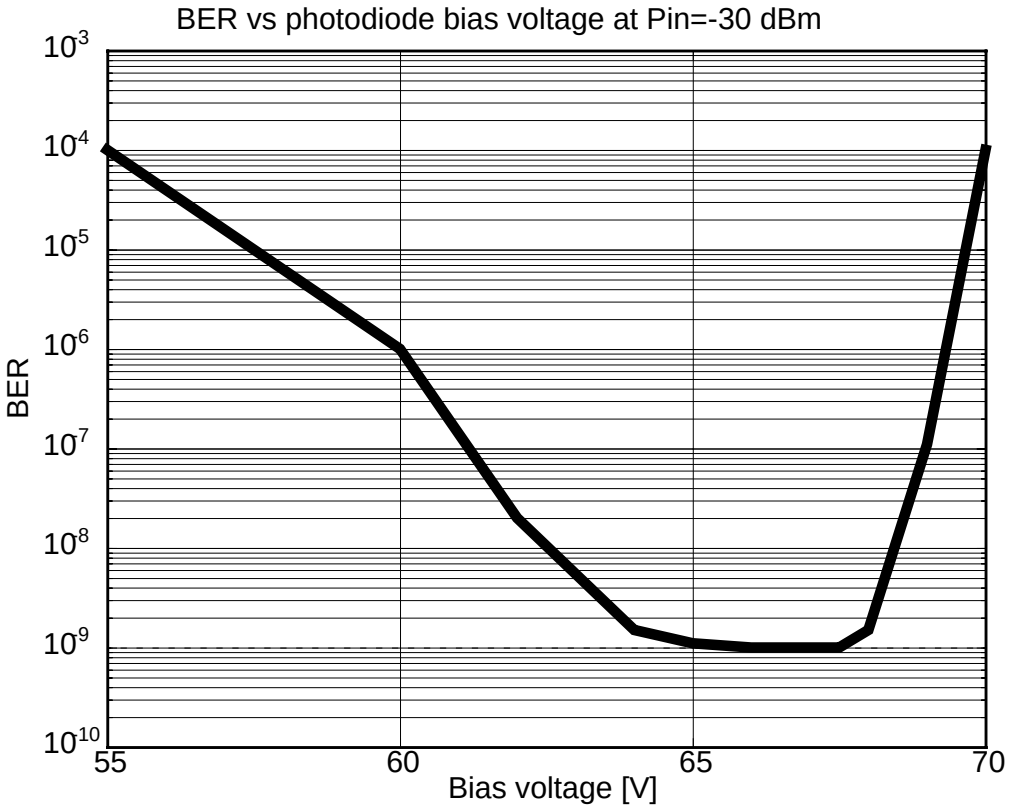


Fig.4 .BER vs Bias voltage at Pin (optical) = -30 dBm. This measurment must be performed to distinguish the optimal bias voltage.

5.2.6 Electrical input.

This can only be used when the photo diode is not mounted. This input has been added to test the board without photo diode mounted. If it must be used mount a resistor from M242 to the photodiode pad. The resistor should be approximately 4.7 kohm.

5.2.7 Offset control loop

The transimpedance amplifier needs no offset compensation. The only offset which should be compensated is the main amplifier, of the main amplifier-data and clock recovery combination. The main amplifier itself has a build in offset control loop. Adjustments can be made a the decoupling capacitor COFF (pins 44 and 45). Either the offset sense output of the data and clock recovery IC can be connected, or a set value. Both possibilities are availbable on the board. (Close ST213 for set value, close ST212 for DCR offset loop, or leave all jumpers open for internal compensation only). The set offset possibility can be used to gain 1 dB in sensitivity with very noisy optical signals. Resistors R228 and R235 should have values in the 10 kohm range.

5.2.8 LOS detection

Los of signal is detected by amplifing and comparing the LOS/LOSDC outputs of the main amplifier. Amplification is done by 1/2 2272 (IC203, pins 1,2 and3), comparing by the other half (pins 5,6 and 7).

ITU recommends LOS when the BER > 1E-3. However, with Avalanche Photo Diode, the dark-current, multiplicated with the APD factor gives approximately the same output level at the rectifiers as asignal will give, at the strength corresponding with a BER of 1E-3. Therefore, the rectifier circuit has been designed so that at an input signal corresponding to BER > 1E-5, LOS will be given. (M207). To distinguish between small signal or amplified noise, the DCR’s LOS (LOS_DCR) has also been taken into account: the main amplifiers' LOS (M207) is ANDed with the DCRs' LOS. (LOS_DCR). The ANDed signal LOS_D controls LED OT621, “LOS” and JUMB, pin 5.

5.2.9 Level detection

The input level detection circuit amplifies the AGC/AGCDC signals from the main amplifier in a 2272 (IC204). The output signal is clamped to prevent output underflow. The LEVEL signal is fed to JUMB, pin 1.

5.2.10 Photodiode bias

The photodiode bias circuit has been build up with standard lumped components, except for the capacitor direct at the photodiode. This capacitance is a copper plane on layer 5, guarded with ground planes on layer 4 and 6. The plane measures 10.795x8.255 mm, yielding 33.7 pF. Alternative circuits should give values between 20 and 40 pF.

5.2.11 Transimpedance amplifier

The transimpedance amplifier is a CIC100B type. (equivalence of CGY2100). For proper functioning the following precautions should be taken:

- VDD1 (pins 46 and 47) and VDD2 (pins 38, 39, 40 and 41) should have seperate power supply filtering. This to prevent parasitic feedback.
- VDD1 (pins 46 and 47) needs a RC combination, to reduce resonances. This is achieved by R208-C207.
- The unused pins (BW-ADJ, pin 21; G-ADJ, pin 19; REF, pin 43 and 44) are terminated with 51E1 resistors, 51E1 resistor + 10 nF capacitors respectively. This gives the least disturbance of the transfer function.
- All power supply filtering has been done by double LC combinations.

5.2.12 Noise lowpass filter

To limit the bandwidth before the main amplifier, a lowpass filter has been implemented. This filter is optimized in conjunction with the main amplifier. The circuit and layout are shown below.

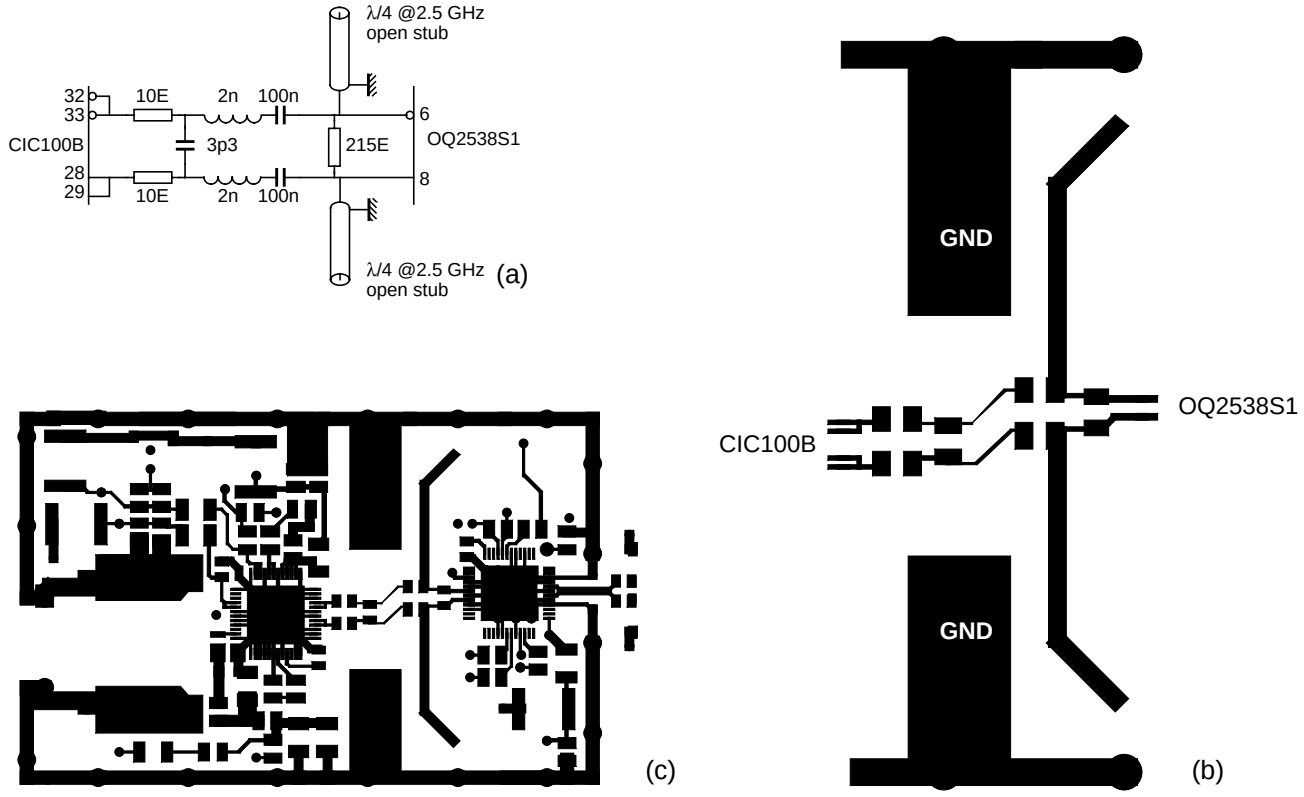


Fig.5 Lowpass filter for noise reduction. The filter is placed between transimpedance amplifier and main amplifier. The circuit is shown in (a). The enlarged layout in (b). The complete layout within the EMC shielding is shown in (c)

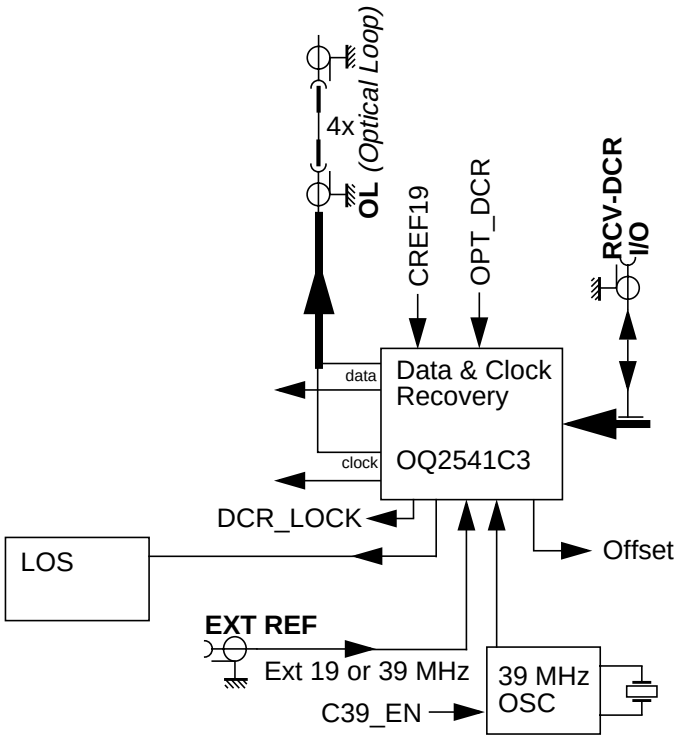
5.3 Layout

The transimpedance- and main amplifier are placed in a metal shielding.

- The lines from the photo diode have been made as short as possible.
- The capacitance at the input has been reduced to the minimum: A CUTOUT HAS BEEN MADE IN THE GROUND PLANE AT LAYER 3.
- An extra ground plane was placed at layer 1.
- To minimize the plane-capacitance area, two ground layers are made as sandwich around the capactior. These planes are on layers 4 and 6
- No thermal releases were made in the vias at the ground planes on layers 1, 3, 4, 6, 7 and 8.
- To enhance EMC immunity a complete ground plane was made on layer 8.
- The path from transimpedance amplifier via main amplifier to data and clock recovery has been made as symmetrical as possible.
- The transmission line to the data and clock recovery is a balanced 50 ohm line on layer 1.

6. Data and clock recovery

6.1 Block diagram



6.2 Circuit setup

The data and clock recovery circuit is drawn on schematics page “DCR/1.drw”. The schematics can be found in appendix 1, “Schematics”.

The data and clock recovery circuit consists of the following circuits:

-DCR IC OQ2541
-39 MHz crystal oscillator

The OQ2541 has been set up in DCR mode. The on-chip power supply needs a booster stage, which is build up with transistors T551, T552, R560, R559, R561, R563, and C561. In general, any transistor with DC current amplification over 100 can be used. Two transistors are used because the available type did not meet the current sink requirements. Alternative circuits should have a power supply rejection ratio of more than 60 dB for all frequencies.

The data and clock recovery has two outputs: the ‘normal’ signal to the demultiplexer (REC_BUS) and the optical loop signals (OL_BUS). The selection is done by signal OPT_DCR~ (active low). OPT_DCR~ is controlled by switch ST611-6.3 “OPT-DCR”. When enabled, OT611 “OPT DCR” will light up.

RF power supply filtering is achieved by C554-R571. The load impedance as seen by the power supply is 15 ohm, in series with two forward biased diodes. To maintain stability, series resistor R571 should be 2.15 ohm. Alternatively, R571 and C554 can be left away when C554 is changed to 47 nF.

The frequency locked loop reference frequency is applied on pins 21 and 22. The reference signal is fed by a 50 ohm differential transmission line from the boards' reference oscillator/external input. The source side of the reference is 50 ohm, made by attenuators R526, R558, R521 and R527. The setup guarentees a 50 ohm noise immune transport of the reference signals

The LOS and LOCK outputs are open collector outputs. They have been pulled to +5V with 10k resistors. (R546 and R550). Both outputs are fed to a LED driver and to JUMB. The signal names are LOS_DCR and LOCK. The LOS is the output of an error detection circuit. This circuits uses the outputs of the Alexander phase detector. If both the previous sample (A) and the next sample (B) have the same state, no transition should have occurred between sample A and B. Thus, the sampling moment (T) should also have that state. If this is not the case, an error has occurred. If the error rate is higher then 10^{-3}, LOS will become high. The LOCK is high when the on-chip VCO is at 2488320 kHz.

6.3 Layout

For the layout, the following considerations were taken into account:

- An extra ground plane was placed at layer 1 and 8
- No signals were placed under the input lines of the IC
- A row of vias was placed under the IC, to guarentee good RF ground
- No thermal releases were made in the via connection in all layers
- RF decoupling capacitors were placed as close as possible to the IC
- Both input and output were build up as symmetric as possible
- Lengths of data and clock lines to laserdriver and data and clock recovery are shown in appendix 5, "Critical line lengths".

6.4 Operational information

6.4.1 Reference oscillator signal

The reference signal for the OQ2541 can be taken from either the board oscillator or an external applied signal. The board oscillator can be turned on with the switch S661, "39 MHz XTAL on". OT660 "39 MHz XTAL on" will light up in this case. The OQ2541 is able to work with a 19 MHz reference signal. The mode is set by switch S661 "DRC at 19 MHz". When set, LED OT669 "DCR at 19 MHz" will lit up. The signal must be externally applied. The board oscillator must be turned off in this case. The reference signal possibilities are shown in table 9.

TABLE 7 OQ2541 reference signal setup possibilities

Mode	S661/OT660 "39 MHz XTAL on"	S661/OT669 "DRC at 19 MHz"	SMA "EXT REF DCR"	FLL CAP value
39 MHz board osc.	On	Off	Open	100 nF
39 MHz ext. osc	Off	Off	39 MHz signal	100 nF
19 MHz	Off	On	19 MHz signal	200 nF

Notes:
1) FLL CAP: Frequency locked loop capacitor. On the PCB pad space is reserved for an extra 100 nF capacitor.
2) If the external applied signal is not large enough to drive the OQ2541, R458 can be adjusted.

6.4.2 Phase Detector Output

For applications in which an external VCO is used, the output of the Alexander Phase detector is available. To prevent DC current, this output is biased with GR452 and R483. Outputs are availlable at measure point M459.

6.4.3 Loss Of Signal

The loss of signal output (pin 39) can be measured at R471.

6.4.4 Output Amplitude Reference

The output amplitude reference pin has been left open. This because the board is dimensioned to work with CML logic inputs at the demultiplexer and laserdriver. For operation with other levels, the loop connectors can be used. The output level can be adjusted, by adding an appropriate resistor value to ground or VEE, which should only be applied for test purposes.

6.4.5 Global frequency acquisition (FLL)

The VCRO is designed to oscillate at a frequency of 2.5 GHz. The recovery of the different data rates is done by applying an appropriate setting to Frequency Divider 1. In order to keep the VCRO in a frequency window of 1 000 ppm around the set clock frequency, a frequency locked loop is included in the IC. The reference frequency needs to be as stable as 1 000 ppm. If the OQ2541 is out of lock and in recovery mode, the phase locked loop is disabled. Only the FLL is closed.

The frequency detector consists of two counters and additional logic. After each count the output of the frequency window detector produces an output signal (either high or low), if the oscillator frequency is outside the set window. This is applied to the loop filter. The loopfilter controls the VCRO.

If the reference frequency is 19 MHz, the count time of the FWD is double as long as with a 39 MHz reference clock. for stability reasons, the integrator capacitance must be kept inversely proportional with the reference frequency.

6.4.6 LOCK signal

The lock signal (DCR pin 12, also measurable at M452) controls LED OT611 “DCR-lock”. The lock is such implemented that it is frequency driven and not phase driven. LOCK indicates that the on-chip VCO is at 2488320 kHz. It gives no indication whether an input signal is applied or not.

6.4.7 Data recovery

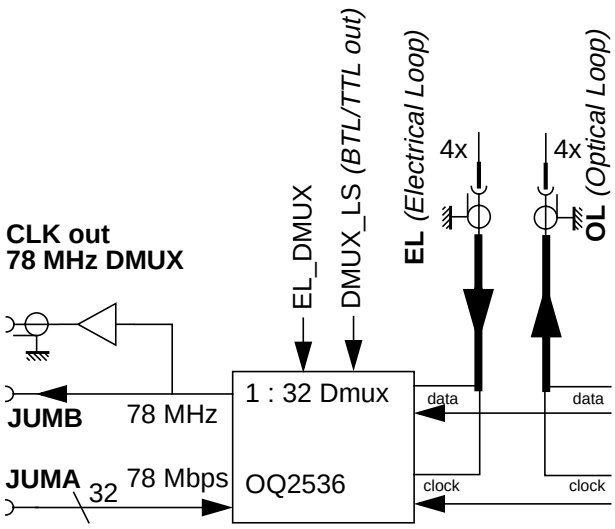
In the data recovery mode, the PLL is active. The PLL is build around the Alexander Phase detector, the loop filter, VCRO and frequency divider 1.

The Alexander Phase detector is used to guarantee the best possible sampling moment. The detector has a non linear transfer characteristic. K_D is depending on the amount of jitter of the inputsignal. The loop is therefore non-linear. No simple equations can be given for the dynamic behaviour. The loop has been designed such that:

- The pull-in range is larger than the FLL frequency window: therefore if the input signal has a spectral component which is within the FLL frequency window, direct pull in occurs.
- The ITU jitter tolorance recommendation (G.958) is met. The proportional path input (PGAIN, pin 13) can be left open.

7. Demultiplexer

7.1 Block diagram



7.2 Circuit setup

The demultiplexer circuit consists of the following subcircuits:

-OQ2536A demultiplexer
-1.5/2.0 volt Pulse Width Modulator (PWM) voltage reference
-78 MHz clock buffer
-Power supply filtering

The circuit of the demultiplexer is drawn on schematics page “DCR/2.drw”, the buffer is drawn on page “CONNECTORS/2.drw”. The schematics can be found in appendix 1, “Schematics”.

The selection of the input signal (either from REC_BUS or EL_BUS) is done by signal EL_DMUX~ (active low). EL_DMUX~ is controlled by switch ST611-4,5 “En EL-DMUX”. When enabled, OT611 “EL-DMUX” will light up.

The unused boundary scan inputs of the demultiplexer are left open.

The output high voltage can be set by applying a voltage to pins 13, 14, 36, 37, 63, 85 and 86. This voltage is made from the +5 board voltage by a PWM IC MAXIM750 (IC451). To change the output voltage, this voltage can be altered by switching T459. Switching occurs when DMUX_LS is high. DMUX_LS is controlled by switch S631-4,5 “BTL/to MUX”. LED OT651 “DMUX to MUX” will light up when enabled. Otherwise LED OT652 “BTL” will light up. Mind that the same control switch is used to modify the demultiplexer output voltages. Selection which ICs will be controlled is implemented by mounting a FET on the appropriate place. Either T719 (multiplexer) or T459 (demultiplexer).

In “BTL” mode the voltage is 1.5 V, in “DMUX to MUX” state the voltage is 2.0 V. By changing the value of R458 other values can be achieved, when necessary. Keep in mind that the maximum current through the output transistors should not exceed 14 mA.

Each data line has a 21.5 ohm series resistor to reduce ringing.

The clock buffer is build up around IC661 (74ABT244) and IC681 (3205). The multiplexer clock output signal is amplified with an BFR92A.

7.3 Layout

The following considerations have been taken in the generation of the layout:

- The demultiplexer IC has an extra ground plane on layer 1 and 8. This plane is not a must, but it helps reducing interference.
- The TTL lines (from JUMA, signals D78R0 .. D78R7) are thin lines. The lines are kept short, to reduce the load capacitance.
- IC661 is placed close to the multiplexer. This is done to keep the unbuffered clock line short. The booster IC681 is placed near JUMB.
- The spacing between the electrical loop - SMA connectors depicts the distance between multiplexer and demultiplexer. The SMA connectors have been distributed equally between multiplexer and demultiplexer. The lines to the SMA connectors are in symmetrical triplate lines.
- No holes are made in the thermal releases of the ground planes
- Lengths of data and clock lines from multiplexer and data and clock recovery are shown in appendix 5, “Critical line lengths”.

7.4 Operational information

The output stage of the demultiplexer consists of the circuit shown below.

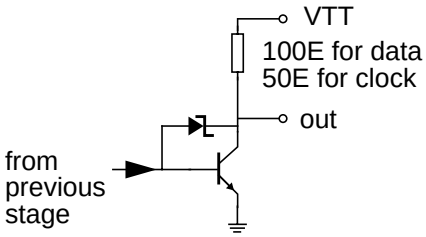


Fig.6 Output stage of demultiplexer. Maximum current through output transistor is 14 mA.

8. Evaluations

8.1 Possible modes

The following performance tests can be executed:

1) Normal mode

2) Optical loop.

3) Electrical loop

These setups are shown in the following figures:

First the posibilities are shown, followed by the individual modes. Combinations of the shown setups are also possible, but not shown in the figures

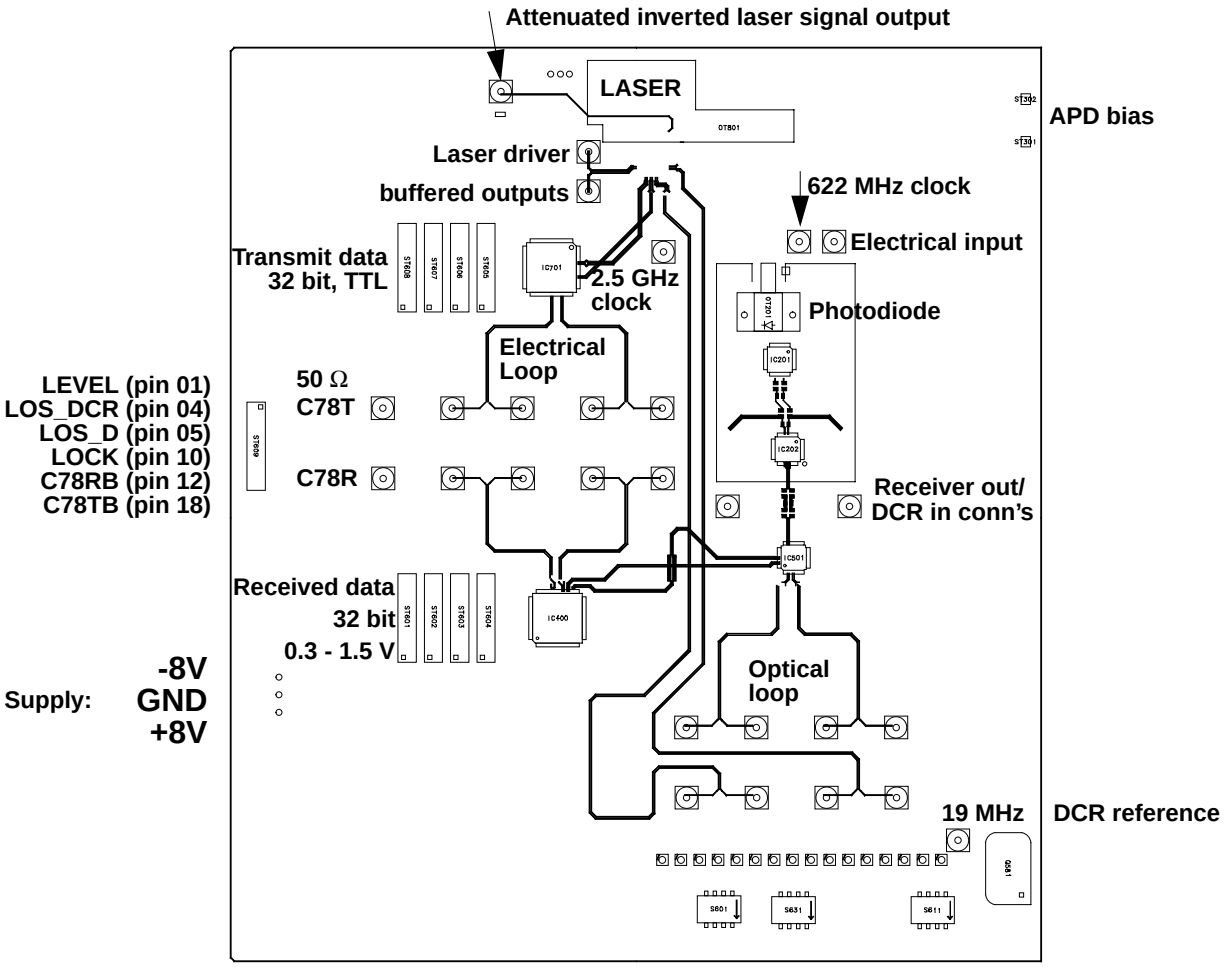


Fig.7 Board with main connectors designated, and high bitrate lines highlighted. Receive and transmit part can work independently. Signal flow is dependent on mode setting: each IC, when applicable, can be set in normal or loop mode. This enables various test possibilities. Various possibilities are shown in the following figures

8.1.1 Normal mode, measurements at optical side

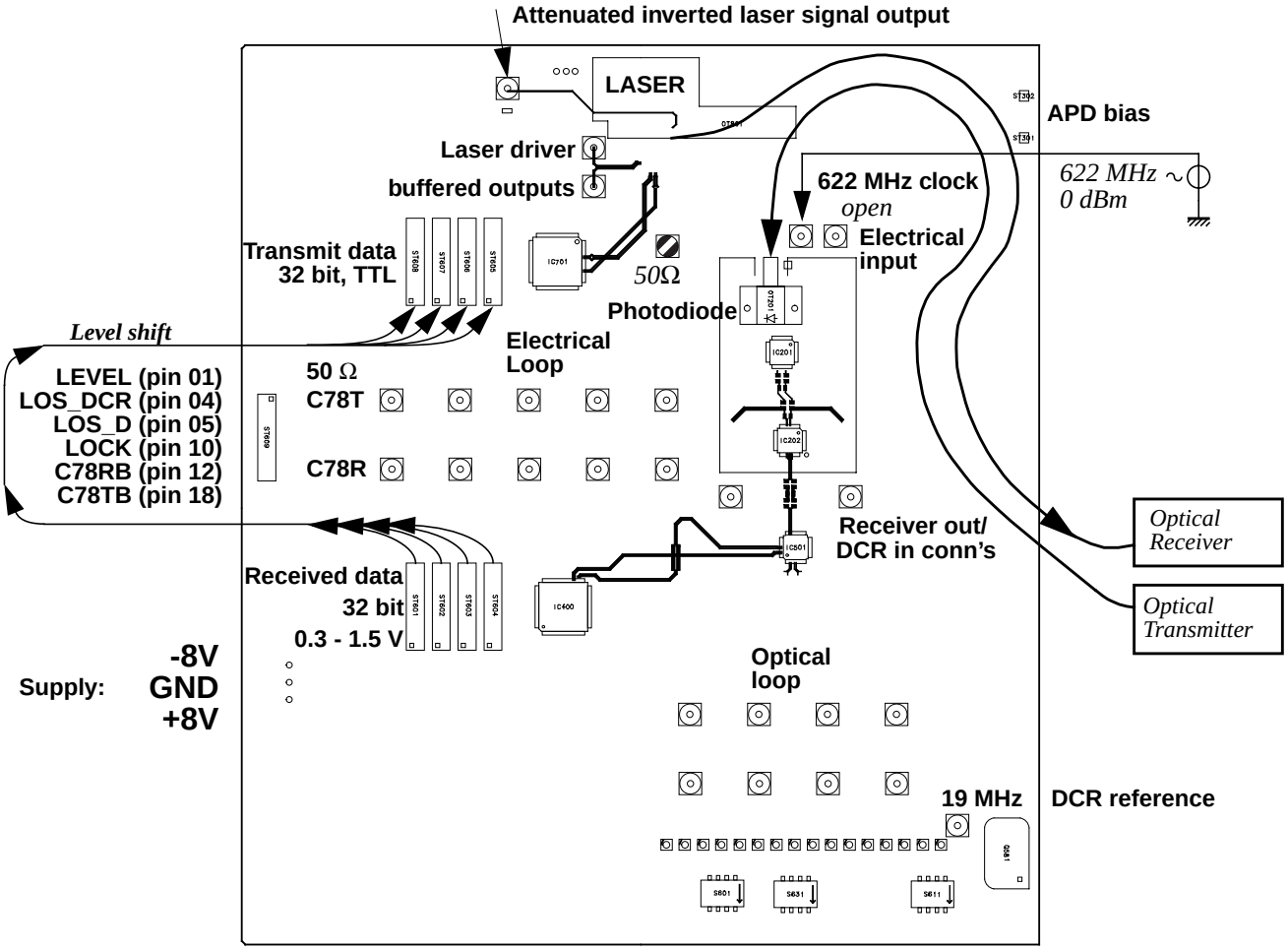


Fig.8 Signal flow with board in normal mode, measurements at optical side. The input signal is generated in an optical transmitter. The signal is received, amplified, data and clock are seperated and demultiplexed. The demultiplexed data can be fed to the mux, but needs a level shift for proper working. The multiplexer needs a 2.5 GHz clock to drive. In this case the clock is converted from a 622 MHz clock. Signals as are received by the laserdriver can be monitored at LAB and $\overline{\text{LAB}}$. The not used side of the laser driving stage is attenuated and fed to $\overline{\text{LA}}$. This corresponds with the laser current.

8.1.2 Normal mode, measurements and generation at 78 Mbps side

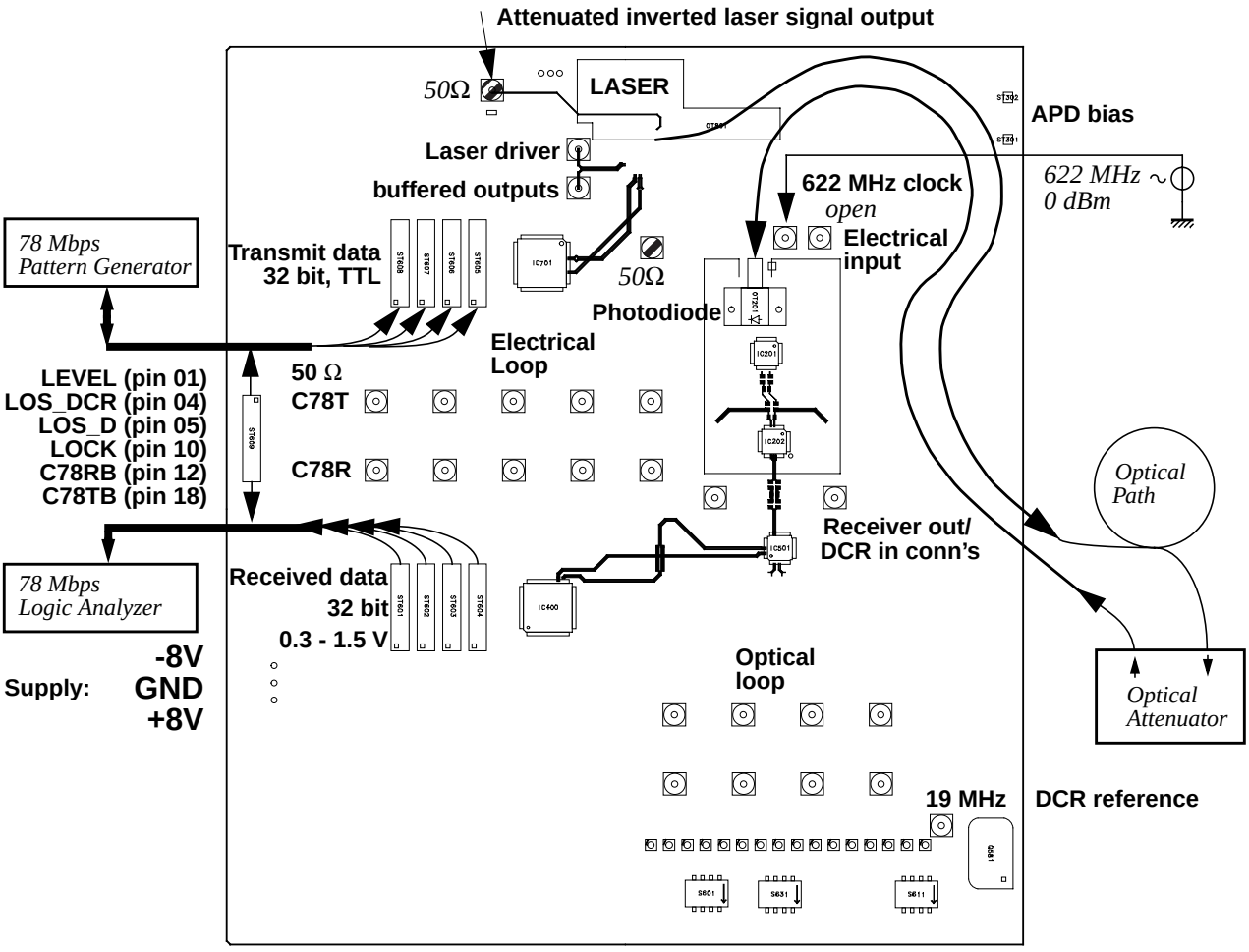


Fig.9 Signal flow with board in normal mode, measurements at 78 Mbps side. The input signal is generated with a 78 Mbps pattern generator. The pattern generator is triggered by the divided 2.5 GHz multiplexer clock, which is converted from the applied 622 MHz clock. The signal is transmitted, fed to an optical path and attenuator and received. The received signal is demultiplexed and fed to a logic analyzer.

8.1.3 Optical loop mode: transmitter measurement

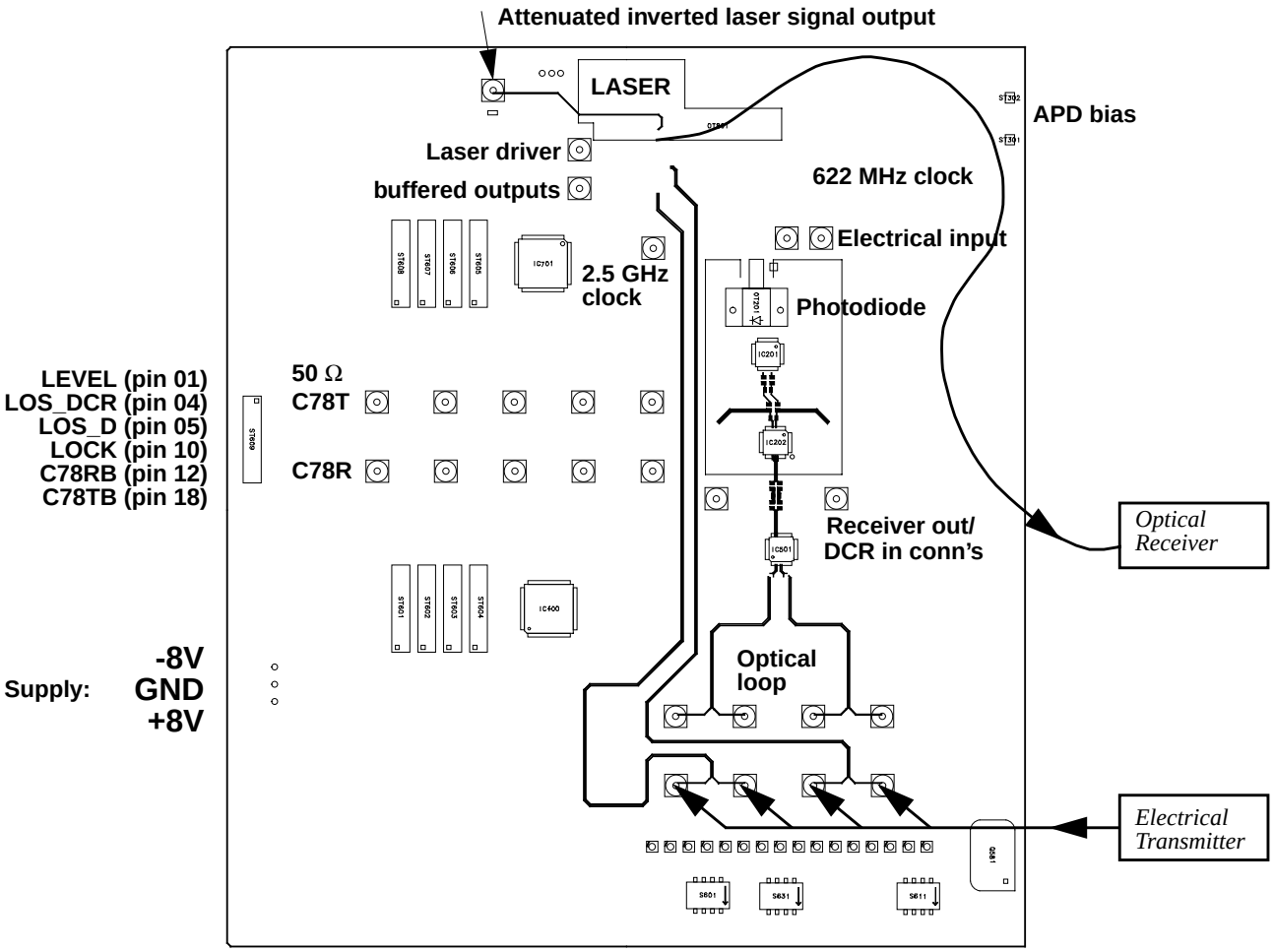


Fig.10 Signal flow with board in optical loop mode, with the transmit part under test. The loop jumpers are removed and the CML level clock and data signal (differential) is applied to the loops' input connectors. The laser signal can be measurd at the laser buffer outputs (LAB and $\overline{\text{LAB}}$) and at the inverted laser output ($\overline{\text{LA}}$).

8.1.4 Optical loop mode: receiver measurement

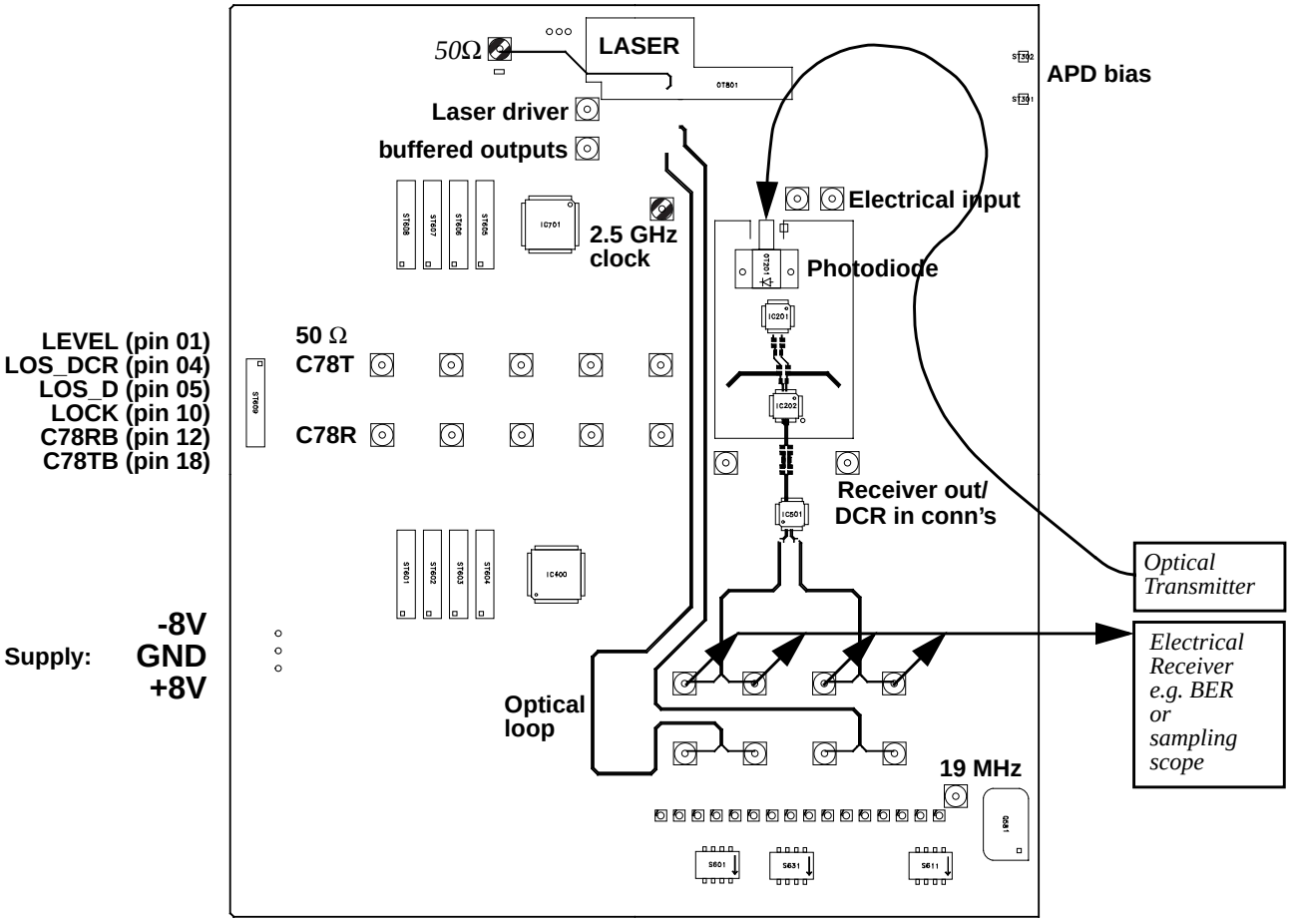


Fig.11 Signal flow with board in Optical loop mode, with the receiver part under test. Optically a signal is applied to the photo-dioe. The received signal can be monitored at the Receiver out/DCR in connectors. In the figure are the loop jumpers removed for connection of receiving equipment, e.g. a BER receiver or sampling scope

8.1.5 Electrical loop mode: high data rate input

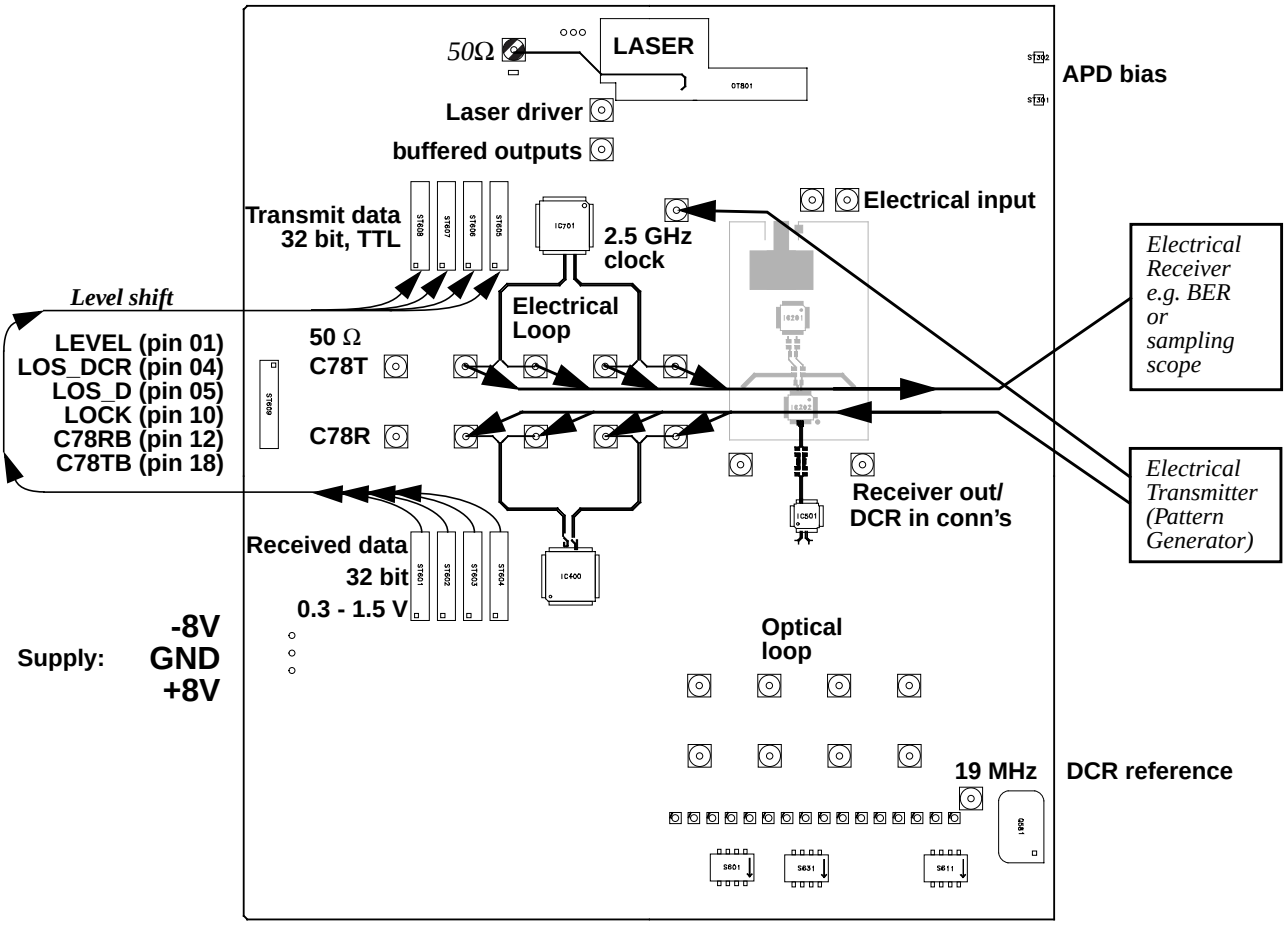


Fig.12 Signal flow with board in Electrical loop mode. In the setup shown above, the input signal is at the high data rate channels. Connection of the demultiplexer to multiplexer needs a level shift.

8.1.6 Electrical loop mode: lowdata rate input

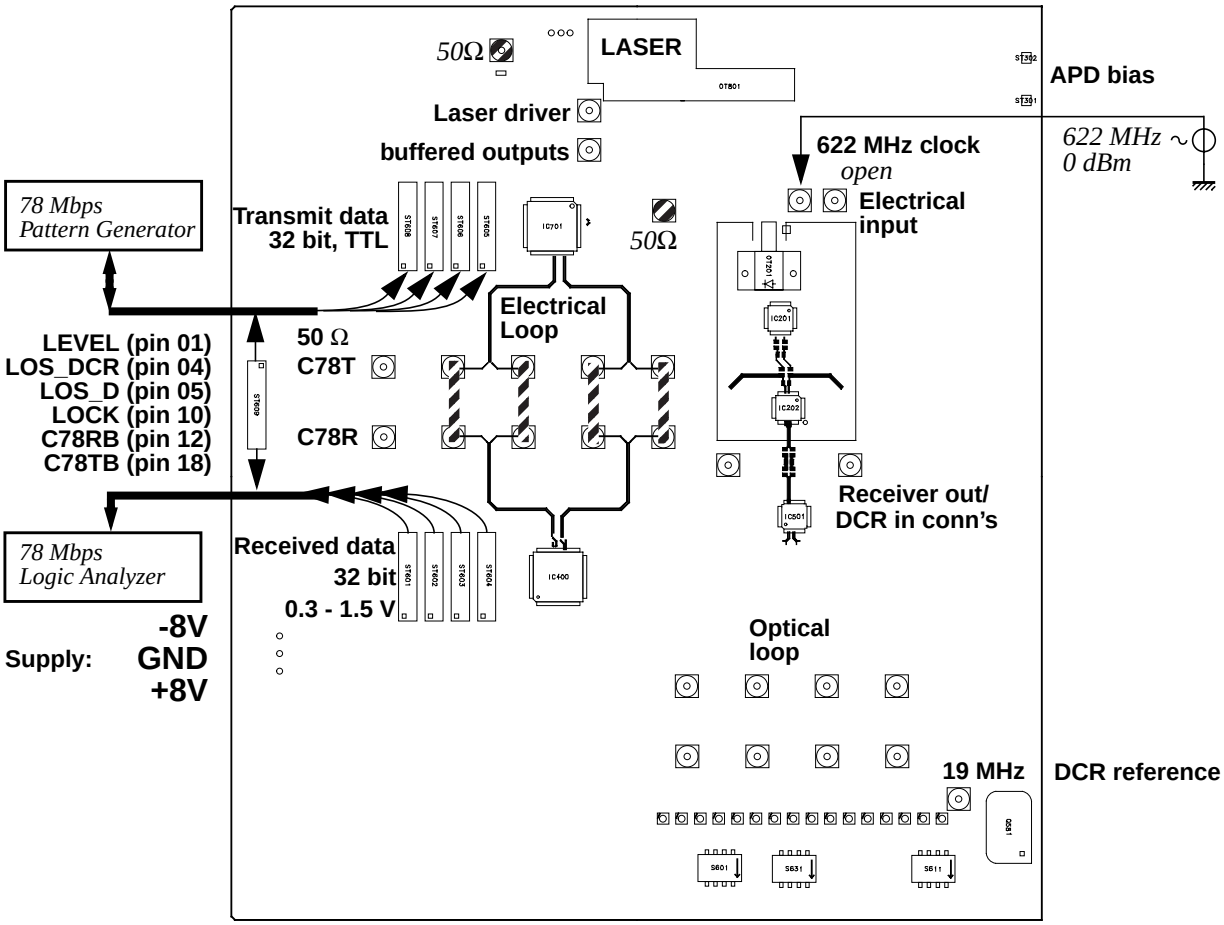


Fig.13 Signal flow with board in Electrical loop mode. In the setup shown above, the input signal is at the low data rate channels. Connection of the multiplexer to demultiplexer is done by the SMA jumpers.

8.2 Performance measurements

To illustrate the behaviour of the board, the following measurements are performed:

- Bandwidth of receiver with PIN and APD diode
- BER vs input power with PIN and APD diode
- Transmitted signals

The recorded measurements are performed at room temperature.

The measurements are performed on board 01.

Board 01 is was mounted with optical components with the folling data:

Photo diode

Device:	ATT InGaAs Avalanche Photodetector	
Product:	127E	
Device#:	18867	
Wafer-ID:	qe2899b1-93	
Vbr:	69.6 V	Breakdown voltage
V(12)	64.2 V	Voltage at M=12
V(4)	53.6 V	Voltage at M=4
V(2.7)	47.9 V	Voltage at M=2.7
Mmax	38	Maximum gain
Idp	1.8 nA	Primary dark current
id(12)	31 nA	Dark current at M=12
Id(0.9V)	26 nA	Total dark current at 0.9 Vbr
F(12)	4.9	Excess noise factor at M=12
F(17)	6.4	Excess noise factor at M=17
A	65 V	Gain coefficient
BW(2.7)	2401 Mx	Bandwidth at M=2.7 in MHz
BW(12)	2059 Mx	Bandwidth at M=12 in MHz
TEMP(C)	27.9	Measurement temperature
M(0.9Vbr)	9.34	Calculated value of A, from value at 0.1 Vbr
R	0.85	Responsivity at 1550 nm

Laser diode

Manufacturer:	Philips Optoelectronics Centre
Type:	CQF910/D #4737
Wavelength:	1540.40
RMS	-

Parameter vs. temperature behaviour:

Temp	-10	25	75	˚C
Ith	11.4	11.4	11.6	mA
Ec	58	57	55	mW/A
Rs	30.2	30.2	30.1	Ohm
V30mA	1.79	1.79	1.78	mA
Iop	55.1	55.7	57.8	mA
Rntc	8.1	8.0	7.7	kOhm
Ipelt	429	57	-751	mA
Ms	369	370	381	uA/mW

Tracking Error max	0.5	% (relative to 25 ˚C)
Tracking Erro min	-1.2	% (relative to 25 ˚C)
Wavelength	1538.10	nm
Rpelt	1.282	ohm

8.3 Measurement setup

8.3.1 Receiver transfer

The measurement of the receiver bandwidth has been executed under small signal conditions.
The following equipement was used:

- HP8702 Lightwave component analyzer
- HP85047 300 kHz - 6 GHz S parameter testset
- HP83402A 300 kHz - 6 GHz Lightwave source 1300 nm

The optical input power was -30 dBm with PIN diode and -40 dBm with Ternary APD. The setup is shown in the figure below.

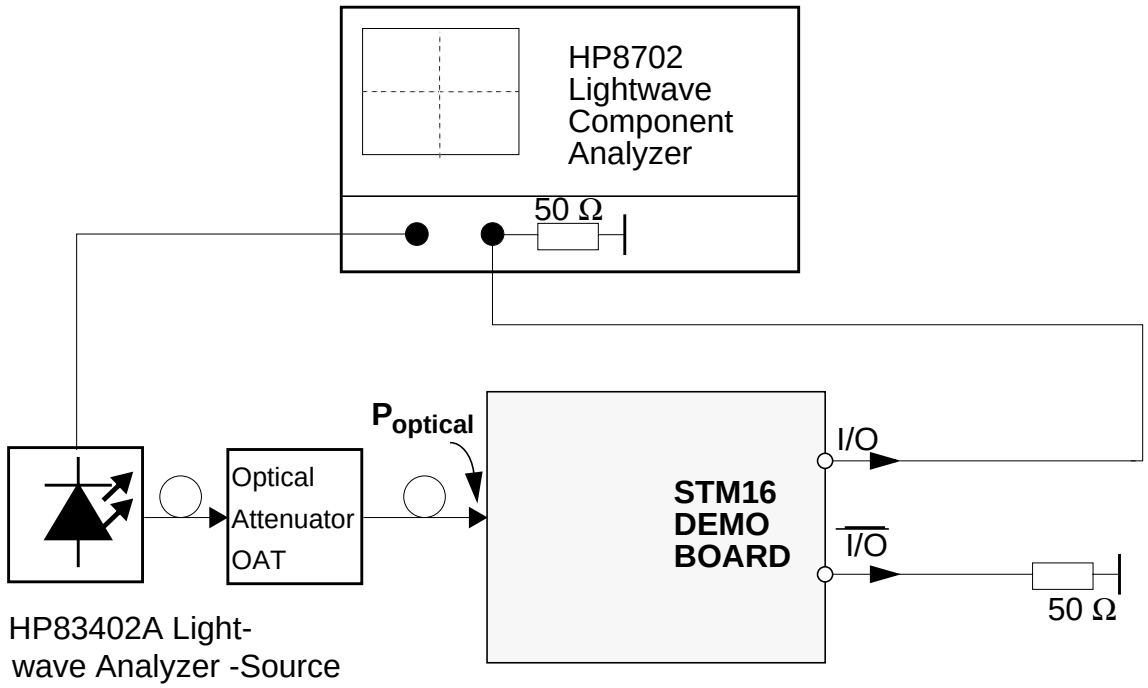


Fig.14 Frequency Response Measurement at the Receiver-Data & Clock recovery Input/Ouputs

8.3.2 Bit Error Rate versus input power

The following equipment was used:

- A standard STM16 system board
- 2 x HP 8157A Optical attenuator (ATT)

The measurement of the Bit Error Rate was performed with the equipment in the following configuration:

-The standard STM16 system board was used as transmitter and receiver. The STM bit B1/B2 error count was used to measure the bit error rate.

-The optical signal was attenuated and fed to the STM16 demo board.

-The optical loop was enabled.

-The oscilloscope was used to check the waveform at $\overline{LA}$.

-The output of the board was fed via an attenator to the system board.

-The output attenuator was set such that the system board was not overloaded.

-A PC was used to read out the value of B1/B2.

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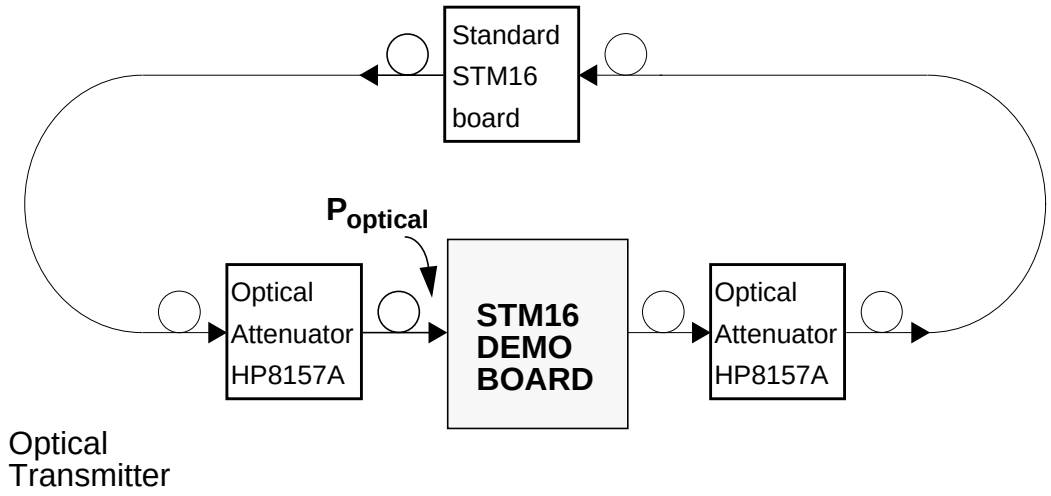


Fig.15 Bit Error Rate Measurement setup.

8.3.3 Eye diagram of transmitted signals

The following equipment was used:

- A Rohde & Schwarz 376.8011.52 signal generator
- A HP83480A Digital Cummunications Analyzer, with HP83485A optical module
- A HP16500A logic analyzer with 16520A Pattern generator.

The measurement of the output eye diagram was performed with the following setup:

-The multiplexer and laser driver were set in “normal” mode.

-The signal generator was used to clock the multiplexer at 2.5 GHz and to trigger the Digital Cummunications Analyzer

-The pattern generator was triggered with the 78 MHz clock output (JUMB). It applied 32 bit wide 2^7-1 PRBS to the multiplexer

-The optical output signal of the STM16 demoboard was fed to the Digital Cummunications Analyzer.

-The measurement setup is shown in the following figure.

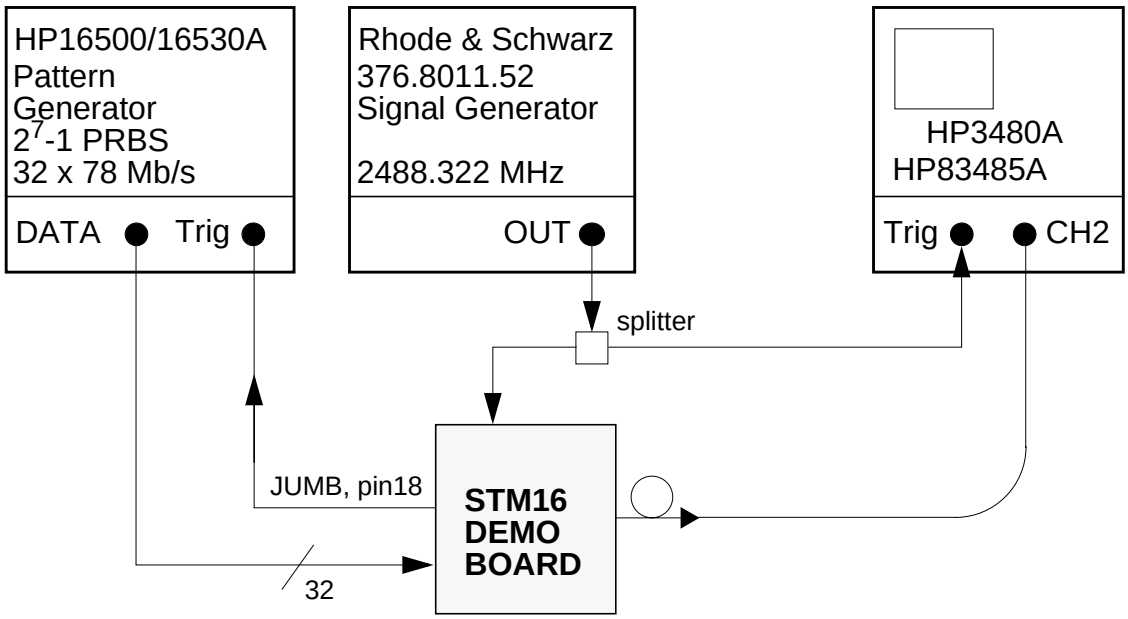


Fig.16 Output eye diagram measurement setup.

8.4 Measurement results

8.4.1 Receiver transfer

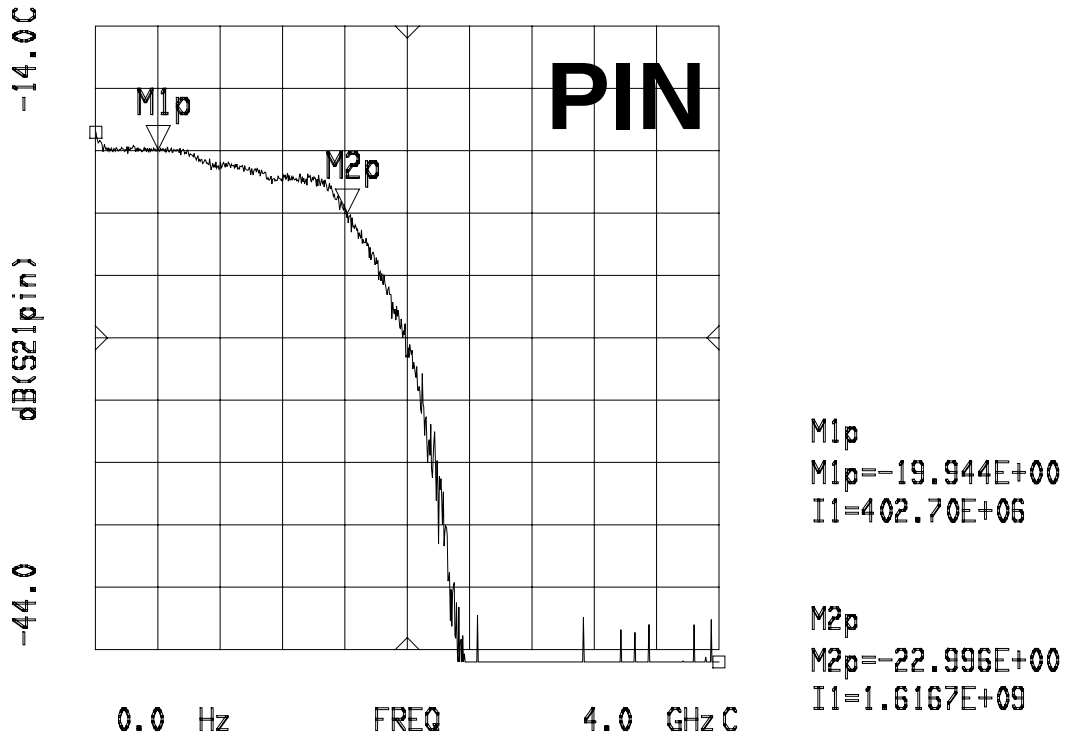


Fig.17 Small signal bandwidth, measured at board 01, with PIN photodiode.

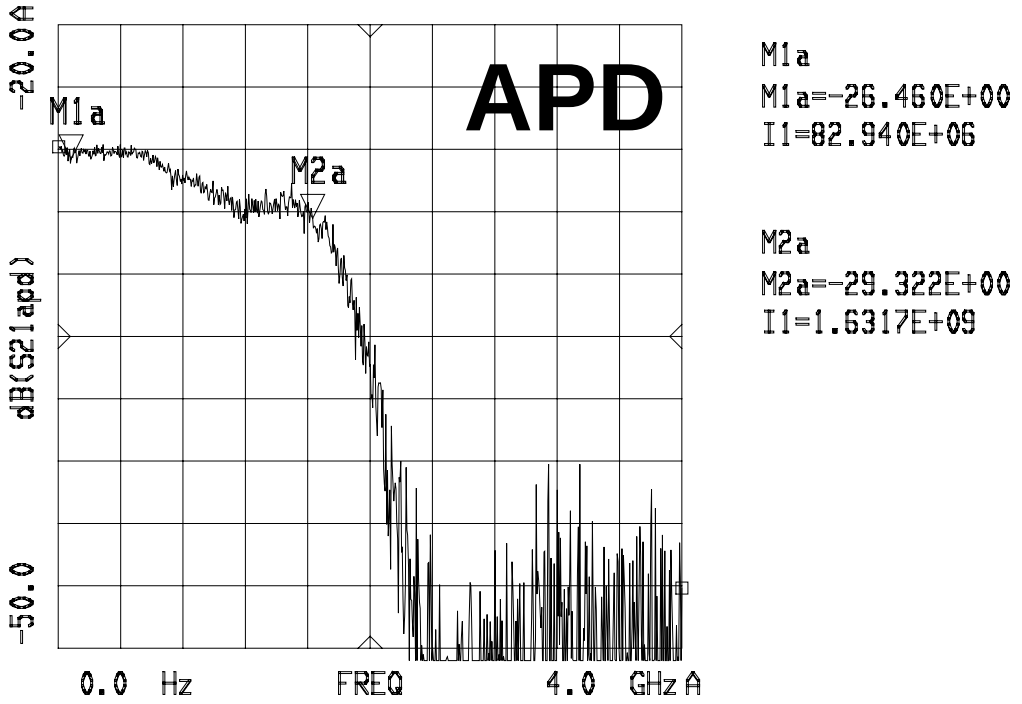


Fig.18 Small signal bandwidth, measured at board 01, with APD photodiode.

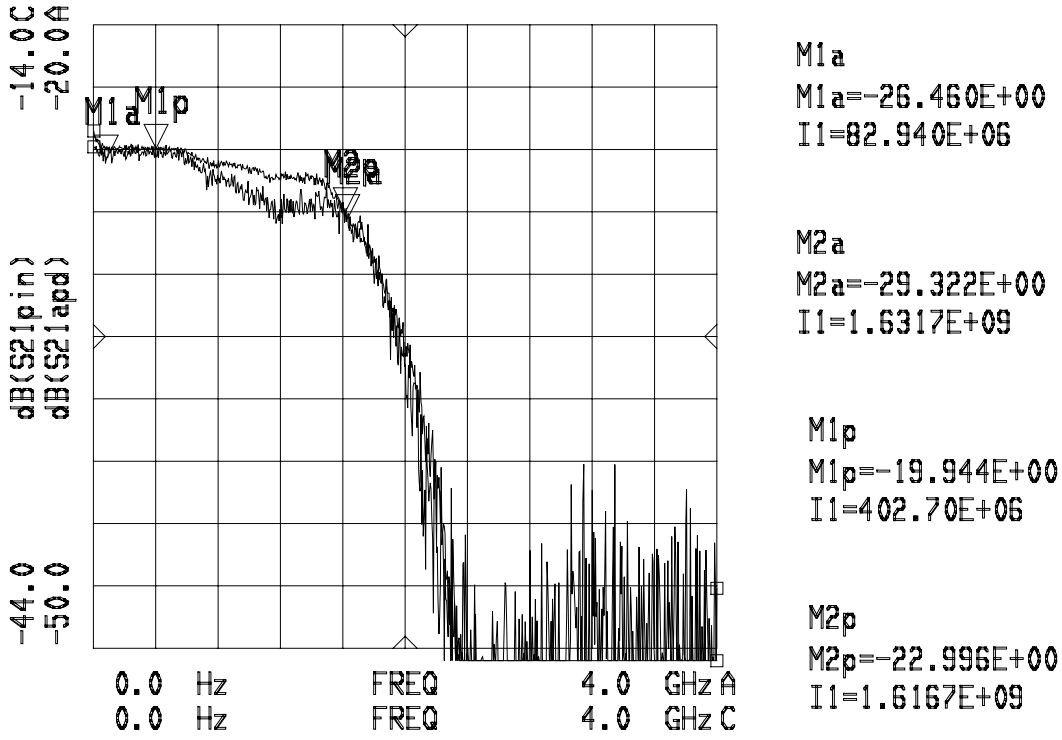


Fig.19 Small signal bandwidth, measured at board 01, results of PIN and APD photodiode measurement.

8.4.2 Bit Error Rate versus input power

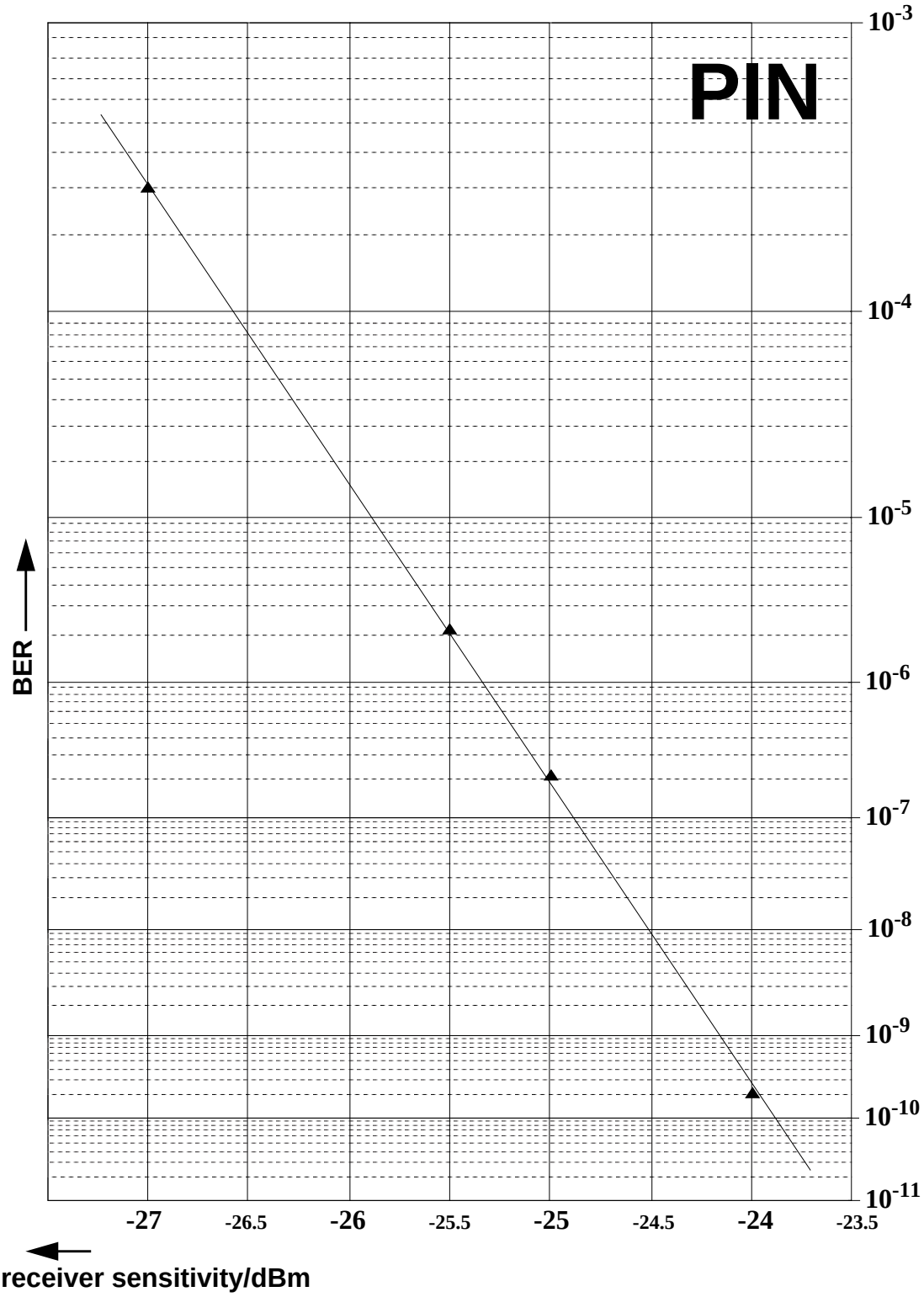


Fig.20 Bit Error Rate (BER), with PIN detector (responsivity diode 0.94 A/W), extinction ratio 10%.

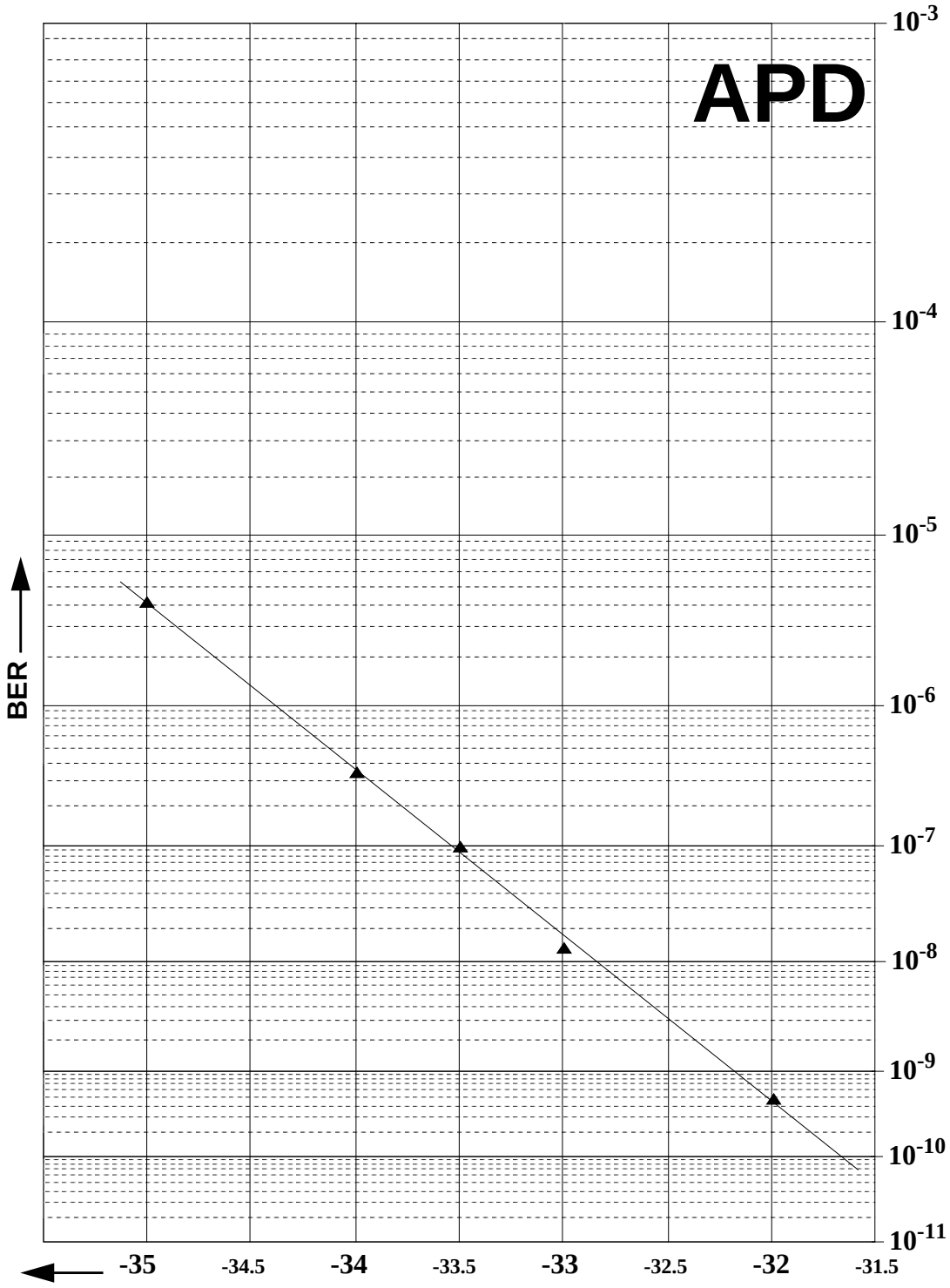


Fig.21 Bit Error Rate (BER), with APD detector (bias voltage 66.8V), extinction ratio 10%.

8.4.3 Eye diagram of transmitted signals

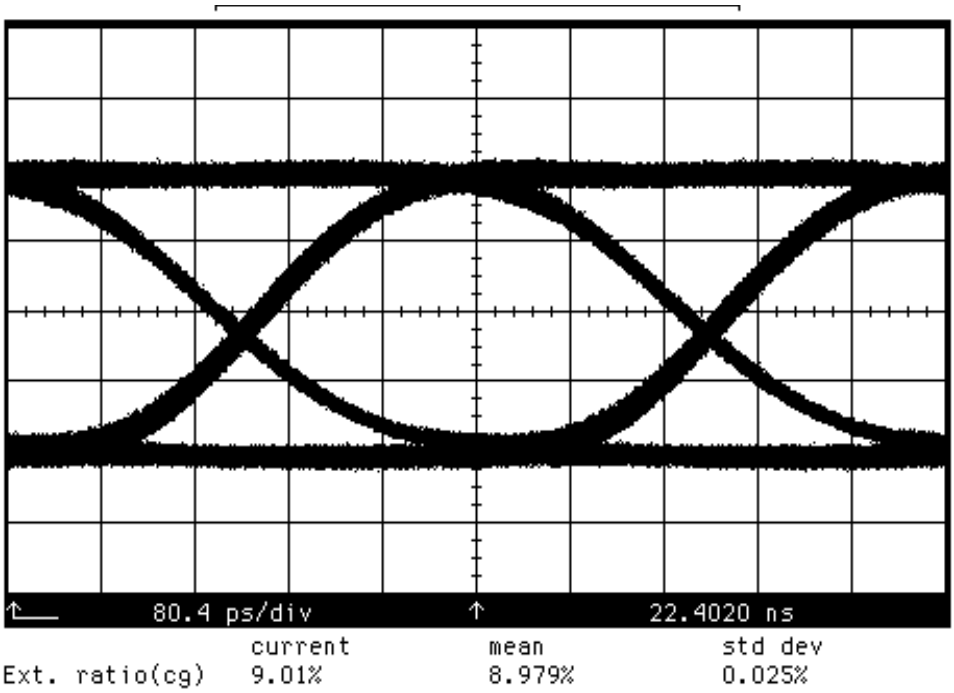
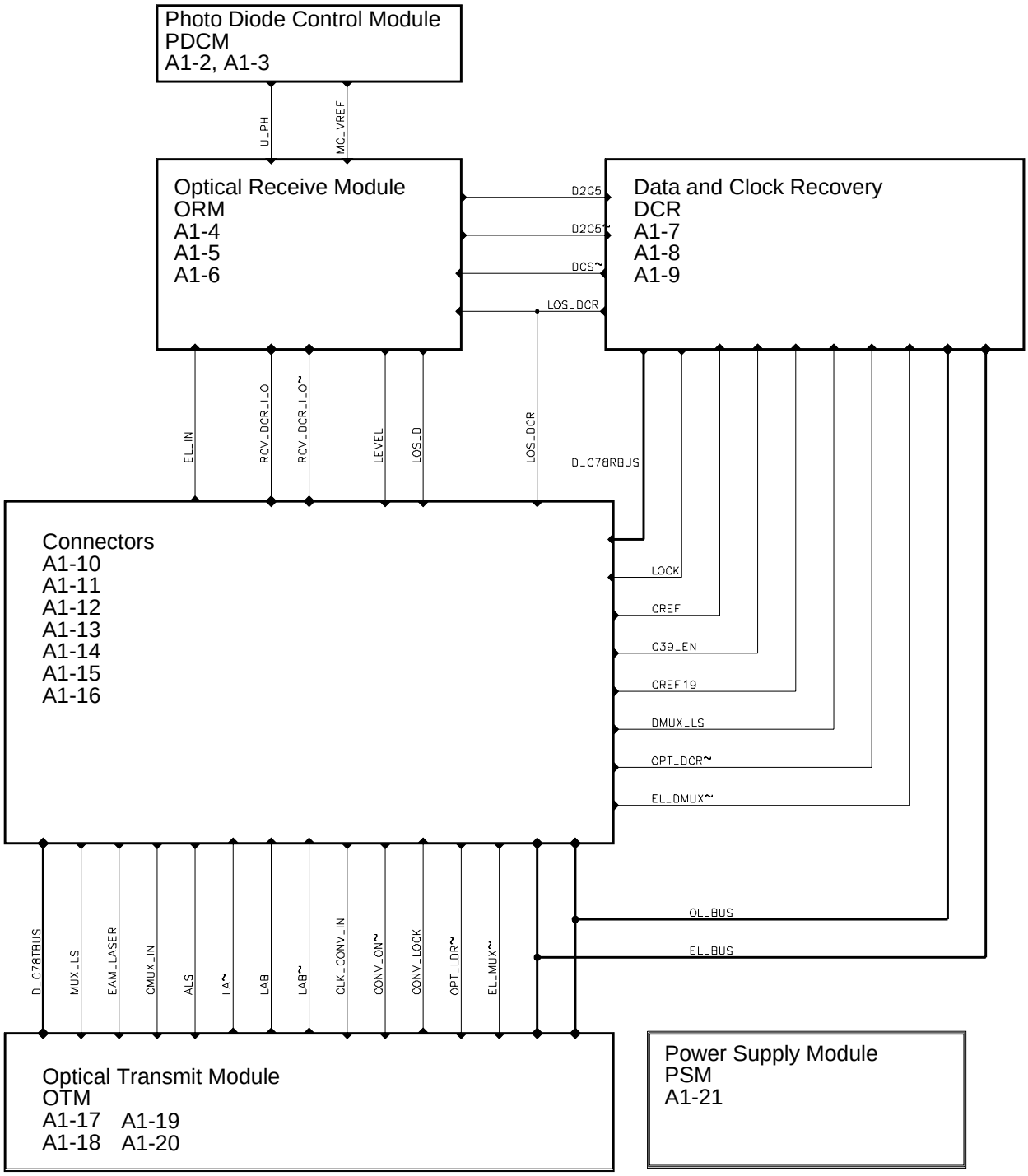


Fig.22 Eye diagram of transmitted signal, after reference receiver

APPENDIX 1 Schematics

The schematics of the board are hierarchically build up, as shown below.
The schematics of the different blocks are shown on the next pages.
The original A3 sized schematics are spread over 2 opposite pages, or compressed at one A4 page
When applicable, these opposite pages should be read as one schematic.
The number of pages indicate how many A4 pages compromise one schematic.
ⓑ indicates that the part is mounted on the bottom side of the PCB



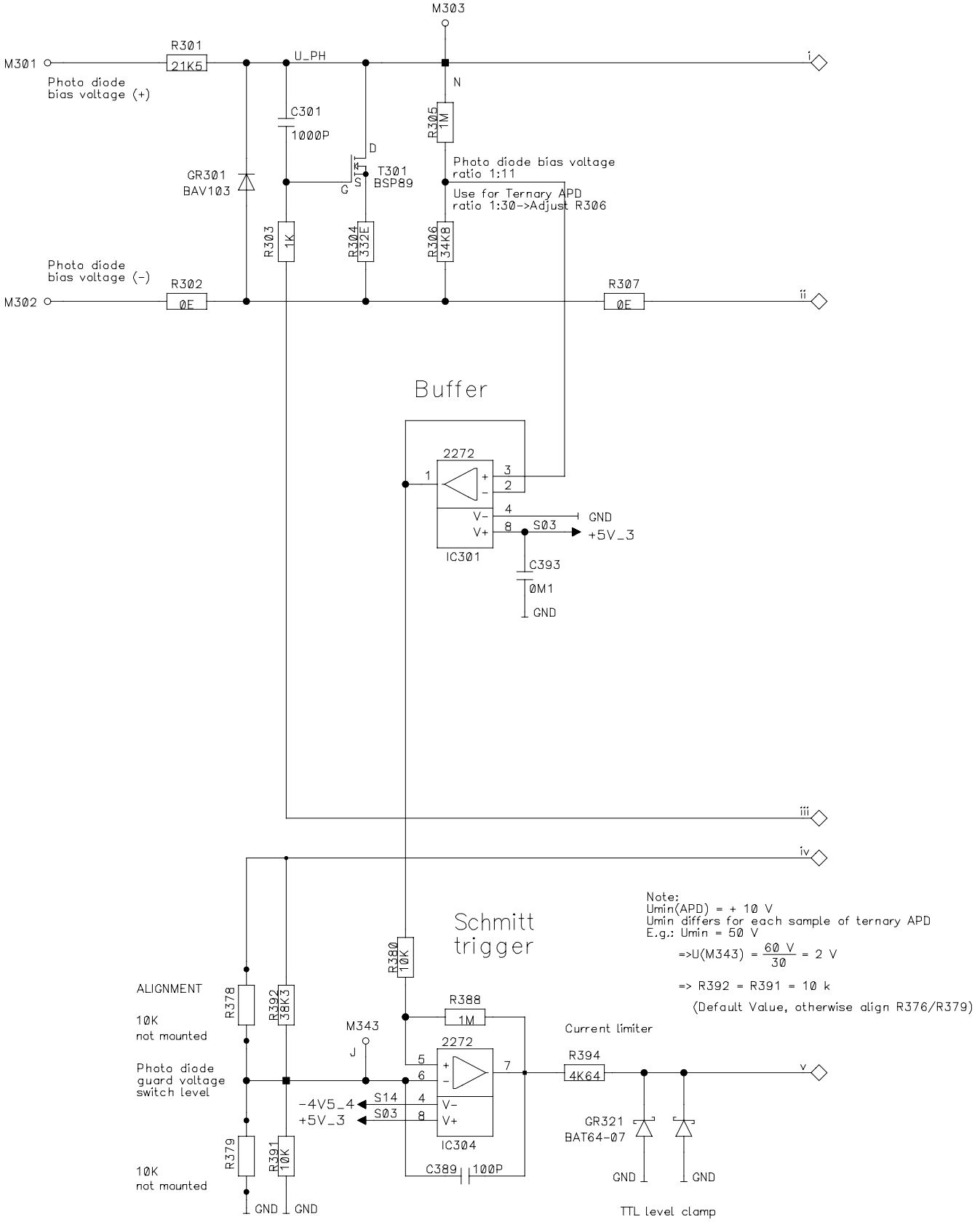


Photo Diode Control Module
PDCM/1.drw
page 1 of 2

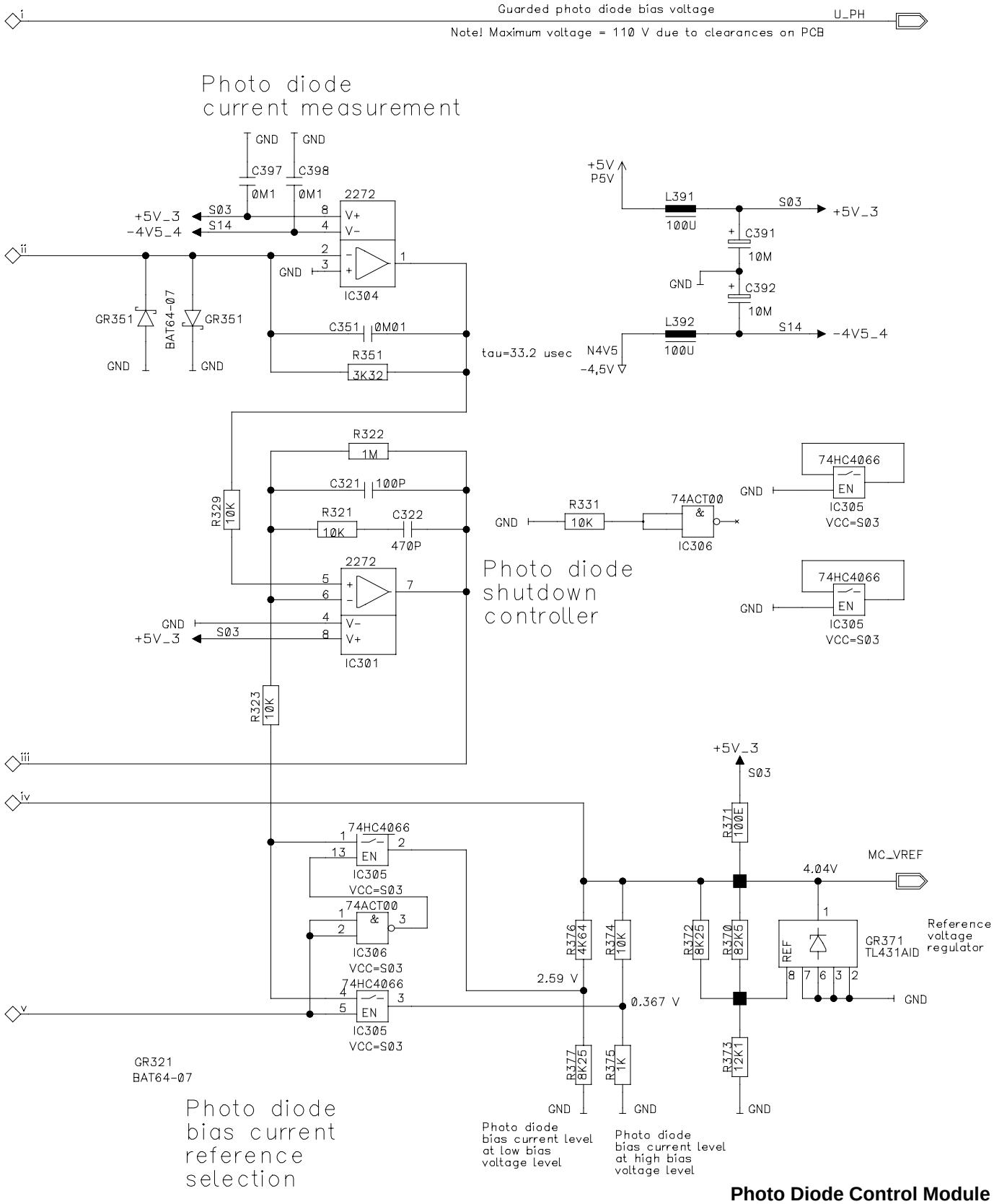
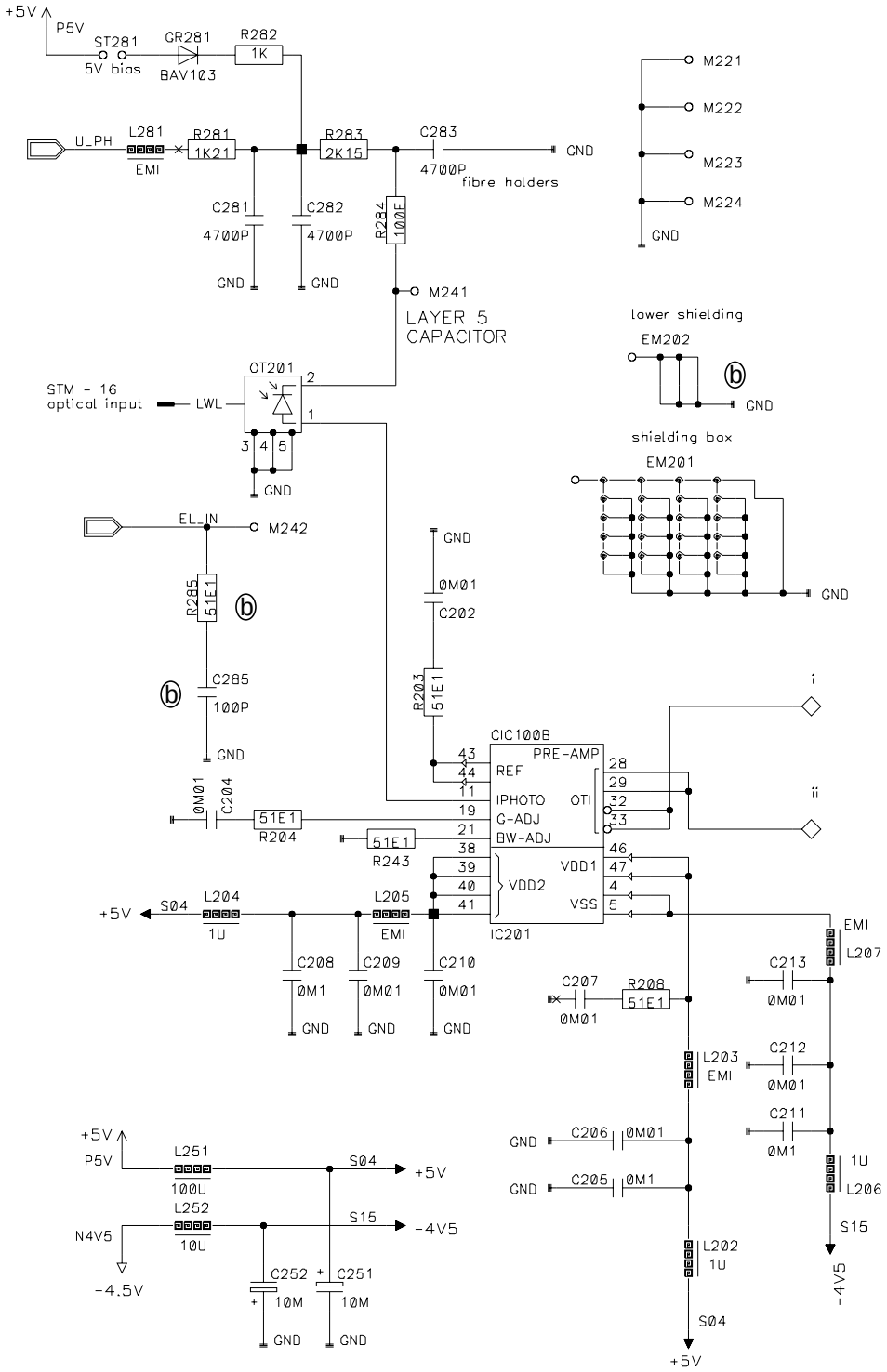
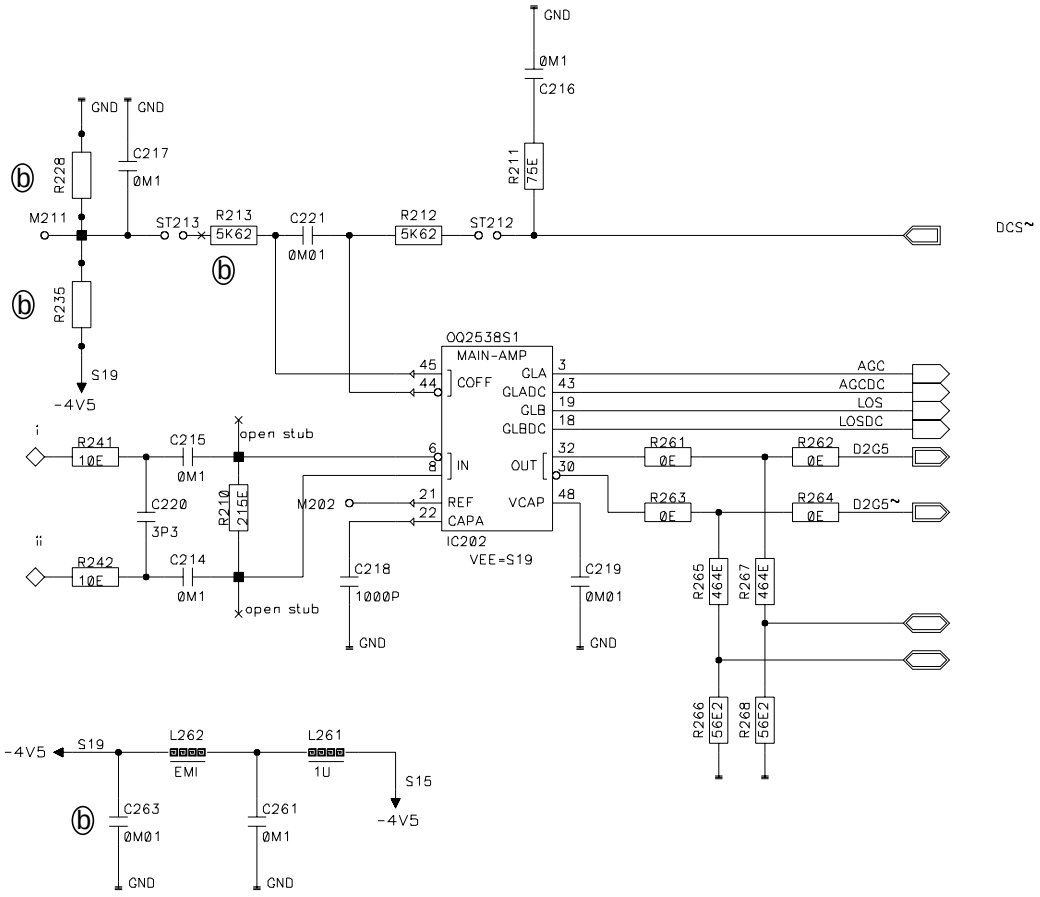
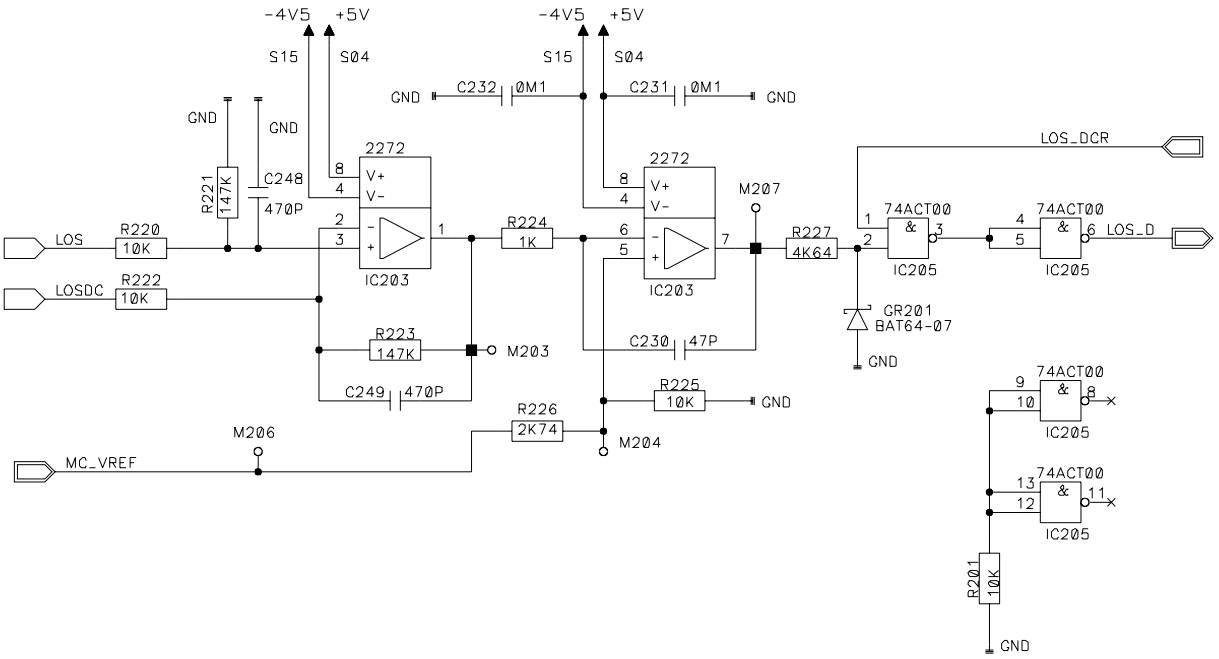


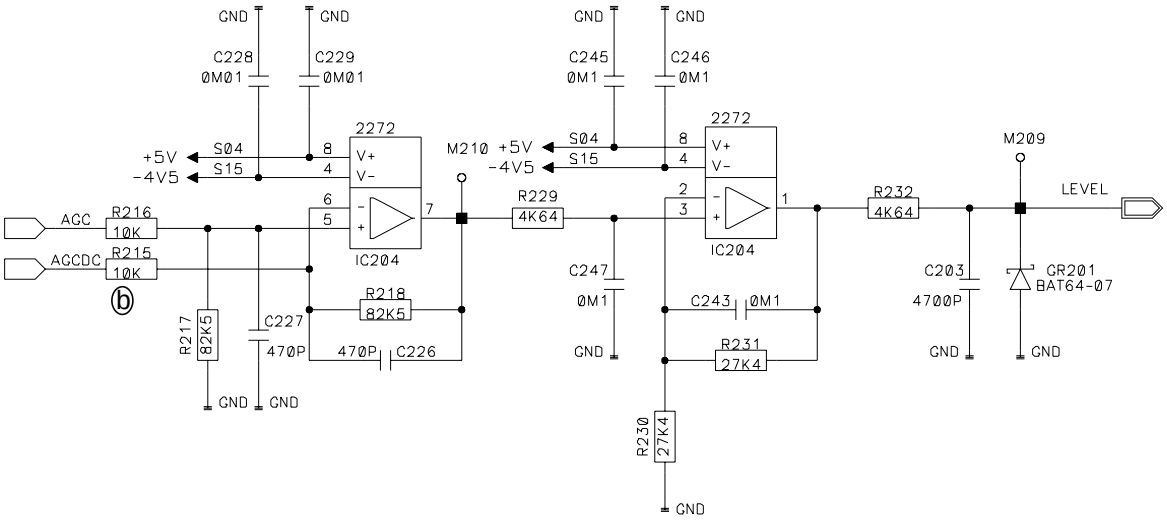
Photo Diode Control Module
PDCM/1.drw
page 2 of 2



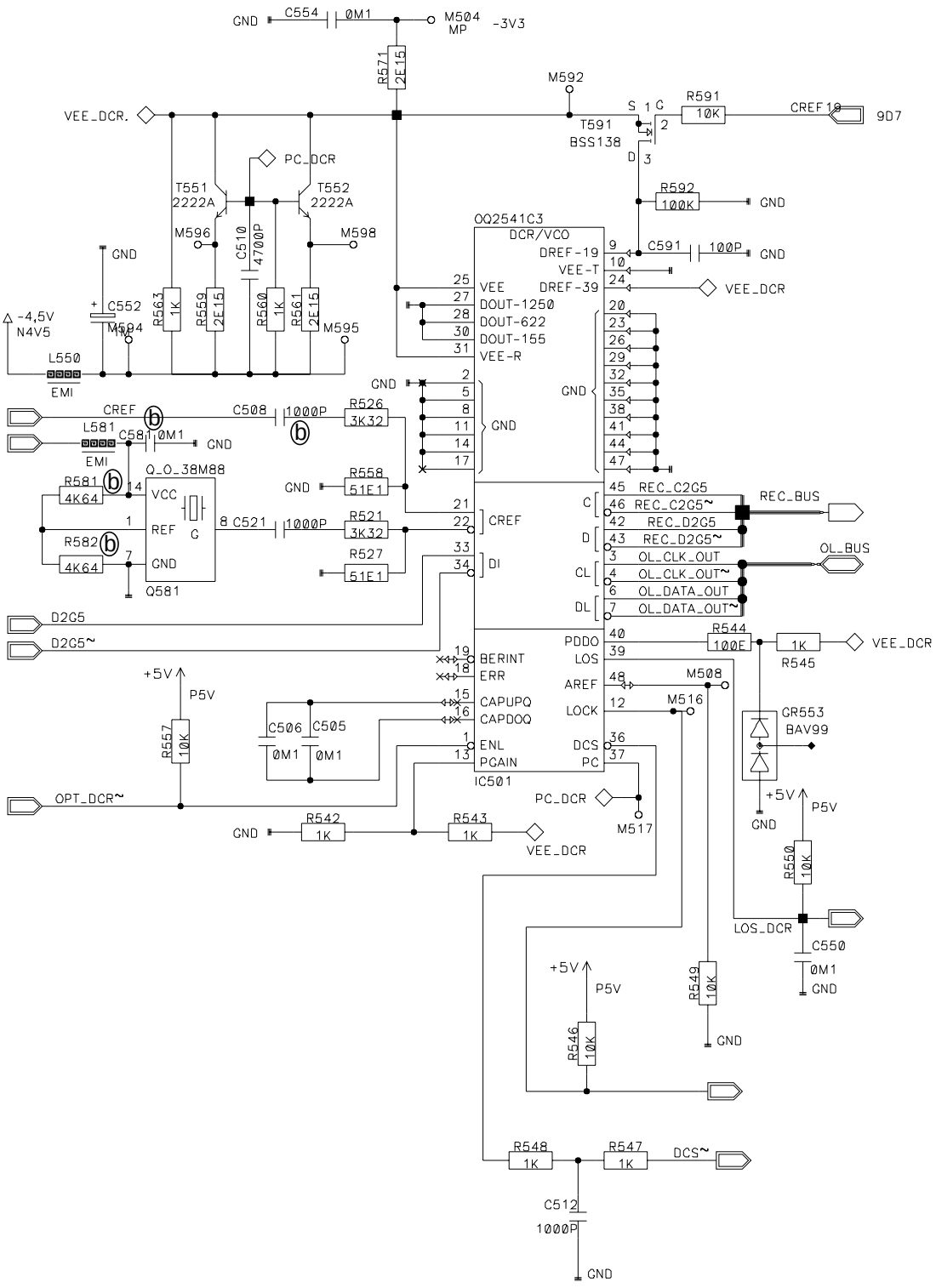
Optical Receiver Module
ORM/1.drw
page 1 of 2


GND
ØM1
C216
R211
75E
GND
GND
C217
ØM1
R228
M211
ST213
R213
5K62
C221
ØM1
R212
5K62
ST212
DCS~
R235
S19
-4V5
OQ2538S1
MAIN-AMP
45
44
COFF
GLA
GLADC
GLB
GLBDC
3
43
19
18
AGC
AGCDC
LOS
LOSDC
i
R241
10E
C215
ØM1
open stub
6
8
IN
OUT
32
30
R261
ØE
R262
ØE
D2G5
C220
3P3
R210
215E
M202
21
22
REF
CAPA
VCAP
48
R263
ØE
R264
ØE
D2G5~
ii
R242
10E
C214
ØM1
open stub
IC202
VEE=S19
C218
1000P
GND
C219
ØM01
GND
R265
464E
R267
464E
R266
56E2
R268
56E2
-4V5
S19
L262
EMI
L261
1U
S15
-4V5
C263
ØM01
GND
C261
ØM1
GND

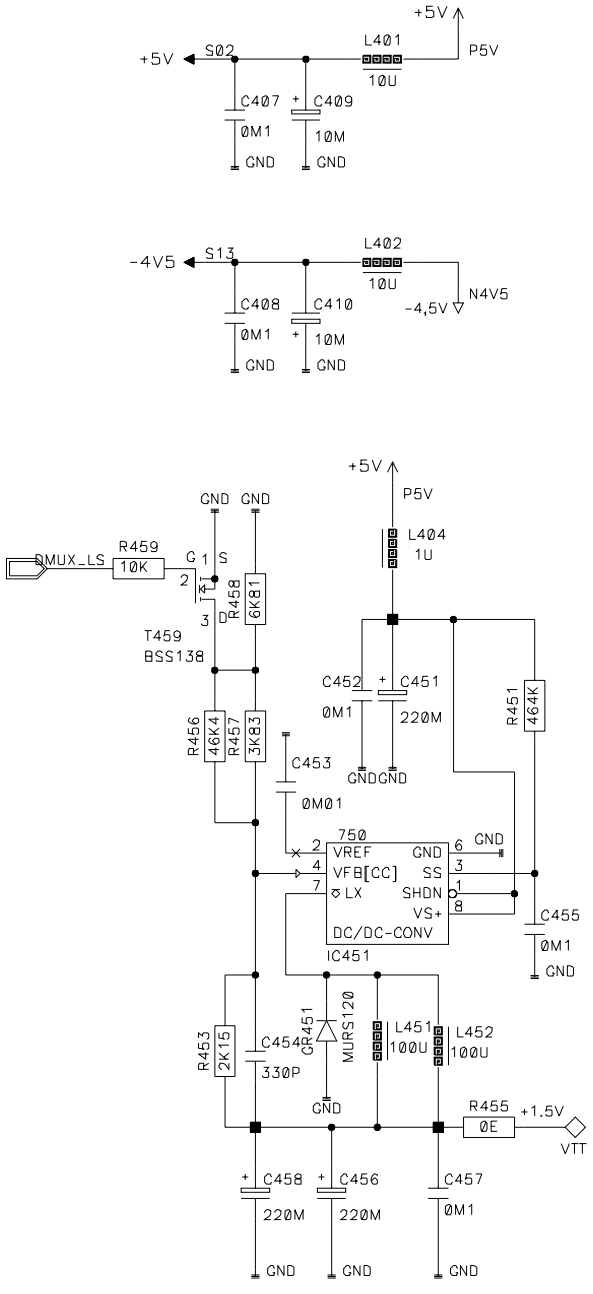




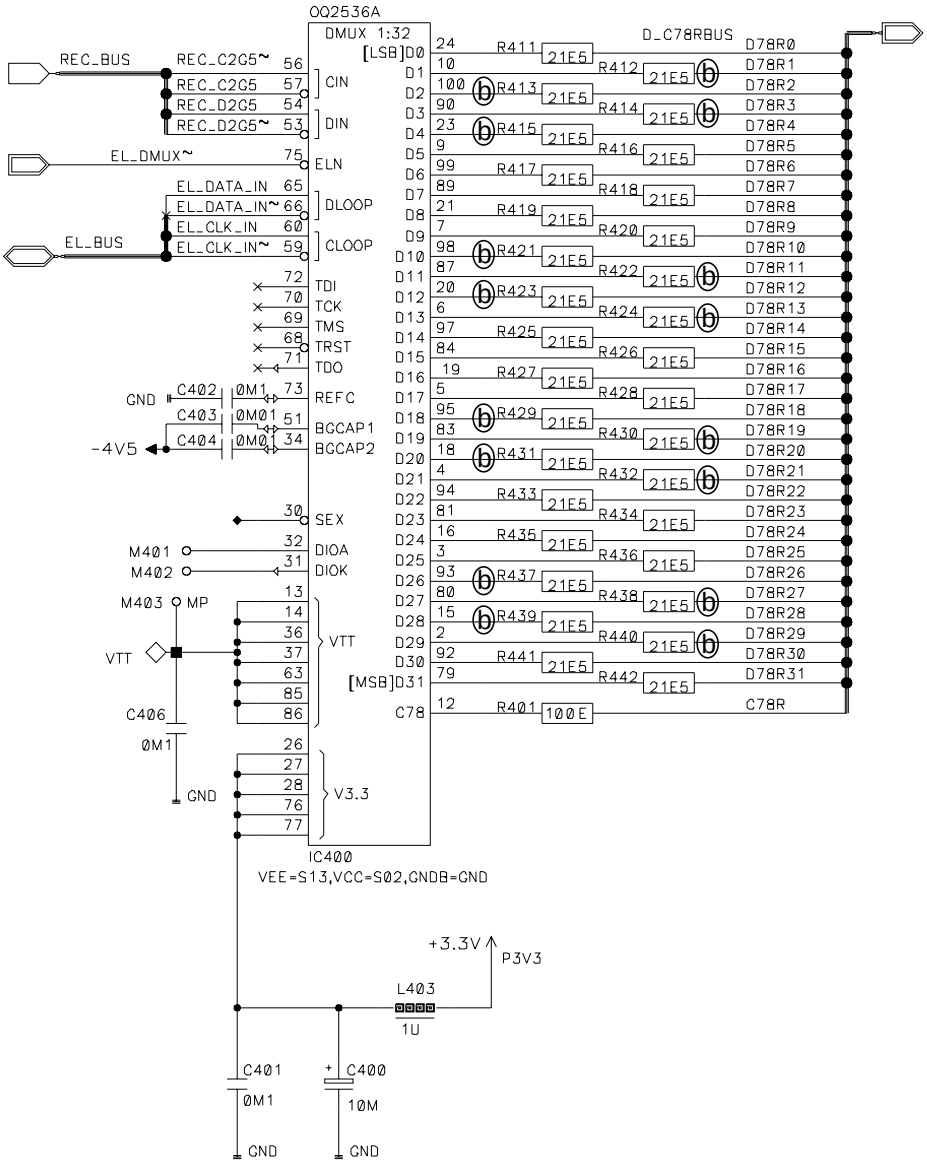
Optical Receiver Module
ORM/2.drw
page 1 of 2



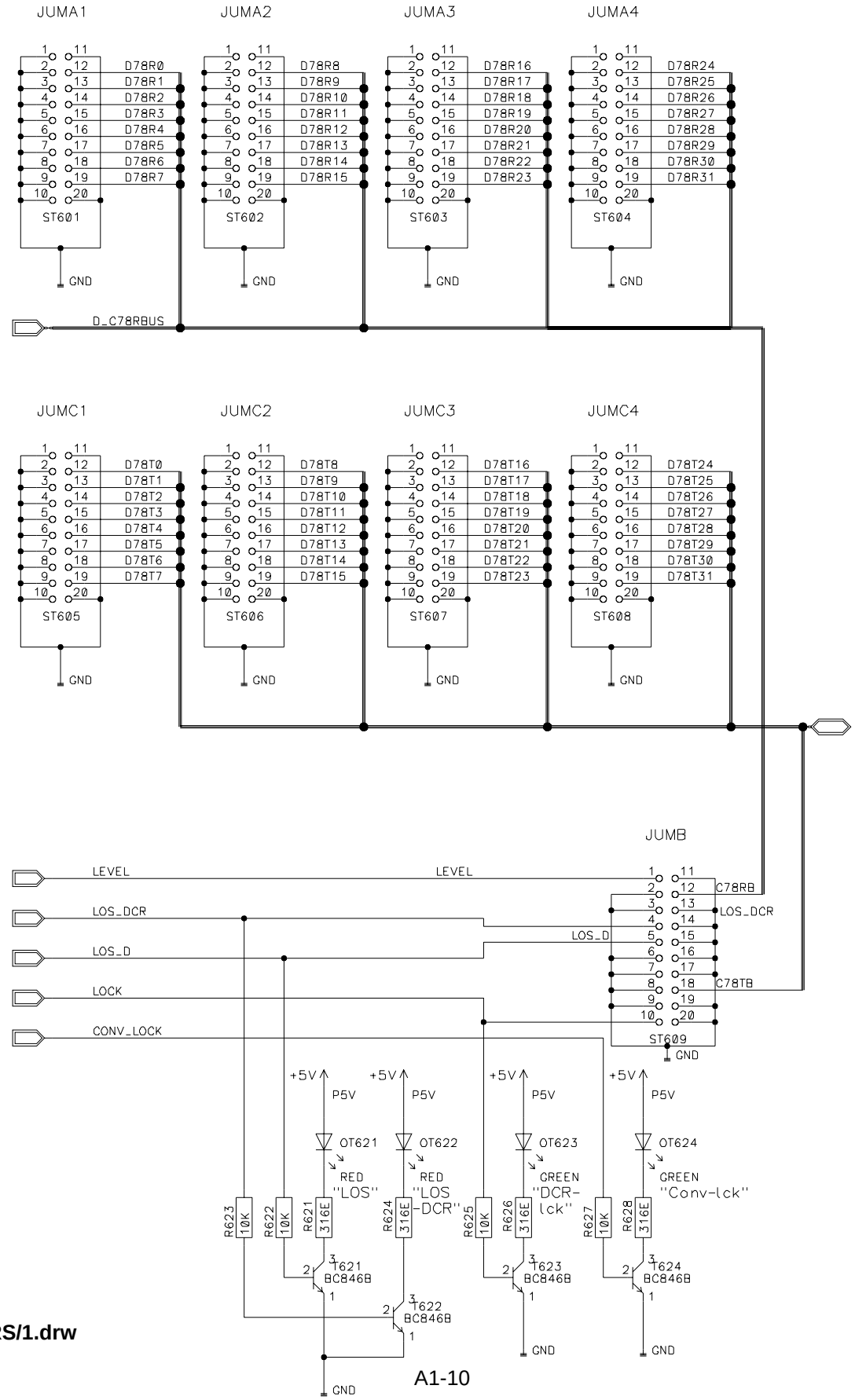
Data and Clock Recovery
DCR/1.drw
page 2 of 2



Data and Clock Recovery
DCR/2.drw
page 1 of 2



Data and Clock Recovery
DCR/2.drw
page 2 of 2


JUMA1
JUMA2
JUMA3
JUMA4
D78R0
D78R1
D78R2
D78R3
D78R4
D78R5
D78R6
D78R7
D78R8
D78R9
D78R10
D78R11
D78R12
D78R13
D78R14
D78R15
D78R16
D78R17
D78R18
D78R19
D78R20
D78R21
D78R22
D78R23
D78R24
D78R25
D78R26
D78R27
D78R28
D78R29
D78R30
D78R31
ST601
ST602
ST603
ST604
GND
D_C78RBUS
JUMC1
JUMC2
JUMC3
JUMC4
D78T0
D78T1
D78T2
D78T3
D78T4
D78T5
D78T6
D78T7
D78T8
D78T9
D78T10
D78T11
D78T12
D78T13
D78T14
D78T15
D78T16
D78T17
D78T18
D78T19
D78T20
D78T21
D78T22
D78T23
D78T24
D78T25
D78T26
D78T27
D78T28
D78T29
D78T30
D78T31
ST605
ST606
ST607
ST608
JUMB
LEVEL
LOS_DCR
LOS_D
LOCK
CONV_LOCK
C78RB
C78TB
ST609
+5V
P5V
OT621
OT622
OT623
OT624
RED
"LOS"
"LOS -DCR"
GREEN
"DCR-lck"
"Conv-lck"
R623 10K
R622 10K
R621 316E
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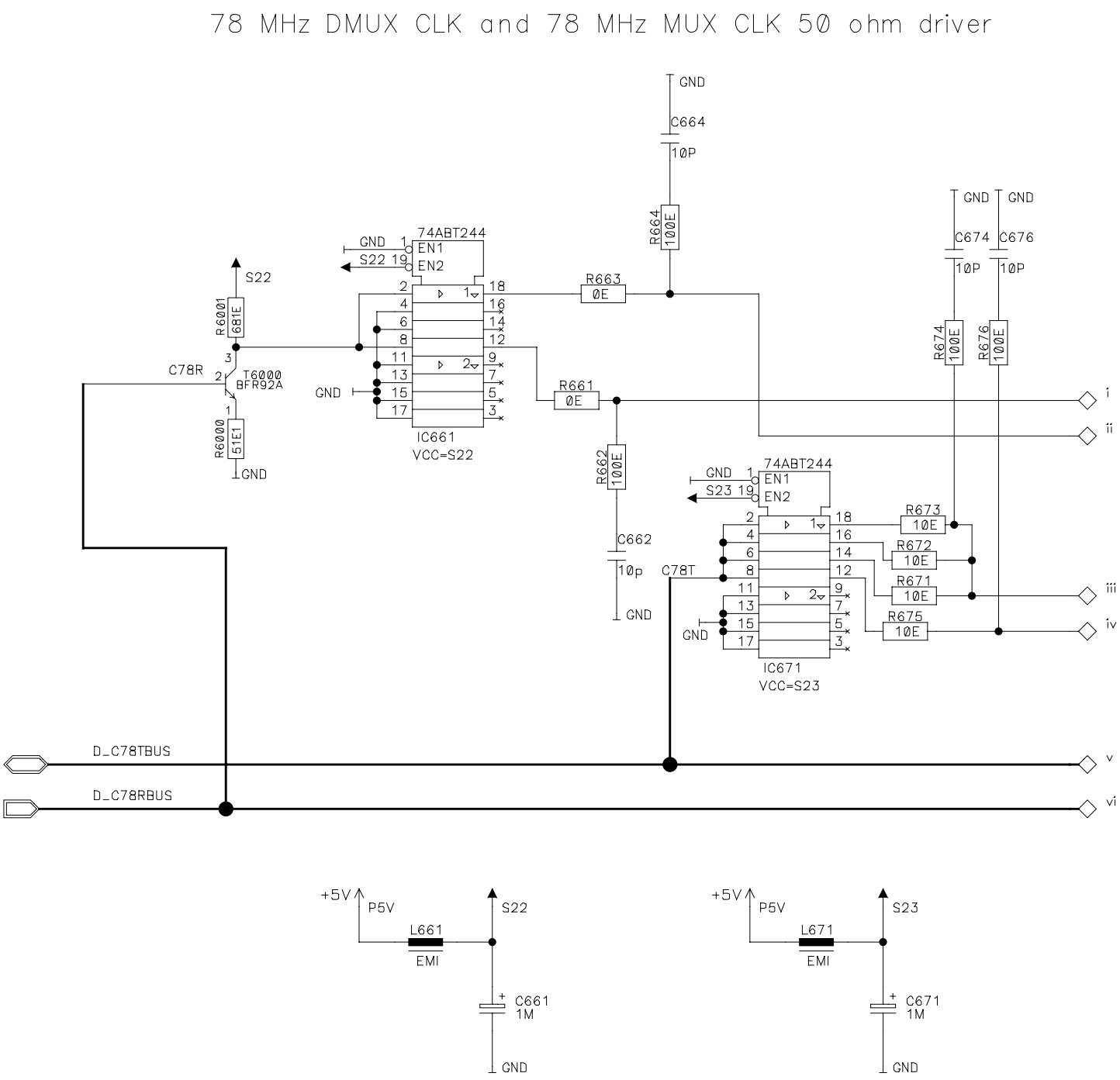
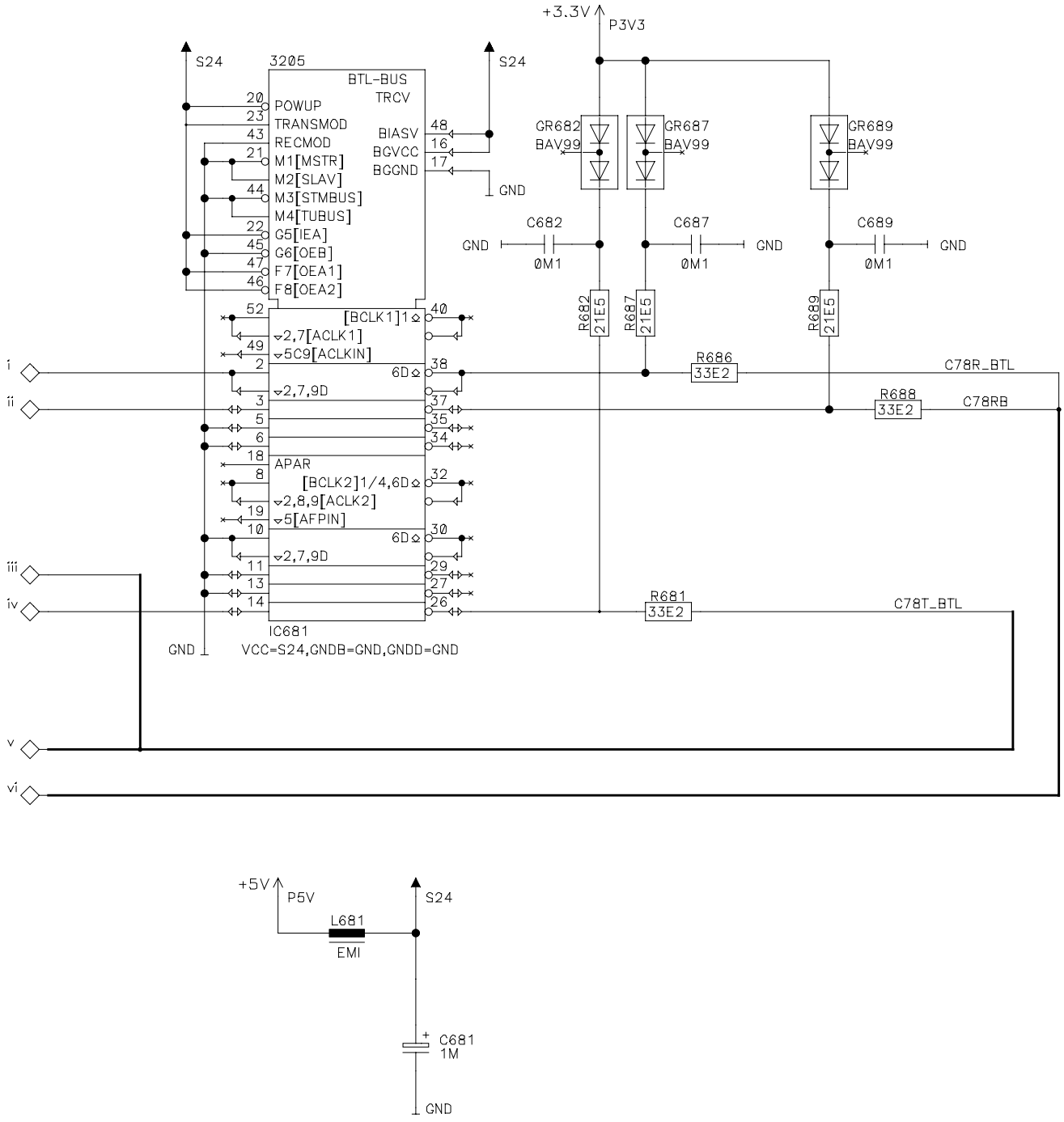
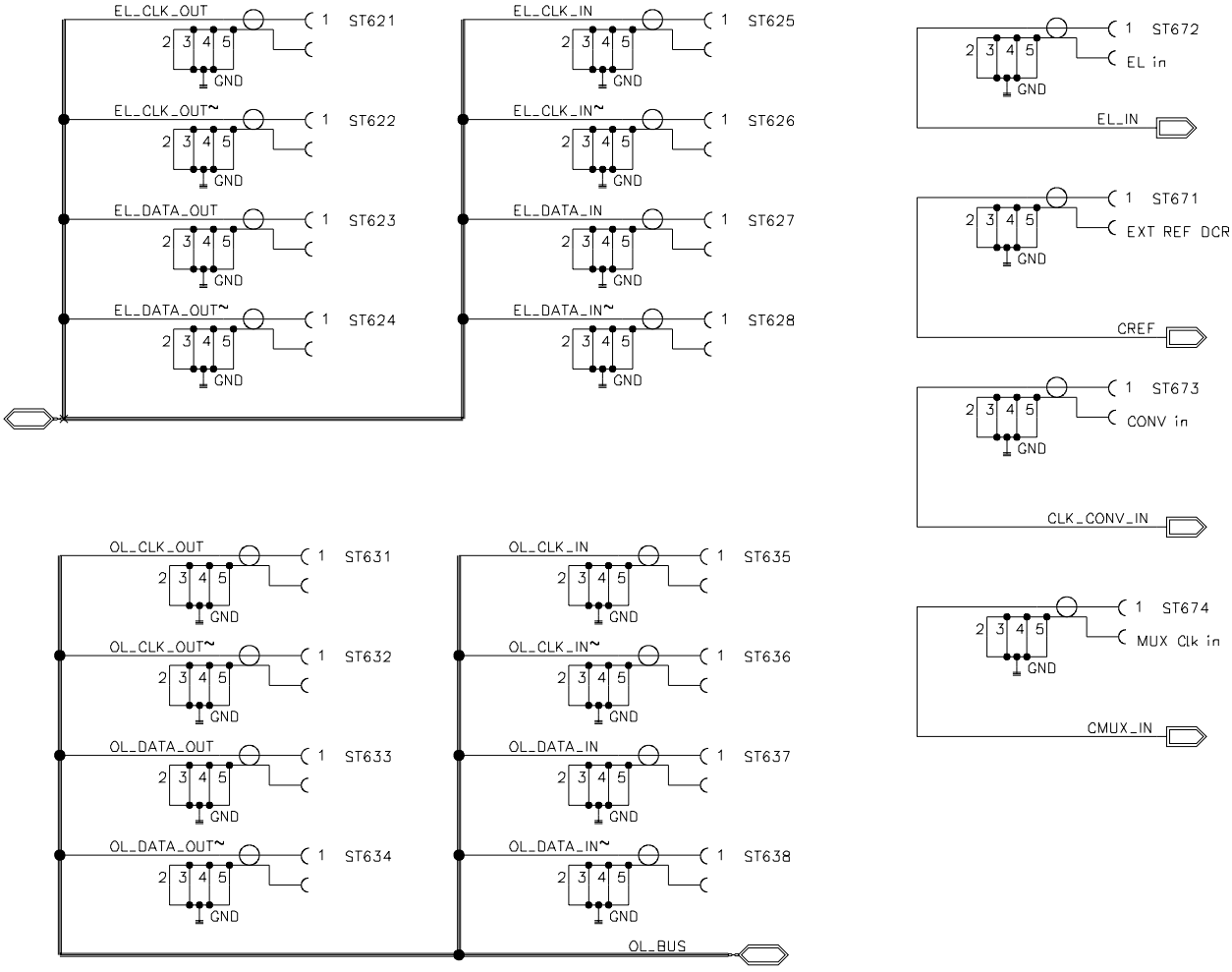
T621 BC846B
T622 BC846B
T623 BC846B
T624 BC846B

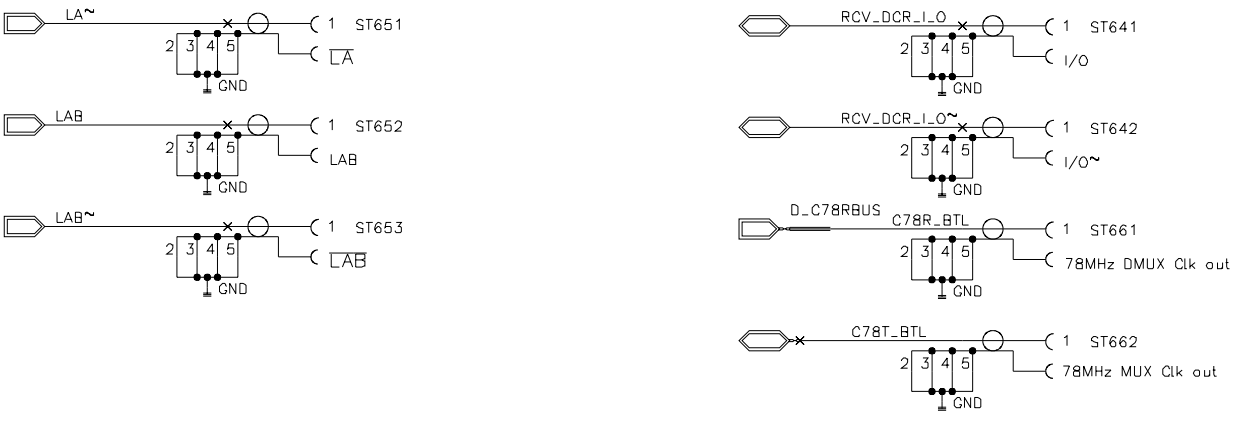


CONNECTORS/2.drw
page 1 of 2



CONNECTORS/2.drw
page 2 of 2





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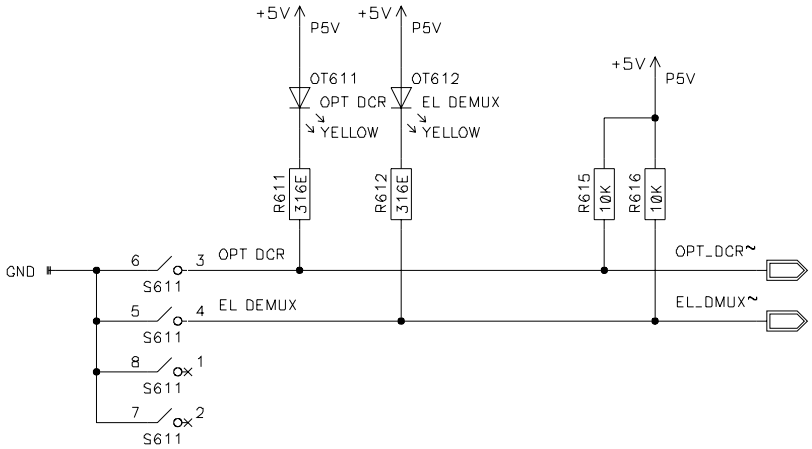
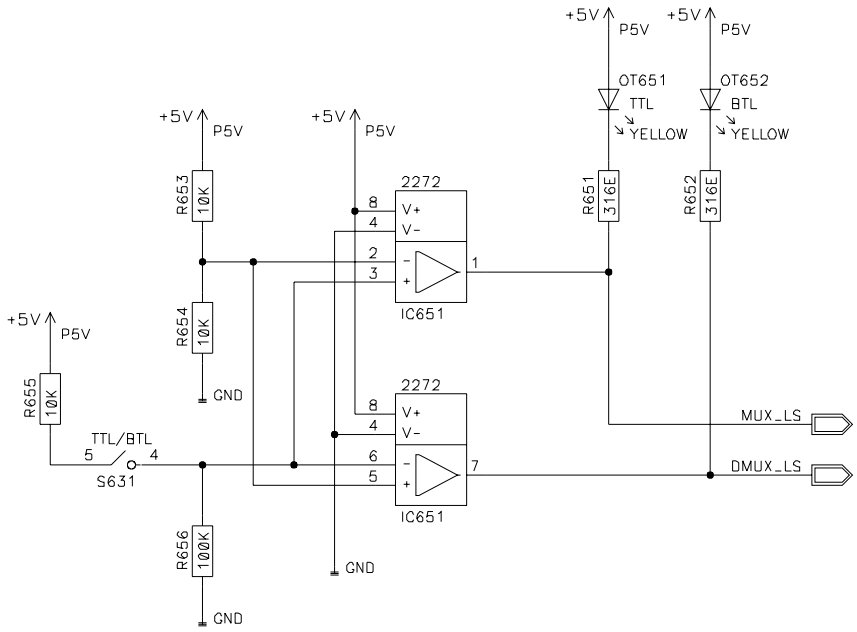
page 1 of 1





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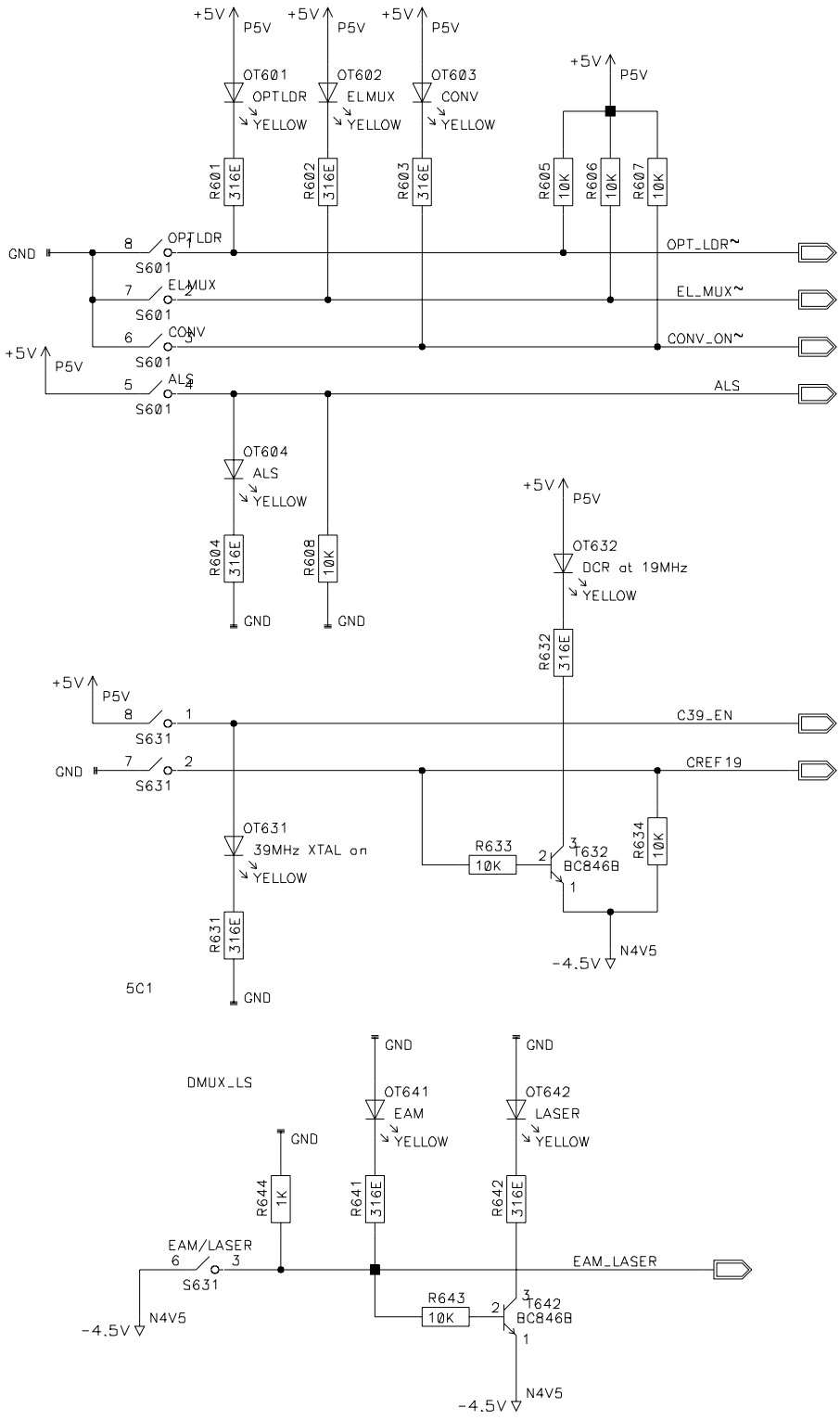
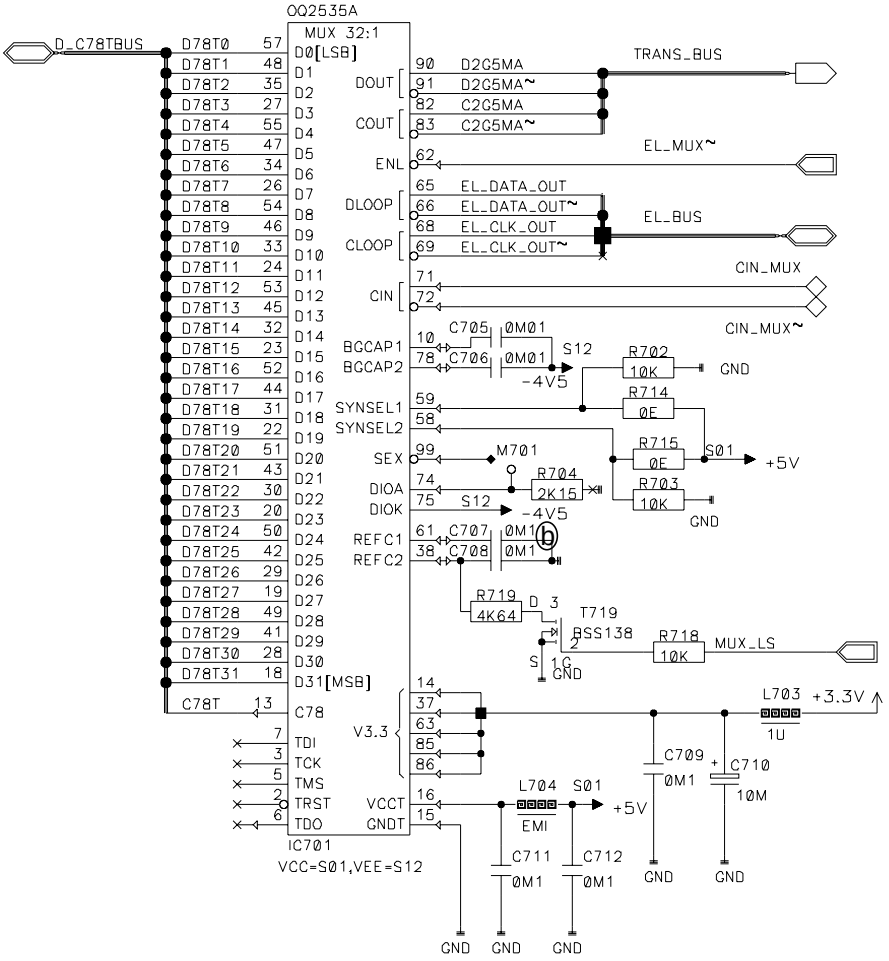
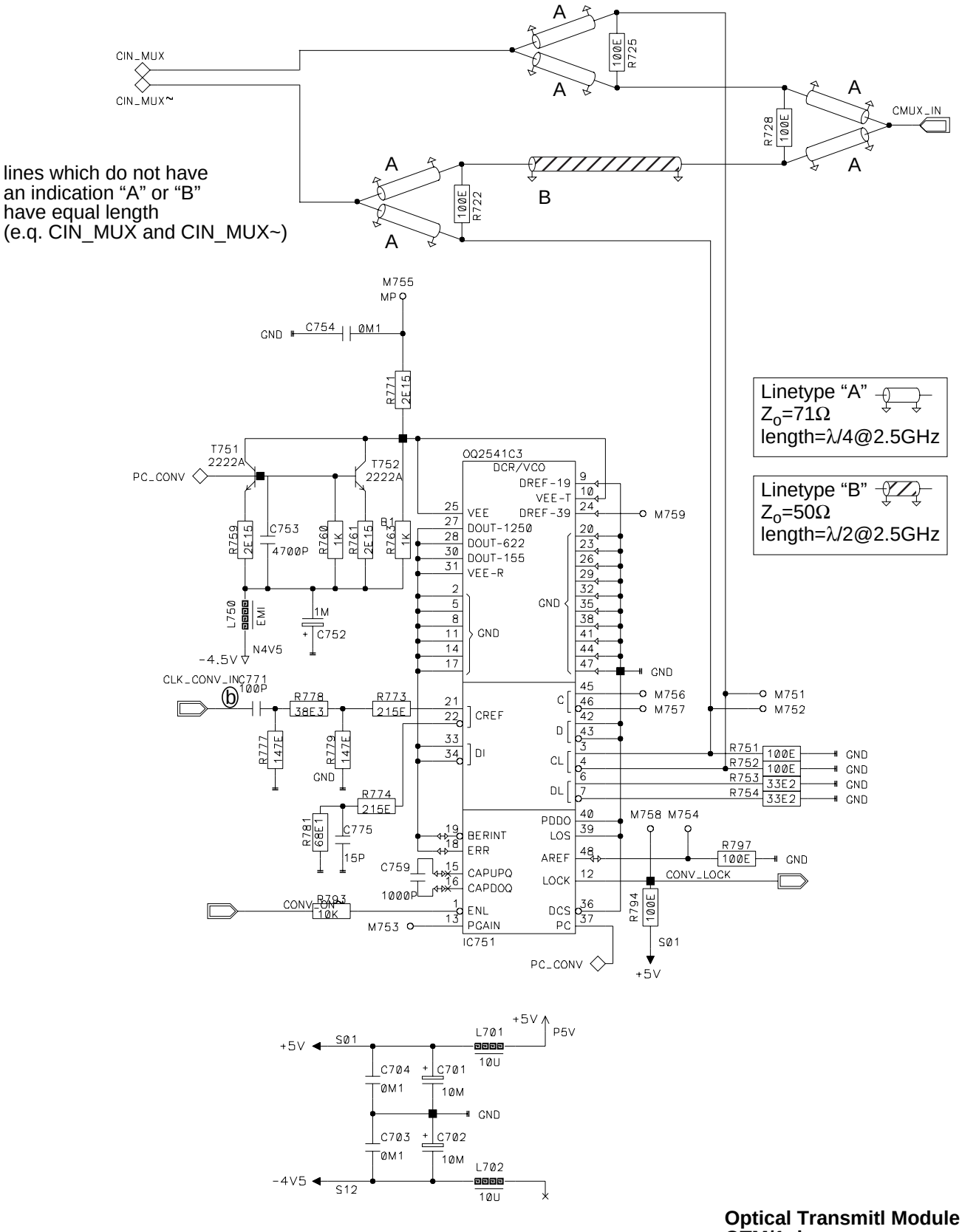
page 1 of 2

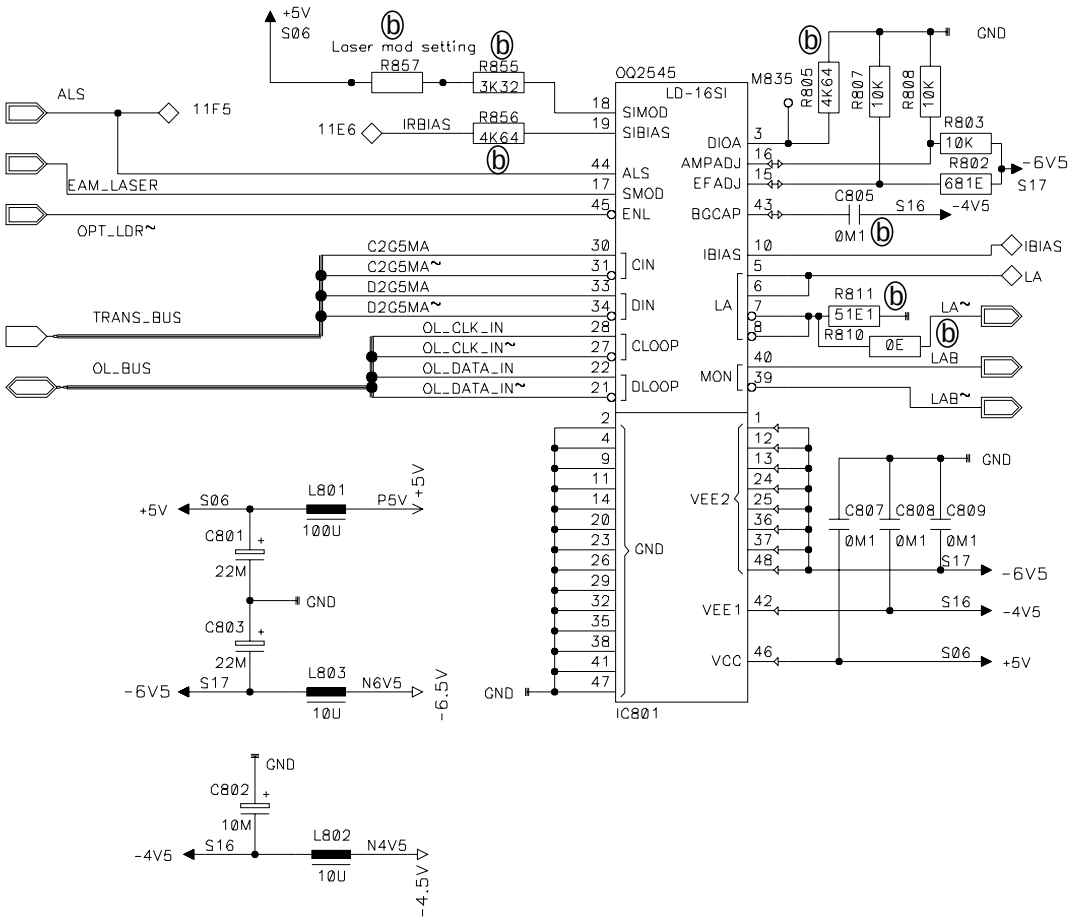


CONNECTORS/4.drw
page 2 of 2

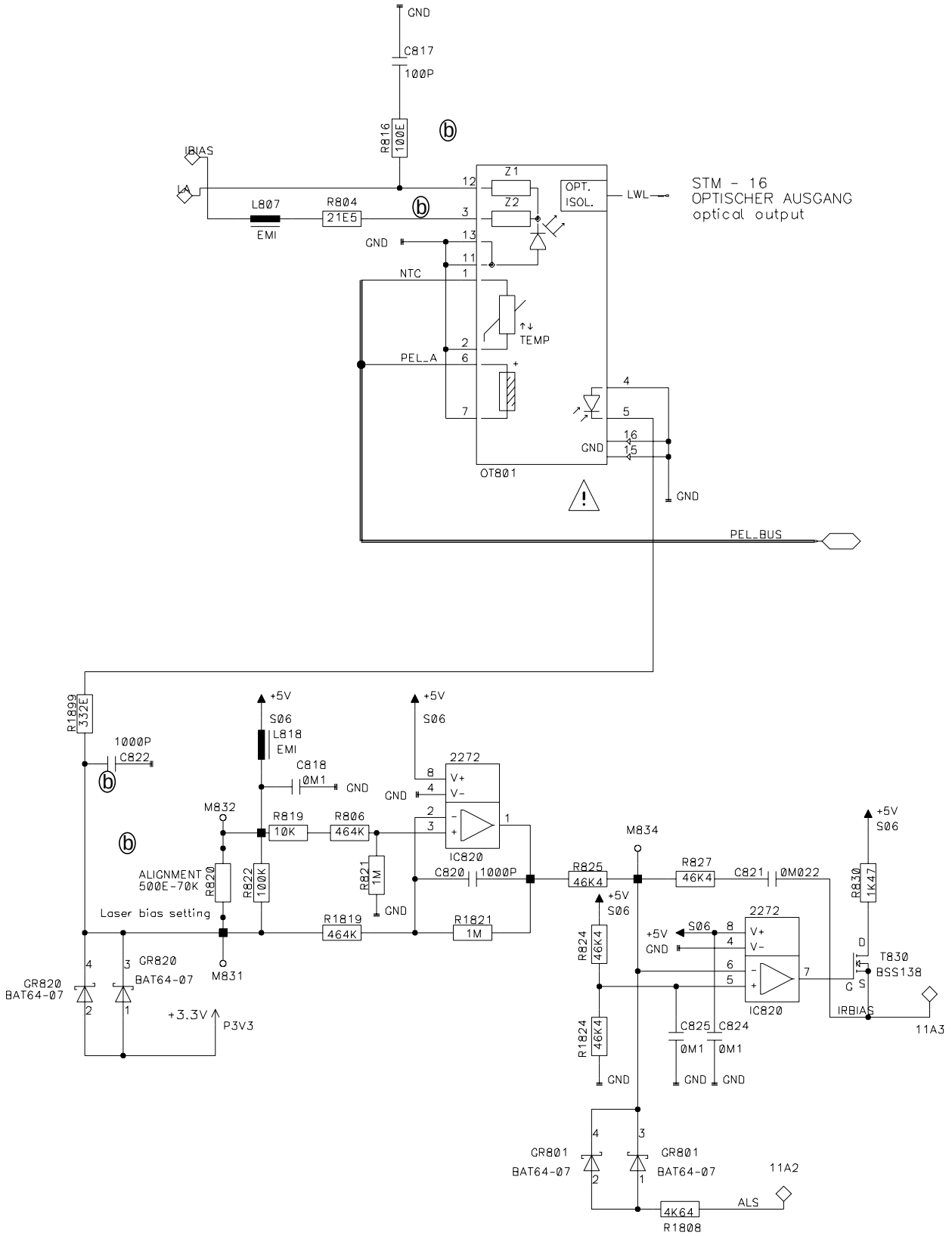

OQ2535A
MUX 32:1
D_C78TBUS
D78T0 57
D78T1 48
D78T2 35
D78T3 27
D78T4 55
D78T5 47
D78T6 34
D78T7 26
D78T8 54
D78T9 46
D78T10 33
D78T11 24
D78T12 53
D78T13 45
D78T14 32
D78T15 23
D78T16 52
D78T17 44
D78T18 31
D78T19 22
D78T20 51
D78T21 43
D78T22 30
D78T23 20
D78T24 50
D78T25 42
D78T26 29
D78T27 19
D78T28 49
D78T29 41
D78T30 28
D78T31 18
C78T 13
D0[LSB]
D31[MSB]
C78
DOUT
COUT
ENL
DLOOP
CLOOP
CIN
BGCAP1
BGCAP2
SYNSEL1
SYNSEL2
SEX
DIOA
DIOK
REFC1
REFC2
V3.3
VCCT
GNDT
TDI
TCK
TMS
TRST
TDO
IC701
VCC=S01,VEE=S12
90 D2C5MA
91 D2C5MA~
82 C2C5MA
83 C2C5MA~
TRANS_BUS
62
EL_MUX~
65 EL_DATA_OUT
66 EL_DATA_OUT~
68 EL_CLK_OUT
69 EL_CLK_OUT~
EL_BUS
71
72
CIN_MUX
CIN_MUX~
C705 0M01
C706 0M01
10
78
S12
-4V5
R702 10K
GND
R714 0E
59
58
M701
R715 0E
S01
+5V
R704 2K15
R703 10K
74
75
S12
-4V5
GND
61 C707 0M1
38 C708 0M1
R719 4K64
D 3
T719 BSS138
2
S 1 G
R718 10K
MUX_LS
GND
14
37
63
85
86
L703 +3.3V
1U
C709 0M1
C710 10M
16
15
L704 EMI
S01
+5V
C711 0M1
C712 0M1
GND
GND
GND
GND
GND



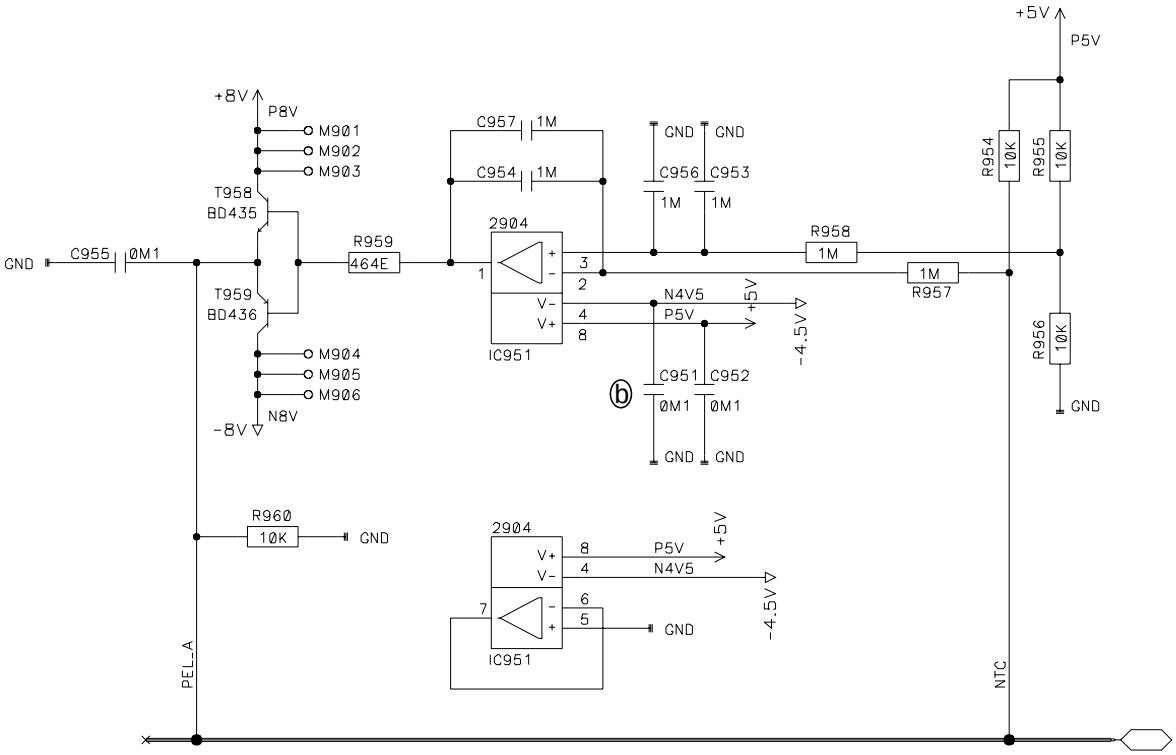
Optical Transmitl Module
OTM/1.drw
page 2 of 2

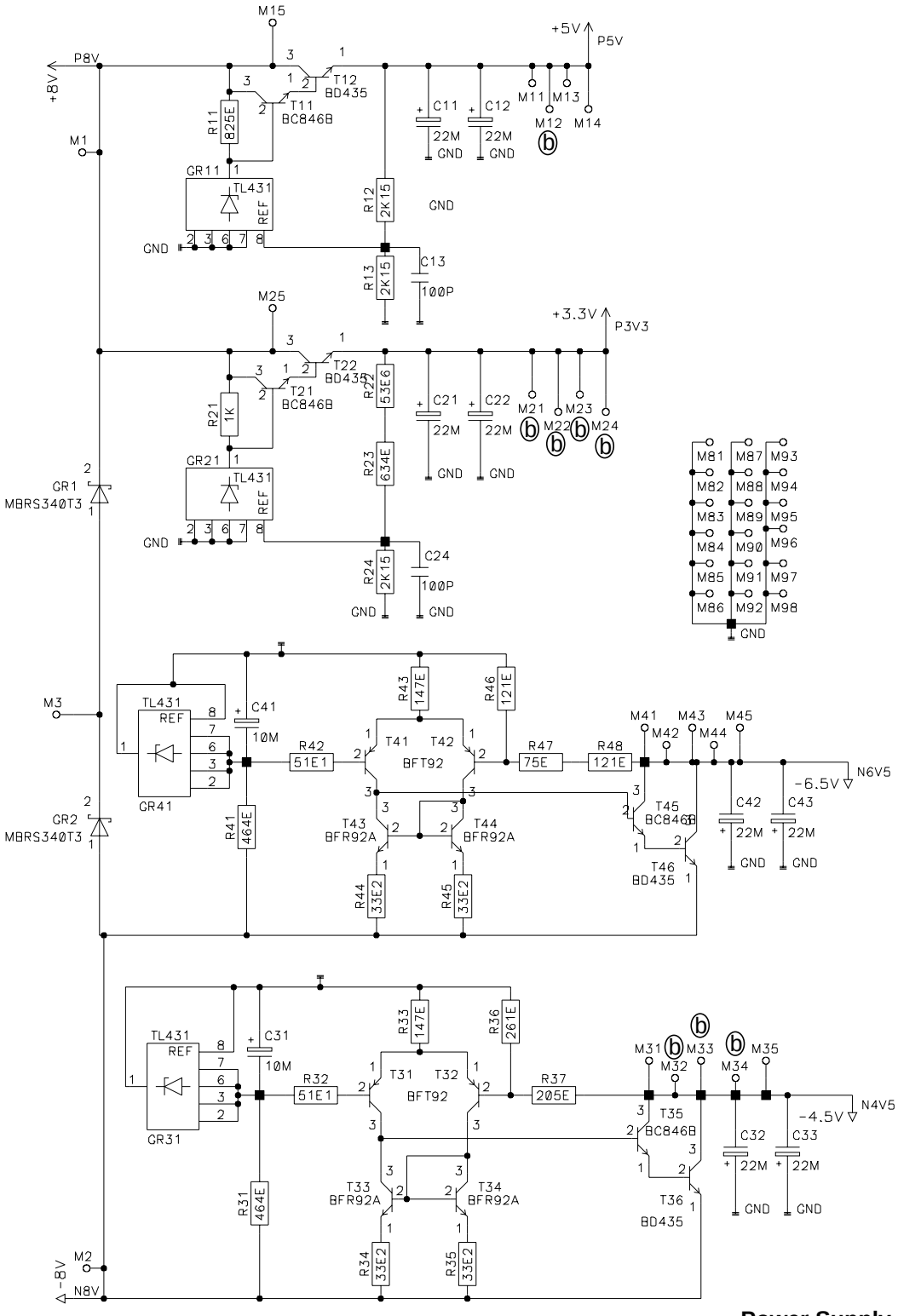


Optical Transmit Module
OTM/2.drw
page 1 of 2



Optical Transmit Module
OTM/2.drw
page 2 of 2


+5V
P5V
+8V
P8V
M901
M902
M903
T958
BD435
T959
BD436
M904
M905
M906
N8V
-8V
GND
C955
0M1
R959
464E
C957
1M
C954
1M
2904
IC951
C956
C953
R958
1M
R957
N4V5
-4.5V
C951
C952
R954
10K
R955
10K
R956
10K
R960
10K
PEL_A
NTC



Power Supply Module
PSM/1.drw
page 1 of 1

APPENDIX 2 CML

CML, Current Mode Logic, is used in the STM16 chipset as high speed point to point logic standard. CML has been chosen above ECL, E2CL and PECL for its high immunity against interference in combination with low power consumption.

Current Mode Logic is a **differential** logic standard, defined in a 50 ohm environment. Load impedance is matched to 50 ohm, source is set to 100 ohm, to meet both matching and power consumption recommendations. The main characteristic of this logic standerd are:

1 - Ground plane as reference voltage

2 - Adapted to 50 ohm

3 - Completely differential transport of signals

4 - Low voltage swing

The reason for these choices are the following:

1 - Ground plane as reference voltage

CML is defined against ground, and not against a bias voltage, as is with ECL. This guarantees a good ground plane, thus high interference immunity.

2 - Adapted to 50 ohm characteristic impedance transmission line

CML is defined in a 50 ohm environment. Sources are differential stages with 100 ohm collector resistors. This guarentees a broadband VSWR lower than 3:1. 100 ohm has been chosen to meet both matching- and power consumption requirements. Inputs are on-chip terminated with 50 ohm resistors, guarenteeing a matched broadband load. Due to this good termination, reflection will not travel back to the output of the previous stage. Internal matching guarentees also no parasitic influences of termination resistor pad capacitance. 50 ohm enables the use of standard transmission lines, or coupled (microstrip) transmission lines.

3 - Completely differential transport of signals

CML is a completely differential logic. Therefore it has a ‘built in’ high interference immunity.

4 - Low voltage swing

Following this high immunity, the voltage swing can be low: 200 mV_{pp}, compared with 800 mV_{pp} for ECL. This reduces the power consumption of the driver stages.

APPENDIX 3 Partslist

TABLE 8 Mounted components

Name	Description	Name	Description
C11	C EL 7343 # 22M 20 % 35V	C243	C 0805H X7R# 0M1 10 % 25V
C12	C EL 7343 # 22M 20 % 35V	C245	C 0805H X7R# 0M1 10 % 25V
C13	C 0805H C0G# 100P 2 % 200V	C246	C 0805H X7R# 0M1 10 % 25V
C21	C EL 7343 # 22M 20 % 35V	C247	C 0805H X7R# 0M1 10 % 25V
C22	C EL 7343 # 22M 20 % 35V	C248	C 0805H C0G# 470P 2 % 50V
C24	C 0805H C0G# 100P 2 % 200V	C249	C 0805H C0G# 470P 2 % 50V
C31	C EL 6032 # 10M 20 % 16V	C251	C EL 6032 # 10M 20 % 16V
C32	C EL 7343 # 22M 20 % 35V	C252	C EL 6032 # 10M 20 % 16V
C33	C EL 7343 # 22M 20 % 35V	C261	C 0805H X7R# 0M1 10 % 25V
C41	C EL 6032 # 10M 20 % 16V	C263	C 0805H X7R# 0M01 10 % 50V
C42	C EL 7343 # 22M 20 % 35V	C281	C 1206H X7R# 4700P 10 % 200V
C43	C EL 7343 # 22M 20 % 35V	C282	C 1206H X7R# 4700P 10 % 200V
C202	C 0805H X7R# 0M01 10 % 50V	C283	C 1206H X7R# 4700P 10 % 200V
C203	C 0805H X7R# 4700P 10 % 50V	C285	C 0805H C0G# 100P 2 % 200V
C204	C 0805H X7R# 0M01 10 % 50V	C301	C 0805H X7R# 1000P 10 % 200V
C205	C 0805H X7R# 0M1 10 % 25V	C321	C 0805H C0G# 100P 2 % 200V
C206	C 0805H X7R# 0M01 10 % 50V	C322	C 0805H C0G# 470P 2 % 50V
C207	C 0805H X7R# 0M01 10 % 50V	C351	C 0805H X7R# 0M01 10 % 50V
C208	C 0805H X7R# 0M1 10 % 25V	C389	C 0805H C0G# 100P 2 % 200V
C209	C 0805H X7R# 0M01 10 % 50V	C391	C EL 6032 # 10M 20 % 16V
C210	C 0805H X7R# 0M01 10 % 50V	C392	C EL 6032 # 10M 20 % 16V
C211	C 0805H X7R# 0M1 10 % 25V	C393	C 0805H X7R# 0M1 10 % 25V
C212	C 0805H X7R# 0M01 10 % 50V	C397	C 0805H X7R# 0M1 10 % 25V
C213	C 0805H X7R# 0M01 10 % 50V	C398	C 0805H X7R# 0M1 10 % 25V
C214	C 0805H X7R# 0M1 10 % 25V	C400	C EL 6032 # 10M 20 % 16V
C215	C 0805H X7R# 0M1 10 % 25V	C401	C 0805H X7R# 0M1 10 % 25V
C216	C 0805H X7R# 0M1 10 % 25V	C402	C 0805H X7R# 0M1 10 % 25V
C217	C 0805H X7R# 0M1 10 % 25V	C403	C 0805H X7R# 0M01 10 % 50V
C218	C 0805H X7R# 1000P 10 % 50V	C404	C 0805H X7R# 0M01 10 % 50V
C219	C 0805H X7R# 0M01 10 % 50V	C406	C 0805H X7R# 0M1 10 % 25V
C220	C 0805H HQ # 3P3 0,1P 50V	C407	C 0805H X7R# 0M1 10 % 25V
C221	C 0805H X7R# 0M01 10 % 50V	C408	C 0805H X7R# 0M1 10 % 25V
C226	C 0805H C0G# 470P 2 % 50V	C409	C EL 6032 # 10M 20 % 16V
C227	C 0805H C0G# 470P 2 % 50V	C410	C EL 6032 # 10M 20 % 16V
C228	C 0805H X7R# 0M01 10 % 50V	C451	C EL 7343 # 220M 20 % 10V
C229	C 0805H X7R# 0M01 10 % 50V	C452	C 0805H X7R# 0M1 10 % 25V
C230	C 0805H C0G# 47P 2 % 50V	C453	C 0805H X7R# 0M01 10 % 50V
C231	C 0805H X7R# 0M1 10 % 25V	C454	C 1206H C0G# 330P 10 % 200V
C232	C 0805H X7R# 0M1 10 % 25V	C455	C 0805H X7R# 0M1 10 % 25V

TABLE 8 Mounted components

Name	Description	Name	Description
C457	C 0805H X7R# 0M1 10 % 25V	C775	C 0805H C0G# 15P 0,25P 50V
C458	C EL 7343 # 220M 20 % 10V	C801	C EL 7243 # 22M 20 % 20V
C505	C 0805H X7R# 0M1 10 % 25V	C802	C EL 6032 # 10M 20 % 16V
C506	C 0805H X7R# 0M1 10 % 25V	C803	C EL 7243 # 22M 20 % 20V
C508	C 0805H X7R# 1000P 10 % 50V	C805	C 0805H X7R# 0M1 10 % 25V
C510	C 0805H X7R# 4700P 10 % 50V	C807	C 0805H X7R# 0M1 10 % 25V
C512	C 0805H X7R# 1000P 10 % 50V	C808	C 0805H X7R# 0M1 10 % 25V
C521	C 0805H X7R# 1000P 10 % 50V	C809	C 0805H X7R# 0M1 10 % 25V
C550	C 0805H X7R# 0M1 10 % 25V	C817	C 0805H HQ # 1P 0,1P 50V
C552	C EL 3528 # 1M 20 % 35V	C817	C 0805H C0G# 100P 2 % 200V
C554	C 0805H X7R# 0M1 10 % 25V	C818	C 0805H X7R# 0M1 10 % 25V
C581	C 0805H X7R# 0M1 10 % 25V	C820	C 0805H X7R# 1000P 10 % 50V
C591	C 0805H C0G# 100P 2 % 200V	C821	C 0805H X7R# 0M022 10 % 50V
C661	C EL 3528 # 1M 20 % 35V	C822	C 0805H X7R# 1000P 10 % 50V
C662	C 0805H HQ # 10P 1 % 50V	C824	C 0805H X7R# 0M1 10 % 25V
C664	C 0805H HQ # 10P 1 % 50V	C825	C 0805H X7R# 0M1 10 % 25V
C671	C EL 3528 # 1M 20 % 35V	C951	C 0805H X7R# 0M1 10 % 25V
C674	C 0805H HQ # 10P 1 % 50V	C952	C 0805H X7R# 0M1 10 % 25V
C676	C 0805H HQ # 10P 1 % 50V	C953	C 2220H X7R# 1M 10 % 50V
C681	C EL 3528 # 1M 20 % 35V	C954	C 2220H X7R# 1M 10 % 50V
C682	C 0805H X7R# 0M1 10 % 25V	C955	C 0805H X7R# 0M1 10 % 25V
C687	C 0805H X7R# 0M1 10 % 25V	C956	C 2220H X7R# 1M 10 % 50V
C689	C 0805H X7R# 0M1 10 % 25V	C957	C 2220H X7R# 1M 10 % 50V
C701	C EL 6032 # 10M 20 % 16V	EM201	EMC SHIELD
C702	C EL 6032 # 10M 20 % 16V	EM202	EMC SHIELD TOP
C703	C 0805H X7R# 0M1 10 % 25V	GR1	SI DIODE # MBRS 340
C704	C 0805H X7R# 0M1 10 % 25V	GR2	SI DIODE # MBRS 340
C705	C 0805H X7R# 0M01 10 % 50V	GR11	REF-ELEMENT# TL 431AID
C706	C 0805H X7R# 0M01 10 % 50V	GR21	REF-ELEMENT# TL 431AID
C707	C 0805H X7R# 0M1 10 % 25V	GR31	REF-ELEMENT# TL 431AID
C708	C 0805H X7R# 0M1 10 % 25V	GR41	REF-ELEMENT# TL 431AID
C709	C 0805H X7R# 0M1 10 % 25V	GR201	2SI DIODE # BAT 64-07
C710	C EL 6032 # 10M 20 % 16V	GR281	SI DIODE # BAV 103
C711	C 0805H X7R# 0M1 10 % 25V	GR301	SI DIODE # BAV 103
C712	C 0805H X7R# 0M1 10 % 25V	GR321	2SI DIODE # BAT 64-07
C752	C EL 3528 # 1M 20 % 35V	GR351	2SI DIODE # BAT 64-07
C753	C 0805H X7R# 4700P 10 % 50V	GR371	REF-ELEMENT# TL 431AID
C754	C 0805H X7R# 0M1 10 % 25V	GR451	SI DIODE # MURS 120
C759	C 0805H X7R# 1000P 10 % 50V	GR553	SI DIODE # BAV 99
C771	C 0805H C0G# 100P 2 % 200V	GR682	SI DIODE # BAV 99

TABLE 8 Mounted components

Name	Description	Name	Description
GR687	SI DIODE # BAV 99	L403	INDUCTOR # 1U 10 % 1A8
GR689	SI DIODE # BAV 99	L404	INDUCTOR # 1U 10 % 1A8
GR801	2SI DIODE # BAT 64-07	L451	INDUCTOR # 100U 10 % 0A25
GR820	2SI DIODE # BAT 64-07	L452	INDUCTOR # 100U 10 % 0A25
IC201	TRIMP-AMP # CIC 100BCP GAAS	L550	CHOKE-CHIP# 1206
IC202	MAIN-AMP # OQ 2538S1CP BIPO	L581	CHOKE-CHIP# 1206
IC203	2OP-AMP # 2272AEP CMOS	L661	CHOKE-CHIP# 1206
IC204	2OP-AMP # 2272AEP CMOS	L671	CHOKE-CHIP# 1206
IC205	4NAND-2INP # 74ACT00EP CMOS	L681	CHOKE-CHIP# 1206
IC301	2OP-AMP # 2272AEP CMOS	L682	CHOKE-CHIP# 1206
IC304	2OP-AMP # 2272AEP CMOS	L701	INDUCTOR # 10U 10 % 0A69
IC305	4SWI BILATR# 74HC4066EP CMOS	L702	INDUCTOR # 10U 10 % 0A69
IC306	4NAND-2INP # 74ACT00EP CMOS	L703	INDUCTOR # 1U 10 % 1A8
IC400	DMUX 1:32 # OQ 2536EP BMOS	L704	CHOKE-CHIP# 1206
IC451	VLG RGT PWM# 750EP BIPO	L750	CHOKE-CHIP# 1206
IC501	DCR/VCO-16 # OQ 2541-C3CP BIPO	L801	INDUCTOR # 100U 10 % 0A25
IC651	2OP-AMP # 2272AEP CMOS	L802	INDUCTOR # 10U 10 % 0A69
IC661	8BU-DRV TST# 74ABT244EP BMOS	L803	INDUCTOR # 10U 10 % 0A69
IC671	8BU-DRV TST# 74ABT244EP BMOS	L807	CHOKE-CHIP# 1206
IC681	BTL BUS TRC# 3205EP BMOS	L818	CHOKE-CHIP# 1206
IC701	MUX 32:1 # OQ 2535C4EP BMOS	M221	WRAPSTIFT
IC751	DCR/VCO-16 # OQ 2541-C3CP BIPO	M222	WRAPSTIFT
IC801	LD-16 # OQ 2545CP BIPO	M223	WRAPSTIFT
IC820	2OP-AMP # 2272AEP CMOS	M224	WRAPSTIFT
IC951	2 OP-AMP # 2904EP BIPO	OT201	PHOTODIODE PHASE SIU SCHIRMNR
L202	INDUCTOR # 1U 10 % 1A8	OT201	PHOTODIODE PHASE SIU SCHIRMNR
L203	CHOKE-CHIP# 1206	OT601	LED # LYT 670-JK GE
L204	INDUCTOR # 1U 10 % 1A8	OT602	LED # LYT 670-JK GE
L205	CHOKE-CHIP# 1206	OT603	LED # LYT 670-JK GE
L206	INDUCTOR # 1U 10 % 1A8	OT604	LED # LYT 670-JK GE
L207	CHOKE-CHIP# 1206	OT611	LED # LYT 670-JK GE
L251	INDUCTOR # 100U 10 % 0A25	OT612	LED # LYT 670-JK GE
L252	INDUCTOR # 10U 10 % 0A69	OT621	LED # LST 670-HK RT
L261	INDUCTOR # 1U 10 % 1A8	OT622	LED # LST 670-HK RT
L262	CHOKE-CHIP# 1206	OT623	LED # LGT 670-JK GN
L281	CHOKE-CHIP# 1206	OT624	LED # LGT 670-JK GN
L391	INDUCTOR # 100U 10 % 0A25	OT631	LED # LYT 670-JK GE
L392	INDUCTOR # 100U 10 % 0A25	OT632	LED # LYT 670-JK GE
L401	INDUCTOR # 10U 10 % 0A69	OT641	LED # LYT 670-JK GE
L402	INDUCTOR # 10U 10 % 0A69	OT642	LED # LYT 670-JK GE

TABLE 8 Mounted components

Name	Description	Name	Description
OT651	LED # LYT 670-JK GE	R221	R 0805 100# 147K 1 % 0W1
OT652	LED # LYT 670-JK GE	R222	R 0805 100# 10K 1 % 0W1
OT801	LASERDIODE PHASE 2.5GB/S SCHIRM	R223	R 0805 100# 147K 1 % 0W1
OT801	LASERDIODE PHASE 2.5GB/S SCHIRM	R224	R 0805 100# 1K 1 % 0W1
Q581	Q-OSZILLATOR 38M88 VCXO	R225	R 0805 100# 10K 1 % 0W1
R11	R 0805 100# 825E 1 % 0W1	R226	R 0805 100# 2K74 1 % 0W1
R12	R 0805 100# 2K15 1 % 0W1	R227	R 0805 100# 4K64 1 % 0W1
R13	R 0805 100# 2K15 1 % 0W1	R228	ALIGN R 100 # 211 3711 1 % 0805
R21	R 0805 100# 1K 1 % 0W1	R228	ALIGN R 100 # 211 3711 1 % 0805
R22	R 0805 100# 53E6 1 % 0W1	R229	R 0805 100# 4K64 1 % 0W1
R23	R 0805 100# 634E 1 % 0W1	R230	R 0805 100# 27K4 1 % 0W1
R24	R 0805 100# 2K15 1 % 0W1	R231	R 0805 100# 27K4 1 % 0W1
R31	R 0805 100# 464E 1 % 0W1	R232	R 0805 100# 4K64 1 % 0W1
R32	R 0805 100# 51E1 1 % 0W1	R235	ALIGN R 100 # 211 3711 1 % 0805
R33	R 0805 100# 147E 1 % 0W1	R235	ALIGN R 100 # 211 3711 1 % 0805
R34	R 0805 100# 33E2 1 % 0W1	R241	R 0805 100# 10E 1 % 0W1
R35	R 0805 100# 33E2 1 % 0W1	R242	R 0805 100# 10E 1 % 0W1
R36	R 0805 100# 261E 1 % 0W1	R243	R 0805 100# 51E1 1 % 0W1
R37	R 0805 100# 205E 1 % 0W1	R261	R 0805 # 0E
R41	R 0805 100# 464E 1 % 0W1	R262	R 0805 # 0E
R42	R 0805 100# 51E1 1 % 0W1	R263	R 0805 # 0E
R43	R 0805 100# 147E 1 % 0W1	R264	R 0805 # 0E
R44	R 0805 100# 33E2 1 % 0W1	R265	R 0805 100# 464E 1 % 0W1
R45	R 0805 100# 33E2 1 % 0W1	R266	R 0805 100# 56E2 1 % 0W1
R46	R 0805 100# 121E 1 % 0W1	R267	R 0805 100# 464E 1 % 0W1
R47	R 0805 100# 75E 1 % 0W1	R268	R 0805 100# 56E2 1 % 0W1
R48	R 0805 100# 121E 1 % 0W1	R281	R 0805 100# 1K21 1 % 0W1
R201	R 0805 100# 10K 1 % 0W1	R282	R 0805 100# 1K 1 % 0W1
R203	R 0805 100# 51E1 1 % 0W1	R283	R 0805 100# 2K15 1 % 0W1
R204	R 0805 100# 51E1 1 % 0W1	R284	R 0805 100# 100E 1 % 0W1
R208	R 0805 100# 51E1 1 % 0W1	R285	R 0805 100# 51E1 1 % 0W1
R210	R 0805 100# 215E 1 % 0W1	R301	R 0805 100# 21K5 1 % 0W1
R211	R 0805 100# 75E 1 % 0W1	R302	R 0805 # 0E
R212	R 0805 100# 5K62 1 % 0W1	R303	R 0805 100# 1K 1 % 0W1
R213	R 0805 100# 5K62 1 % 0W1	R304	R 0805 100# 332E 1 % 0W1
R215	R 0805 100# 10K 1 % 0W1	R305	R MINI-M 50# 1M 1 % 0W25
R216	R 0805 100# 10K 1 % 0W1	R306	R MINI-M 50# 34K8 1 % 0W25
R217	R 0805 100# 82K5 1 % 0W1	R306	R MINI-M 25# 100K 0,25% 0W25
R218	R 0805 100# 82K5 1 % 0W1	R307	R 0805 # 0E
R220	R 0805 100# 10K 1 % 0W1	R321	R 0805 100# 10K 1 % 0W1

TABLE 8 Mounted components

Name	Description	Name	Description
R322	R 0805 100# 1M 1 % 0W1	R425	R 0805 100# 21E5 1 % 0W1
R323	R 0805 100# 10K 1 % 0W1	R426	R 0805 100# 21E5 1 % 0W1
R329	R 0805 100# 10K 1 % 0W1	R427	R 0805 100# 21E5 1 % 0W1
R331	R 0805 100# 10K 1 % 0W1	R428	R 0805 100# 21E5 1 % 0W1
R351	R 0805 100# 3K32 1 % 0W1	R429	R 0805 100# 21E5 1 % 0W1
R370	R 0805 100# 82K5 1 % 0W1	R430	R 0805 100# 21E5 1 % 0W1
R371	R 0805 100# 100E 1 % 0W1	R431	R 0805 100# 21E5 1 % 0W1
R372	R 0805 100# 8K25 1 % 0W1	R432	R 0805 100# 21E5 1 % 0W1
R373	R 0805 100# 12K1 1 % 0W1	R433	R 0805 100# 21E5 1 % 0W1
R374	R 0805 100# 10K 1 % 0W1	R434	R 0805 100# 21E5 1 % 0W1
R375	R 0805 100# 562E 1 % 0W1	R435	R 0805 100# 21E5 1 % 0W1
R375	R 0805 100# 1K 1 % 0W1	R436	R 0805 100# 21E5 1 % 0W1
R376	R 0805 100# 4K64 1 % 0W1	R437	R 0805 100# 21E5 1 % 0W1
R377	R 0805 100# 8K25 1 % 0W1	R438	R 0805 100# 21E5 1 % 0W1
R378	ALIGN R 100 # 211 3711 1 % 0805	R439	R 0805 100# 21E5 1 % 0W1
R378	ALIGN R 100 # 211 3711 1 % 0805	R440	R 0805 100# 21E5 1 % 0W1
R379	ALIGN R 100 # 211 3711 1 % 0805	R441	R 0805 100# 21E5 1 % 0W1
R379	ALIGN R 100 # 211 3711 1 % 0805	R442	R 0805 100# 21E5 1 % 0W1
R380	R 0805 100# 10K 1 % 0W1	R451	R 0805 100# 464K 1 % 0W1
R388	R 0805 100# 1M 1 % 0W1	R453	R 0805 100# 2K15 1 % 0W1
R391	R 0805 100# 27K4 1 % 0W1	R455	R 0805 # 0E
R391	R 0805 100# 10K 1 % 0W1	R456	R 0805 100# 46K4 1 % 0W1
R392	R 0805 100# 38K3 1 % 0W1	R457	R 0805 100# 3K83 1 % 0W1
R392	R 0805 100# 10K 1 % 0W1	R458	R 0805 100# 6K81 1 % 0W1
R394	R 0805 100# 4K64 1 % 0W1	R459	R 0805 100# 10K 1 % 0W1
R401	R 0805 100# 21E5 1 % 0W1	R521	R 0805 100# 3K32 1 % 0W1
R411	R 0805 100# 21E5 1 % 0W1	R526	R 0805 100# 3K32 1 % 0W1
R412	R 0805 100# 21E5 1 % 0W1	R527	R 0805 100# 51E1 1 % 0W1
R413	R 0805 100# 21E5 1 % 0W1	R542	R 0805 100# 1K 1 % 0W1
R414	R 0805 100# 21E5 1 % 0W1	R543	R 0805 100# 1K 1 % 0W1
R415	R 0805 100# 21E5 1 % 0W1	R544	R 0805 100# 100E 1 % 0W1
R416	R 0805 100# 21E5 1 % 0W1	R545	R 0805 100# 1K 1 % 0W1
R417	R 0805 100# 21E5 1 % 0W1	R546	R 0805 100# 10K 1 % 0W1
R418	R 0805 100# 21E5 1 % 0W1	R547	R 0805 100# 1K 1 % 0W1
R419	R 0805 100# 21E5 1 % 0W1	R548	R 0805 100# 1K 1 % 0W1
R420	R 0805 100# 21E5 1 % 0W1	R549	R 0805 100# 10K 1 % 0W1
R421	R 0805 100# 21E5 1 % 0W1	R550	R 0805 100# 10K 1 % 0W1
R422	R 0805 100# 21E5 1 % 0W1	R557	R 0805 100# 10K 1 % 0W1
R423	R 0805 100# 21E5 1 % 0W1	R558	R 0805 100# 51E1 1 % 0W1
R424	R 0805 100# 21E5 1 % 0W1	R559	R MINI-M 50# 2E15 1 % 0W25

TABLE 8 Mounted components

Name	Description	Name	Description
R560	R 0805 100# 1K 1 % 0W1	R655	R 0805 100# 10K 1 % 0W1
R561	R MINI-M 50# 2E15 1 % 0W25	R656	R 0805 100# 100K 1 % 0W1
R563	R 0805 100# 1K 1 % 0W1	R661	R 0805 # 0E
R571	R MINI-M 50# 2E15 1 % 0W25	R662	R 0805 100# 100E 1 % 0W1
R581	R 0805 100# 4K64 1 % 0W1	R663	R 0805 # 0E
R582	R 0805 100# 4K64 1 % 0W1	R664	R 0805 100# 100E 1 % 0W1
R591	R 0805 100# 10K 1 % 0W1	R671	R 0805 100# 10E 1 % 0W1
R592	R 0805 100# 100K 1 % 0W1	R672	R 0805 100# 10E 1 % 0W1
R601	R 0805 100# 316E 1 % 0W1	R673	R 0805 100# 10E 1 % 0W1
R602	R 0805 100# 316E 1 % 0W1	R674	R 0805 100# 100E 1 % 0W1
R603	R 0805 100# 316E 1 % 0W1	R675	R 0805 # 0E
R604	R 0805 100# 316E 1 % 0W1	R676	R 0805 100# 100E 1 % 0W1
R605	R 0805 100# 10K 1 % 0W1	R681	R 0805 100# 33E2 1 % 0W1
R606	R 0805 100# 10K 1 % 0W1	R682	R 0805 100# 21E5 1 % 0W1
R607	R 0805 100# 10K 1 % 0W1	R686	R 0805 100# 33E2 1 % 0W1
R608	R 0805 100# 10K 1 % 0W1	R687	R 0805 100# 21E5 1 % 0W1
R611	R 0805 100# 316E 1 % 0W1	R688	R 0805 100# 33E2 1 % 0W1
R612	R 0805 100# 316E 1 % 0W1	R689	R 0805 100# 21E5 1 % 0W1
R615	R 0805 100# 10K 1 % 0W1	R702	R 0805 100# 10K 1 % 0W1
R616	R 0805 100# 10K 1 % 0W1	R703	R 0805 100# 10K 1 % 0W1
R621	R 0805 100# 316E 1 % 0W1	R704	R 0805 100# 2K15 1 % 0W1
R622	R 0805 100# 10K 1 % 0W1	R714	R 0805 # 0E
R623	R 0805 100# 10K 1 % 0W1	R715	R 0805 # 0E
R624	R 0805 100# 316E 1 % 0W1	R718	R 0805 100# 10K 1 % 0W1
R625	R 0805 100# 10K 1 % 0W1	R719	R 0805 100# 4K64 1 % 0W1
R626	R 0805 100# 316E 1 % 0W1	R722	R 0805 100# 100E 1 % 0W1
R627	R 0805 100# 10K 1 % 0W1	R725	R 0805 100# 100E 1 % 0W1
R628	R 0805 100# 316E 1 % 0W1	R728	R 0805 100# 100E 1 % 0W1
R631	R 0805 100# 316E 1 % 0W1	R751	R 0805 100# 100E 1 % 0W1
R632	R 0805 100# 316E 1 % 0W1	R752	R 0805 100# 100E 1 % 0W1
R633	R 0805 100# 10K 1 % 0W1	R753	R 0805 100# 33E2 1 % 0W1
R634	R 0805 100# 10K 1 % 0W1	R754	R 0805 100# 33E2 1 % 0W1
R641	R 0805 100# 316E 1 % 0W1	R759	R MINI-M 50# 2E15 1 % 0W25
R642	R 0805 100# 316E 1 % 0W1	R760	R 0805 100# 1K 1 % 0W1
R643	R 0805 100# 10K 1 % 0W1	R761	R MINI-M 50# 2E15 1 % 0W25
R644	R 0805 100# 1K 1 % 0W1	R763	R 0805 100# 1K 1 % 0W1
R651	R 0805 100# 316E 1 % 0W1	R771	R MINI-M 50# 2E15 1 % 0W25
R652	R 0805 100# 316E 1 % 0W1	R773	R 0805 100# 215E 1 % 0W1
R653	R 0805 100# 10K 1 % 0W1	R774	R 0805 100# 215E 1 % 0W1
R654	R 0805 100# 10K 1 % 0W1	R777	R 0805 100# 147E 1 % 0W1

TABLE 8 Mounted components

Name	Description	Name	Description
R778	R 0805 100# 38E3 1 % 0W1	R1899	R 0805 100# 332E 1 % 0W1
R779	R 0805 100# 147E 1 % 0W1	S601	SWITCH # DIL 4 IN 1 1POL
R781	R 0805 100# 68E1 1 % 0W1	S611	SWITCH # DIL 4 IN 1 1POL
R793	R 0805 100# 10K 1 % 0W1	S631	SWITCH # DIL 4 IN 1 1POL
R794	R 0805 100# 100E 1 % 0W1	ST212	JUMPER PIN 2P A
R797	R 0805 100# 100E 1 % 0W1	ST213	JUMPER PIN 2P A
R802	R 0805 100# 681E 1 % 0W1	ST281	JUMPER PIN 2P A
R803	R 0805 100# 10K 1 % 0W1	ST301	JUMPER PIN 1P A
R804	R MINI-M 50# 21E5 1 % 0W25	ST302	JUMPER PIN 1P A
R805	R 0805 100# 4K64 1 % 0W1	ST601	JUMPER PIN 20P L 1 2-REIHIG
R806	R 0805 100# 464K 1 % 0W1	ST602	JUMPER PIN 20P L 1 2-REIHIG
R807	R 0805 100# 10K 1 % 0W1	ST603	JUMPER PIN 20P L 1 2-REIHIG
R808	R 0805 100# 10K 1 % 0W1	ST604	JUMPER PIN 20P L 1 2-REIHIG
R810	R 0805 # 0E	ST605	JUMPER PIN 20P L 1 2-REIHIG
R811	R 0805 100# 51E1 1 % 0W1	ST606	JUMPER PIN 20P L 1 2-REIHIG
R816	R 0805 100# 100E 1 % 0W1	ST607	JUMPER PIN 20P L 1 2-REIHIG
R819	R 0805 100# 10K 1 % 0W1	ST608	JUMPER PIN 20P L 1 2-REIHIG
R820	ALIGN R 100 # 211 3711 1 % 0805	ST609	JUMPER PIN 20P L 1 2-REIHIG
R820	ALIGN R 100 # 211 3711 1 % 0805	ST621	PCB MOUNTED CONNECTOR SMA
R821	R 0805 100# 1M 1 % 0W1	ST622	PCB MOUNTED CONNECTOR SMA
R822	R 0805 100# 100K 1 % 0W1	ST623	PCB MOUNTED CONNECTOR SMA
R824	R 0805 100# 46K4 1 % 0W1	ST624	PCB MOUNTED CONNECTOR SMA
R825	R 0805 100# 46K4 1 % 0W1	ST625	PCB MOUNTED CONNECTOR SMA
R827	R 0805 100# 46K4 1 % 0W1	ST626	PCB MOUNTED CONNECTOR SMA
R830	R 0805 100# 1K47 1 % 0W1	ST627	PCB MOUNTED CONNECTOR SMA
R855	R 0805 100# 3K32 1 % 0W1	ST628	PCB MOUNTED CONNECTOR SMA
R856	R 0805 100# 4K64 1 % 0W1	ST631	PCB MOUNTED CONNECTOR SMA
R857	ALIGN R 100 # 211 3711 1 % 0805	ST632	PCB MOUNTED CONNECTOR SMA
R857	ALIGN R 100 # 211 3711 1 % 0805	ST633	PCB MOUNTED CONNECTOR SMA
R954	R 0805 100# 10K 1 % 0W1	ST634	PCB MOUNTED CONNECTOR SMA
R955	R 0805 100# 10K 1 % 0W1	ST635	PCB MOUNTED CONNECTOR SMA
R956	R 0805 100# 10K 1 % 0W1	ST636	PCB MOUNTED CONNECTOR SMA
R957	R 0805 100# 1M 1 % 0W1	ST637	PCB MOUNTED CONNECTOR SMA
R958	R 0805 100# 1M 1 % 0W1	ST638	PCB MOUNTED CONNECTOR SMA
R959	R 0805 100# 464E 1 % 0W1	ST641	PCB MOUNTED CONNECTOR SMA
R960	R 0805 100# 10K 1 % 0W1	ST642	PCB MOUNTED CONNECTOR SMA
R1808	R 0805 100# 4K64 1 % 0W1	ST651	PCB MOUNTED CONNECTOR SMA
R1819	R 0805 100# 464K 1 % 0W1	ST652	PCB MOUNTED CONNECTOR SMA
R1821	R 0805 100# 1M 1 % 0W1	ST653	PCB MOUNTED CONNECTOR SMA
R1824	R 0805 100# 46K4 1 % 0W1	ST661	PCB MOUNTED CONNECTOR SMA

TABLE 8 Mounted components

Name	Description	Name	Description
ST662	PCB MOUNTED CONNECTOR SMA		
ST671	PCB MOUNTED CONNECTOR SMA		
ST672	PCB MOUNTED CONNECTOR SMA		
ST673	PCB MOUNTED CONNECTOR SMA		
ST674	PCB MOUNTED CONNECTOR SMA		
T11	TRS-NPN # BC 846B		
T12	TRS-NPN BD 435		
T21	TRS-NPN # BC 846B		
T22	TRS-NPN BD 435		
T31	TRS-PNP # BFT 92		
T32	TRS-PNP # BFT 92		
T33	TRS-NPN # BFR 92A		
T34	TRS-NPN # BFR 92A		
T35	TRS-NPN # BC 846B		
T36	TRS-NPN BD 435		
T41	TRS-PNP # BFT 92		
T42	TRS-PNP # BFT 92		
T43	TRS-NPN # BFR 92A		
T44	TRS-NPN # BFR 92A		
T45	TRS-NPN # BC 846B		
T46	TRS-NPN BD 435		
T301	N-FET # BSP 89		
T459	N-FET # BSS 138		
T551	TRS-NPN # SMBT 2222A		
T552	TRS-NPN # SMBT 2222A		
T591	N-FET # BSS 138		
T621	TRS-NPN # BC 846B		
T622	TRS-NPN # BC 846B		
T623	TRS-NPN # BC 846B		
T624	TRS-NPN # BC 846B		
T632	TRS-NPN # BC 846B		
T642	TRS-NPN # BC 846B		
T719	N-FET # BSS 138		
T751	TRS-NPN # SMBT 2222A		
T752	TRS-NPN # SMBT 2222A		
T830	N-FET # BSS 138		
T958	TRS-NPN BD 435		
T959	TRS-PNP BD 436		

APPENDIX 4 Manufacturers & Second sources list

TABLE 9

TYPE	N	Schematics no.	Manufacterer	Type	Order no.	Philips Type/No.
BD436	1	T959,	No order info			BD436
2PA	3	ST212,ST213,ST281,	BERG ELEKTRONIK		75160-102-02	
20P L 1	9	ST601,ST602,ST603,	BERG ELEKTRONIK		75914-901-20	
		ST604,ST605,ST606,				
		ST607,ST608,ST609,				
BD435	5	T12,T22,T36,T46,T958,	No order info			BD435
1PA	2	ST301,ST302,				
BAV99	4	GR553,GR682,GR687,				BAV99
		GR689,				
BC846B	10	T11,T21,T35,T45,T621,				BC846B
		T622,T623,T624,T632,				
		T642,				
100P 2% 200V	7	C13,C24,C285,C321,	VITRAMON	VJ0805	VJ0805A101GXCT	2222 9301 1436
		C389,C591,C771,				
0M01 10% 50V	19	C202,C204,C206,C207,	SIEMENS MATSUSHI	B37941	B37941-K5103-K	2222 5901 6627
		C209,C210,C212,C213,				
		C219,C221,C228,C229,				
		C263,C351,C403,C404,				
		C453,C705,C706,				
4700P 10% 50V	3	C203,C510,C753,	SIEMENS MATSUSHI	B37941	B37941-K5472-K	2222 59 01 6623
	4	M221,M222,M223,M224,	No order info			
0M022 10% 50V	1	C821,	SIEMENS MATSUSHI	B47941	B37941-K5223-K	2222 5901 6632
470P 2% 50V	5	C226,C227,C248,C249,	VITRAMON	VJ0805	VJ0805A471GXAT	2222 8611 4471
		C322,				
SMBT 2222A	4	T551,T552,T751,T752,	SIEMENS AG	SMBT2222A	Q680000-A6473	PMBT2222A
47P 2% 50V	1	C230,	VITRAMON	VJ0805	VJ0805 A470GXAT	2222 8611 4470
10M 20% 16V	13	C31,C41,C251,C252,	AVX KYOCERA	TAJ	TAJC106M016R	
		C391,C392,C400,C409,				
		C410,C701,C702,C710,				
		C802,				
22M 20% 20V	2	C801,C803,				
1000P 10% 50V	7	C218,C508,C512,C521,	SIEMENS MATSUSHI	B37941	B37941-K5102-K	2222 5901 6614
		C759,C820,C822,				
BFT 92	4	T31,T32,T41,T42,	SIEMENS AG	BFT92	Q62702-F1062	BFT92
1M 1% 0W25	1	R305,	BEYSCHLAG	MMA0204	MMA0204-50BL1%	2322 711 6106
BFR 92A	4	T33,T34,T43,T44,	MOTOROLA SEMCON	BFR92AL	BFR92ALT1	BFR92A
CONN SMA	27	ST621,ST622,ST623,	SUHNER			
		ST624,ST625,ST626,				
		ST627,ST628,ST631,				
		ST632,ST633,ST634,				
		ST635,ST636,ST637,				
		ST638,ST641,ST642,				
		ST651,ST652,ST653,				
		ST661,ST662,ST671,				

TABLE 9

TYPE	N	Schematics no.	Manufacterer	Type	Order no.	Philips Type/No.
		ST672,ST673,ST674,				
21E5 1 % 0W25	1	R804,				
34K8 1 % 0W25	1	R306,				
1M 20 % 35V	5	C552,C661,C671,C681,				
		C752,				
74HC4066EP	1	IC305,	PHILIPS SEMICOND	74HC4066D		
BAV 103	2	GR281,GR301,	PHILIPS SEMICOND	BAV103		
BSS 138	3	T591,T719,T830,	PHILIPS SEMICOND	BSS138		
2E15 1 % 0W25	6	R559,R561,R571,R759,	BEYSCHLAG	MMA0204	MMA0204- 50BL 1%	2322 7116 1228
		R761,R771,				
15P 0,25P 50V	1	C775,	SIEMENS AG	B37940	B37940 K5150 C62	2222 8611 1159
74ACT00EP	2	IC205,IC306,	NATIONAL SEMICON	74ACT00SC		
51E1 1% 0W1	10	R32,R42,R203,R204,	DRALORIC ELECTRO	CR0805	CR0805TK 100 51R	2322 7346 5119
		R208,R243,R285,R527,				
		R558,R811,				
2904EP	1	IC951,	MOTOROLA SEMICON	LM2904D		
100E 1% 0W1	15	R284,R371,R544,R662,	DRALORIC ELECTRO	CR0805	CR0805TK 100 100	2322 7346 1001
		R664,R674,R676,R722,				
		R725,R728,R751,R752,				
		R794,R797,R816,				
10E 1% 0W1	5	R241,R242,R671,R672,	DRALORIC ELECTRO	CR0805	.	2322 7346 1009
		R673,				
10K 1% 0W1	42	R201,R215,R216,R220,	DRALORIC ELECTRO	CR 0805	CR0805 TK100 10	2322 7346 1003
		R222,R225,R321,R323,				
		R329,R331,R374,R380,				
		R459,R546,R549,R550,				
		R557,R591,R605,R606,				
		R607,R608,R616,R622,				
		R623,R625,R627,R633,				
		R634,R643,R653,R654,				
		R655,R702,R703,R718,				
		R793,R819,R954,R955,				
		R956,R960,				
1K 1% 0W1	14	R21,R224,R282,R303,	DRALORIC ELECTRO	CR0805	CR0805 TK100 01K	2322 7346 1002
		R542,R543,R545,R547,				
		R548,R560,R563,R644,				
		R760,R763,				
2K74 1% 0W1	1	R226,	DRALORIC ELECTRO	CR0805	CR0805 TK100 2K7	2322 7346 2742
3K32 1% 0W1	4	R351,R521,R526,R855,	DRALORIC ELECTRO	CR0805	CR0805 TK100 3K3	2322 7346 3322
4K64 1 % 0W1	11	R227,R229,R232,R376,	DRALORIC ELECTRO	CR0805	CR0805 TK100 4K6	2322 7346 4642
		R394,R581,R582,R719,				
		R805,R856,R1808,				
8K25 1 % 0W1	2	R372,R377,				2322 7346 8252
100K 1 % 0W1	3	R592,R656,R822,				2322 7346 1004
33E2 1 % 0W1	9	R34,R35,R44,R45,R681,				2322 7346 3329
		R686,R688,R753,R754,				
68E1 1 % 0W1	1	R781,				2322 7346 6819

TABLE 9

TYPE	N	Schematics no.	Manufacterer	Type	Order no.	Philips Type/No.
56E2 1 % 0W1	2	R266,R268,				2322 7346 5629
75E 1 % 0W1	2	R47,R211,				2322 7346 7509
121E 1 % 0W1	2	R46,R48,				2322 7346 1211
147E 1 % 0W1	4	R33,R43,R777,R779,				2322 7346 1471
205E 1 % 0W1	1	R37,				2322 7346 2051
215E 1 % 0W1	3	R210,R773,R774,				2322 7346 2151
261E 1 % 0W1	1	R36,				2322 7346 261 1
316E 1 % 0W1	16	R601,R602,R603,R604,				2322 7346 3161
		R611,R612,R621,R624,				
		R626,R628,R631,R632,				
		R641,R642,R651,R652,				
332E 1 % 0W1	2	R304,R1899,				2322 7346 3321
464E 1 % 0W1	5	R31,R41,R265,R267,				2322 7346 4641
		R959,				
562E 1 % 0W1	1	R375,				2322 7346 5621
681E 1 % 0W1	1	R802,				2322 7346 6811
825E 1 % 0W1	1	R11,				2322 7346 8251
1K21 1 % 0W1	1	R281,				2322 7346 1212
1K47 1 % 0W1	1	R830,				2322 7346 1472
2K15 1 % 0W1	6	R12,R13,R24,R283,R453,				2322 7346 2152
		R704,				
3K83 1 % 0W1	1	R457,				2322 7346 3832
5K62 1 % 0W1	2	R212,R213,				2322 7346 5622
6K81 1 % 0W1	1	R458,				2322 7346 6812
12K1 1 % 0W1	1	R373,				2322 7346 1213
21K5 1 % 0W1	1	R301,				2322 7346 2153
27K4 1 % 0W1	3	R230,R231,R391,				2322 7346 2743
38K3 1 % 0W1	1	R392,				2322 7346 3833
46K4 1 % 0W1	5	R456,R824,R825,R827,				2322 7346 4643
		R1824,				
82K5 1 % 0W1	3	R217,R218,R370,				2322 7346 8253
147K 1 % 0W1	2	R221,R223,				2322 7346 1474
464K 1 % 0W1	3	R451,R806,R1819,				2322 7346 4644
1M 1 % 0W1	6	R322,R388,R821,R957,				2322 7346 1005
		R958,R1821,				
21E5 1 % 0W1	36	R401,R411,R412,R413,				2322 7346 2159
		R414,R415,R416,R417,				
		R418,R419,R420,R421,				
		R422,R423,R424,R425,				
		R426,R427,R428,R429,				
		R430,R431,R432,R433,				
		R434,R435,R436,R437,				
		R438,R439,R440,R441,				
		R442,R682,R687,R689,				
38E3 1 % 0W1	1	R778,				2322 7346 3839
BSP 89	1	T301,	SIEMENS AG	BSP89	Q62702-S652	BSP89
634E 1 % 0W1	1	R23,				2322 7346 6341

TABLE 9

TYPE	N	Schematics no.	Manufacterer	Type	Order no.	Philips Type/No.
330P 10 % 200V	1	C454,				
4700P 10 % 200V	3	C281,C282,C283,				2222 9311 6632
0E	13	R261,R262,R263,R264,				2322 730 90001
		R302,R307,R455,R661,				
		R663,R675,R714,R715,				
		R810,				
MBRS 340	2	GR1,GR2,	MOTOROLA SEMICON	MBRS340	MBRS340T3	
TL 431AID	5	GR11,GR21,GR31,GR41,	MOTOROLA SEMICON	TL431AID	TL431AIDR2	
		GR371,				
DIL 4TEIL 1POL	3	S601,S611,S631,	SIEMENS AG	DIL A3000	V23756-A3002-A4	
53E6 1 % 0W1	1	R22,				
LGT 670-JK GN	2	OT623,OT624,				
1000P 10% 200V	1	C301,				
LYT 670-JK GE	12	OT601,OT602,OT603,				
		OT604,OT611,OT612,				
		OT631,OT632,OT641,				
		OT642,OT651,OT652,				
38M88 VCXO	1	Q581,	TELEQUARZ ELECTR	VCXO	ID NR. 317088-3	
74ABT244EP	2	IC661,IC671,	PHILIPS SEMICOND	74ABT244D		74ABT244D
0M1 10 % 25V	51	C205,C208,C211,C214,	VITRAMON	VJ0805	VJ0805Y104KXXT	2222 9101 6649
		C215,C216,C217,C231,				
		C232,C243,C245,C246,				
		C247,C261,C393,C397,				
		C398,C401,C402,C406,				
		C407,C408,C452,C455,				
		C457,C505,C506,C550,				
		C554,C581,C682,C687,				
		C689,C703,C704,C707,				
		C708,C709,C711,C712,				
		C754,C805,C807,C808,				
		C809,C818,C824,C825,				
		C951,C952,C955,				
1P 0,1P 50V	1	C817,				
3P3 0,1P 50V	1	C220,				
10P 1 % 50V	4	C662,C664,C674,C676,	VITRAMON	VJ0805	VJ0805Q100FXAT	2222 5741 1323
2272AEP	6	IC203,IC204,IC301,	TEXAS INSTRUMENT	TLC2272AID	TLC2272AIDR	
		IC304,IC651,IC820,				
3205EP	1	IC681,	PHILIPS SEMICOND	CD3205B	.	CD3205B
1U 10% 1A8	7	L202,L204,L206,L261,	TOYO DEMPA KOGYO	NLC565050	NLC565050T-1R0K	
		L403,L404,L703,				
10U 10% 0A69	7	L252,L401,L402,L701,	TOYO DEMPA KOGYO	NLC565050	NLC565050T-100K	
		L702,L802,L803,				
100U 10% 0A25	6	L251,L391,L392,L451,	TOYO DEMPA KOGYO	NLC565050	NLC565050T-101K	
		L452,L801,				
1M 10% 50V	4	C953,C954,C956,C957,				
OQ 2538S1CP	1	IC202,	PHILIPS SEMICOND	OQ 2538S1CP		
1206	14	L203,L205,L207,L262,				

TABLE 9

TYPE	N	Schematics no.	Manufacterer	Type	Order no.	Philips Type/No.
		L281,L550,L581,L661,				
		L671,L681,L704,L750,				
		L807,L818,				
MURS 120	1	GR451,				
LST 670-HK RT	2	OT621,OT622,				
750EP	1	IC451,				
CIC 100BCP	1	IC201,				
22M 20% 35V	8	C11,C12,C21,C22,C32,	AVX KYOCERA	TPS	TPS E 226 M 035	
		C33,C42,C43,				
220M 20% 10V	3	C451,C456,C458,	AVX KYOCERA	TPS	TPS E 227 M 010	
	1	EM202,				
OQ 2545CP	1	IC801,	PHILIPS SEMICOND	OQ 2545CP		
OQ 2541-C3CP	2	IC501,IC751,	PHILIPS SEMICOND	OQ 2541-C3CP		
OQ 2535C4EP	1	IC701,	PHILIPS SEMICOND	OQ 2535C4EP		
OQ 2536EP	1	IC400,	PHILIPS SEMICOND	OQ 2536EP		
BAT 64-07	5	GR201,GR321,GR351,	SIEMENS AG	BAT 64-07	Q62702-A964	
		GR801,GR820				

APPENDIX 5 Critical line length reports

ICs with corresponding ID numbers

IC201	CIC100B (CGY2100 equivalent) Transimpedance Amplifier
IC202	OQ2538S1 Main Amplifier
IC501	OQ2541C3 used as Data and Clock Recovery
IC400	OQ2536A Demultiplexer
IC701	OQ2535A Multiplexer
IC751	OQ2541C3 used as Clock Converter
IC801	OQ2545 Laserdriver

NOTICE: To correct for internal IC delay times, the line length differences between data and clock lines in optical loop mode and normal mode is not equal.

Optical loop

OL_CLK_IN	Line length between ST635-1 and IC801-28 = 278.6335 mm
OL_CLK_IN~	Line length between ST636-1 and IC801-27 = 278.1824 mm
OL_CLK_OUT	Line length between ST631-1 and IC501-3 = 69.6209 mm
OL_CLK_OUT~	Line length between ST632-1 and IC501-4 = 69.0926 mm
OL_DATA_IN	Line length between ST637-1 and IC801-22 = 262.6203 mm
OL_DATA_IN~	Line length between ST638-1 and IC801-21 = 263.3369 mm
OL_DATA_OUT	Line length between ST633-1 and IC501-6 = 69.9077 mm
OL_DATA_OUT~	Line length between ST634-1 and IC501-7 = 69.8059 mm

Electrical loop

EL_CLK_IN	Line length between ST625-1 and IC400-60 = 58.7433
EL_CLK_IN~	Line length between ST626-1 and IC400-59 = 58.431 mm
EL_CLK_OUT	Line length between ST621-1 and IC701-68 = 58.2342 mm
EL_CLK_OUT~	Line length between ST622-1 and IC701-69 = 58.7872 mm
EL_DATA_IN	Line length between ST627-1 and IC400-65 = 58.0616 mm
EL_DATA_IN~	Line length between ST628-1 and IC400-66 = 58.4792 mm
EL_DATA_OUT	Line length between ST623-1 and IC701-65 = 58.8616 mm
EL_DATA_OUT~	Line length between ST624-1 and IC701-66 = 58.4874 mm
EL_DATA_OUT~	Line length between ST635-1 and IC801-28 = 278.6335 mm

Normal receive side

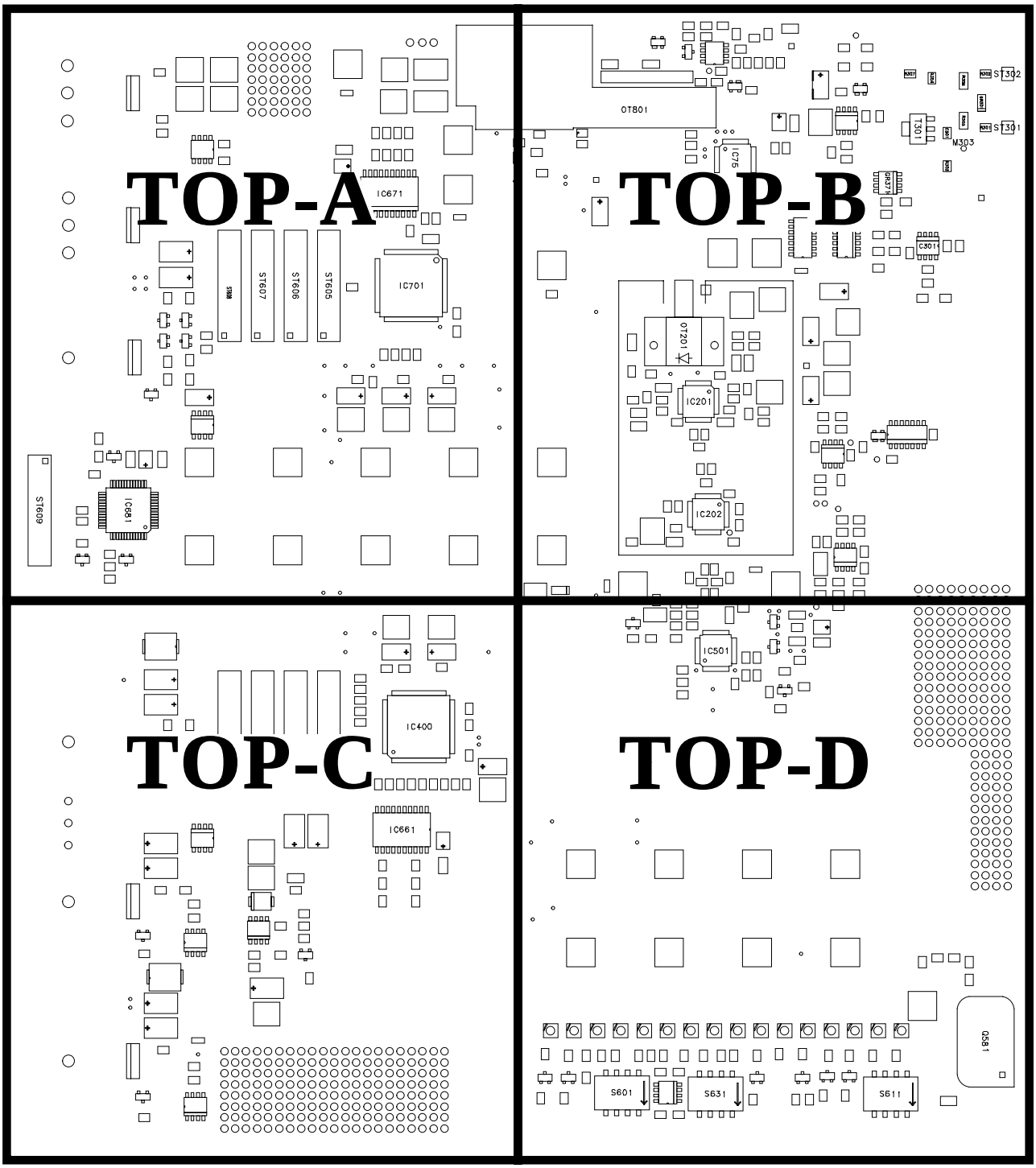
REC_D2G5	Line length between IC501-42 and IC400-54 = 81.2132 mm
REC_D2G5~	Line length between IC501-43 and IC400-53 = 80.2864 mm

REC_C2G5	Line length between IC501-45 and IC400-57 = 65.662 mm
REC_C2G5~	Line length between IC501-46 and IC400-56 = 64.8188 mm
Normal send side	
C2G5MA	Line length between IC801-30 and IC701-82 = 39.5343 mm
C2G5MA~	Line length between IC801-31 and IC701-83 = 38.6807 mm
D2G5MA	Line length between IC801-33 and IC701-90 = 39.4649 mm
D2G5MA~	Line length between IC801-34 and IC701-91 = 38.3285 mm

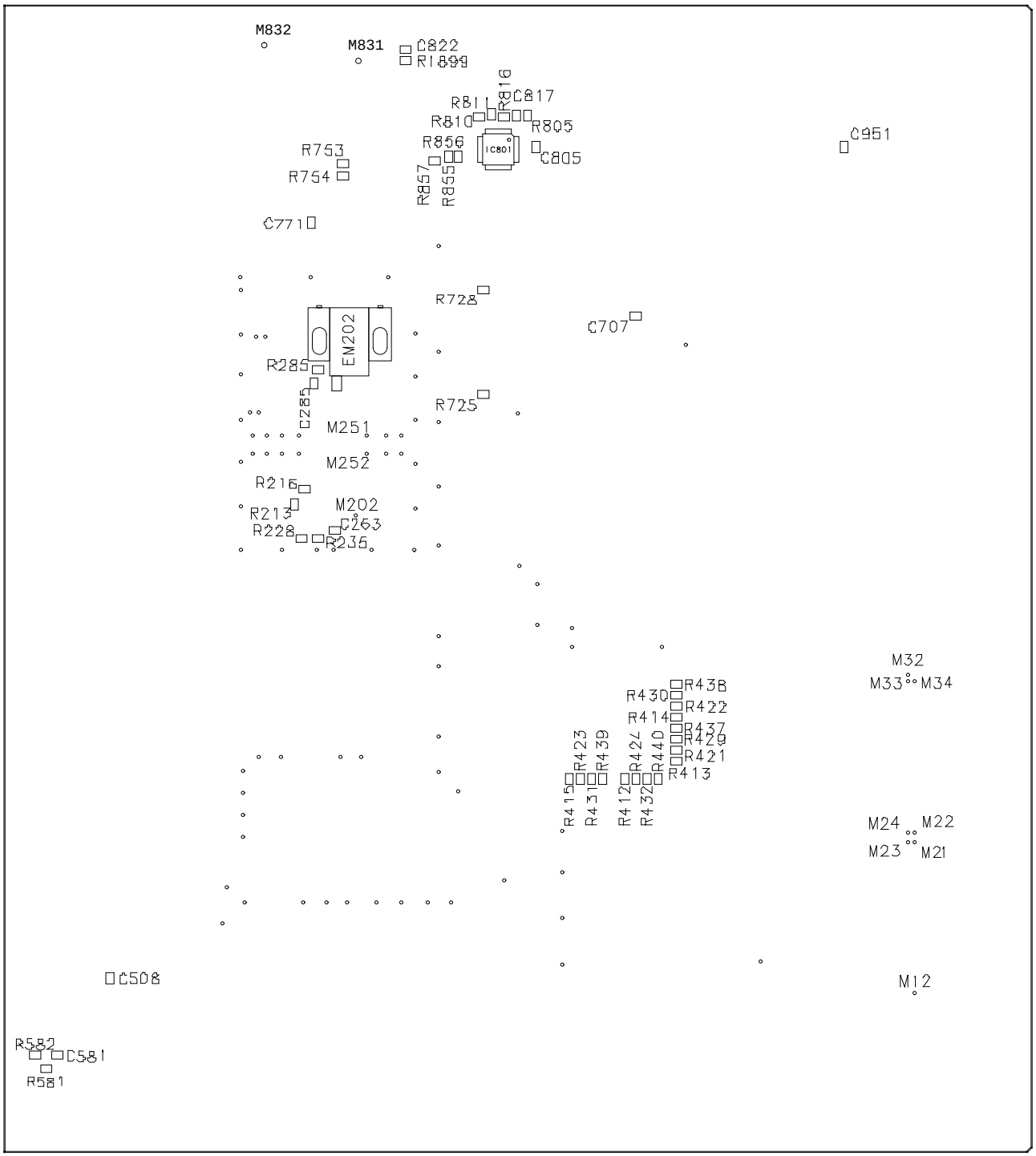
APPENDIX 6 Parts placements

The placement of the parts is shown on the following pages. Due to the size of the board, the placement figures have been divided over 4 pages for the top side, and one for the bottom. First, an overview of the top and bottom placement is given, followed by the enlarged 0.25 boardarea placement of the top side.

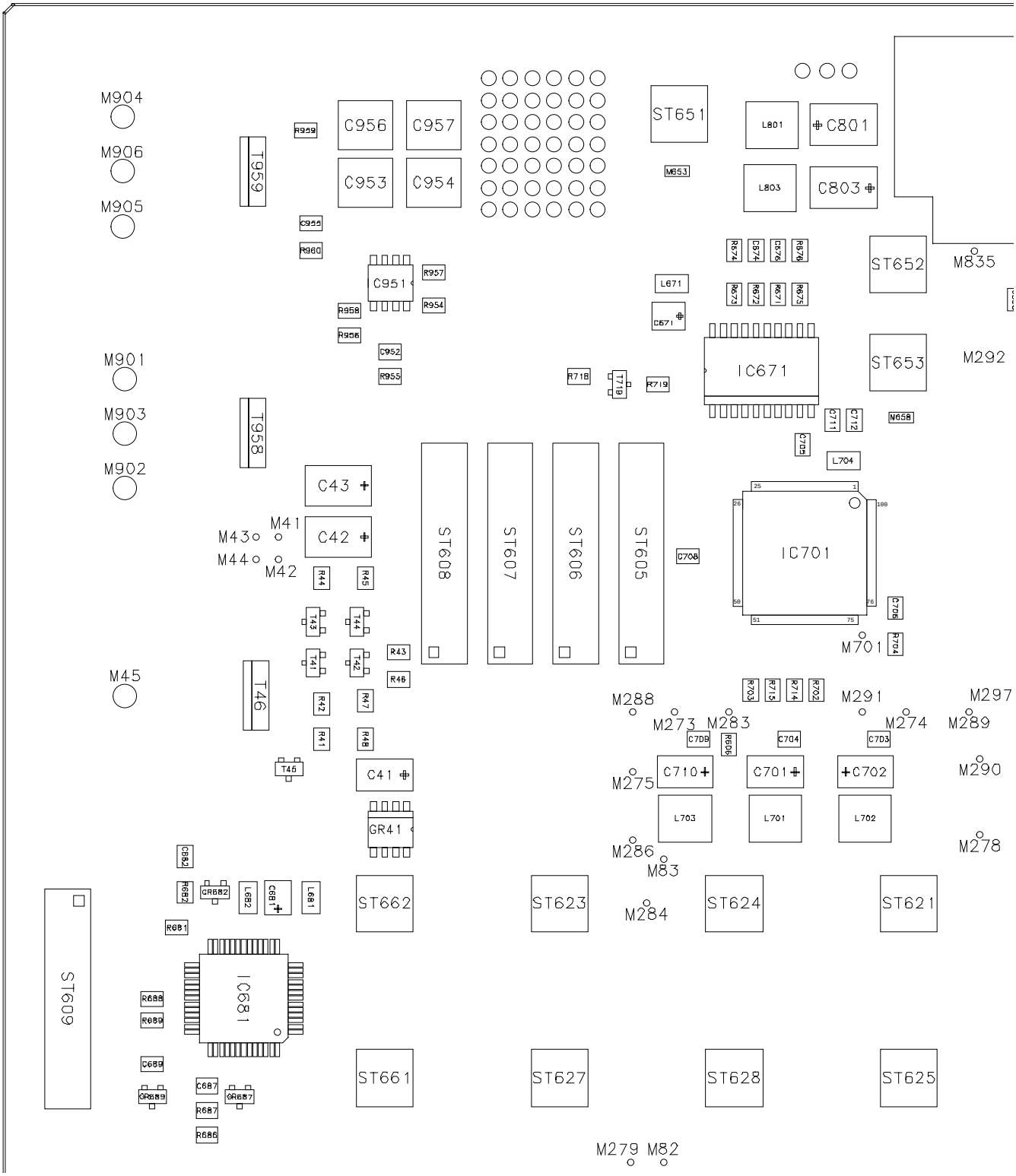
PARTS - TOP


TOP-A
TOP-B
TOP-C
TOP-D
IC671
IC701
ST607
ST606
ST605
ST609
IC681
0T801
ST302
ST301
T301
M303
IC75
C301
0T201
IC201
IC202
IC501
IC400
IC661
Q581
S601
S631
S611

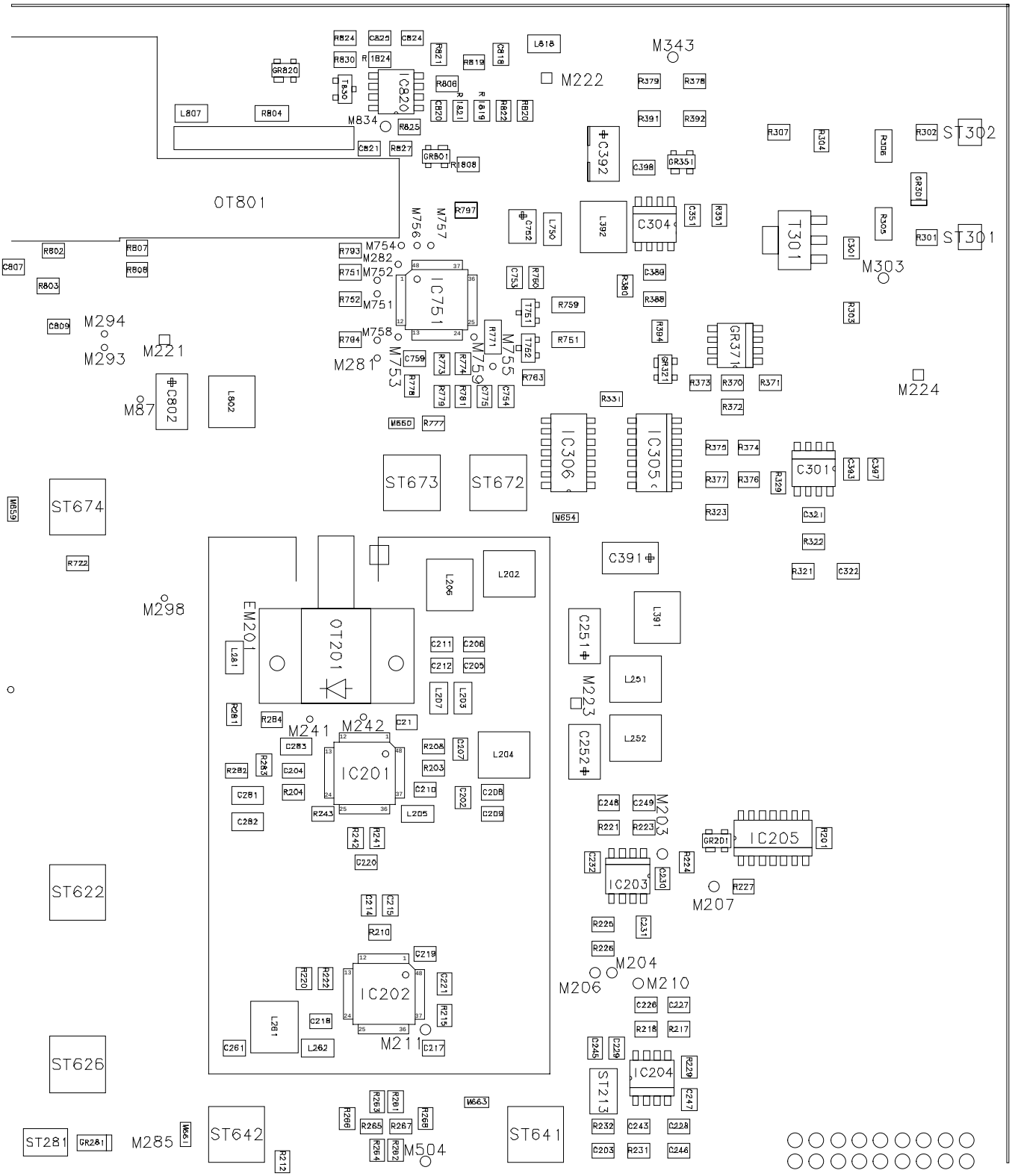
PARTS - BOTTOM



TOP-A


M904
M906
M905
M901
M903
M902
M45
T959
T958
T46
C956
C957
C953
C954
R959
C955
R960
C951
R957
R954
R958
R956
C952
R955
C43
C42
M41
M43
M44
M42
R44
R45
T43
T44
T41
T42
R43
R46
R42
R47
R41
R48
T45
C41
GR41
C652
R652
CR652
L682
C681
L681
R681
R688
R689
C689
CR689
C687
CR687
R687
R686
IC681
ST609
ST662
ST623
ST624
ST621
ST661
ST627
ST628
ST625
M279
M82
ST651
L801
C801
M653
L803
C803
R674
C674
C676
R676
R673
R672
R671
R675
L671
C671
ST652
M835
IC671
ST653
M292
R718
L719
R719
C711
C712
M658
C705
L704
ST608
ST607
ST606
ST605
C708
IC701
C706
M701
R704
R703
R715
R714
R702
M288
M291
M297
M273
M283
M274
M289
C709
R606
C704
C703
C710
C701
C702
M275
M290
L703
L701
L702
M286
M83
M278
M284

TOP-B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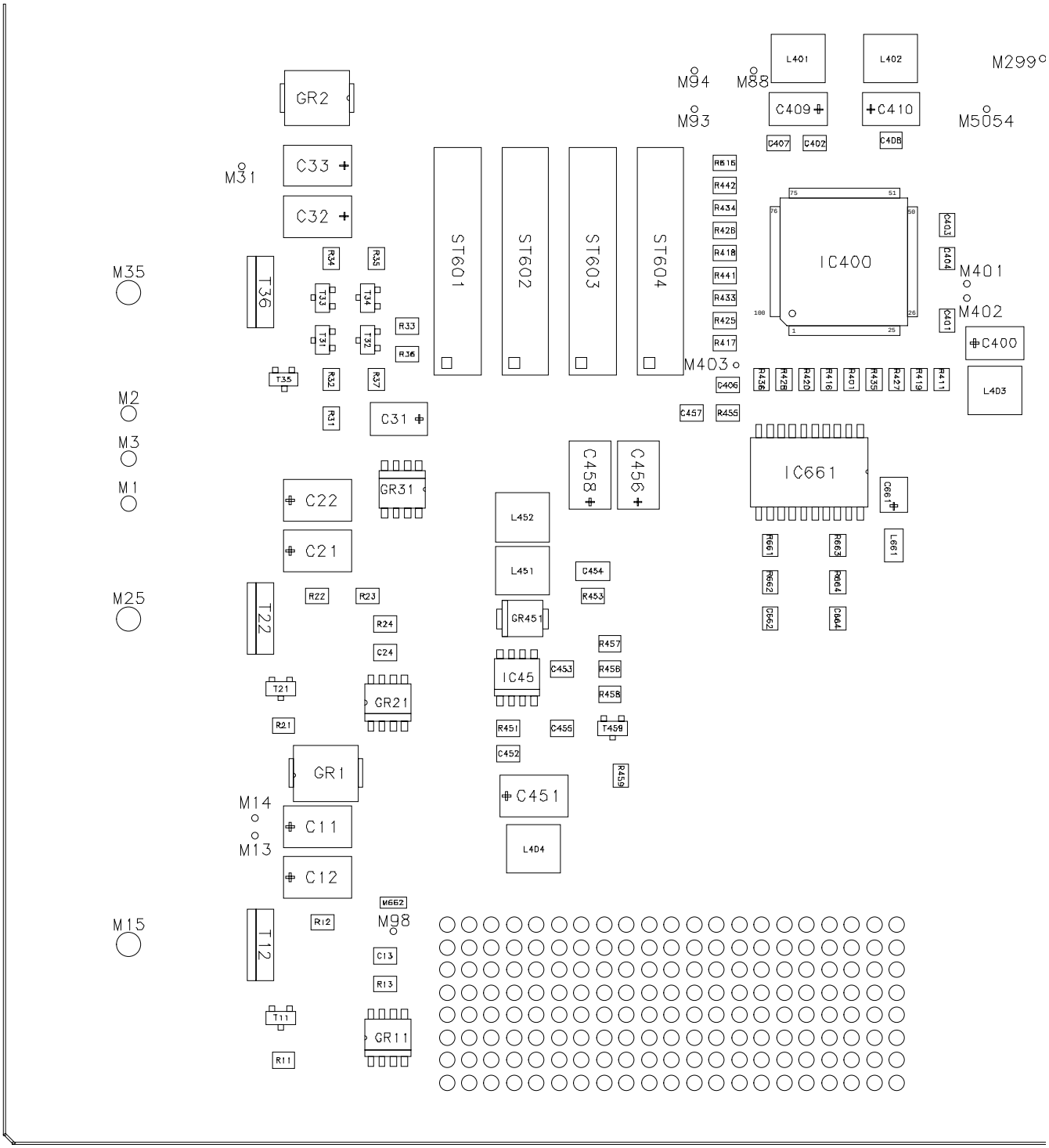
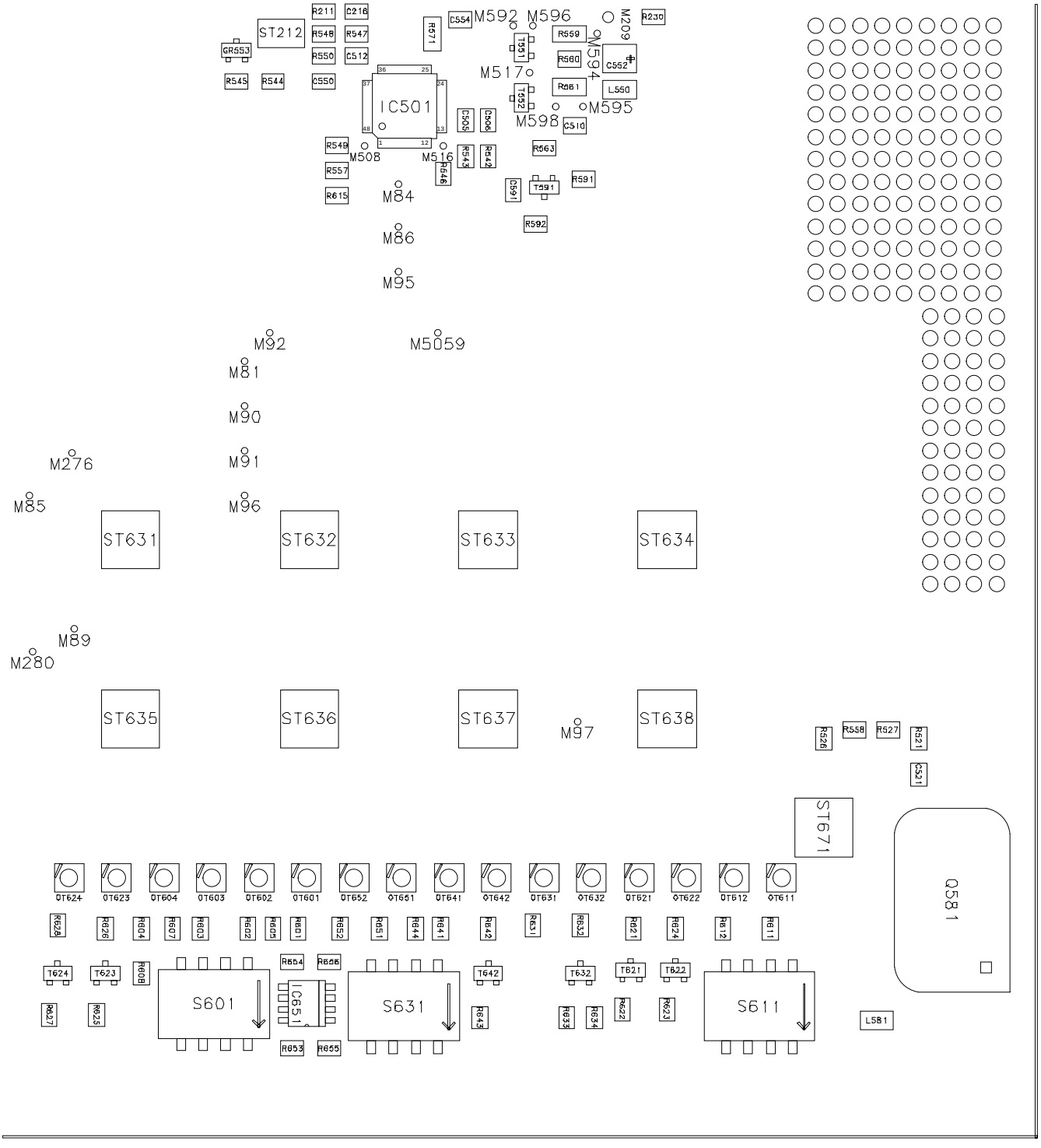
M222
OT801
M834
ST302
ST301
M303
M294
M293
M221
M281
M87
M224
ST673
ST672
ST674
M654
M298
EM201
OT201
M241
M242
M223
M203
M207
M204
M206
M210
ST622
ST626
ST213
ST642
ST641
ST281
M285
M504
M211

TOP-C


GR2
C33
C32
M31
M35
T36
T33
T34
T31
T32
T35
R34
R35
R33
R36
R32
R37
R31
C31
M2
M3
M1
C22
C21
M25
T22
R22
R23
R24
C24
T21
R21
GR21
GR1
M14
M13
C11
C12
M15
T12
R12
M662
M98
C13
R13
T11
R11
GR11
GR31
ST601
ST602
ST603
ST604
L452
L451
C454
R453
GR451
IC45
C453
R457
R456
R458
R451
C455
T458
C452
R459
C451
L4D4
C458
C456
L401
L402
M299
M94
M88
M93
C409
C410
M5054
C407
C402
C408
R415
R442
R434
R426
R418
R441
R433
R425
R417
M403
C406
C457
R455
IC400
C403
C404
M401
M402
C401
C400
L4D3
R438
R428
R420
R416
R401
R435
R427
R419
R411
IC661
C661
L661
R661
R663
R662
R664
C662
C664

TOP-D


ST212
IC501
M592
M596
M594
M595
M598
M517
M508
M516
M84
M86
M95
M92
M5059
M81
M90
M91
M96
M276
M85
M89
M280
M97
ST631
ST632
ST633
ST634
ST635
ST636
ST637
ST638
ST671
Q581
S601
S631
S611
IC651