APPLICATION NOTE
on the
PCB2421 1k Dual Mode CMOS Serial EEPROM for Monitor Application

AN96039

Philips
Semiconductors

PHILIPS

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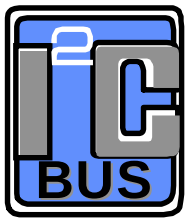
Keywords
PCD2421 1K EEProm
I²C Bus
Microchip
DDC1
DDC2

1 Table of Contents

2 Revision History

Version	Remarks
0.1	Provisional release November 95
1.0	Final release April 96



Purchase of Philips I²C components conveys a licence under the Philips I²C patent to use the components in the I²C system, provided the system conforms to the I²C specifications defined by Philips

Philips Semiconductors Zürich

3 Introduction

- The purpose of this application note is to show the differences between the Philips PCB2421 Vesa EEprom and the Microchip 24LC21.
- A short introduction of DDC1 mode is given and the transition from DDC1 to DDC2 mode is described.
- This application note should be read in conjunction with the follwing literature.
    - Data Sheet of the PCB 2421 "1k Dual Mode CMOS Serial EEPROM for Monitor Applications"
    - Display Data Channel (DDC^{TM}) Proposal (issued by the Video Electronics Standards Association)
    - The I^2C-bus and how to use it, 1995 update, by PHILIPS, NR. 9398 393 40011

3.1 Definition of terms:

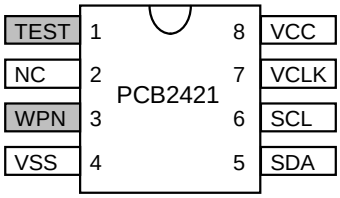
- DDC1	An unidirectional data channel from the device to the host, which continuously transmits information about the monitor.
- DDC2	A bi-directional data channel based on the I^2C protocol[1]. The host can request monitor information over the DDC2 channel.
- DDC2 Command Set	A set of commands to read information from an I^2C slave memory location[2].

3.2 General description of the PCB2421:

The PCB2421 is a 128 byte EEPROM used for automatic monitor configuration. A Monitor equipped with this device can transmit all relevant information about itself to the computer or the graphics controller card inside the host system. As soon as the whole system starts up, the computer will receive information about the monitor (such as mode, resolution, frequency,...) from the PCB2421 device. This feature is needed to implement the Plug and Play philosophy used in new PC's. The computer is then able to use this information to configure his hardware. This device was developed to meet the VESA Display Data Channel (DDC) communication standard (see 1.1 Definition of terms).

[1] see 'The I^2C-bus and how to use it', 1995 update, by PHILIPS, NR. 9398 393 40011
[2] see '1K Dual Mode CMOS Serial EEPROM for Monitor Application', Rev 9 May 95, by PHILIPS

3.3 Pin Configuration:



Pin NR.	Name	Function
1	TESTN	Must be tied to VDD (factory use only) if connected to the ground, the device will switch to a test mode
2	NC	Not connected
3	WPN	EEPROM write protection (low = write protected)
4	VSS	Ground
5	SDA	Serial data line for every mode; open drain; (needs a pull up resistor)
6	SCL	Transmission clock for DDC2 mode; input only; (needs a pull up resistor)
7	VCLK	Transmission clock for DDC1 mode; input only
8	VDD	Power supply (4.5 - 5.5 V/DC)

3.4 How it works...:

Inside a monitor, the PCB2421 device will transmit monitor configuration information to the host system. This information is stored in a EEPROM (128 Bytes). There are two communication modes:

- The first mode is DDC1. This mode can only be entered at the start-up of the device. It is an unidirectional and serial transmission of the whole memory contents (128 Bytes of EEPROM) as a continuous data stream (see '3.1 DDC1 mode').
- The second mode, DDC2, is a bi-directional and serial communication. This mode uses an I^2C protocol (see '3.3 DDC2 mode').

The EEPROM can only be programmed in DDC2 mode, while pin 3 (WPN) is connected to VDD (write protection disabled).

4 Mode handling

4.1 DDC1 mode:

At power up, the device is in DDC1 mode. There are two channels between host and device in the DDC1 mode. The channel on VCLK (pin 7) is the transmission clock. The clock must be generated by the host. The channel on SDA (pin 5) is the data line, where the device sends the data stream. Nine clock cycles on the VCLK must be given first to the device for it to perform internal synchronisation. During this period, the SDA pin will be in a high impedance state. On rising edge of the tenth clock cycle, the device will output the first data bit (MSB first) (Fig. 1).

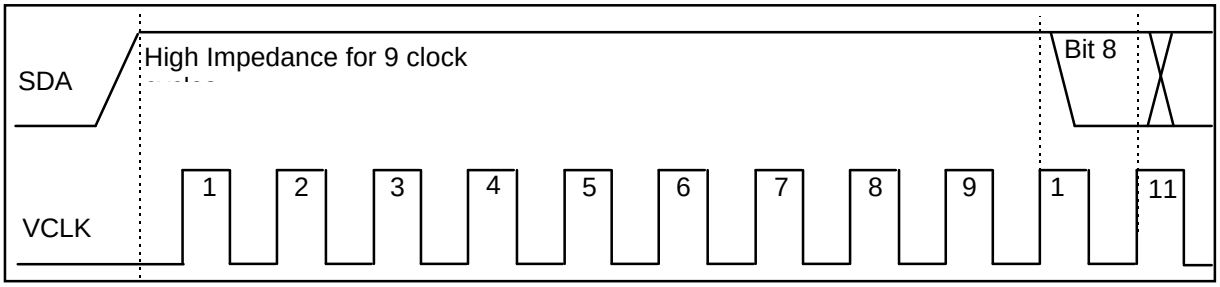


Fig. 1 Syncronisation

In this mode, the data on the SDA line must be stable during the low state of the clock. The data is transmitted in 8 bit bytes, each byte followed by a ninth clock pulse during which time SDA is left high impedance (Fig. 2).

Byte transition

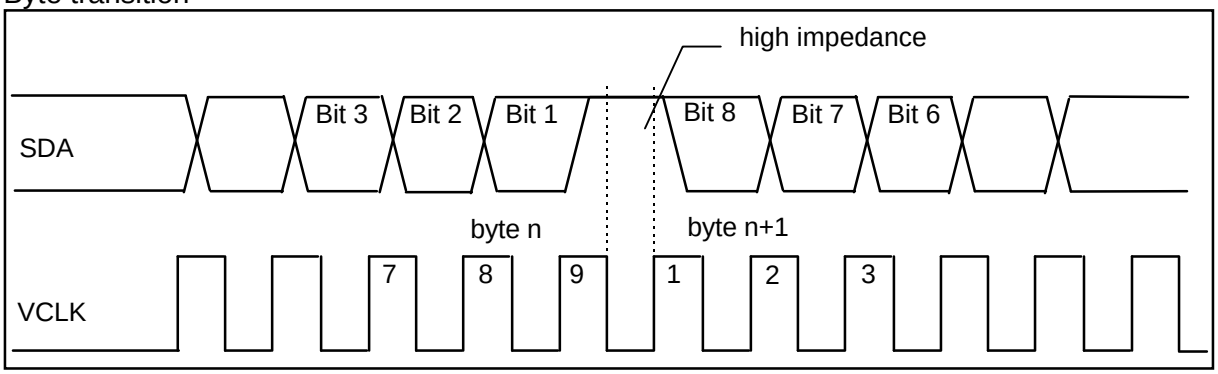


Fig. 2 Byte Transition

At the end of these 128 memory bytes, the output will wrap around to the first location and continue. There is no end-byte or resyncronisation. The output of the last byte in the memory array is followed by the first byte (Fig. 3).

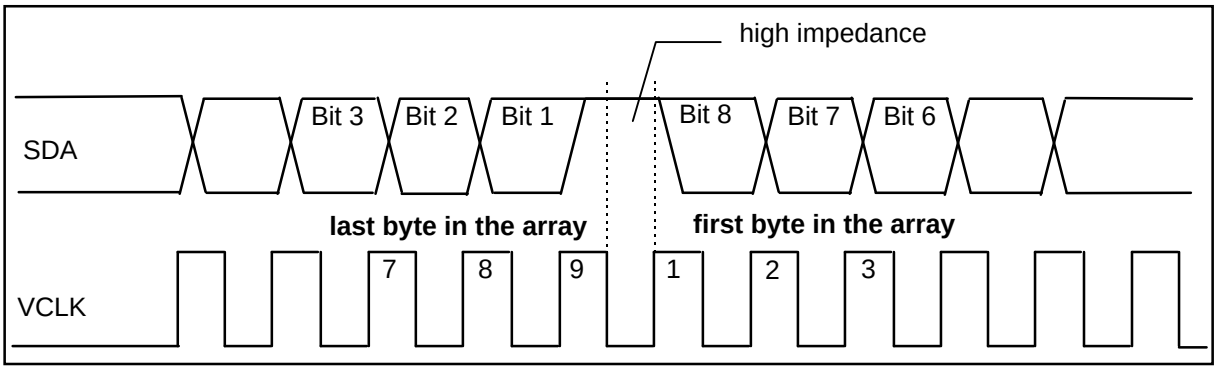


Fig. 3 Wrap Around

There are tree possibilities to recognise a new start of the array:
1. The host must count the data bytes
2. The host must count the clocks
3. A special data pattern must be wirtten to the first memory locations in the device.

4.2 Mode Switch:

At power on, the device will wait for a clock on VCLK pin. Nine clock cycles on VCLK pin must be given to the device for a successful synchronisation, then, the device sends continuously all information stored in the EEPROM (with the signal on VCLK as clock). This is the DDC1 (Display Data Channel) mode.
If a falling edge is detected on the SCL pin of typically 500ns width (t_{VHZ}), transmission will change from DDC1 to DDC2 mode (Fig. 4). SDA is now ready to receive a signal. In DDC2 mode the device is an I^2C slave.

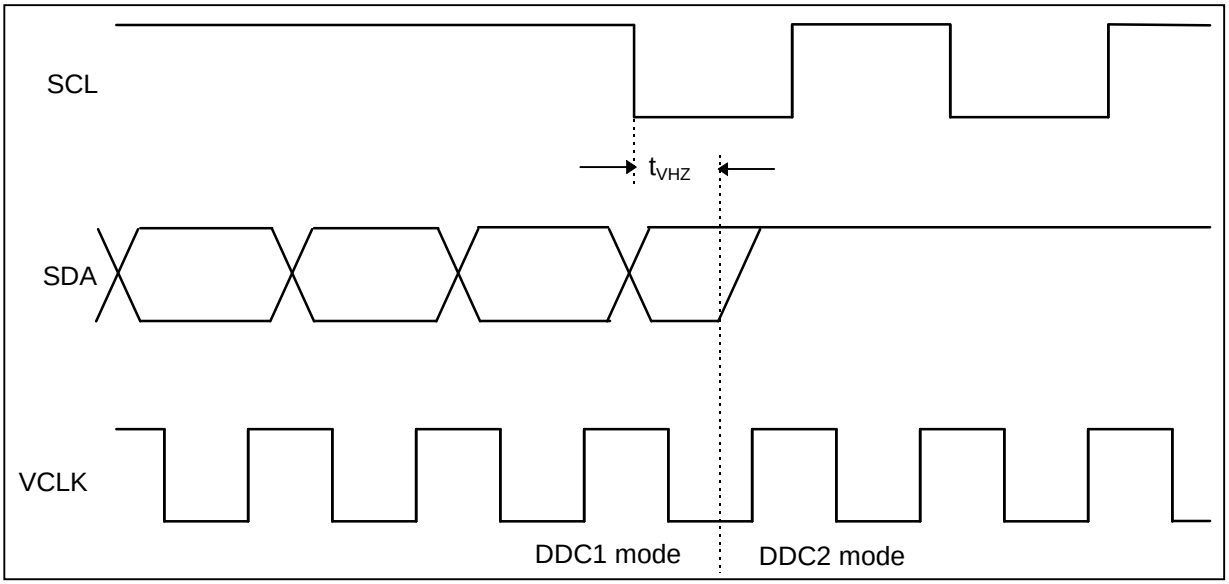


Fig. 4 Mode Switch

Once in DDC2 mode, there is no return to DDC1 mode (unless the device is powered up again). The DDC2 mode is a bi-directional, serial transmission. The serial transmission clock

must be supplied to pin 6 (SCL). In this mode, the device waits as a slave for a command from the master (host system).

Attention:

- In DDC1 mode the data on SDA line is stable during the LOW state of the clock (VCLK), when data is valid.
- In DDC2 mode the data on SDA line must be stable during the HIGH state of the clock (SCL). Changes in the data line while the clock line is high, will be interpreted as a START or STOP condition.[3]

4.3 DDC2 mode:

In DDC2 mode the host and the device communicate as master and slave using the I^2C protocol (see objective specification, rev 9, may 95). Only two lines are required: The serial data line SDA (bi-directional) and the clock line SCL (unidirectional). The generation of clock signals on the I^2C-bus is always the responsibility of the master device. For detailed information see '1K Dual Mode CMOS Serial EEPROM for Monitor Application', Rev 9 May 95, by PHILIPS.

4.4 Implementation with 15 pin VGA-style connector:

In a configuration, that uses a 15 pin VGA-style connector, the clock of DDC1 mode (VCLK) must be connected to the pin 14 of the VGA style connector and the clock of DDC2 mode (SCL) to pin 15 of the VGA style connector. The data line (SDA pin on device) stays the same in both modes (connected to pin 12).

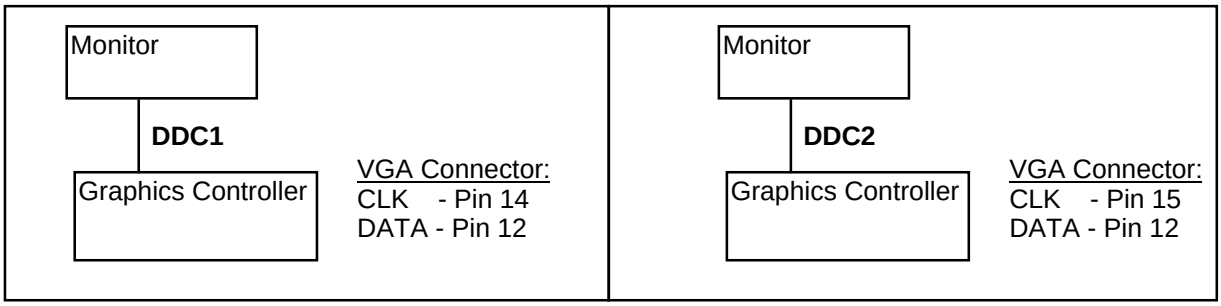
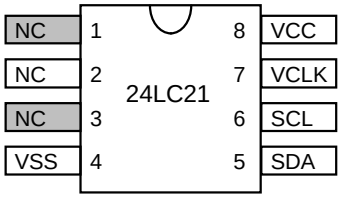
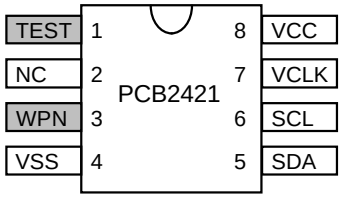


Fig. 5 Connection

[3] see 'The I^2C-bus and how to use it', 1995 update, by PHILIPS, NR. 9398 393 40011

5 Differences between 24LC21 by MICROCHIP and PCB2421 by PHILIPS

There shaded pins have different functions on the two devices. The differences are explained in the Table below.

Differences	24LC21 by MICROCHIP	PCB2421 by PHILIPS
Pin Configuration		
Write Protection	There is no WPN pin. VCLK low -> EEPROM write protected VCLK high -> EEPROM not write protected	There is a special pin (WPN) to select write protection of the EEPROM. VCLK has no influence on the write protection.
Test Mode	There is no TESTN pin.	There is a test pin (TESTN), that must be tied on VDD (factory use only).

- The write protection of the 24LC21 by MICROCHIP is dependent on the VCLK signal.
- The write protection of the PCB 2421 by PHILIPS is separated from the VCLK, there is a special to select write protection (WPN).