AN937
APPLICATION NOTE

Designing with L4971, 1.5A High Efficiency DC-DC Converter

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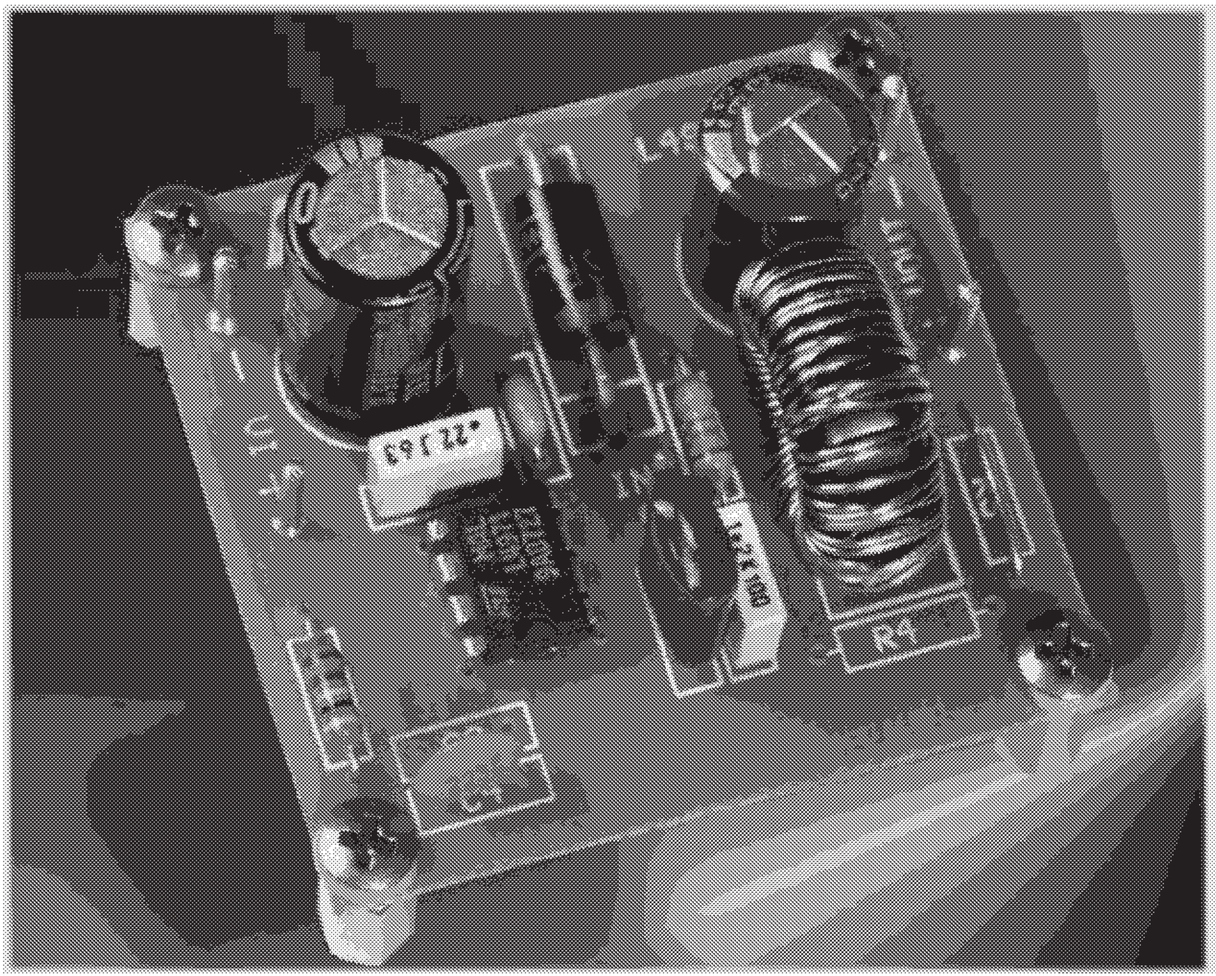
INTRODUCTION

The L4971 is a 1.5A monolithic dc-dc converter, step- down , operating at fix frequency continuous mode. It is realised in BCD60 II technology, and it is available in two plastic packages, MINIDIP and SO16L.
One direct fixed output voltage at 3.3V ±1% is available, adjustable for higher output voltage values, till 40V, by an external voltage divider.
The operating input supply voltage ranges from 8V to 55V, while the absolute value, with no load, is 60V.
New internal design solutions and superior technology performance allow to generate a device with improved efficiency in all the operating conditions and with reduced EMI due to an innovative internal driving circuit, and reduced external component counts.
While internal limiting current and thermal shutdown are today considered standard protection functions, mandatory for a safe load supply, oscillator with voltage feedforward improves line regulation and overall control loop.
Soft-start avoids output overvoltages at turn-on, while, shorting this pin to ground, the device is completely disabled, going into zero consumption state.



DEVICE DESCRIPTION

For a better understanding of the device and its working principles, a short description of the main building blocks is given here below, with packaging options and complete block diagram.

Figure 1 show s the two packaging options, with the pin function assignments.

Figure 1. Pins connection.

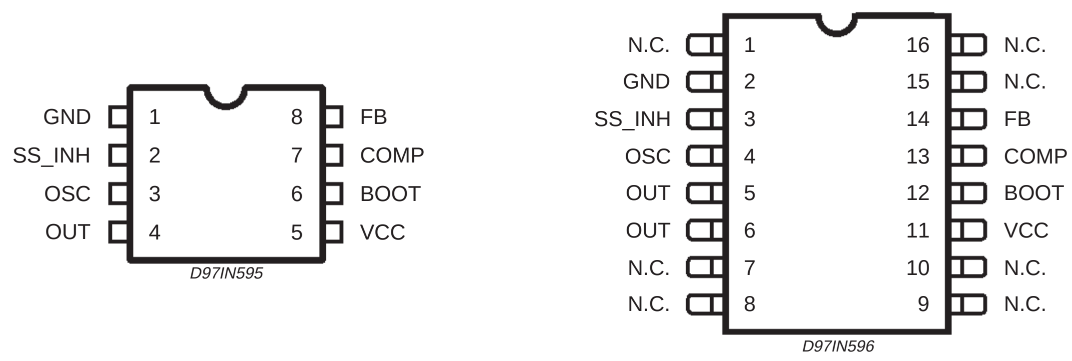
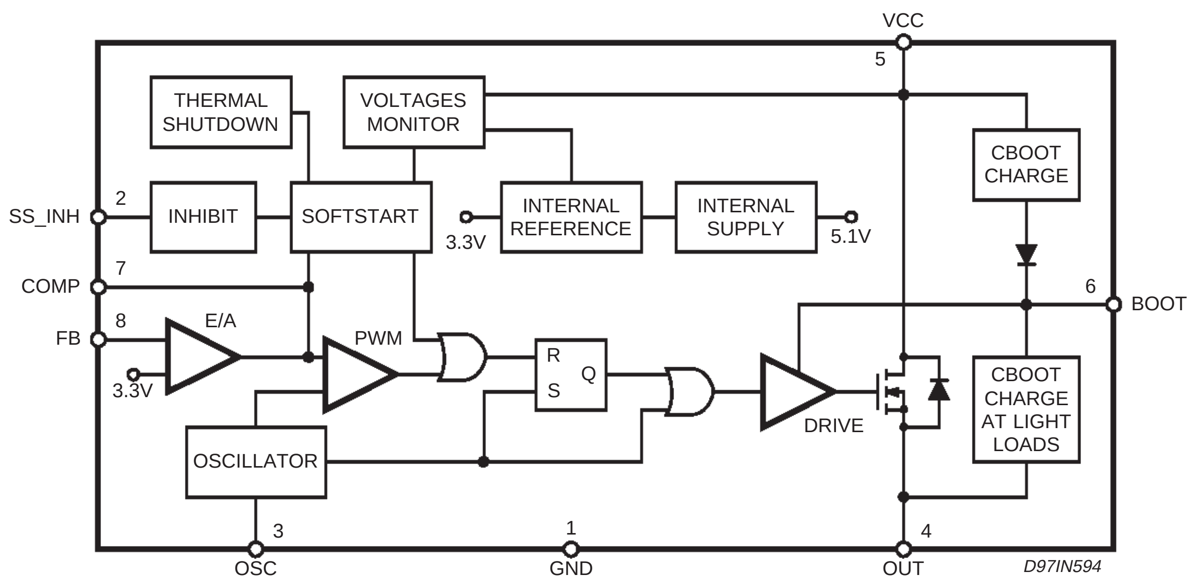


Figure 2. Block diagram.



Power supply & Voltage reference

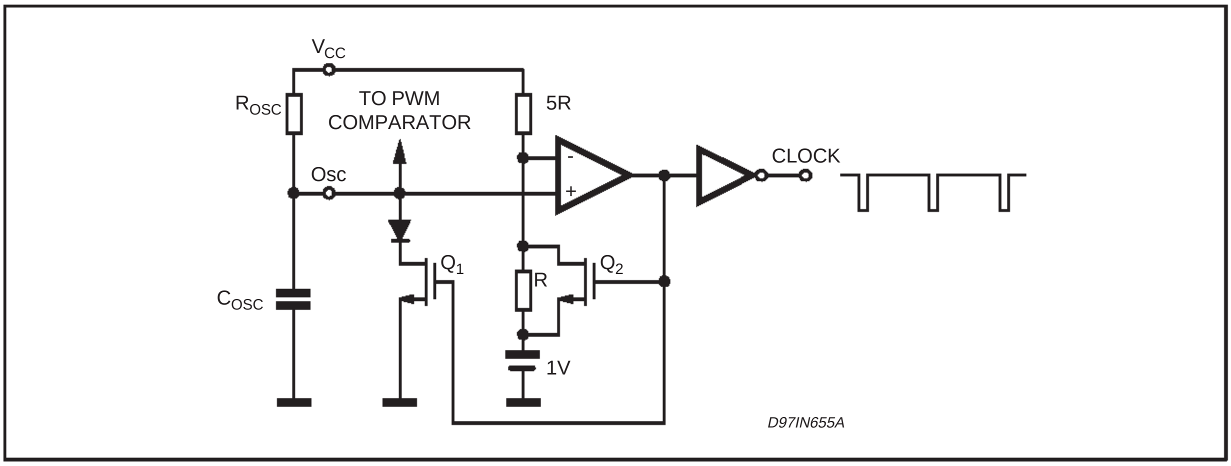
The device is provided with an internal stabilised power supply (of about 12V typ.) that powers the analog and digital control blocks and the bootstrap section.

From this preregulator, a 3.3V reference voltage ±2%, is internally available.

Oscillator and voltage feedforward.

Just one pin is necessary to implement the oscillator function, with inherent voltage feedforward.

Figure 3. Oscillator internal circuit.



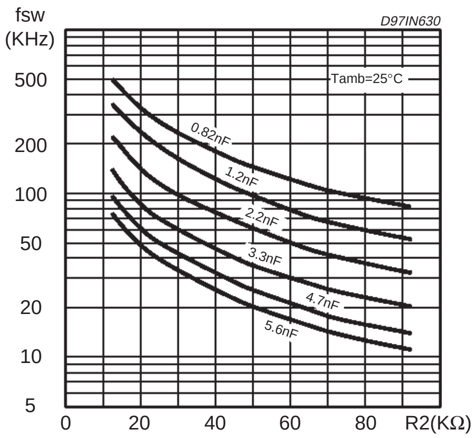
A resistor Rosc and a capacitor Cosc connected as shown in fig. 3, allow the setting of the desired switching frequency in agreement with the below formula:

$$F_{SW} = \frac{1}{R_{osc} \cdot C_{osc} \ln\left(\frac{6}{5}\right) + 100 \cdot C_{osc}}$$

Where F_{sw} is in kHz, R_{osc} in KΩ and C_{osc} in nF.

The oscillator capacitor, C_{osc}, is discharged by an internal mos transistor with 100Ω of R_{dson} (Q1) and during this period the internal threshold is set at 1V by a second mos, Q2 . When the oscillator voltage capacitor reaches the 1V threshold, the output comparator turns off the mos Q1 and turns on the mos Q2, restarting the C_{osc} charge.

Figure 4. Switching frequency vs. R_{osc} and C_{osc}.



The oscillator block, shown in fig.4, generates a sawtooth wave signal that sets the switching frequency of the system.

This signal, compared with the output of the error amplifier, generates the PWM signal that will modulate the conduction time of the power output stage.

The way the oscillator has been integrated,does not require additional external components to benefit of the voltage feedforward function.

The oscillator peak-to-valley voltage is proportional to the supply voltage, and the voltage feedforward is operative from 8V to 55V of input supply.

$$\Delta V_{osc} = \frac{V_{CC} - 1}{6}$$

Also the ΔV/Δt of the sawtooth is directly proportional to the supply voltage. As Vcc increases, the Ton time of the power transistor decreases in such a way to provide to the chocke, and finally also the load, the product Voltxsec constant.

Fig 5 shows how the duty cycle varies as a result of the change on the ΔV/Δt of the sawtooth with the Vcc.

Figure 5. Voltage Feedforward Function.

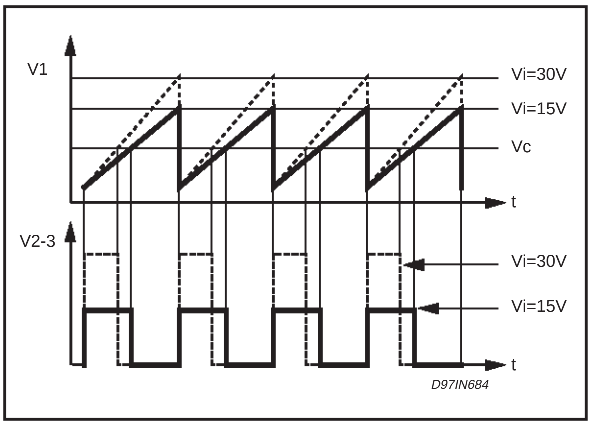
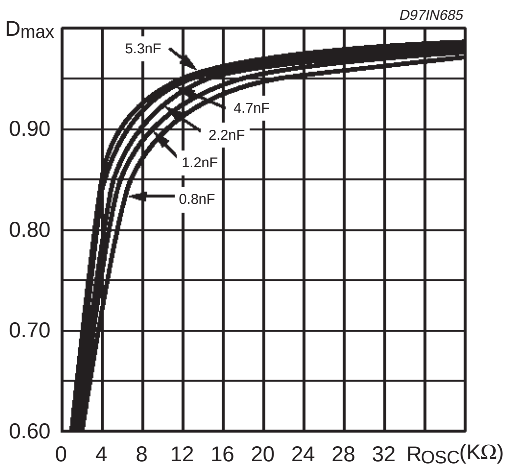


Figure 6. Maximum Duty Cycle vs Rosc and Cosc as parameter



The output of the error amplifier doesn't change in order to maintain the output voltage constant and in regulation.

With this function on board, the output response time is greatly reduced in presence of an abrupt change on the supply voltage, and the output ripple voltage at the mains frequency is greatly reduced too.

In fact, the slope of the ramp is modulated by the input ripple voltage, generally present in the order of some tens of Volt, for both off-line and dc-dc converters using mains transformers.

The charge and discharge time are approximable to:

$$T_{ch} = R_{osc} \cdot Cosc \cdot \ln\left(\frac{6}{5}\right)$$

$$T_{dis} = 100 \cdot C_{osc}$$

The maximum duty cycle is a function of Tch, Tdis and an internal delay and is expressed by the equation:

$$D_{max} = \frac{R_{osc} \cdot C_{osc} \cdot \ln\left(\frac{6}{5}\right) - 80 \cdot 10^{9}}{R_{osc} \cdot C_{osc} \cdot \ln\left(\frac{6}{5}\right) + 100 \cdot C_{osc}}$$

It is represented in figure 6.

Current Protection

The L4971 has two current limiting levels, pulse by pulse and hiccup modes.

Increasing the output current till the pulse by pulse limiting current threshold (Ith1 typ. value of 2.5A) the controller reduces the on time, maintaining the peak current at the value:

$$I_P = I_{th1} + (V_{CC} - V_O - R_{on} \cdot I_{th1}) \cdot \frac{T_d}{L}$$

where t_d is the internal propagation delay of the current protection loop (typical 300ns).

If the operating conditions define a minimum on-time lower than td, the current increases to the following value:

$$I_{max} = \frac{(V_{CC} \cdot t_d \cdot F_{sw} - V_f \cdot (1 - t_d \cdot F_{sw}))}{(R_o + R_{on} \cdot T_d \cdot F_{sw})}$$

Where R_o is the load resistance, Vf is the diode forward voltage and Fsw is the switching frequency.

The output characteristic is represented in fig7. At point A the output voltage drops, and the device is going to pulse by pulse limiting current. Going versus the output short circuit, the current is shifting to point B, a bit higher because of the ripple current reduction and hiccup intervention, set 20% higher than pulse by pulse. Once the hiccup limiting current is operating, in output short circuit conditions the delivered average output current is the value at point C.

Figure 7. Output Characteristic

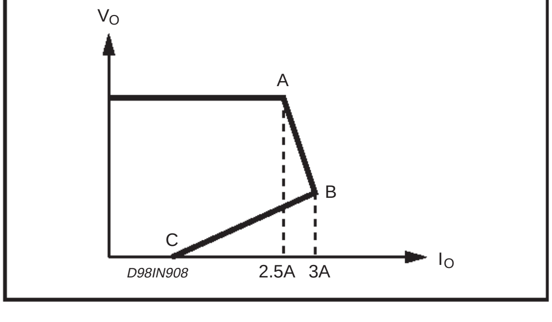


Figure 8. Current Limit internal schematic circuit.

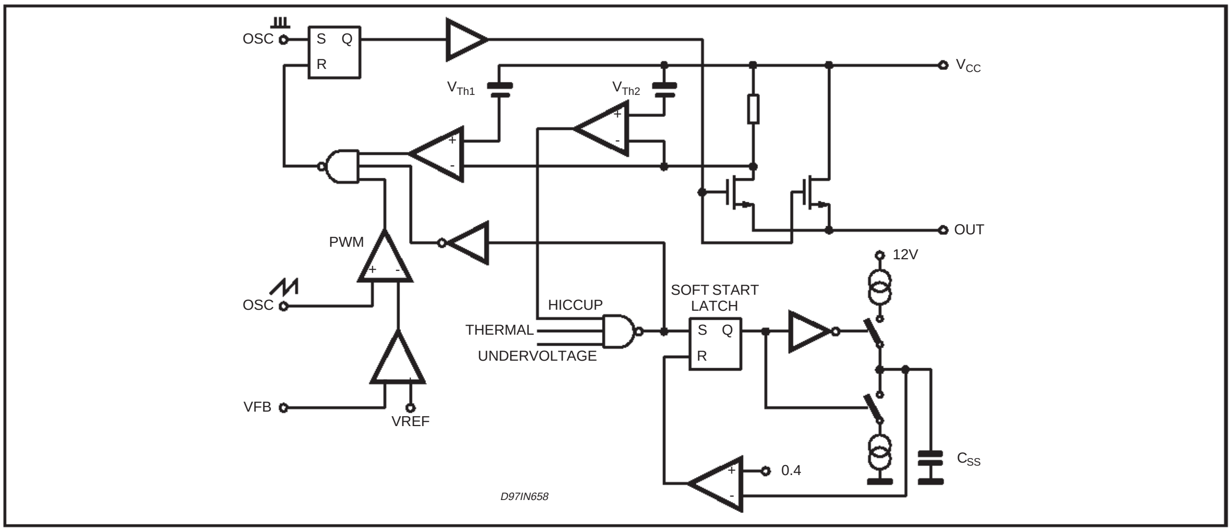


Fig. 8 shows the internal current limiting circuitry. Vth1 is the pulse by pulse while Vth2 is the hiccup threshold.

The sense resistor is in series with a small mos realised as a partition of the main DMOS.

The Vth2 comparator (20% higher than Vth1) sets the soft start latch, initialising the discharge of the soft start capacitor with a constant current (about 22µA). Reaching about 0.4V, the valley comparator resets the soft start latch, restarting a new recharge cycle.

Fig. 9 Shows the typical waveforms of the current in the output inductor and the soft start voltage (pin 2).

If the short circuit is permanent when the on time reaches the internal delay, the system recognises that the short circuit is still present and discharge again the soft-start capacitor.

The soft start capacitor value must not be too high because the system cannot intervene before the on time reaches the internal delay time. In output short circuit condition, the current increase cycle by cycle because the inductor during the off time cannot recycle all the flux stored during the on time.
It is necessary to ensure that during the soft start slope the current does not reach values that exceed 5A.

The following diagrams of Fig10a and Fig10b show the maximum allowed soft-start capacitor as a function of the input voltage, inductor value and switching frequency. The soft start capacitance must not be

Figure 9. Output current and soft-start voltage

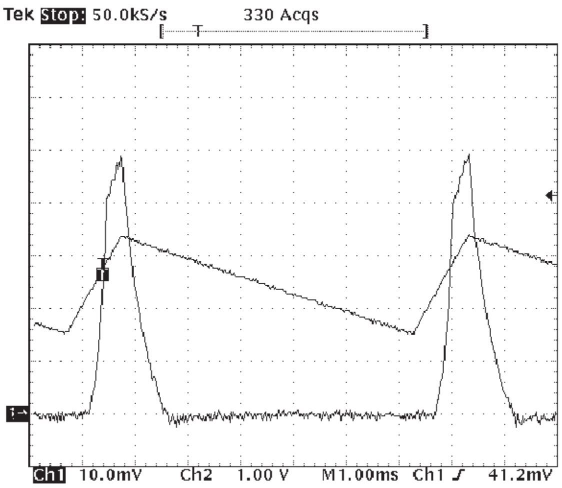


Figure 10a. Maximum Soft Start Capacitance with f_{SW} = 100kHz

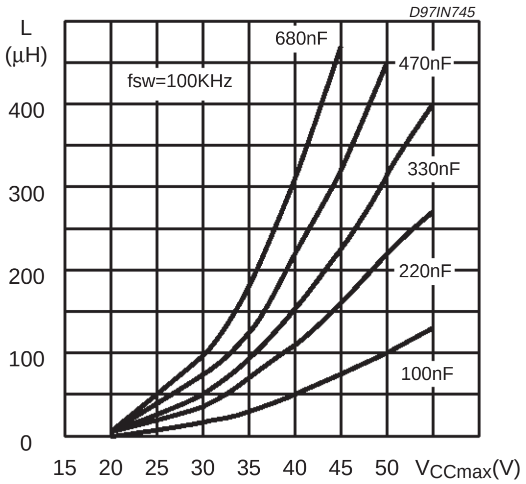
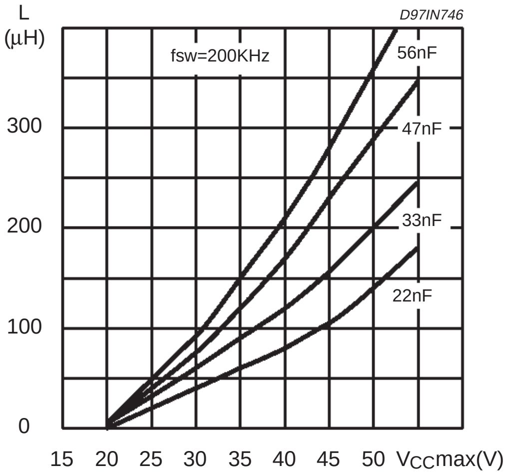


Figure 10b. Maximum Soft Start Capacitance with f_{SW} = 200kHz



zero. A minimum value is necessary to guarantee, in short circuit condition, the correct functionality of the internal limiting current circuitry.

Example: for a maximum input voltage of 55V at 100kHz, with an inductor of 260µH, it is possible to use a soft start capacitor lower than 220nF, the best compromise is 100nF . With such a value, the soft-start time (see Fig12) of about 3ms for an output voltage of 5V.

Soft Start and Inhibit functions.

The soft start and the inhibit functions are realised using one pin only, pin2. Soft-start is requested to inizialise all internal functions with a correct start-up of the system without overstressing the power stage, avoiding the intervention of the current protection, and having an output voltage rising smoothly without output overshoots.

At Vcc Turn-on or having had an intervention of inhibit function, an initial 5µA internal current generator starts to charge the soft-start capacitor, from 0V to about 1.8V. From this hysteretic threshold, a 40µA current generator is activated, putting in off state the previous generator.

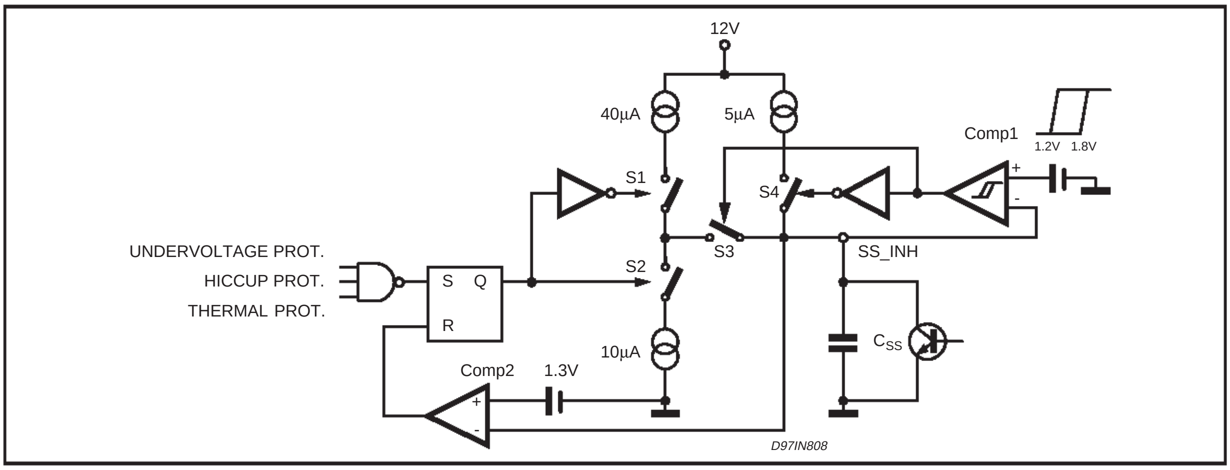
At this point, the output PWM starts, initiating the rising phase of the output voltage.

The soft-start capacitor is quickly discharged in case of:

- Thermal protection intervention
- Hiccup limiting current condition
- Supply voltage lower than UVLO off threshold.

The soft-start and inhibit schematic diagram is shown in fig 11.

Figure 11. Soft-Start and inhibit functions Internal Circuit .



At device turn-on, the soft-start capacitor has no charge, with 0V at its terminals.

From 0V to 1.8V, switch S3 is opened and S4 is closed.

Soft-start capacitor is charged with 5µA.

At 1.8V, comp1 change the output status, opening S4 and closing S3, and the device starts to generate the PWM signal, rising smothly the output voltage.

Till this moment, S2 is opened, S1 closed.

By closing S3, the soft-start capacitor is charged with 40µA reaching its saturation voltage.

This procedure is repeated at each Vcc turn-on.

Turning Vcc off, the soft-start capacitor is discharged with a constant 10µA (S2 closed, S3 closed, S1 and S4 open), from the moment when Vcc is crossing the UVLO off threshold.

The final discharge value is 1.2V.

In case of the Css is discharged using an external grounded element when the voltage at Css reaches the threshold of 1.3V Comp2 resets the flip flop, S1 is closed, S2 is opened and the 40µA current generator is activated.

The external switch, sinking some mA, discharges the soft-start under the 1.2V Comp1 threshold, opening S3 and closing S4. At this point the device is in disable, sourcing only 5µA through pin 2.

When the external grounding element is removed, the device restarts charging the soft start capacitance, initially, with 5µA till the voltage reaches the 1.8V threshold and Comp1 connects the 40µA charging current generator.

In case of thermal shutdown or overcurrent protection intervention the power is turned off and the flip flop turns off S2 and turns on S1. The soft-start is discharged till the voltage reaches the 1.3V threshold, and Comp2 resets the flip flop. S1 is closed, S2 is opened and the soft-start capacitance is charged again.

Fig 11a shows the systems signals during Inhibit, overcurrent and Vcc turn off.

Figure 11a. Timing Diagram in Inhibit, overcurrent and turn off condition

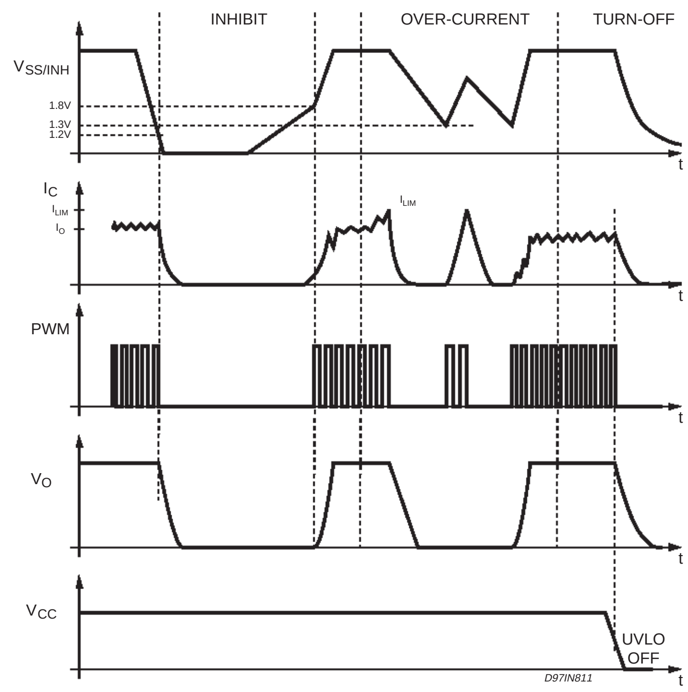
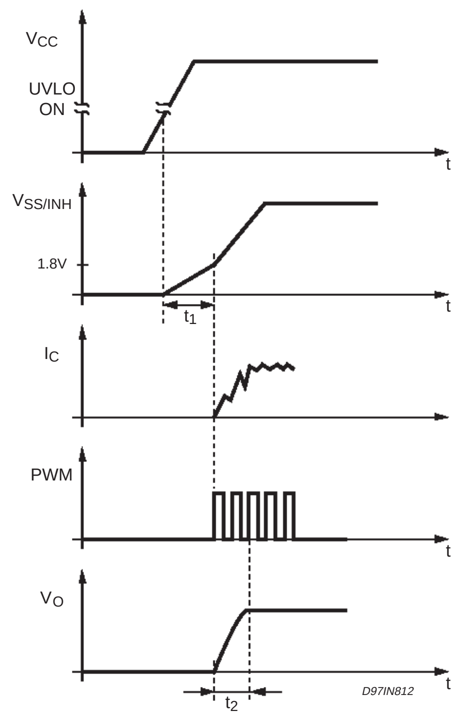


Figure 11b. Start up sequence.



t1 and t2 can be calculated by the following equations:

$$t1 = 0.36 \cdot Css; \quad t2 = \frac{V_o}{Ich \cdot 6 \cdot D_{max}} \cdot C_{SS}$$

where Dmax is 0.95, Css is in µF and Ich is in µA .

Soft-start time (t2) versus output voltage and Css is shown in Fig12.

Figure 12. Soft start time(t2) vs Vo and Css

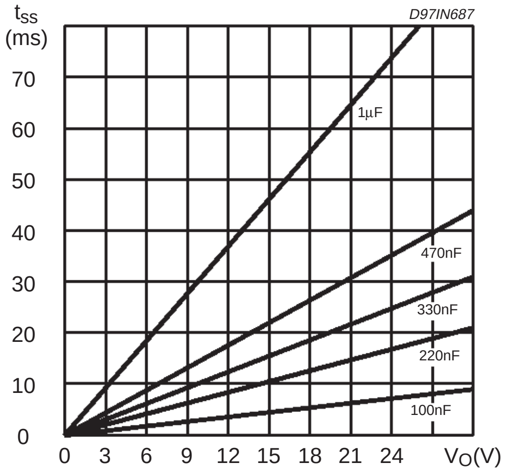
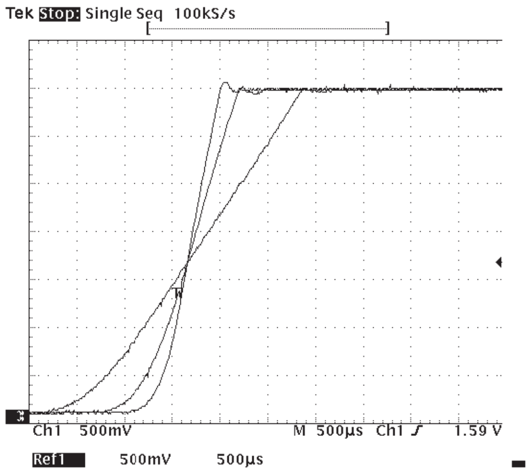


Figure 13. Output rising voltage with Css 56nF, 100nF, 220nF.



Thanks to the voltage feedforward, the start-up time (t2) is not affected by the input voltage.

Fig13 shows the output voltage start-up using different soft-start capacitance values:

It is mandatory a minimum capacitor value of 22nF. The pin 2 cannot be left open.

Feedback disconnection

In case of feedback disconnection, the duty cycle increases versus the max allowed value bringing the output voltage close to the input supply. This condition could destroy the load.

To avoid this dangerous condition, the device is forcing a little current(1.4µA typical) out of the pin 8 (E/A Feedback). If the feedback is disconnected, open loop, and the impedance at pin 8 is higher than 3.5M Ohm, the voltage at this pin goes higher than the internal reference voltage located on the non-inverting error amplifier input , and turns-off the power device.

Zero load

In normal operation, the output regulation is also guaranteed because the bootstrap capacitor is recharged, cycle by cycle, by means of the energy flowing into the choke.

Under light load conditions, this topology tends to operate in burst mode, with random repetition rate of the bursts.

An internal new function makes this device capable of keeping the output voltage in full regulation with 1mA of load current only.

Between 1mA and 500µA, the output is kept in regulation up to 8% above the nominal value.

Here the circuitry providing the control :

- 1- a comparator located on the bootstrap section is sensing the bootstrap voltage; when this is lower than 5V, the internal power VDMOS is forced ON for one cycle and OFF for the next.
- 2- during this operation mode, i.e. 500µA of load current, the E/A control is lost. To avoid output overvoltages, a comparator with one input connected to pin 8, and the second input connected to a threshold 8% higher that nominal output, turns OFF the internal power device the output is reaching that threshold.

When the output current, or rather, the current flowing into the choke, is lower than 500µA, that is also the consumption of the bootstrap section, the output voltage starts to increase, approaching the supply voltage.

Output Overvoltage Protection (OVP)

The output overvoltage protection, OVP, is realised by using an internal comparator, which input is connected to pin 8, the feedback, that turns-off the power stage when the OVP threshold is reached.

This threshold is typically 8% higher than the feedback voltage.

When a voltage divider is requested for adjusting the output voltage, the OVP intervention will be set at:

$$Vovp = 1.08 \cdot Vfb \cdot (Ra+Rb)/Rb$$

where Ra is the resistor connected to the output.

Power Stage

The power stage is realised by a N-channel D-mos transistor with a Vdss in excess of 60V and typ Rdson of 290mOhm (measured at to device pins).

To minimise the Rdson, means also minimise the conduction losses.

But also the switching losses have to be taken into consideration mainly for the two following reasons:

a- they are affecting the system efficiency and the device power dissipation

b- because they generate EMI.

TURN - ON

At turn-on of the power element, or better, the rise time of the current(di/dt) at turn-on is the most critical parameter to compromise.

At a first approach, it looks that the faster it is the rise time and the lower are the turn-on losses.

It's not completely true.

There is a limit, and it's introduce by the recovery time of the recirculation diode.

Above this limit, about 100A/usec, only disadvantages are obtained:

1- turn-on overcurrent is decreasing efficiency and system reliability

2- big EMI encreasing.

The L4971 has been developed with a special focus on this dynamic area.

An innovative and proprietary gate driver, with two different timings, has been introduced.

When the diode reverse voltage is reaching about 3V, the gate is sourced with low current (see fig 14) to assure the complete recovery of the diode without generating unwanted extra peak currents and noise.

After this threshold, the gate drive current is quickly increased, producing a fast rise time till the peak current, so maintaining the efficiency very high.

TURN - OFF

The turn-off behaviour, is shown at Fig 14.

Fig 15 shows the details of the internal power stage and driver, where at Q2 is demanded the turn-off of the power switch, S.

Figure 14. Turn on and Turn off (pin 2, 3)

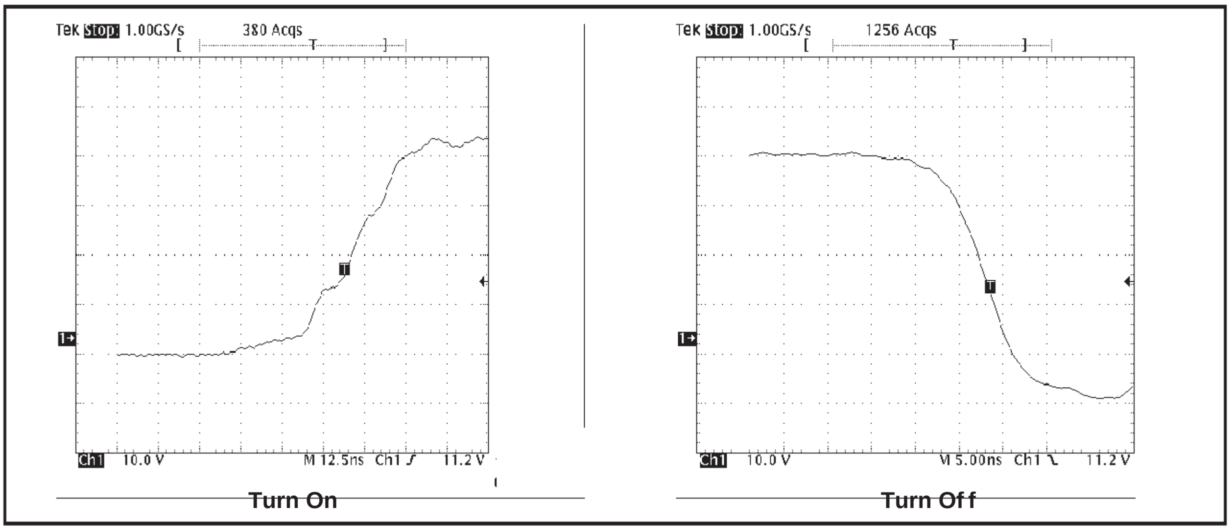
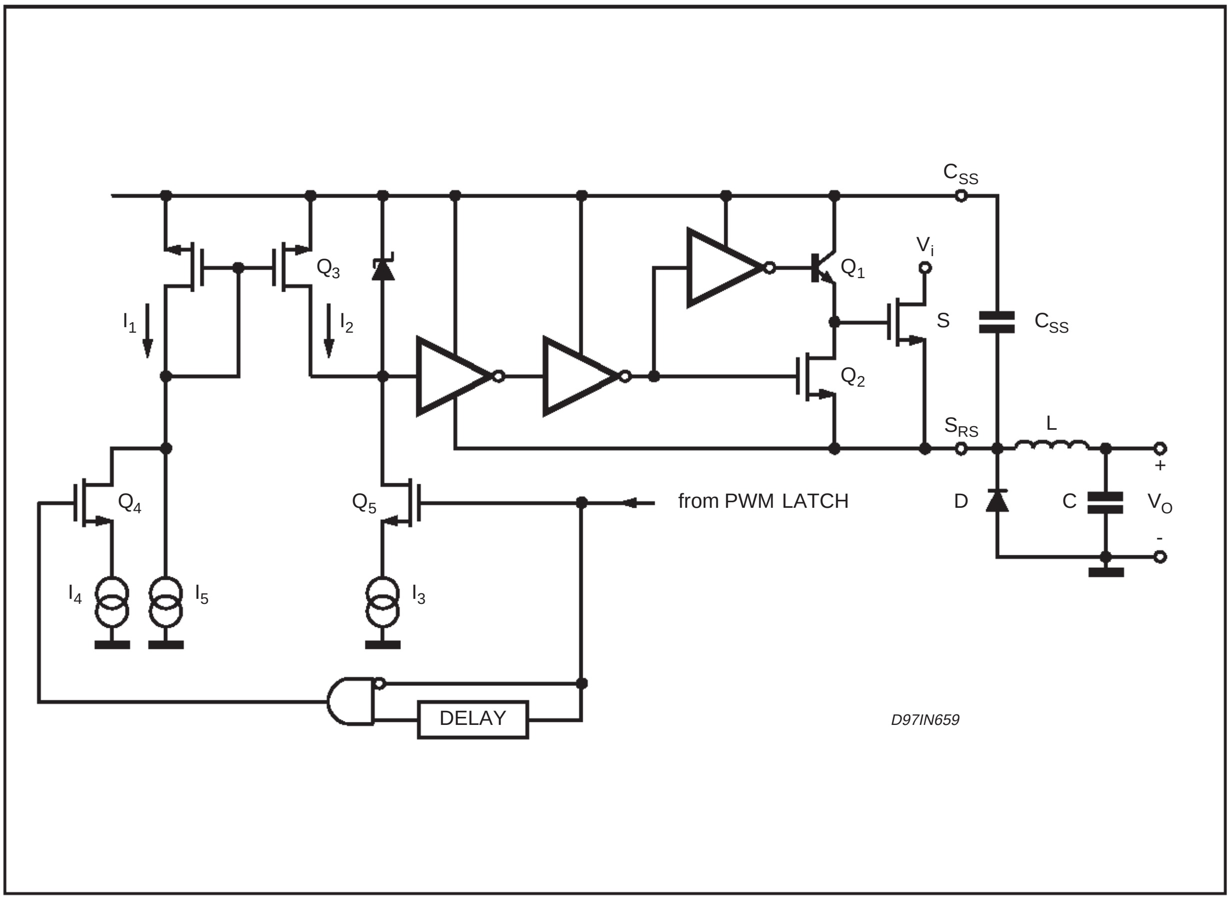


Figure 15. Power stage internal circuit.

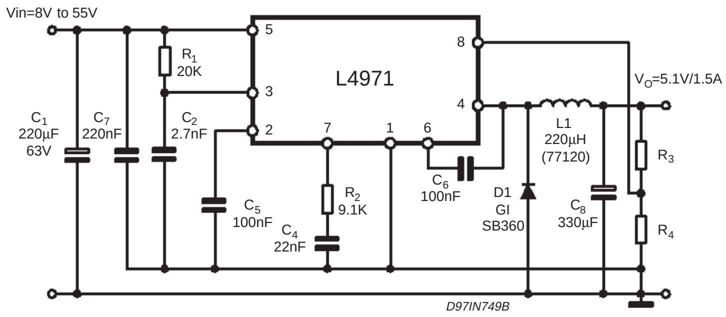


TYPICAL APPLICATION

Fig. 16 shows the typical application circuit, where the input supply voltage, Vcc, can range from 8 to 55V operating, and the output voltage adjustable from 3.3V to 40V.

The selected components, and in particular input and output capacitors, are able to sustain the device voltage ratings, and the corresponding RMS currents.

Figure 16. Application Circuit



C1=220µF/63V EKE
C2=2.7nF
C5=100nF
C6=100nF
C7=220nF/63V
C8=330µF/35V CG Sanyo
L1=220µH KoolMu 77120 - 65 Turns - 0.5mm
R1=20K
R2=9.1K
D1=GI SB360

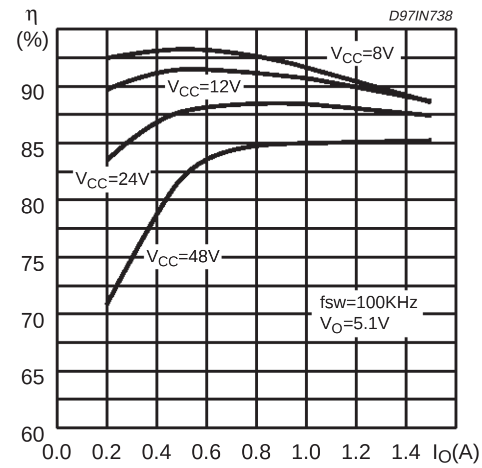
L4971

V_O(V)	R3(KΩ)	R4(KΩ)
3.3	0	
5.1	2.7	4.7
12	12	4.7
15	16	4.7
18	20	4.7
24	30	4.7

Electrical Specification

Input Voltage range	8V-55V
Output Voltage	5.1V ±3% (Line, Load and Temperature)
Output ripple	20mV
Output Current range	1mA-1.5A
Max Output Ripple current	15% Iomax
Current limit	2.5A
Switching frequency	100kHz
Target Efficiency	85%@1.5A Vi=55V 91%@0.5A Vi=12V

Figure 17. Efficiency vs Output Current



Main components description

INPUT CAPACITOR

The input capacitors have to be able to support the max input operating voltage of the device and the max rms input current.

The input current is squared and the quality of these capacitors has to be very high to minimise its power dissipation generated by the internal ESR, improving the system reliability. Moreover, input capacitors are also affecting the system efficiency.

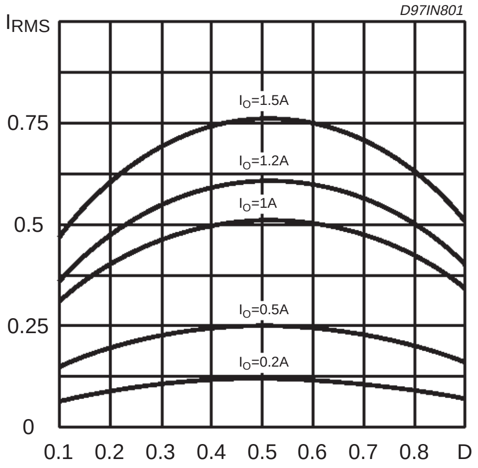
The max Irms current flowing through the input capacitors is:

$$I_{rms} = I_o \cdot \sqrt{D - \frac{2 \cdot D^2}{\eta} + \frac{D^2}{\eta^2}}$$

where η is the expected system efficiency, D is the duty cycle and Io the output dc current. This function reaches the maximum value at D = 0.5 and the equivalent rms current is equal to Io/2.

The following diagram is the graphical representation of the above equation, with an estimated efficiency of 85% at different output currents.

Figure 18. Input Capacitance rms current vs duty cycle



The maximum and minimum duty cycles are:

$$D_{max} = \frac{V_o + V_f}{V_{in\,min} + V_f} = 0.66$$

$$D_{min} = \frac{V_o + V_f}{V_{in\,max} + V_f} = 0.1$$

where Vf is the freewheeling diode forward voltage.

This formula is not taking into account the power mos Rdson, considering negligible the inherent voltage drop, respect input and output voltages.

At full load, 1.5A and D = 0.5% the rms capacitor current to be sustained is of 0.75A.

The selected EKE 220µF/63V Roderstain is able to support this current.

Inductor Selection

The inductor ripple current is fixed at 10% of Iomax and is 0.15A, the inductor needed is:

$$L_o = (V_o + V_f) \cdot \frac{(1 - D_{min})}{\Delta I_o \cdot f_{SW}} = 310\mu H \quad (eq1)$$

The $Lo \cdot Io^2$ is 0.58 and the size core chose is 77120 (125µ) Magnetics KoolMµ material and are wiring 65Turns. At full load the magnetising force is about 25 Oersted, the inductance value is reduced at about L = 220µH and the ripple current increases at 0.24A (16% I_{omax}).

It is possible to graficate the Eq 1 as a function of Vo and Vinmax at 100kHz and 200kHz (see Fig19a-b).

These curves are useful to define the inductor value immediately.

Figure 19a. Inductor needed as a function of maximum input voltage and output voltage at fsw=100kHz

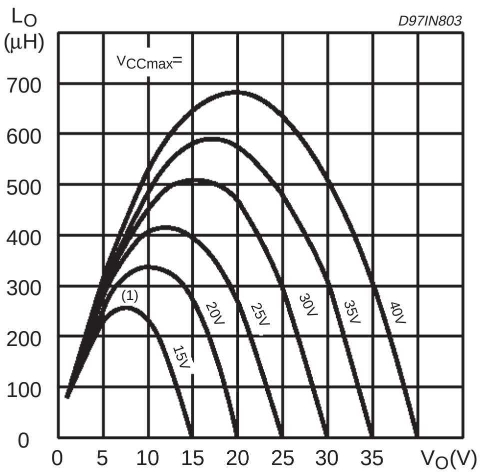
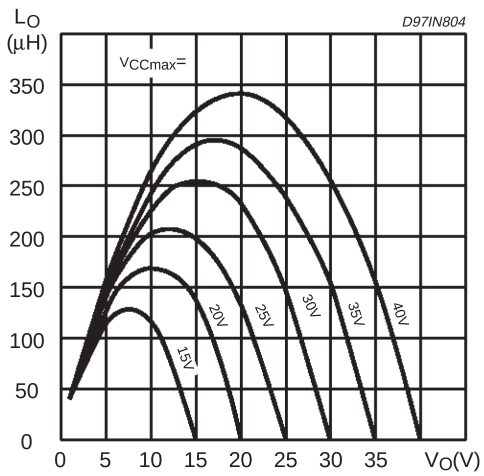


Figure 19b. Inductor needed as a function of maximum input voltage and output voltage at fsw=200kHz



Example: With a maximum input voltage of 15V at 100kHz, fixed the curve (1) in Fig19a and with an output voltage of 5V the inductor needed is 220μH.

-core losses

Core losses are proportional to the magnetic flux swing into the core material. To evaluate the flux swing is used the following formula:

$$\Delta B = \frac{L \cdot \Delta I_o \cdot 10^4}{N_o \cdot A_{le}} = 423 \text{ Gauss}$$

where Ale is the core cross section [m^2].

The choosen core material family has an empirical equation to calculate the losses:

$$P_L = \Delta B^2 \cdot f_{sw}^{1.5} \cdot V_L \cdot 10^2 = 141\text{mW}$$

Where ΔB is in KGauss, fsw in kHz and V_L is the core volume in cm^3. The core increasing temperature is:

$$\Delta T = \left(\frac{P_l}{13.6}\right)^{0.833} = 7°C$$

Output Capacitor

The selection of Cout is driven by the output ripple voltage required, 1% of Vo. This is defined by the output capacitance ESR and with the maximum ripple current (0.24A) the maximum ESR is:

$$ESR = \Delta V_o / \Delta I_o = 0.051/0.24 = 212m\Omega$$

The selected capacitance is 330μF/35V CG Sanyo with ESR = 86mΩ and the ripple voltage is 0.40% of V_o (20mV).

The drop due to a fast load variation of 1A produce an output drop of :

$$ESR \cdot \Delta I_o = 86mV$$

that is the 1.6% of the output voltage.

Output capacitance has to support a load transient until the inductor current reaches the increased current. The output drop during an output current variation is:

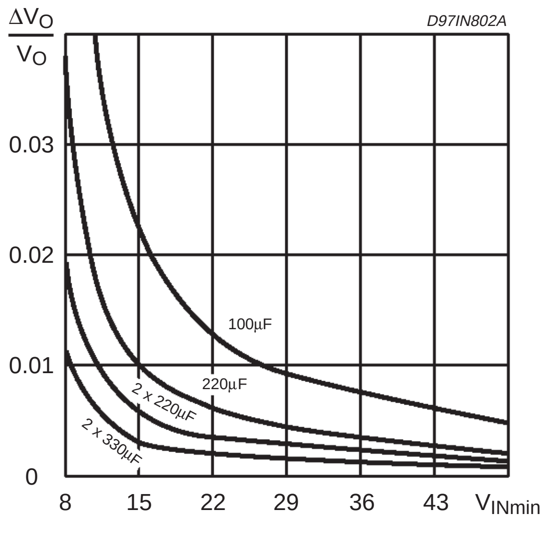
$$\Delta V_o = \frac{(\Delta I_O)^2 \cdot L_o}{2 \cdot C_o \cdot (V_{inmin} \cdot D_{max} - V_o)} \qquad \text{Eq(2)}$$

Where ΔI_o is the current load variation (0.5A to 1.5A), D_{max} is the maximum duty cycle (95%), V_o is 5.1V and L_o is 220μH .

Equation 2, normalised by Vo is represented in the following diagram(Fig. 20) as a function of the minimum input voltage.

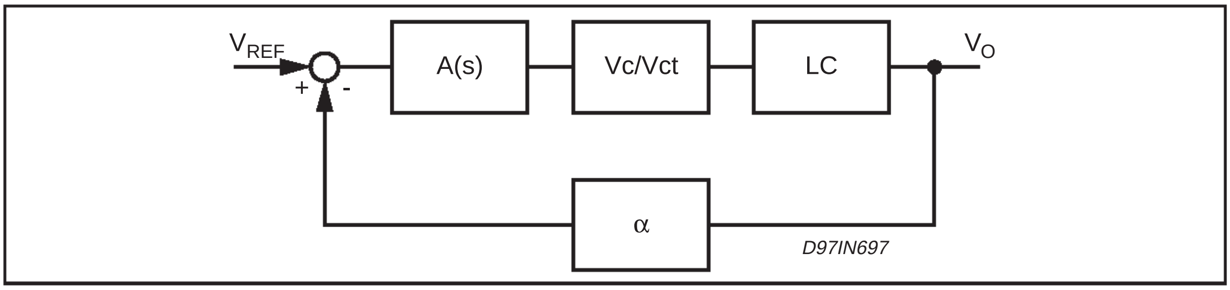
These curves are represented for different output capacitor 100μF, 220μF, 2x220μF, 2x330μF.

Figure 20. Output drop vs minimum input voltage



Compensation Network

Figure 21. Block diagram compensation loop



The complete control loop block diagram is shown in fig. 21

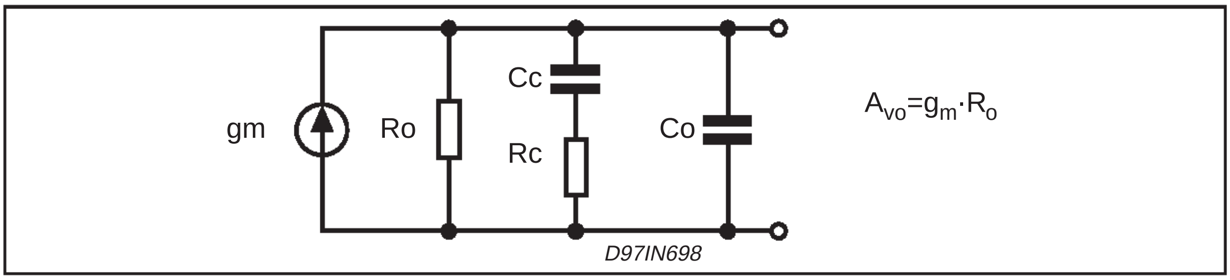
The transfer functions described are:

Error amplifier and compensation block

$$A_{(s)} = \frac{A_{vo} \cdot (1 + s \cdot R_c \cdot C_c)}{s^2 \cdot R_o \cdot C_o \cdot R_c \cdot C_c + s \cdot (R_o \cdot C_c + R_o \cdot C_o + R_c \cdot C_c) + 1}$$

C_o is the parallel between the output capacitance and the external capacitance of the Error Amplifier
R_c and C_c are the compensation values

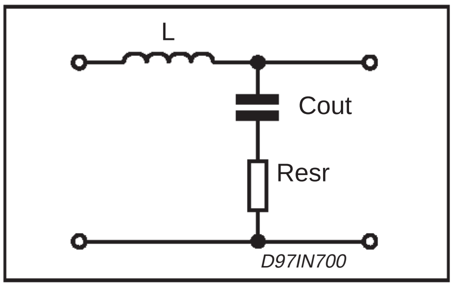
Figure 22. Error Amplifier Compensation Circuit



LC filter

$$A_{o(s)} = \frac{1 + R_{esr} \cdot C_{out} \cdot s}{L \cdot C_{out} \cdot s^2 + R_{esr} \cdot C \cdot s + 1}$$

Figure 23. Output Filter



PWM gain

$$\frac{V_{cc}}{V_{ct}} = \frac{V_{cc} \cdot 6}{V_{cc} - 1} \approx 6$$

where Vct is the peak to peak sawtooth oscillator

Voltage divider

$$\alpha = \frac{R4}{R3 + R4}$$

The Error Amplifier basic characteristics are:

$R_o = 1.2M\Omega$

$A_{vo} = 60dB$

$C_o = 220pF$

The poles and zeros value are:

$$F_o = \frac{1}{2 \cdot \pi R_{esr} \cdot C_{out}} = \frac{1}{2 \cdot \pi \cdot 0.086 \cdot 330 \cdot 10^{-6}} = 5.6KHz$$

$$F_p = \frac{1}{2 \cdot \pi \cdot \sqrt{L \cdot C_{out}}} = \frac{1}{2 \cdot \pi \cdot \sqrt{220 \cdot 10^{-6} \cdot 330 \cdot 10^{-6}}} = 590Hz$$

$$F_{ocomp} = \frac{1}{2 \cdot \pi \cdot R_C \cdot C_C} = \frac{1}{2 \cdot \pi \cdot 9.1 \cdot 10^3 \cdot 22 \cdot 10^{-9}} = 795Hz$$

$$F_{p1} = \frac{1}{2 \cdot \pi \cdot R_o \cdot C_c} = \frac{1}{2 \cdot \pi \cdot 1.2 \cdot 10^6 \cdot 22 \cdot 10^{-9}} = 6.92KHz$$

$$F_{p2} = \frac{1}{2 \cdot \pi \cdot R_c \cdot C_o} = \frac{1}{2 \cdot \pi \cdot 9.1 \cdot 10^3 \cdot 220 \cdot 10^{-12}} = 80KHz$$

The compensation is realised choosing the Focomp nearly the frequency of the double pole due to the LC filter.

Using compensation network R1 = 9.1K, C6 = 22nF and C5 = 220pF obtain the Gain and Phase Bode plot of Figg. 24-25. Is possible to omit C5 because does not influence the system stability but is useful only to reduce the noise. The cut off frequency and a phase margin are:

Fc = 3.5KHz; Angle = 20°

Figure 24. Gain Bode open loop plot

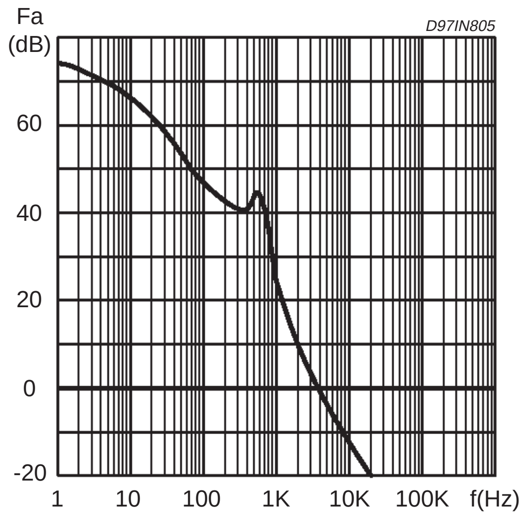


Figure 25. Phase Bode open loop plot