SGS-THOMSON MICROELECTRONICS

AN933 APPLICATION NOTE

WRITE PROTECT FUNCTION for 2Mb and 4Mb BOOT BLOCK FLASH MEMORIES

INTRODUCTION

The performance of the 2Mb and 4Mb Dual Voltage Boot Block Flash memories, M28F2xx and M28F4xx families has been enhanced by the introduction of a Write Protect function using the $\overline{WP}$ pin.

This new function is coupled with the introduction of the SGS-THOMSON 20% shrink generation of the CMOS T6 0.6µ flash process (CMOS T6-U20).

The application note deals about the impact for existing and new boards designs.

The introduction of this new feature maintains the product backward compatibility for existing applications for which hardware redesign is not required. It also permits the optimization, cost and functionnality of existing and new designs by removing the circuitry overhead previously required to unprotect the Boot Block.

The new version of 2Mb and 4Mb Flash memories from SGS-THOMSON bring added application flexibility and functionality in line with the Intel SmartVoltage products. They also maintain the backward compatibility with previous version of the products.

PRODUCTS

The generic part numbers affected are listed in Table 1. The change applies for all speed classes, package options and temperature ranges.

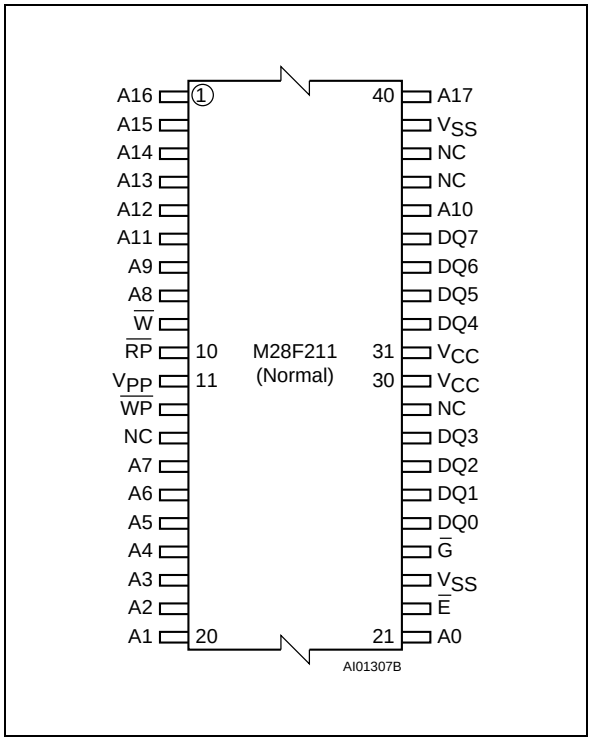
The $\overline{WP}$ function has been introduced on the products taking into consideration their compatibility with Intel SmartVoltage™ products.

On TSOP40 package the $\overline{WP}$ is located on pin 12; on SO44 it is located on pin 2; on TSOP48 it is located on pin 14. The new products pinouts are described in the Figures 1 to 8.

Table 1. The Dual Voltage Boot Block Flash Memory Products

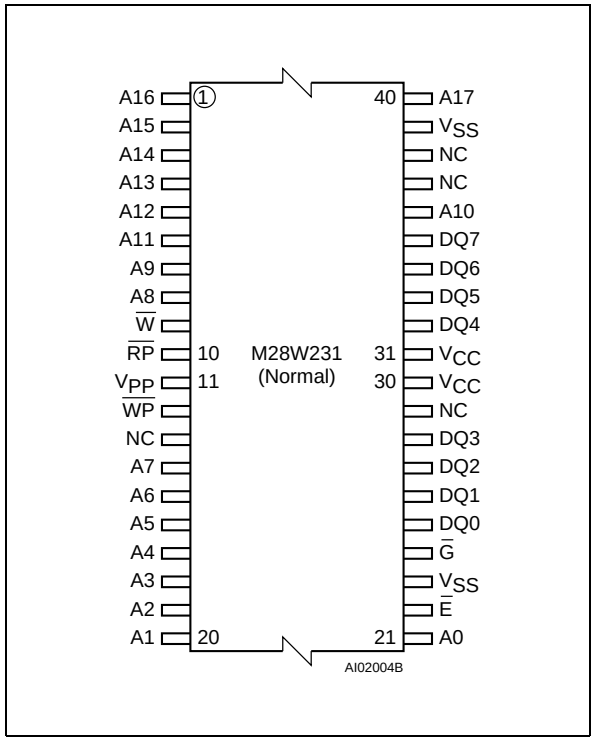
	Top Boot Block		Bottom Boot Block
	5V/12V	3V/12V	5V/12V
2Mb (x8)	M28F211	M28W231	N.A.
2Mb (x8,x16)	N. A.	N.A.	M28F220
4Mb (x8)	M28F411	M28W431	N.A.
4Mb (x8,x16)	M28F410	N.A.	M28F420

Figure 1. 2Mb (x8) TSOP Pin Connections



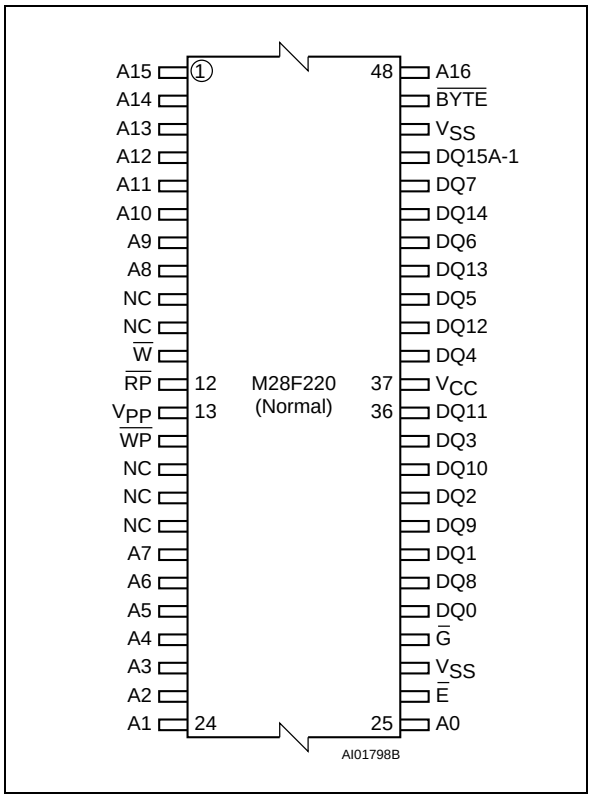
Warning: NC = Not Connected.

Figure 2. 2Mb (x8) TSOP Pin Connections



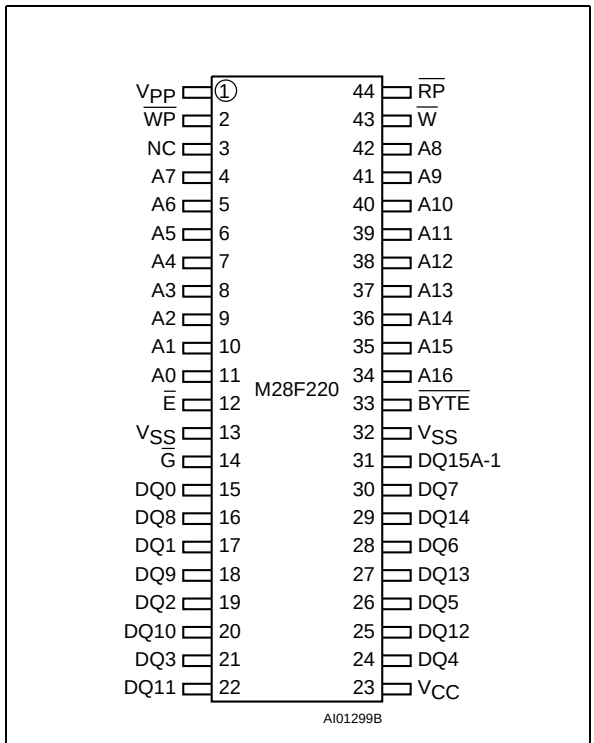
Warning: NC = Not Connected.

Figure 3. 2Mb (x8,x16) TSOP Pin Connections



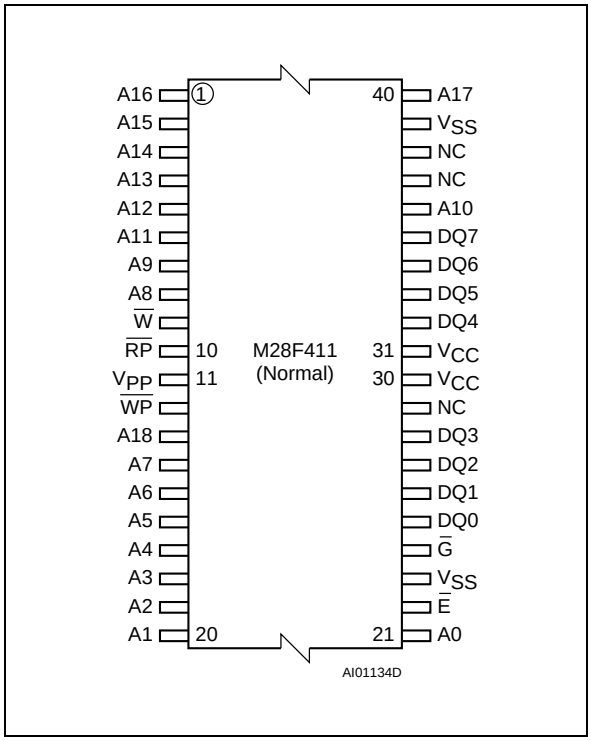
Warning: NC = Not Connected.

Figure 4. 2Mb (x8,x16) SO Pin Connections



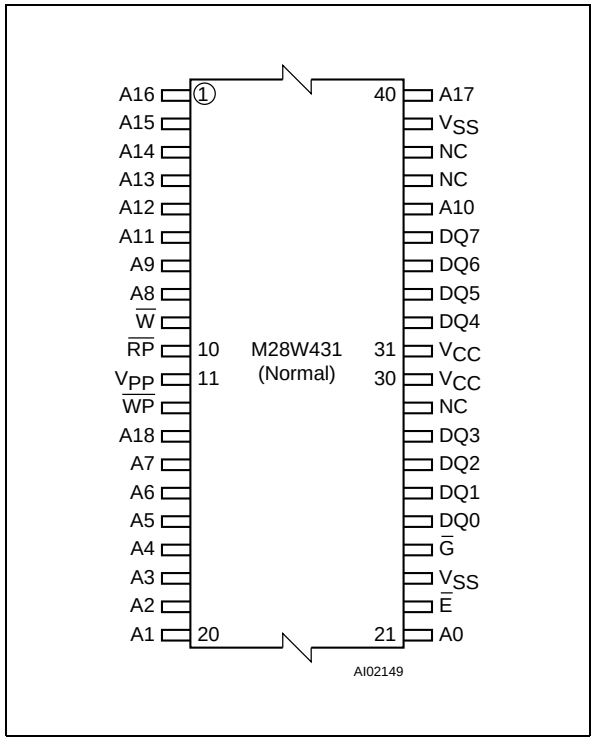
Warning: NC = Not Connected.

Figure 5. 4Mb (x8) TSOP Pin Connections



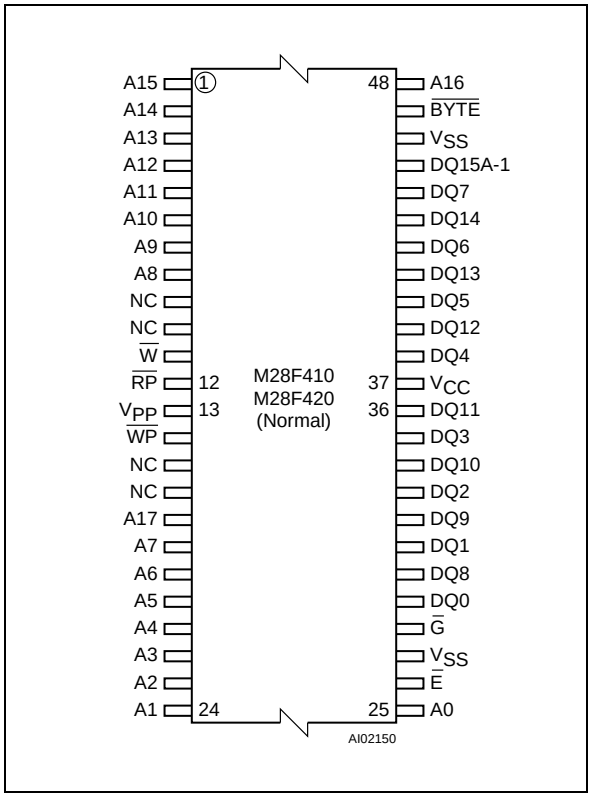
Warning: NC = Not Connected.

Figure 6. 4Mb (x8) TSOP Pin Connections



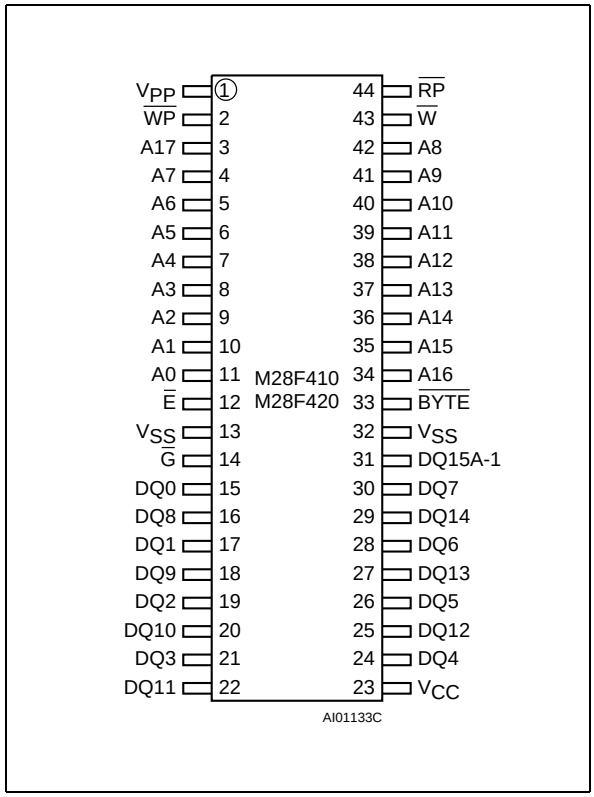
Warning: NC = Not Connected.

Figure 7. 4Mb (x8,x16) TSOP Pin Connections



Warning: NC = Not Connected.

Figure 8. 4Mb (x8,x16) SO Pin Connections



BLOCK PROTECTION SCHEME

The blocks protection scheme, previously ensured by V_{PP} and $\overline{RP}$ pins is now enhanced by the presence of the $\overline{WP}$ pin. The memory blocks protection thruth table, in Table 2, explains how the various blocks are protected or unprotected.

The new possible configuration offered by the $\overline{WP}$ pin is highlighted in the table.

Table 2. Memory Blocks Protection Truth Table

V_{PP}	$\overline{RP}$	$\overline{WP}$	Boot Block	Other Blocks
V_{PPL}	X	X	Protected	Protected
V_{PPH}	V_{IL}	X	Protected	Protected
V_{PPH}	V_{IH}	V_{IL}	Protected	Unprotected
V_{PPH}	V_{IH}	V_{IH}	Unprotected	Unprotected
V_{PPH}	V_{HH}	X	Unprotected	Unprotected

Notes: X' = Don't Care
RP is the Reset/Power Down/ Boot Block Unlock tri-level input.
V_{PP} is the program or erase supply voltage.
V_{IH}/V_{IL} are logic high and low levels.
V_{HH} is specified from 11.4V to 13V.
V_{PPH} is specified from 11.4V to 12.6V.

THE $\overline{WP}$ FUNCTION

The connection change with respect to the previous version of the products is described in Table 3.

When V_{PP} is at V_{PPL}, the whole chip is protected and no write operation is possible. Write operations are permitted only with V_{PP} at V_{PPH}, specified from 11.4V to 12.6V, and the Write protect input works as described in Table 4.

More detailed information about the blocks protection scheme is available from the individual products datasheets. Please refer to those documents for a complete understanding.

Table 3. $\overline{WP}$ Function and Pin Changes

Package	Pin Number	Previous Connection	New Connection	Intel Connection
TSOP40	12	DU	$\overline{WP}$	WP#
SO44	2	DU	$\overline{WP}$	WP#
TSOP48	14	NC	$\overline{WP}$	WP#

Notes: DU = Don't Use. NC = Not Connected

Table 4. Write Protect Pin Function

VPP	$\overline{WP}$ Level	Description
V_{PPH}	V_{IH} or V_{CC}	The boot block is unprotected $\overline{RP}$ can be either V_{IH} or V_{HH}
V_{PPH}	V_{IL} or V_{SS}	The boot block is protected or unprotected depending on $\overline{RP}$ level
V_{PPH}	Not Connected	The boot block is protected or unprotected depending on $\overline{RP}$ level

IMPACT AT THE APPLICATION LEVEL

The consequences of the implementation of the $\overline{WP}$ function on the 2Mb and 4Mb Boot Block Flash memories is described below. Two separate sections deal with two different cases: the first for applications where no modification is possible, the second for applications taking advantage of the additional performance and cost saving offered by the $\overline{WP}$ presence.

Applications where no Modification is Made or Possible

In this case, the new ST generation of the products can be used as the previous ones. This is possible as the unprotection of the Boot Block, through the $\overline{RP}$ tri-state input, is maintained the same. The compatibility to the previous generation product is also reinforced by the design of the $\overline{WP}$ input, that tolerates the previous "NC" or "DU" connections. In fact, the Table 4 explains the consequences of the different possible connections of $\overline{WP}$. It shows that whatever the level applied to $\overline{WP}$, the new product will work exactly the same as the old one, except in the case described here after.

There is a possibility to have the Boot Block unprotected whereas it was protected with the previous device version. This will happen if the $\overline{WP}$ pin is connected to V_{CC} or set at V_{IH}, and if V_{PP} is at V_{PPH}. In this case ($V_{PP} = V_{PPH}$ and $\overline{WP} = V_{IH}$) the memory will be fully functional both in read and write mode, but the Boot Block will be unprotected.

Applications where the New Feature is Used

The implementation of the $\overline{WP}$ pin functionality allows designers to optimise the applications and reduce the cost of their board.

Cost reduction. The implementation of the $\overline{WP}$ pin to unprotect the Boot Block is possible with a standard logical level, whereas it was previously necessary to have a V_{HH} level (Specified from 11.4V to 13.0V) on the $\overline{RP}$ pin to have the same function. Practically, this means that the circuitry needed to bring this V_{HH} level to $\overline{RP}$ can be removed. This circuitry could be as simple as a pull up to 12V or more elaborated like a full switch and its associated logic.

Performance enhancement. The introduction of the $\overline{WP}$ now allows programming and erasure of the Boot Block in those applications that could not afford the additionnal circuitry needed to set $\overline{RP}$ at V_{HH}.