AN924
APPLICATION NOTE

Watchdog Timer Functionality (and Errata)

The purpose of this document is to discuss the functionality of watchdog timers, and to correct the erroneous information that was inadvertently given in the M48T59 and M48T559 data sheets, dated July 1995.

A watchdog timer generally has a single output, the “watchdog flag”, that is asserted if a given condition does not occur on its inputs within a given time. The condition can be as simple as the output from a single edge detector, looking for pulses from a cooling fan; or it can be a detector of a complex, but recurrent, pattern of activity on the control bus of a microprocessor as it fetches instructions for execution. The output from the watchdog timer can be used to shut down the equipment if the cooling fan stops turning, or to reset the microcomputer if its processor gets stuck in an un-interruptible state.

Generally, a watchdog timer consists of a counter that is decremented by a simple clock (either an internal one, for measuring absolute time, or external one, for an event counter or some other flexible notion of time). Whenever the specific condition is detected on the input line, the counter is re-initialised. If the counter reaches zero, the watchdog flag is asserted.

FOR THE M48T59 AND M48T559

The watchdog timer is re-initialised whenever the microprocessor performs a write to the watchdog register. By writing the original value into the watchdog timer the time-out period resets to its initial value and the count-down starts again.

The default state of the watchdog timer is all zeros when the device powers-up.

The counter is initialised by writing to the watchdog register and can be set to values ranging from 0.0625 seconds to 124 seconds. The bits in the 8-bit watchdog register are defined as follows:

- D1-D0: Two bits to represent the resolution of the counter (between 1/16 second to 4 seconds)
- D6-D2: Five bits to represent the multiplier, in the range 1 to 31. This gives the time-out period of the timer (in the units of time given by the resolution bits).
- D7: The 1-bit Watchdog Steering bit (WDS). This causes the following behaviour of the device:
  - If WDS=0:the watchdog activates the $\overline{IRQ}$ pin when it times out. The $\overline{IRQ}$ pin is returned to its normal state by writing “all zeros” to the watchdog register.
  - If WDS=1:the watchdog activates the $\overline{RST}$ pin for a duration of 40 ms to 200 ms. The Watchdog timer is then set to all zeros.

RESETTING THE WATCHDOG TIMER

All ST devices that include watchdog timers have a hardware Watchdog-In pin (WDI) and a software reset facility. The method of forcing a software reset has been described above. A hardware reset is accomplished by feeding a pulse train to the WDI pin (the watchdog timer resets on each transition of the WDI pin). The WDI pin should be left unconnected if it is not needed (it already contains a pull-up resistor, with a value greater than 100 kΩ).

Please refer to the latest edition of the data sheet for a complete description of the functionality of the device.

If you have any questions or suggestions concerning the matters raised in this document, please send them to one of the following electronic mail addresses:

apps.nvram@st.com

Please remember to include your name, company, location, telephone number and fax number.